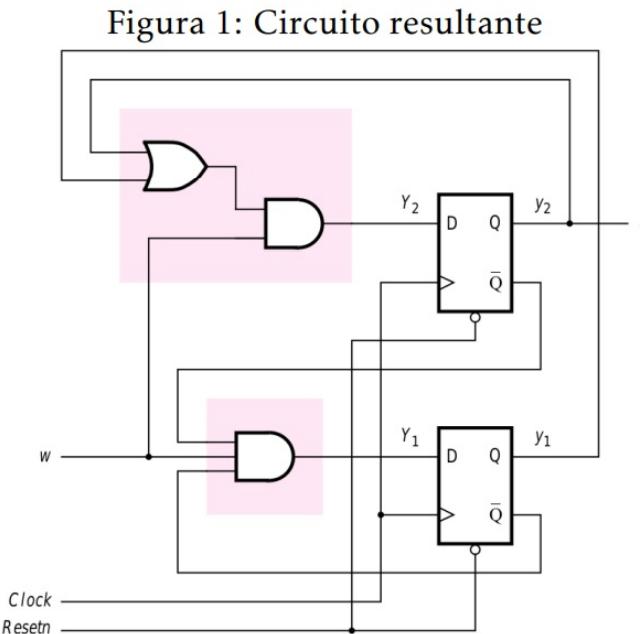


1. Implemente o código VHDL a partir da Figura 1:



Equações de Excitação:

$$Y_2 = w(\bar{y}_2 \bar{y}_2)$$

$$Y_2 = w(y_1 + y_2)$$

$$Z = y_2$$

Tabela de Estados:

$y_2 \ y_1$	$Y_2 \ Y_1$		$Z$
	$w=0$	$w=1$	
0 0	0 0	0 1	0
0 1	0 0	1 0	0
1 0	0 0	1 0	1
1 1	0 0	1 0	1

↳ Tabela de Estados Reduzida

$y_2 y_1$	$Y_2 Y_1$		$Z$
	$w=0$	$w=1$	
0 0	0 0	0 1	0
0 1	0 0	1 0	0
1 0	0 0	1 0	1

↳ Decodificação dos Estados

\* A (00)      \* C (10)

\* B (01)

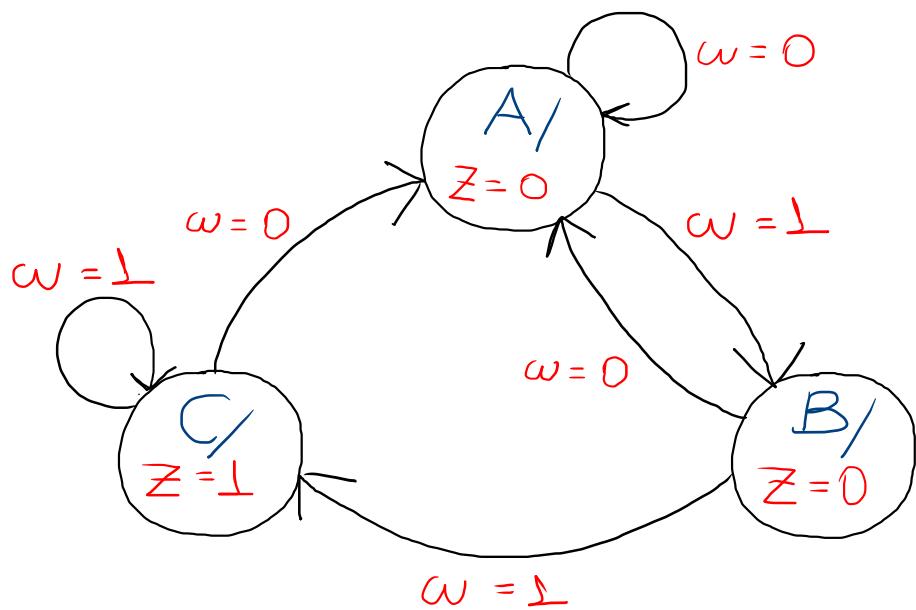
↳ Tabela de Estados Decodificada

$y_2 y_1$	$Y_2 Y_1$		$Z$
	$w=0$	$w=1$	
A	A	B	0
B	A	C	0
C	A	C	1

↳ Tabela de Estados Decodificada

$y_2\ y_1$	$Y_2\ Y_1$		$Z$
	$w=0$	$w=1$	
A	A	B	0
B	A	C	0
C	A	C	1

↳ FSM de Moore:

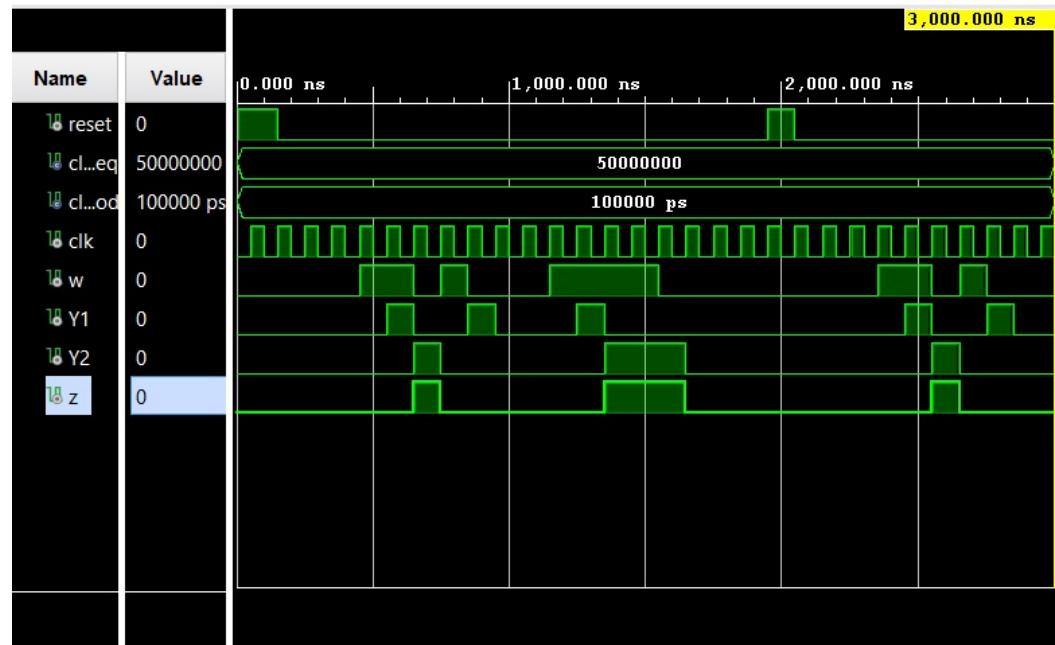
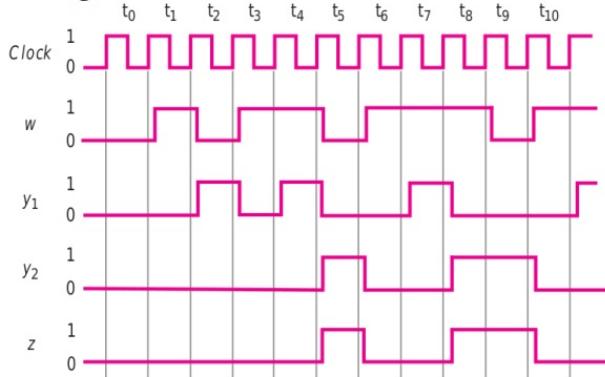


↳ Problema:

"Acionava a saída quando há entradas for  $1$  por mais de um ciclo."

2. Gere a **Wave** da Figure 2 que é baseada no circuito da questão 1 (Analizador de ondas, onde é possível verificar os sinais em determinados instantes de tempo) para **Reset**, **Clock**, **w**, **y1**, **y2** e **z** (estados A, B e C).

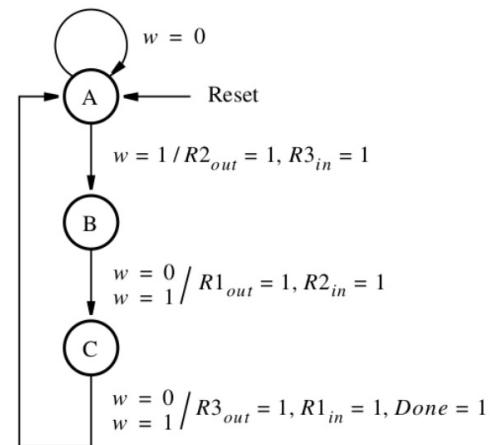
Figura 2: Sinal resultante do circuito



3. Desenvolva o circuito da Máquina de estados finitos (Mealy) da Figura 3.

- (a). Tabela de estados
- (b). Tabela de atribuição de estados
- (c). Expressões com mapa de Karnaugh
- (d). Circuito resultante
- (e). Sinal Wave resultante

@Tabela de Estados



Estado Atual	Estado Próximo		Saída												Done
	$R_3_{out}$	$R_2_{out}$	$R_3_{out}$	$R_2_{in}$	$R_3_{in}$	$w=0$	$w=1$								
$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$
A	A	B	0 0	0 1	0 0	0 1	0 0	0 1	0 0	0 1	0 0	0 1	0 0	0 0	0 0
B	C	C	0 0	0 0	0 0	1 1	0 0	0 0	1 1	1 1	0 0	0 0	0 0	0 0	0 0
C	A	A	1 1	1 1	0 0	0 0	0 0	0 0	0 0	0 0	0 1	1 1	1 1	1 1	1 1

# ⑥ Tabela de Atribuição de Estados (Codificação):

Estado Atual	Estado Próximo		Saída													
			$R_{3_{out}}$		$R_{2_{out}}$		$R_{2_{out}}$		$R_{3_{in}}$		$R_{2_{in}}$		$R_{2_{in}}$		Done	
	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$
00	00	01	0	0	0	1	0	0	0	1	0	0	0	0	0	0
01	10	10	0	0	0	0	1	1	0	0	1	1	0	0	0	0
10	00	00	1	1	0	0	0	0	0	0	0	0	1	1	1	1

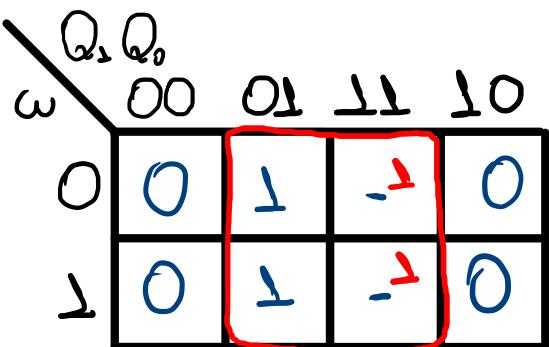
→ A: 00  
                

→ B: 01  
                

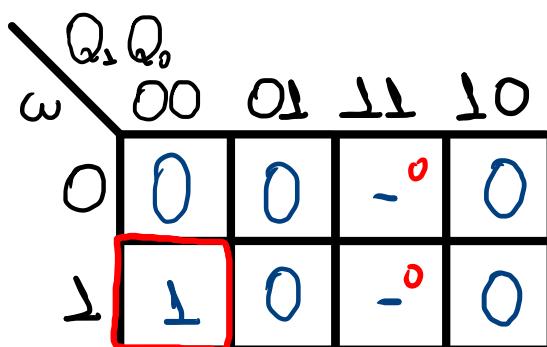
→ C: 10

# C Expressões lógicas (Próximo Estado)

Estado Atual	Estado Próximo		Saida												
			$R_{3_{out}}$		$R_{2_{out}}$		$R_{1_{out}}$		$R_{3_{in}}$		$R_{2_{in}}$		$R_{1_{in}}$		Desej.
	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	
00	00	01	00	00	01	01	00	01	00	01	00	01	00	00	00
01	10	10	00	00	00	01	11	00	01	11	10	00	11	00	00
10	00	00	11	11	00	00	00	00	00	00	00	01	11	11	11



$$Y_1 = Q_0$$



$$Y_0 = \omega \bar{Q}_1 \bar{Q}_0$$

# C Expressões lógicas (Saída $R_{2_{out}}$ & $R_{3_{in}}$ )

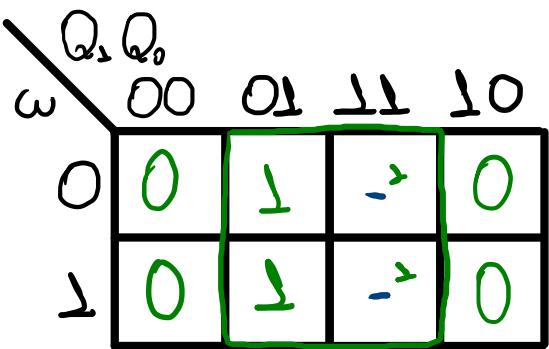
Estado Atual	Estado Próximo		Saída											
			$R_{3_{out}}$		$R_{2_{out}}$		$R_{2_{out}}$		$R_{3_{in}}$		$R_{2_{in}}$		$R_{2_{in}}$	
	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$
00	00	01	00	00	01	00	00	01	00	01	00	00	00	00
01	10	10	00	00	00	00	11	11	00	00	11	11	00	00
10	00	00	11	11	00	00	00	00	00	00	00	01	11	11

$\omega$	Q <sub>1</sub> Q <sub>0</sub>	00	01	11	10
0	0 0	0 0	- 0	0	
1	1 0	0 -	0 0		

$$\begin{aligned}
 R_{2_{out}} &= \underbrace{\omega \bar{Q}_1 \bar{Q}_0}_{Y_0}, \quad R_{2_{out}} = Y_0 \\
 R_{3_{in}} &= \underbrace{\omega \bar{Q}_1 \bar{Q}_0}_{Y_0}, \quad R_{3_{in}} = Y_0
 \end{aligned}$$

# Exercícios lógicos (Saída $R_{1_{out}}$ & $R_{2_{in}}$ )

Estado Atual	Estado Próximo		Saída											
			$R_{3_{out}}$		$R_{2_{out}}$		$R_{1_{out}}$		$R_{3_{in}}$		$R_{2_{in}}$		$R_{1_{in}}$	
	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$
00	00	01	00	01	00	10	00	00	01	01	00	00	00	00
01	10	10	00	00	00	00	11	11	00	00	11	11	00	00
10	00	00	11	11	00	00	00	00	00	00	00	00	11	11

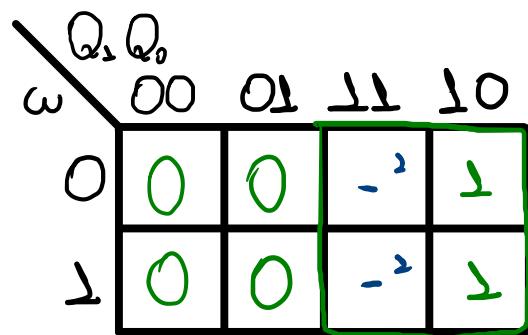


$$R_{1_{out}} = Q_0 \quad R_{1_{out}} = Y_2$$

$$R_{2_{in}} = \underbrace{Q_0}_{Y_2} \quad R_{2_{in}} = Y_2$$

# C Expressões lógicas (Saída $R_{3_{out}}$ & $R_{1_{in}}$ & Done)

Estado Atual	Estado Próximo		Saída													
			$R_{3_{out}}$		$R_{2_{out}}$		$R_{2_{out}}$		$R_{3_{in}}$		$R_{2_{in}}$		$R_{1_{in}}$		Done	
	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$
00	00	01	0	0	0	1	0	1	0	0	0	1	0	0	0	0
01	10	10	0	0	0	0	1	1	0	0	1	1	0	0	0	0
10	00	00	1	1	0	0	0	0	0	0	0	0	1	1	1	1



$$R_{3_{out}} = Q_1$$

$$R_{1_{in}} = Q_1$$

$$\text{Done} = Q_1$$

# Expresso lógicas:

Estado Atual	Estado Próximo		Saída											
	$R_{3_{out}}$	$R_{2_{out}}$	$R_{2_{out}}$	$R_{3_{in}}$	$R_{2_{in}}$	$R_{2_{in}}$	Done							
	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$	$w=0$	$w=1$
00	00	01	0	0	0	1	0	0	0	1	0	0	0	0
01	10	10	0	0	0	0	1	1	0	0	1	1	0	0
10	00	00	1	1	0	0	0	0	0	0	0	0	1	1

$$Y_1 = Q_0$$

$$Y_0 = \omega \bar{Q}_1 \bar{Q}_0$$

$$R_{3_{out}} = Q_1$$

$$R_{1_{in}} = Q_1$$

$$Done = Q_1$$

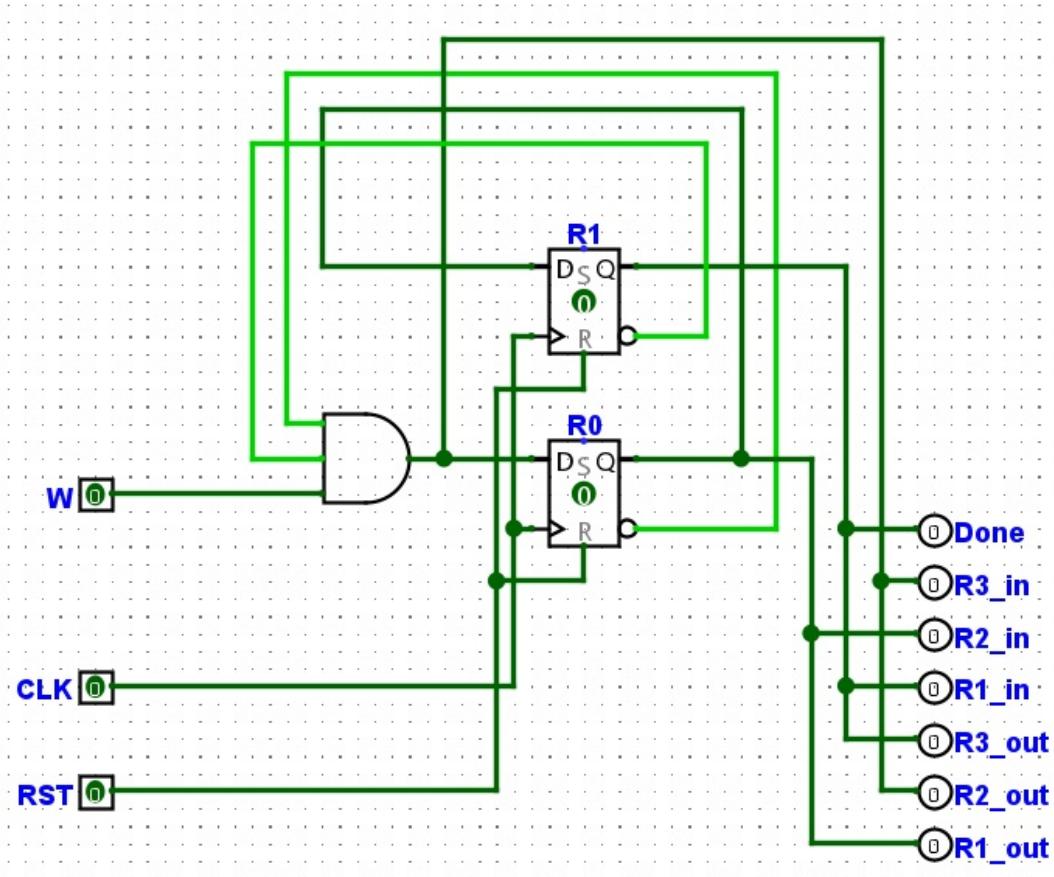
$$R_{3_{in}} = Y_0$$

$$R_{2_{out}} = Y_0$$

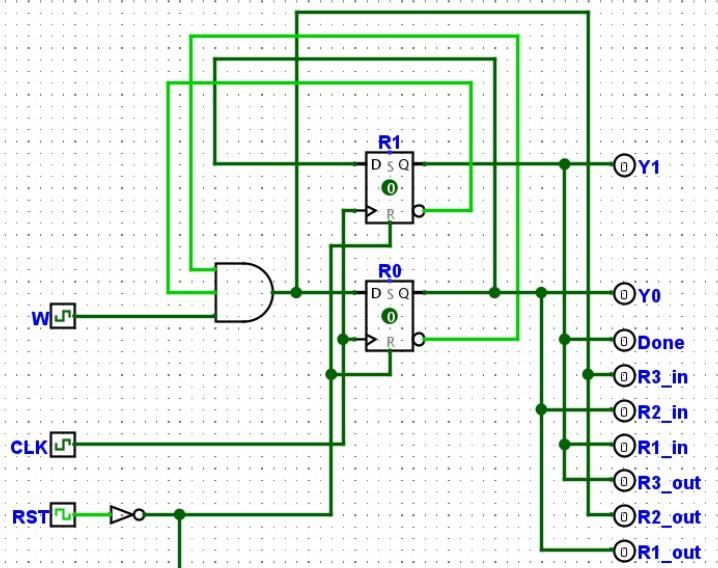
$$R_{2_{in}} = Q_0$$

$$R_{1_{out}} = Q_0$$

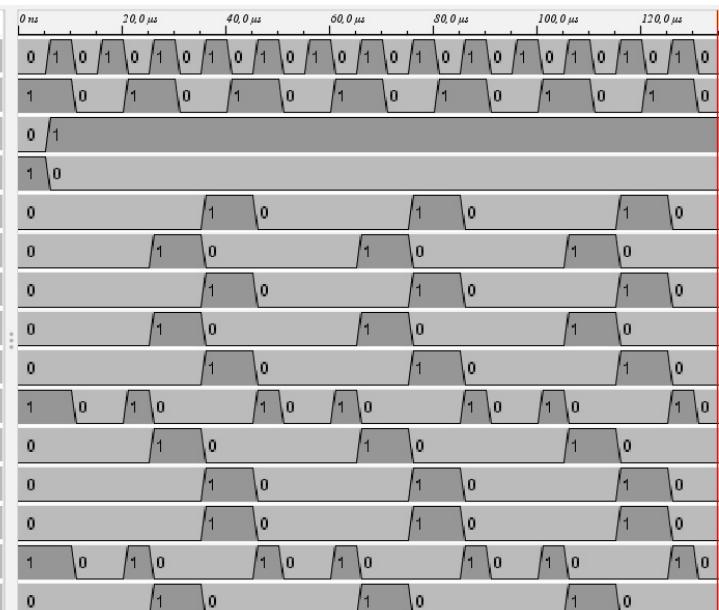
# Círcito Resultante :



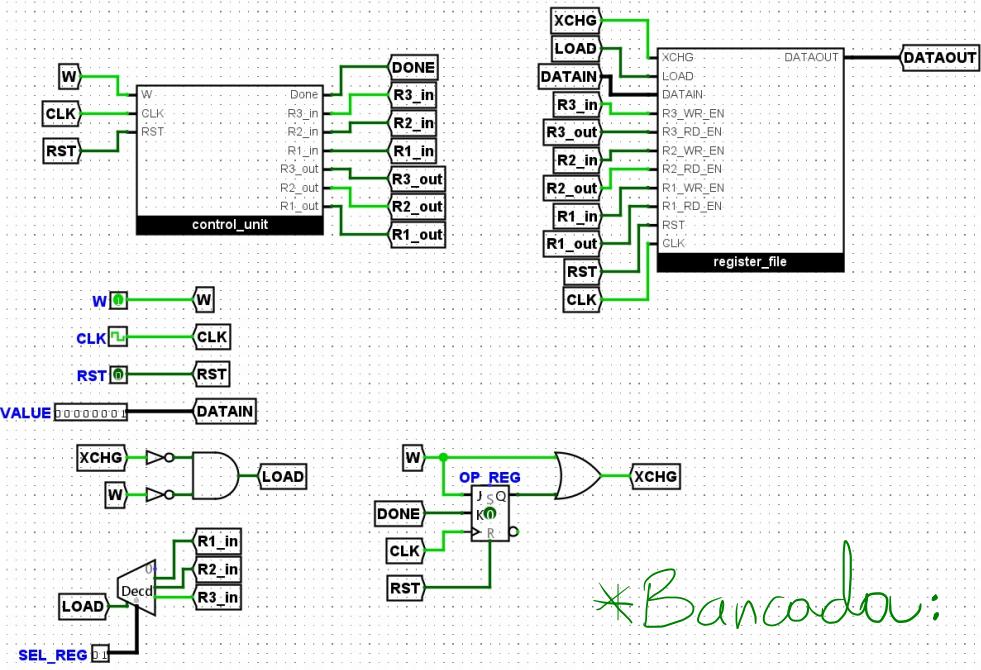
# d-Bonade de Testes:



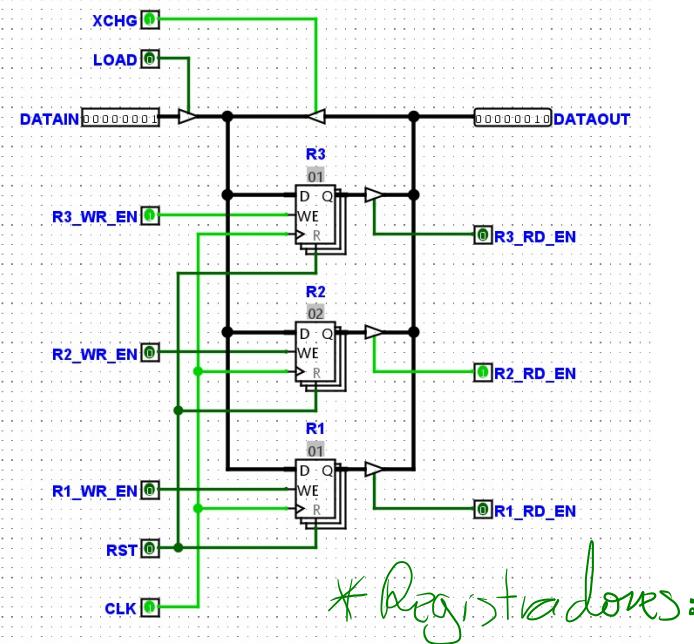
Nome do sinal	Valor do sinal
CLK	0
W	0
RST	1
Reset	0
R1	0
R0	0
Y1	0
Y0	0
Done	0
R3_in	0
R2_in	0
R1_in	0
R3_out	0
R2_out	0
R1_out	0



# d Aplicaçōo :



\*Bancada:



\* Registradores: