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Assembly Guidelines for MAPBGA (Molded Array Process Ball Grid Array) Package

1 Introduction

This application note provides guidelines for the handling and assembly of Freescale MAPBGA packages during printed circuit board (PCB) assembly. PCB design, rework, and package performance information such as Moisture Sensitivity Level (MSL) rating, board level reliability, mechanical, and thermal resistance data are also included for reference.

2 Scope

This document contains generic information that encompasses various Freescale MAPBGA packages assembled internally or at external subcontractors. Specific information about each device is not provided. To develop a specific solution, actual experience and development efforts are required to optimize the assembly process and application design per individual device requirements, industry standards (such as IPC and JEDEC), and prevalent practices in the assembly environment. For more details about the specific devices contained in this note, visit www.freescale.com or contact the appropriate product application team.

Contents

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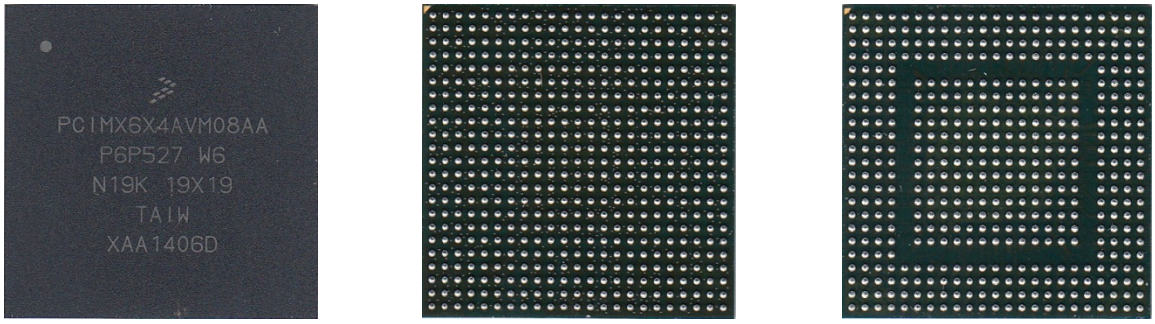
3 MAPBGA Package

3.1 Package Descriptions

The MAPBGA is a Molded Array Process Ball Grid Array package. This is a surface mount package using a grid of solder balls for electrical connections. The individual units are arranged in a matrix array on a substrate strip which are molded together and then singulated by sawing. Singulated units are distinguished by mold compound completely covering the substrate.

Figure 1 shows a typical MAPBGA offering from Freescale (1a) including examples of a fully populated BGA matrix (1b) and a depopulated BGA matrix (1c). Different sizes and configurations of MAPBGA packages are available. Contact your Freescale representative for specific size and BGA matrix configuration requirements.



1a 1b 1c

Figure 1. Example of a Freescale MAPBGA Offering

3.2 Package Dimensioning

Freescale offers industry standard MAPBGA sizes and thicknesses with various options of I/O (solder balls) quantity and pitch. Package sizes range from 4.0 x 4.0 to 27 x 27 mm with ball pitch ranging from 0.4 mm to 1.27 mm pitch. Refer to Freescale package case outline drawings to obtain detailed dimensions and tolerances. Package size and ball pitch are continually in review, check with the Freescale sales team for more information.

3.3 Package Cross-section

The cross-section drawing in Figure 2 is included to show the representative internal layers of a typical MAPBGA package with a 2-layer substrate (referring to the two conductive metal layers used to redistribute the I/O within the substrate). Standard configuration for a MAPBGA typically uses 2-layer substrates. High performance products may use 4-layer substrates.

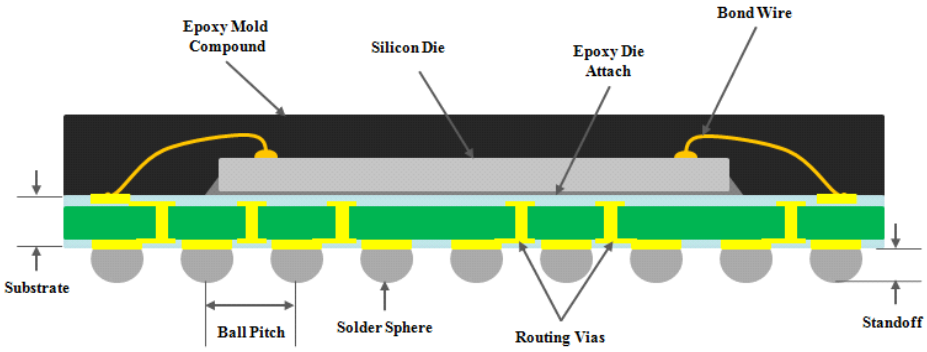


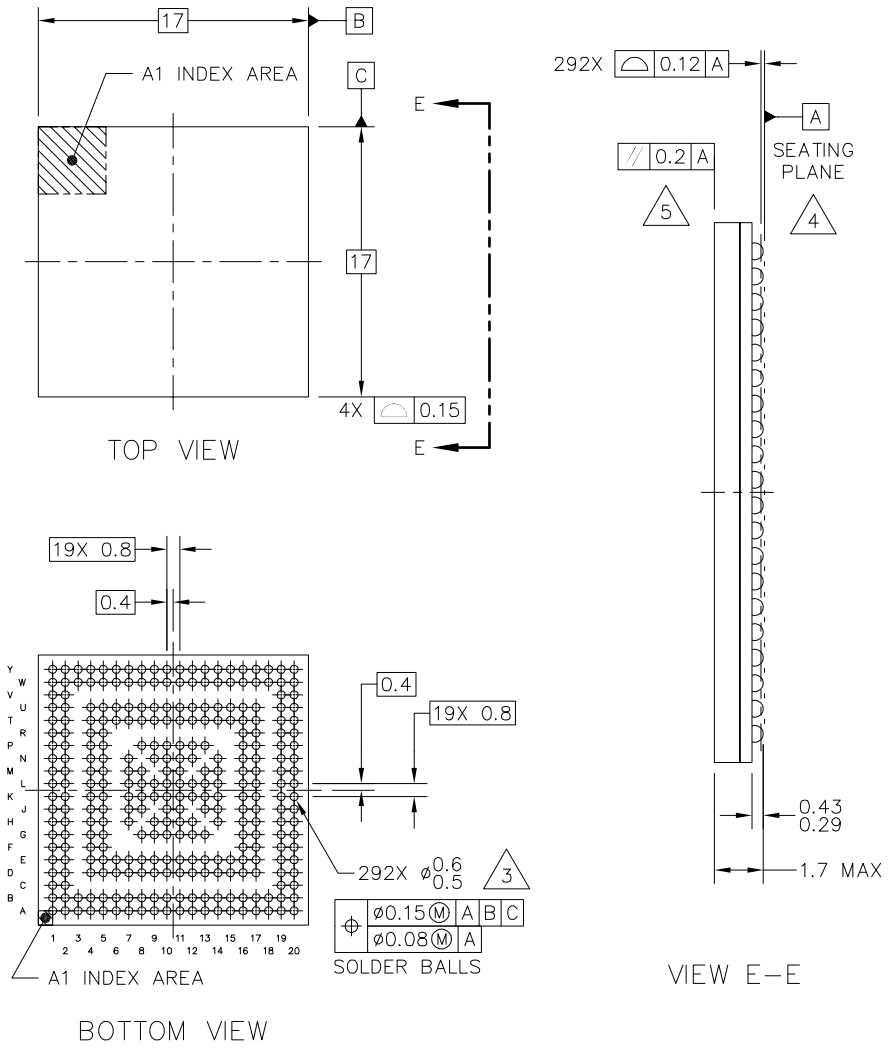
Figure 2. MAPBGA Cross-section with 2-Layer Substrate Configuration

4 Printed Circuit Board Guidelines

4.1 PCB Design Guidelines

Proper PCB footprint and stencil designs are critical to ensure high surface mount assembly yields, and electrical and mechanical performance. The design starts with obtaining the correct package drawing. Package Case Outline drawings are available at www.freescale.com.

Follow the procedures in the Downloading the Information from Freescale. Figure 3 shows an example of a 17 x 17 mm 292 MAPBGA Case Outline drawing. The goal is a well soldered MAPBGA as shown in Figure 4.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: MAPBGA, LOW PROFILE, 17 X 17 PKG, 292 I/O, 0.8 MM PITCH	DOCUMENT NO: 98ASA00261D	REV: A
	CASE NUMBER: 2151–02	23 FEB 2012
	STANDARD: NON JEDEC	

Figure 3. 17 x 17 292 MAPBGA Case Outline (98ASA00261D)

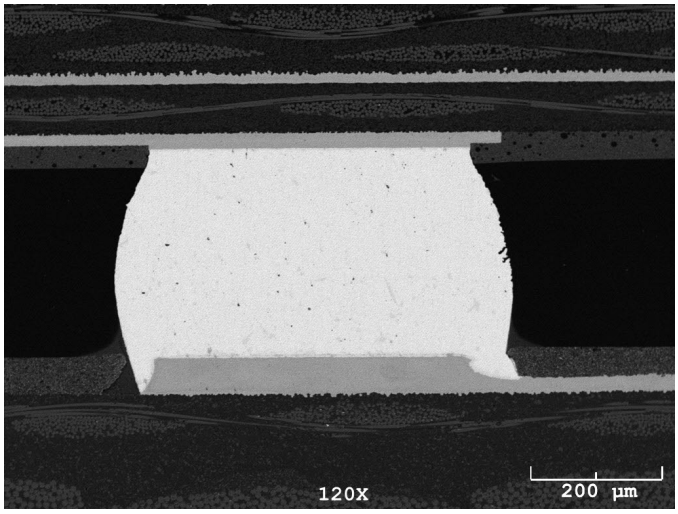


Figure 4. Scanning Electron Microscope (SEM) Image of a Well Soldered 292 MAPBGA Solder-Joint (Package Top / PCB Bottom)

4.2 PCB Pad Design

Freescale follows the Generic Requirements for Surface Mount Design and Land Pattern Standards from the Institute for Printed Circuits (IPC), IPC-7351B. This document and an accompanying land pattern calculator can be purchased from the IPC's website (http://landpatterns.ipc.org/default.asp) and includes guidelines for BGAs based on assumed package dimensions.

Many MAPBGA products do not have fully populated arrays to allow for better PCB (printed circuit board) routing. PCB design must ensure the final footprint matches the part.

4.2.1 Pad Diameter

For pitches at or above 0.80 mm, the first estimate for PCB solderable diameter is one half the pitch. For pitches at or below 0.65 mm, the solderable diameter is generally larger than one-half pitch in diameter (Table 1).

Table 1. Suggested PCB Pad Diameters by BGA Pitch

BGA Pitch (mm)	Suggested PCB Pad Diameter (mm)
1.00	0.500
0.80	0.400
0.65	0.325
0.50	0.300
0.40	0.225

Note: Some legacy products may have alternate pitches.

4.2.2 Pad Surface Finishes

Almost all PCB finishes are compatible with MAPBGAs, including Hot Air Solder Leveled (HASL), Organic Solderability Protectant (OSP), Electroless Nickel Immersion Gold (ENIG), Immersion Sn, and Immersion Ag. Freescale suggests the PCB surface finish shelf life be monitored to ensure the life has not “expired”. Surfaces should always be free of dirt and grease before PCB assembly.

4.2.3 Solder Mask Layer

Freescale encourages customers to use Non-solder Mask Defined (NSMD) PCB pad designs, which typically provides better thermal fatigue life. Some field use conditions may require the use of Solder Mask Defined (SMD) pads for better drop/shock survivability. The difference between NSMD and SMD is shown in Figure 5.

NSMD Pad Design **SMD Pad Design**

Figure 5. NSMD and SMD Pad Designs

The NSMD solder mask opening diameter is suggested to be 0.125 mm larger than the solderable area (i.e. Cu diameter). However, it is critical to understand the PCB fabrication capabilities of PCB suppliers. Also, finer BGA pitches may require <0.125 mm in order to meet PCB routing requirements.

SMD pads (compared to NSMD) have a larger Cu diameter which means more Cu is joined to the PCB laminate. Copper diameter for SMD is 0.125 mm larger than solder mask opening diameter. This increased diameter makes pad cratering on the PCB more difficult, and therefore increases drop/shock life. For SMD at smaller pitches, a key factor of picking the Cu diameter and solder mask diameter is PCB vendor capabilities. Inspection of delivered PCBs for solder mask registration is encouraged.

5 Board Assembly

5.1 Assembly Process Flow

A typical Surface Mount Technology (SMT) process flow is shown in Figure 6.

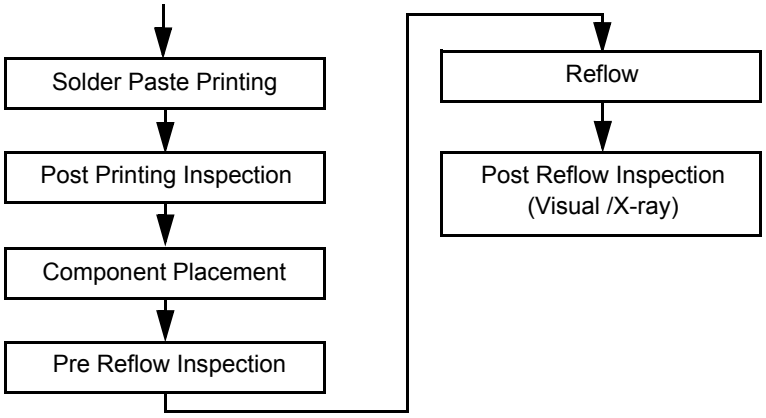


Figure 6. SMT Process Flow

5.2 Solder Stencil/Solder Paste

5.2.1 Stencil Thickness

Solder paste stencil design is critical for good solder joint formation, especially as the BGA pitch decreases. The thickness of the stencil determines the amount of solder paste deposited onto the printed circuit board land pattern.

For 1.0 mm pitch parts, a common stencil thickness is 0.125 mm (5 mils), while 0.100 mm thick stencils (4 mils) are also used. In high reliability applications, 0.150 mm (6 mils) thick stencils are preferred. For 0.80 mm pitch, the 0.100 mm thick stencil is common.

For these stencils, well cut openings created with a laser or by chemical etch is preferred. The opening walls should be polished and a Ni finish is recommended. The goal is to have a stencil that properly releases a consistent volume of solder paste, print after print.

The stencils for BGA pitches at or below 0.65 mm have to consider other factors as well. Usually on a PCB, there may be other small size and small pitch components which prevent the stencil opening size to be reduced. Instead, the total stencil thickness is decreased. Typically, stencils are from 0.075 to 0.125 mm thick.

At smaller pitches, it may help to use square openings in place of round as shown in Figure 7 as it allows a slightly larger volume of solder paste to be released. Generally, the opening length or diameter is 1:1 with the solderable PCB diameter. For additional solder paste volume, the opening length/diameter can be increased.

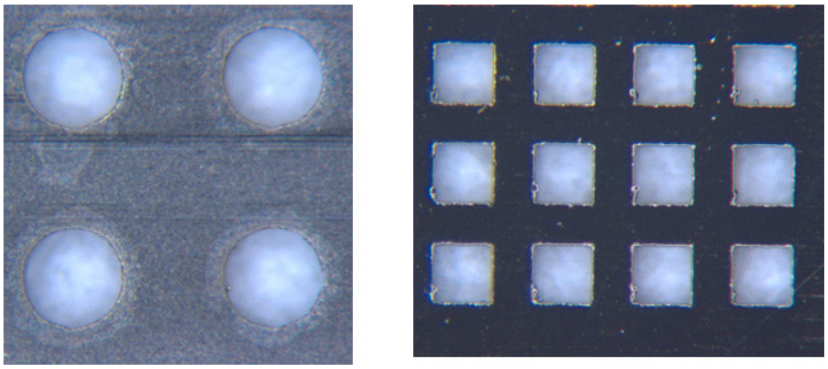


Figure 7. Round 0.8 mm and Square 0.4 mm Pitch Stencil Openings

Small pitch stencils frequently have specialized coatings to help with paste release. These coatings, frequently called nano-coatings, will wear out. A monitoring program for stencil age (number of prints) may be needed.

5.2.2 Solder Paste Properties

Solder paste is one of the most important materials in the SMT assembly process. It is a homogenous mixture of metal alloy, flux, and viscosity modifiers. The metal alloy particles are made in specific size and shape. Flux has a direct effect on soldering and cleaning, and it is used to precondition the surfaces for soldering (by removing minor surface contamination and oxidation).

There are two different flux systems commonly available:

- The first type of flux system requires cleaning, such as standard rosin chemistries and water-soluble chemistries. Standard rosin chemistries are normally cleaned with solvents, semi-aqueous solutions or aqueous/saponifier solutions, while the water-soluble chemistries are cleaned with pure water.
- The second type of flux system type requires no cleaning, but normally a little residue remains on the PCB after soldering.

Solder paste grain size can be useful to manipulate by pitch. For larger pitch parts, 0.80 mm and larger, Type 3 solder powder (25 to 45 micron grain size) is widely used. At the pitches, 0.65 mm and smaller, Type 4 solder (20 to 38 microns grain size) may provide a better solder joint.

5.3 Component Placement

The high lead interconnection and insertion density requires precise and accurate placement tools. To meet this requirement, the placement machine should be equipped with optical recognition systems, i.e., vision system, for the centering of the PCB as well as the components during the pick and place motion. A placement accuracy study is recommended in order to calculate compensations required. Freescale follows EIA-481D standard for tape and reel orientation, as shown in Figure 8. Also see the Packing of Devices section for additional details.

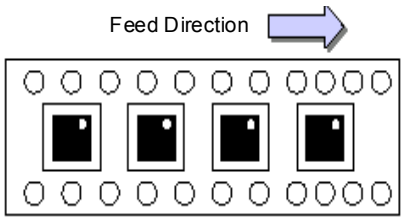


Figure 8. MAPBGA Orientation in Tape and Reel

5.4 Soldering

A typical profile band is shown in Figure 9. The actual profile parameters depend upon the solder paste used, and recommendations from paste manufacturers should be followed. Temperature profile is the most important control in reflow soldering and it must be fine-tuned to establish a robust process. In most cases, thermocouples should be placed under the heaviest thermal mass device on the PCB to monitor the reflow profile. Generally, when the heaviest thermal mass device reaches reflow temperatures, all other components on the PCB will reach reflow temperatures as well.

Dry air is a common reflow furnace atmosphere. Nitrogen reflow is recommended to improve solderability and to reduce defects (like solder balling). It is also recommended to monitor the temperature profile of package top surfaces to validate the package peak temperature does not exceed MSL classification of individual devices.

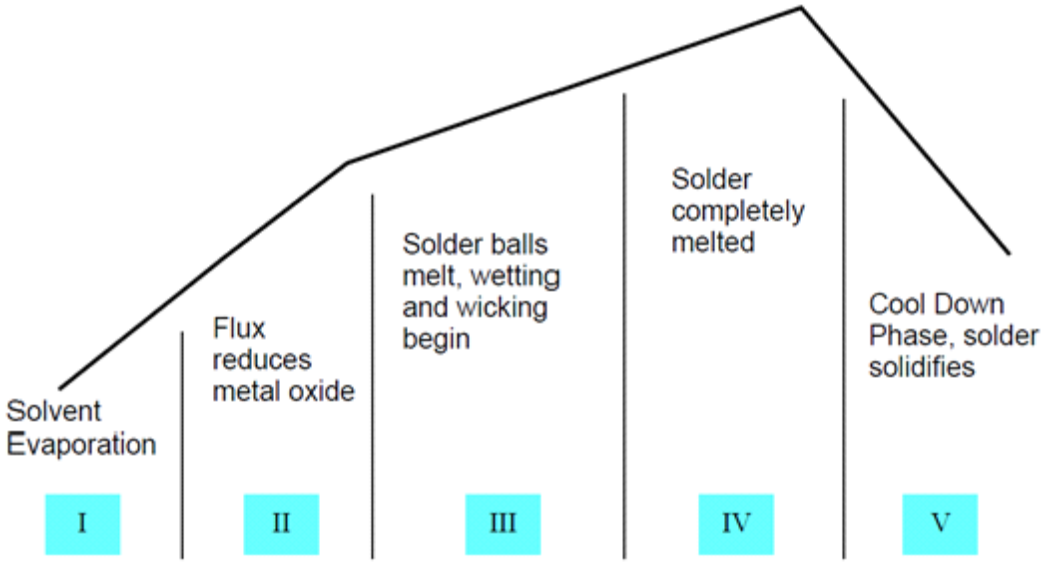


Figure 9. General Solder Reflow Phases

For all devices on the PCB, the solder paste needs to be taken into account for the reflow profile. Every paste has a flux, and the flux dominates the reflow profile for steps like soak time, soak temperature, and ramp rates. Peak reflow temperature is the melting temperature of the metals in the paste, plus a “safety” margin to ensure that all solder paste on the PCB reflows.

Deviation from the reflow profile recommended by the paste manufacturer should be evaluated first using a copper (Cu) coupon test. The horizontal size for a typical solder paste volume is measured as either a diameter or as “x” and “y” lengths. The Cu coupon is then reflowed and the solder paste volume is measured for either diameter or “x” and “y”. The goal is to have a reflow profile with the most horizontal spread. For best results, the Cu coupon should be lightly sanded before use to remove Cu-oxide build up. PCB should be rated for multiple reflow of MSL classification. Cross referencing with the device data sheet is recommended for any additional board assembly guidelines specific to the exact device used.

Freescale provides at www.freescale.com, an application note with general comments on reflow profiles. AN3300 General Soldering Temperature Process Guidelines is a useful starting point.

5.5 Inspection

The solder joints of MAPBGA parts are formed **underneath the package**. To verify any open or short-circuits (bridging) after reflow, non-destructive vision/optical inspection and X-ray inspection are recommended to verify any open or short-circuit after reflow soldering. Micro-sectioning is another method of inspecting solder joint quality during process optimizations, but it is less suitable to production inspection (due to slow processing). Figure 10 shows the expected x-ray image of a soldered component.

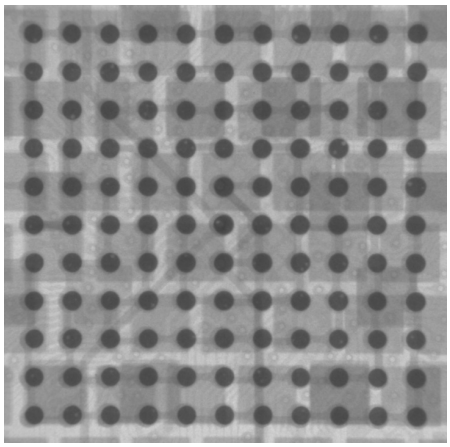
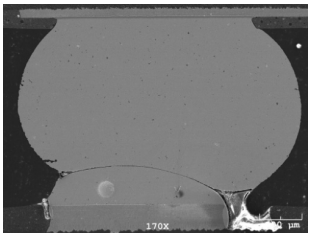


Figure 10. Inspection X-ray of a MAPBGA package

5.6 Common MAPBGA Solder-Joint Defects

Head in Pillow

(Solder paste and solder ball melt but do not join)



Solder Bridge

(Solder paste and solder ball merge during reflow from poor paste printing)

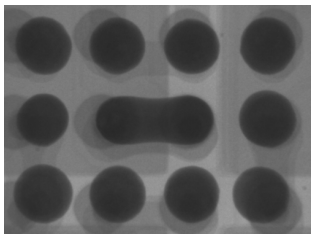


Figure 11. Two Common MAPBGA Solder-Joint Defects

6 Repair and Rework Procedure

6.1 Repairing

Repairing a single solder joint of MAPBGA is not recommended, because the joint is **underneath the package**.

6.2 Reworking

If a defective component is observed after board assembly, the device can be removed and replaced by a new one. This rework can be performed using the heating methods described in this section.

When performing the rework:

- The influence of the heating on adjacent packages must be minimized. Do not exceed the temperature rating of the adjacent package
- Heating conditions will differ due to differences in the heat capacities of the PCB (board thickness, number of layers) and mounted components used. Thus, the conditions must be set to correspond to the actual product and its mounted components
- Freescale follows industry-standard component level qualification requirements, which include three solder reflow passes. The three reflow passes simulate board level attach to a double-sided board and includes one rework pass. The removed package should be properly disposed of, so they will not mix in with new components

A typical rework flow process comprises six stages:

1. Tooling Preparation
2. Package Removal
3. Site Redressing
4. Solder Paste Printing
5. Package Remount
6. Reflow Soldering

NOTE: Freescale product quality guaranty/warranty does not apply to products that have been removed, thus, component reuse should be avoided.

In any rework, the PCB is heated. The thermal limits of PCB and components (e.g., MSL information) must be followed. During heating, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the components and PCB. In order to prevent moisture induced failures, it is recommended the PCBs and components have had strict storage control with a controlled environment (such as dry air or nitrogen). In addition, a pre-bake (e.g., 125 °C for 24 hours for boards with SMT components, or 95 °C for 24 hours for boards with temperature sensitive components) is recommended to remove the moisture from components and the PCB prior to removal of the package, if the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly.

Individual process steps for reworking a MAPBGA package are described in subsequent sections:

6.2.1 Tooling Preparation

Various rework systems are available on the market. In general, the rework station should have a split light system, an XY table for alignment, and a hot air system (with a top and bottom heater for component removal). For processing MAPBGA packages, a system should meet the following requirements:

- **Heating** – Controlled hot air transfer (temperature and air flow) to both the MAPBGA package and its mounted PCB is strongly recommended. The heating must be appropriate for the correct package size and thermal mass. PCB preheating from beneath is recommended. Infrared heating can be applied, especially for preheating the PCB from the underside, but it should only augment the hot air flow from the upper side. Nitrogen can be used instead of air. Additional information can be found in Package Removal.
- **Vision system** – The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of the package to PCB, a split light system should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.
- **Moving and additional tools** – Placement equipment should have good accuracy. In addition, special vacuum tools may be required to remove solder residue from PCB pads.

6.2.2 Package Removal

If a component is suspected to be defective and is returned, no further defects must be introduced to the device during removal of the component from the PCB as this may interfere with subsequent failure analysis. The following recommendations are intended to reduce the chances of damaging a component during removal:

- **Moisture removal** – Dry bake components before removal at 125 °C for 16 to 24 hours for boards with SMT components, or at 95 °C for 16 – 24 hours for boards with temperature-sensitive components
- **Temperature profile** – During de-soldering, ensure that the package peak temperature is not higher and that the temperature ramps are not steeper than the standard assembly reflow process
- **Mechanics** – Do not to apply high mechanical forces for removal. High force can damage the component and/or the PCB, which may limit failure analysis of the package. For large packages, wands can be used (implemented on most rework systems). For small packages, tweezers may be more practical.

If suspected components are fragile, it is especially necessary to determine if they can be electrically tested directly after de-soldering, or if these components have to be preconditioned prior to testing. In this case, or if safe removal of the suspected component is not possible or too risky, the whole PCB or the part of the PCB containing the defective component should be returned.

To remove the faulty component from the board, hot air should be applied from the top and bottom heaters. An air nozzle of correct size should be used to conduct the heat to the MAPBGA package such that a vacuum pick up tool can properly remove the component. The temperature setting for the top heater and the bottom heater is dependent on the component rating. Many assembly sites have extensive in-house knowledge on rework, and their experts should be consulted for further guidance.

If the PCB is large, it is important to avoid bending of the printed circuit material due to thermal stress, so a bending prevention tool must be placed on the bottom of the printed circuit board, and a bottom heater installed to allow heating of the entire printed circuit board in order to raise work efficiency.

6.2.3 Site Redressing

After the component is removed, the PCB pads have to be cleaned to remove solder residue, to prepare for the new component placement. This may be completed by vacuum de-soldering, solder sucker, solder wick braid, etc. after applying flux. Remaining solder residue and projections cause the solder stencil to not closely adhere to the PCB during solder paste printing, leading to improper solder paste supply during component mount.

Moreover, when the solder residue flows all the way to an adjacent through-hole, the solder paste printed on the pad can be transferred, via suction, to the through-hole during reflow, which may cause improper connection. A solvent may be necessary to clean the PCB of flux residue. A de-soldering station can be used for solder dressing. It should be noted that the applied temperature should not exceed 245 °C, which can contribute to PCB pad peeling from the PCB. This is typically a manual operation which is directly attributed to experience and skill.

Non-abrasive or soft bristle brushes should be used as abrasive brushes can contribute to bad solder joints (e.g. steel brushes). Prior to placing a new component on the site, solder paste should be applied to each PCB pad by printing or dispensing. A no-clean solder paste is recommended.

6.2.4 Solder Paste Printing

Solder supply during rework is done using specialized templates and tools. A mini-stencil with the same stencil thickness, aperture opening, and pattern as the normal stencil are placed in the component site. A mini-metal squeegee blade deposits solder paste in the specific area. See Figure 12. The printed pad should be inspected to ensure even and sufficient solder paste before component placement.

In situations where neighboring parts are at close proximity with the MAPBGA components, and the mini-stencil method is not an option, apply solder paste carefully on each pad using a paste dispensing system. The volume of solder paste must be controlled to prevent shorting on the component and/or neighboring components.

Depending upon allowed customer reliability standards, a flux only application to either the replacement part or to the reworked PCB may be sufficient for joining a MAPBGA part to the board. Flux choice is critical and should be of the same standards as for the original PCB assembly.

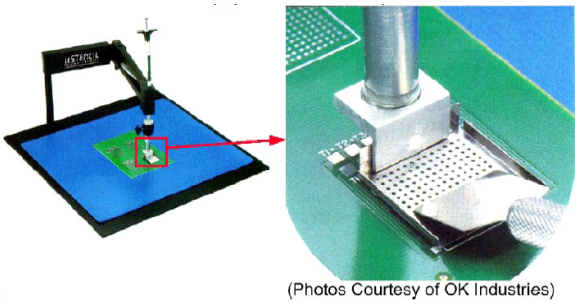


Figure 12. Mini-stencil and Mini-squeegee

6.2.5 Package Remount

After preparing the site, the new package can be placed onto the PCB. Handling of the replacement package should also follow the guidelines of the Moisture Sensitivity Level section. When remounting the package, it is recommended to use rework equipment that has good optical or video vision capability. A split light system displays images of both package balls and PCB pads by superimposing the two images. Alignment of the balls and pads is completed by adjusting the XY table.

Regular ball array MAPBGA exhibits self-alignment in any direction including X-axis shift, Y-axis shift, and rotational misplacement. Thus perfect placement is not required. At least 50% on solder ball on PCB pad for all pads is the minimum goal for part placement accuracy.

6.2.6 Reflow Soldering

The new component is soldered to the PCB using the same temperature profile as the normal reflow soldering process, shown in the Soldering section. Reflow furnaces are not typically used for rework. Rather a dedicated rework station is used that does both part removal and new part joining. During soldering, the package peak temperature and temperature ramps cannot exceed those of the standard assembly reflow process.

In IR or convection processes, the temperature can vary greatly across the PCB depending on the furnace type, size and mass of components, and the location of components on the assembly. Additionally, rework stations only apply heat locally, not to the entire PCB. If nozzles are used to direct the heat, the nozzle size must be sufficiently large to encompass the entire part. Profiles must be carefully tested to determine the hottest and coolest points on the assembly. The hottest and coolest points should fall within recommended temperatures in the reflow profile. To monitor the process, thermocouples must be carefully attached with very small amounts of thermally conductive grease or epoxy directly to the solder joint interface between the package and board.

The materials used in rework do have a higher potential to create conductive traces/corrosion etc. compared to standard materials. The PCB might need to be cleaned if they do not clean in the “normal” process or the rework was not done using “no clean” materials.

7 Board Level Reliability

7.1 Testing Details

Solder Joint Reliability (SJR) testing is performed to determine a measure of board level reliability when exposed to thermal cycling. There are several different names for board-level reliability (BLR) that customers may see. These include: second level reliability (2nd level reliability), solder-joint reliability (SJR), and temperature cycling on board (TCoB).

Information provided here is based on experiments executed on MAPBGA devices using a daisy chain BGA configuration. Actual surface mount process and design optimizations are recommended to develop an application specific solution.

- For automotive grade product applications, the widely accepted temperature range for testing is -40 °C to +125 °C.
- Consumer SJR temperature cycling conditions may vary widely, depending on the application and specific user. Typically, Freescale consumer SJR testing is performed from 0 °C to +100 °C.

The preferred test method will vary by market and industry. For automotive, the primary test is a version of IPC-9701A, air temperature cycling. For the consumer market, JEDEC's drop test will be the primary test (JESD22-B111). Telecommunications uses both IPC-9701A and IPC-9702 (monotonic bend). Freescale may not test an electronic package at all and may not have all the tests for each market and industry.

Table 2 shows the Freescale standard test set-up for performing automotive board level solder joint reliability testing. For consumer markets, the board stack-up found in JESD22-B111 is commonly used, eight Cu layers and 1.0 mm total thickness. Telecommunications market parts use IPC-9701A/9702 stack-ups of eight Cu layers and 2.25 mm total thickness.

Table 2. Board Level Reliability Setup

PCB Board	• 1.58 mm thickness • Four Cu layer • OSP surface finish
Test Board Assembly	• Pb-free solder paste SAC387 • Reflow peak temperature for SAC assembly ~ 240 °C • Pb solder paste Sn63Pb37 • Reflow peak temperature for SnPb assembly ~ 220 °C • 0.100 mm thickness, Ni plated, laser cut and electro-polished stainless steel stencil

Cycling conditions	• Continuous in-situ daisy chain monitoring per IPC-9701A and IPC-SM-785
	• Air Temperature Cycling (ATC) for Automotive
	  • -40 °C/+125 °C
	  • 15 minute ramp/15 minute dwell
	  • One hour cycle time
	• Air Temperature Cycling (ATC) for Commercial & Industrial
	  • 0 °C/+100 °C
	  • 10 minute ramp/10 minute dwell
	  • 40 minute cycle time

Package Test Vehicle	• Production BOM package including die (die mechanically present, without wire bond connection) • Daisy chain in the BGA pattern connecting pairs of solder balls.

7.2 Solder Joint Reliability Results

Freescale experimentally gathers board-level reliability data for a variety of packages. To get results from these experiments (including Weibull plots), contact the Freescale sales team. Customers should interpret the Freescale solder joint reliability data to see how well they meet the final application requirements.

8 Thermal Characteristics

8.1 General Thermal Performance

Since the thermal performance of the package in the final application will depend on a number of factors (i.e. board design, power dissipation of other components on the same board, ambient temperature), the thermal package properties provided by Freescale should only serve as a guideline for the thermal application design. In applications where the thermal performance is considered to be critical, Freescale recommends to run application specific thermal calculations in the design phase to confirm the on-board thermal performance.

8.2 Package Thermal Characteristics

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

Additional factors to be considered in PCB design and the thermal rating of the final application (amongst others) are:

- Thermal resistance of the PCB (thermal conductivity of PCB traces, number of thermal vias, thermal conductivity of thermal vias)
- Quality and size of PCB solder joints (effective PCB pad size, potential solder voiding in the thermal path solder joints that may reduce the effective solder area)

The thermal characteristics of the package provide the thermal performance of the package when there are no nearby components dissipating significant amounts of heat. The stated values are meant to define the package thermal performance in a standardized environment.

Thermal properties of the individual products are usually given in the Freescale product data sheets as appropriate. Product data sheets are available at www.freescale.com. More detailed thermal properties may be requested by customers.

8.3 Package Thermal Properties—Definition

The thermal performance of a MAPBGA package is typically specified by thermal properties such as $R_{\theta JA}$, $R_{\theta JMA}$, $R_{\theta JB}$, $R_{\theta JC}$ and Ψ_{JT} (in °C/W). Thermal characterization is performed by physical measurement and by running complex simulation models under the following conditions:

- Two thermal board types:
  - Single-layer board (1s), per JEDEC JESD51-3 and JESD51-5 (exposed pad packages only)
  - Four-layer board (2s2p), per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only)
- Four boundary conditions:
  - Natural convection (still air), per JEDEC JESD51-2
  - Forced convection, per JEDEC JESD51-6
  - Thermal test board on ring style cold plate method, per JEDEC JESD51-8
  - Cold plate method, per MIL SPEC-883 method 1012.1

8.3.1 $R_{\theta JA}$: Theta Junction-to-Ambient Natural Convection (Still Air)

Junction-to-ambient thermal resistance (Theta-JA or $R_{\theta JA}$ per JEDEC JESD51-2) is a one-dimensional value that measures the conduction of heat from the junction (hottest temperature on die) to the environment (ambient) near the package in a still air environment. The heat that is generated on the die surface reaches the immediate environment along two paths:

- Convection and radiation off the exposed surface of the package, and
- Conduction into-and-through the test board, followed by convection and radiation off the exposed board surfaces.

8.3.2 $R_{\theta JMA}$: Theta Junction-to-Moving-Air Forced Convection

Junction-to-Moving-Air (Theta-JMA or $R_{\theta JMA}$ per JEDEC JESD51-6) is similar to $R_{\theta JA}$, but it measures the thermal performance of the package mounted on the specified thermal test board, when it is exposed to moving air (at 200 feet/minute) environment.

8.3.3 $R_{\theta JB}$: Theta Junction-to-Board

Junction-to-board thermal resistance (Theta-JB or $R_{\theta JB}$ per JEDEC JESD51-8) measures the horizontal spreading of heat between the junction and the board. The board temperature is measured on the top surface of the board near the package. The measurement is done using a high effective thermal conductivity four-layer test board (2s2p) per JEDEC JESD51-7. $R_{\theta JB}$ is frequently used by customers to create thermal models considering both package and application board thermal properties.

8.3.4 $R_{\theta JC}$: Theta Junction-to-Case

Junction-to-Case thermal resistance (Theta-JC or $R_{\theta JC}$ per MIL SPEC-883 Method 1012.1) indicates the average thermal resistance between the die and the case top surface, as measured by the cold plate method per MIL SPEC-883 Method 1012.1, with the cold plate temperature used for the case temperature. $R_{\theta JC}$ can be used to estimate the thermal performance of a package when the board is adhered to a metal housing or heat sink, or when a complete thermal analysis is done.

8.3.5 Ψ_{JT} (Psi JT): Junction-to-Package Top

Junction-to-Package top (Psi JT or Ψ_{JT}) indicates the temperature difference between the package top and the junction temperature, optionally measured in a still air condition (per JEDEC JESD51-2) or in a forced convection environment (per JEDEC JESD51-6). Ψ_{JT} must not be confused with the parameter $R_{\theta JC}$: $R_{\theta JC}$ is the thermal resistance from the device junction to the external surface of the package, with the package surface held at a constant temperature, while Ψ_{JT} is the value of the temperature difference between the package surface and the junction temperature, usually in natural convection.

8.4 Package Thermal Properties: An Example

Table 3 shows an example of the thermal characteristics typically shown in a Freescale product data sheet. The example applies to a package size 17.0 mm x 17.0 mm x 1.5 mm (max.), pitch 0.8 mm, 364 I/O, die size ~ 4.9 mm x 5.9 mm (Freescale case outline drawing 98ASA00418D)

Table 3. Thermal Parameters of a Package (17.0 mm x 17.0 mm x 1.5 mm)

Rating	Board Type	Parameter	W/o HS, 0.7 mold	With HS, 0.7 mold	W/o HS, 0.8 mold	With HS, 0.87 mold	Unit	Notes
Junction to Ambient (Natural Convection)	Single Layer board (1s)	$R_{\theta JA}$	45	37	45	37	°C/W	(1) (2)
Junction to Ambient (Natural Convection)	Four-layer board (2s2p)	$R_{\theta JA}$	28	22	28	22	°C/W	(1) (2) (3)
Junction to Ambient (at 200 ft/min)	Single Layer board (1s)	$R_{\theta JMA}$	37	29	37	30	°C/W	(1) (3)
Junction to Ambient (at 200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	24	19	24	19	°C/W	(1) (3)
Junction to Board		$R_{\theta JB}$	17	11	17	12	°C/W	(4)
Junction to Case		$R_{\theta JC}$	8.0	8.0	10	9.0	°C/W	(5)
Junction to Package Top	Natural Convection	Ψ_{JT}	2.0	7.0	2.0	8.0	°C/W	(6)

Notes
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board temperature) ambient temperature air flow power dissipation of other components on the board, and the thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the exposed pad surface as measured by the cold plate method (MIL Spec-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT

9 Case Outline Drawing, MCDS and MSL Rating

9.1 Downloading the Information from Freescale

Freescale offers Packaging, Environmental and Compliance information at www.freescale.com in the parametric tables and also in the device information details. Enter the part number in the search box and review the package information details of the specific part.

The complete case outline drawing and the Material Composition Declaration Sheet (MCDS), following the IPC-1752 reporting format, can be downloaded as a PDF file. Information on product specific Moisture Sensitivity Level (MSL) is also available in the part details.

9.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) indicates the floor life of the component and its storage conditions and handling precautions after the original container has been opened. The permissible time (from opening the moisture barrier bag until the final soldering process) that a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity.

In many cases, moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process. The expansion of trapped moisture can result in interfacial separation, known as delamination, of the mold compound from the die or substrate, wire bond damage, die damage, and internal cracks. In the most severe cases, the component will bulge and pop, known as the “popcorn” effect.

It is necessary to dry moisture-sensitive components, to seal them in a moisture barrier antistatic bag with a desiccant and a moisture indicator card. It needs to be vacuum sealed according to IPC/JEDEC J-STD-033 and only remove immediately prior to assembly to the PCB.

Table 4 presents the MSL definitions per IPC/JEDEC's J-STD-20. Refer to the “Moisture Sensitivity Caution Label” on the packing material, which contains information about the moisture sensitivity level of Freescale products. Components must be mounted and reflowed within the allowable period of time (floor life out of the bag), and the maximum reflow temperature that shall not be exceeded during board assembly at the customer's facility.

If moisture-sensitive components have been exposed to ambient air for longer than the specified time according to their MSL rating, or the humidity indicator card indicates too much moisture after opening a Moisture Barrier Bag (MBB), the components are required to be baked prior to the assembly process. Please refer to imprints/labels on the respective packing to determine allowable maximum temperature.

The higher the MSL value, the more attention is needed to store the components. Freescale packages use JEDEC standard IPC/JEDEC J-STD-020 for classification of its package.

Table 4. MSL Descriptions

Level Rating	Floor Life	
	Time	Conditions
1	Unlimited	30°C/85%RH
2	1 Year	30°C/60%RH
2a	4 Weeks	30°C/60%RH
3	168 Hours	30°C/60%RH
4	72 Hours	30°C/60%RH
5	48 Hours	30°C/60%RH
5a	24 Hours	30°C/60%RH
6	TOL	30°C/60%RH

TOL = Time on Label

10 Package Handling

10.1 Handling ESD Devices

Semiconductor Integrated Circuits (ICs) and components are Electrostatic-Discharge-Sensitive devices (ESDS), so proper precautions are required for handling and processing them. Electrostatic Discharge (ESD) is one of the significant factors leading to damage and failure of semiconductor ICs and components, and comprehensive ESD controls to protect ESDS during handling and processing should be considered.

The following industry standards describe detailed requirements of proper ESD controls; Freescale recommends meeting the standards before handling and processing ESDS. Detailed ESD specifications of devices are available in each device data sheet.

- JESD615-A, Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- IEC-101/61340-5, Specification for the Protection of Electronic Devices from Electrostatic Phenomena

10.2 Handling Moisture-Sensitive SMD Devices

MAPBGA devices are moisture/reflow-sensitive Surface Mount Devices (SMD) and proper precautions are required for handling, packing, shipping and use. Moisture from atmospheric humidity enters permeable packaging materials by diffusion. Assembly processes (which are used to solder SMD packages to PCBs) expose the entire package body to temperatures higher than 200 °C. As noted in the Moisture Sensitivity Level section, during solder reflow the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the package. Cracking and/or delamination can lead to failure and reliability problems, and proper handling of SMDs should be considered.

Dried moisture-sensitive SMDs are placed in tray or tape-and-reel, and dry packed for proper transportation and storage. SMDs are sealed with a desiccant material and a Humidity Indicator Card inside of a Moisture Barrier Bag (MBB). The shelf life of dry-packed SMDs are 12 months from the dry pack seal date (when stored in ≤ 40 °C/90%RH environment).

Proper use and storage of moisture-sensitive SMDs are required after a MBB is opened. Improper use and storage increases various quality and reliability risks. SMDs subjected to reflow solder or other high temperature process must be mounted within the period of floor environment specified by MSL, or stored per the J-STD-033B standard.

The baking of SMDs is required before mounting if any of following events occur:

- SMDs are exposed to a specified floor environment greater than specified period
- The Humidity Indicator Card shows >10% for level 2a – 5a, or shows >60% for level 2 devices when read at 23 ±5.0 °C environment
- SMDs are not stored according to the J-STD-033B standard

The baking procedure, and more detailed requirements and procedures of handling moisture-sensitive SMDs can be found in:

- IPC/JEDEC J-STD-033B, Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

10.3 Packing of Devices

MAPBGA devices are contained in Tray or Tape-and-Reel configurations; both Trays and Tape-and-Reel are dry packed for transportation and storage. Packing media are designed to protect devices from electrical, mechanical and chemical damages (as well as moisture absorption), but proper handling and storage of dry packs are recommended. Improper handling and storage (dropping dry packs, storage exceeding 40 °C/90%RH environment, excessive stacking of dry packs, etc.) will increase various quality and reliability risks.

- Tray
  - Freescale complies with standard JEDEC tray design configuration – See Figure 13.
  - Pin 1 of devices will be oriented with lead 1 toward the chamfered corner of the tray.
  - Trays are designed to be baked for moisture-sensitive SMDs, but the temperature rating of tray should NOT be exceeded when the devices are baked. The temperature rating can be found on the end-tab of the tray. The recommended baking temperature of trays is 125 °C.
  - Trays are typically banded together with 5 + 1 (5 fully loaded trays and 1 cover tray) stacking, and dry packed in a Moisture Barrier Bag. Partial stacking (1 + 1, 2 + 1, etc.) is also available, depending on individual requirements.

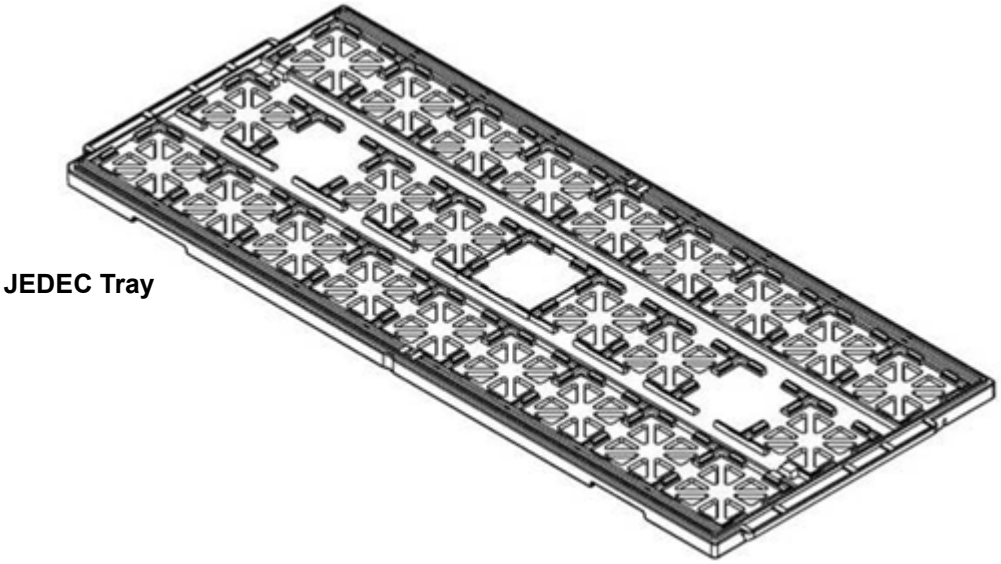


Figure 13. JEDEC Tray Example

- Tape-and-Reel
  - Freescale complies with EIA-481B and EIA-481C for carrier Tape-and-Reel configuration. See Figure 14 and Figure 15.
  - Freescale complies to Pin 1 orientation of devices with EIA-481D.
  - Tape-and-Reels are NOT designed to be baked at high temperatures.
  - Each Tape-and-Reel is typically dry packed in a Moisture Barrier Bag.

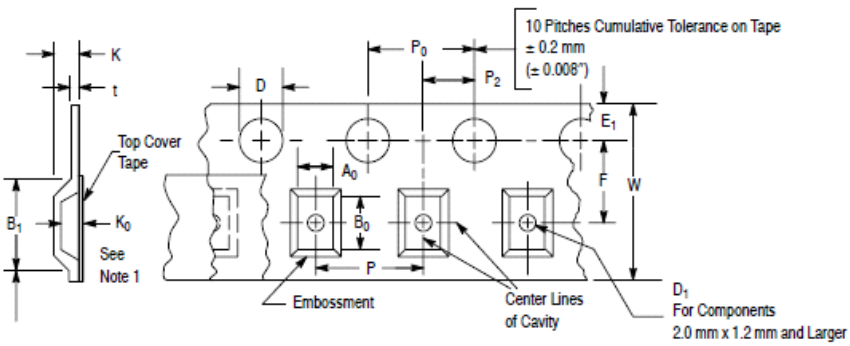


Figure 14. Carrier Tape Specifications

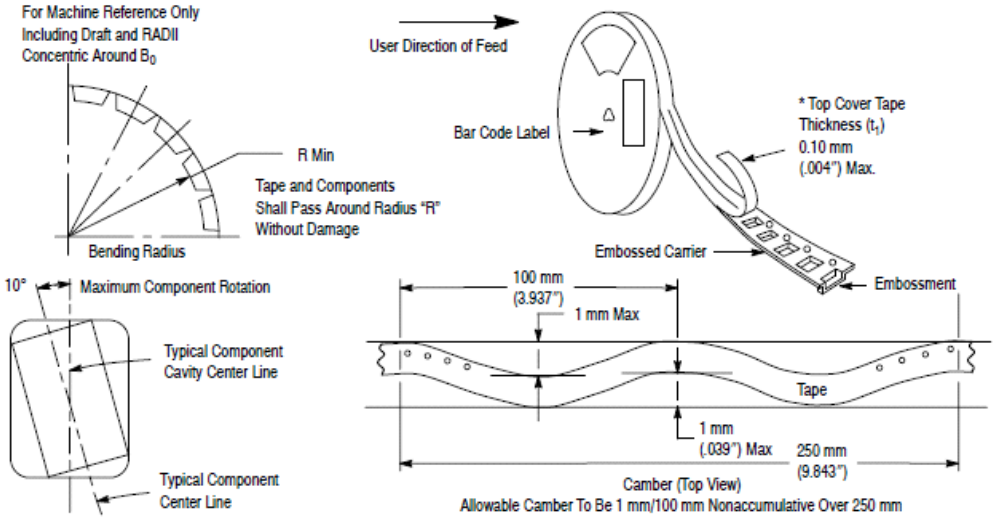


Figure 15. Tape and Reel Example

- Dry Packing:
  - Trays and Tape-and-Reels (loaded with devices) are sealed in a Moisture Barrier Bag, which are labeled and packed in dedicated boxes with dunnage (packing materials) for the final shipment.
  - Each dry pack bag contains a desiccant pouch and a Humidity Indicator Card.
  - Freescale encourages the recycling and reuse of materials whenever possible.
  - Freescale does not use packing media items processed with or containing class 1 Ozone Depleting Substances.
  - Whenever possible, Freescale shall design its packing configurations to optimize volumetric efficiency and package density, to minimize the amount of packing (dunnage) and packaging entering the industrial waste stream.

Freescale complies with following Environmental Standards Conformance guidelines/directives:

- ISPM 15, Guidelines for Regulating Wood Packaging Material in International Trade.
- European Parliament and Council Directive 94/62/EC of 20 December 1994, packaging and packaging waste.

11 References

[1] IPC/JEDEC J-STD-020C, Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices, July 2004.

[2] IPC/JEDEC J-STD-033B, Joint IPC/JEDEC Standard for handling, packing, shipping, and use of moisture/reflow sensitive surface-mount devices, January 2007.

[3] EIA-783, Guideline Orientation Standard for Multi-Connection Package (Design Rules for Tape and Reel Orientation), November 1998.

[4] EIA/JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air), December 1995.

[5] EIA/JESD51-8, Integrated Circuit Thermal Test Method Environmental Conditions - Junction-to-Board, October 1999.

[6] EIA/JESD 51-6, Integrated Circuits Thermal Test Method Environment Conditions - Forced Convection (Moving Air), March 1999.

[7] MIL SPEC-883 Method 1012.1, Thermal characteristics, February 2006.

[8] IPC-7351B, Generic Requirements for Surface Mount Design and Land Pattern Standards, June 2010.

[9]IPC-9701A, Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments, February 2006.

[10] IPC/JEDEC-9702, Monotonic Bend Characterization of Board-Level Interconnects, June 2004.

[11] IPC-SM-785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments, November 1992.

[12] JESD22-B111, Board Level Drop Test Method of Components for Handheld Electronic Products, July 2003.

[13] IPC-1752, Materials Declaration Management, June 2005.

[14] EIA-481, Standards – Excerpts used to assure complete alignment.

[15] JESD615-A, Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices.

[16] IEC-101/61340-5, Specification for the Protection of Electronic Devices from Electrostatic Phenomena.

12 Revision History

Revision	Date	Description
1.0	8/2014	• Initial release
2.0	9/2014	• Updated **Section 9.1**

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