VHDL Power estimation of CMOS Logic Cells

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Abstract— **This paper presents an improved VHDL implementation of a power- and delay model which accounts for input slope, output capacitive loading and glitches. The model parameters are based on a piece-wise linear fitting of the parameters to a number of Spice simulations for both the delay and power models. Results from VHDL simulations typically lie within 10% of the Spice results.**

Keywords— **VHDL, power estimation, Sea of Gates, CMOS, Spice.**

I. Introduction

In this paper we present an improved CMOS power model which accounts for signal slope and output load in deriving the power values. A VHDL power and delay model was developed by Dumitru [1] which showed that Spice accuracy can be achieved at VHDL simulation speeds. This model has been used as a basis for further improvements. A number of problems with Dumitru's approach have been solved and the accuracy of the model for larger circuits has been improved.

This paper is structured as follows: Section II presents a detailed overview of the existing power and delay model and presents three different designs of increasing complexity. Using HSpice and VHDL simulations using these designs the accuracy of Dumitru's model has been determined. Some improvements to increase the accuracy of the model are presented.

Section III presents the improved model as well as the corresponding VHDL implementation. Simulation results for this improved model are presented in section IV. We finish with conclusions and a discussion of the results in section V.

II. The existing Power&Delay model

A. Introduction

Dumitru's model is implemented as a VHDL package containing the needed datatypes and functions. It can be used for all VHDL gate level designs. Circuit power and delay can be determined by including the package with existing or new designs and using the datatypes supplied in the package as follows:

```
library ieee;
use ieee.std_logic_package.all;
use work.s_logic_package.all;

entity my_new_design is

   port (data : in s_logic ...
```

By using the datatype s_logic instead of std_logic signal value as well as the signal slope is passed between interconnected cells. The VHDL functions and descriptions in the package use the slope and capacitive load (passed as a Generic) information to calculate delay and power for the CMOS cells. The model parameters for a CMOS logic cell are derived from circuit simulations based on the cell's extracted layout using parasitic- and coupling capacitances and resistances. The delay and power parameters have been determined for the $1.6\mu m$ two metal layer Sea-of-Gates process.

The model is based on a piece-wise linear fitting of the model parameters to a number of Spice simulations.

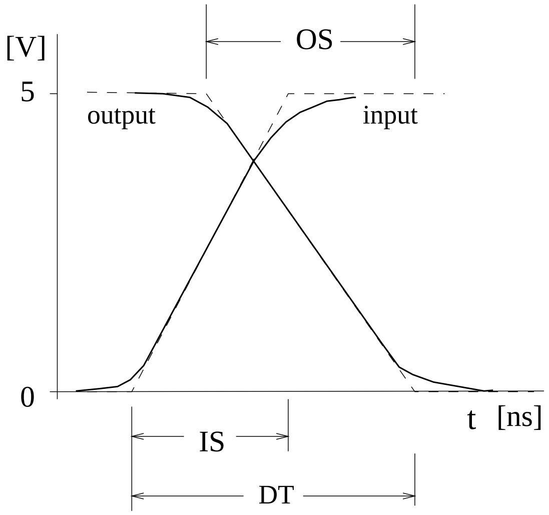

Fig. 1. Invertor delay time derived from input- and output slope.

The linearization is based on the observation that a CMOS logic gate has two modes of operation, one for relatively fast input slope signals and one for relatively slow input slope signals. Therefore the model distinguishes between two regions of operations seperated by a "critical slope" line, which is a linear function of the capacitive output load.

Figure 1 shows the delay time (DT) of an invertor gate as function of the input slope (IS). By modeling the delay time and output slope as functions of the input slope and the capacitive load based on the two modes of operation we can fit the linearizations to a number of Spice simulations. This is shown in figure 2. The model distinguishes between single input changes and simulatious switching inputs for two-input gates. Therefore the model of the nand, nor and exor gates contain two sets of parameters.

Both static and dynamic power is modeled. Energy dissipated during an output transition is estimated as:

$$E_n = \int_0^t V_{dd} \cdot i(t)dt \qquad (1)$$

where $i(t)$ is approximated by the slope of the input signal. For power modeling two global signals are defined in the VHDL package, `added_energy` and I_{med}. The signal I_{med} estimates the short circuit current which flows from V_{dd} to V_{ss} during the transition of the output of the CMOS cell. The value of I_{med} is derived from the output slope and the dissipated energy as:

$$I_{med} = E_n / (V_{dd} \cdot \text{Output Slope}) \qquad (2)$$

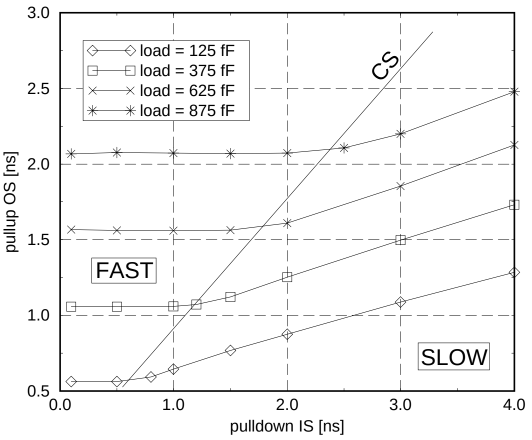

Fig. 2. Signal output slope for an invertor gate as function of the slope of the input signal and output load capacitance

TABLE I
THREE DESIGNS COMPARED

	nand gate	full adder	8 bit csa
Gates	1	6	137
I/O signals	3	6	30
Spice nodes	20	85	1025
Network elements	57	357	5500
MOS transistors	6	44	516

B. *Results*

We have tested the model on three different designs of increasing complexity to test the validity of the existing model, a two-input nand gate, a full-adder and an eight-bit carry select adder. Table I shows the complexity of these three circuits in number of gates, nodes and I/O signals as well as the number of nodes and MOS transistors in the corresponding layout. For HSpice simulations the circuits have been placed and routed on the 1.6μm Sea-of-Gates proces and extracted including lateral coupling capacitances. The simulators used were Vantage 6.000 and HSpice 96.3 from Meta-Software. The system used for all simulations is a HP9000/735 machine.

Table II presents the error of the VHDL model when compared to the HSpice[1] results.

B.1 The 2-input NAND gate

The 2-input Nand gate is simulated to determine the accuracy of a single gate from the model. Figure 3

[1] Level-3 transistor modeling was used

shows a plot of the HSpice circuit current[2] and the current calculated by the model based on the gate delay and capacitive load for a 2-input nand gate. We zoomed in to a single output transition to show a magnification of the error. It is clear from the figure that the amplitude of the approximation and the peak current time are significantly different from the HSpice results. When running HSpice the output node was loaded with a 128fF capacitor, the same load as is used by the model.

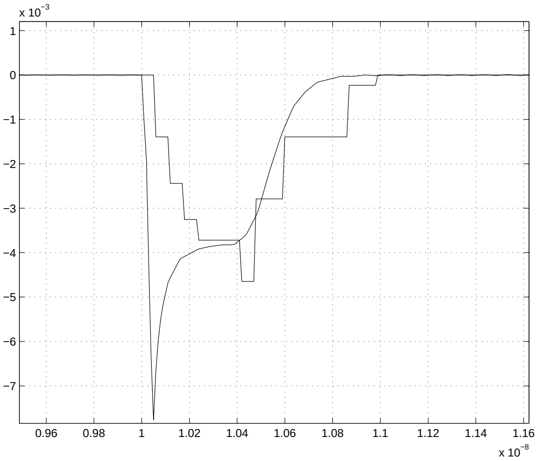

Fig. 3. "Nand" simulation results at the '11→00' input transition

B.2 The Full-Adder

The "full adder" testcircuit is used as a medium complexity test circuit. The full adder is shown in figure 4. As can be seen in the figure the critical path is from the inputs to the C_{out} output through 4 gates. Therefore this circuit's accuracy should give an indication of the model's accuracy for small circuits. Figure 5 shows a plot of the HSpice circuit current and the current calculated by the model based on the gate delay and capacitive load for a full adder. Again we zoomed in to a single transition to show the differences more clearly. The approximation is more accurate than the nand gate but the amplitude and delay in the current are still significantly different. All the outputs were loaded with 128fF capacitors, the same as in the model.

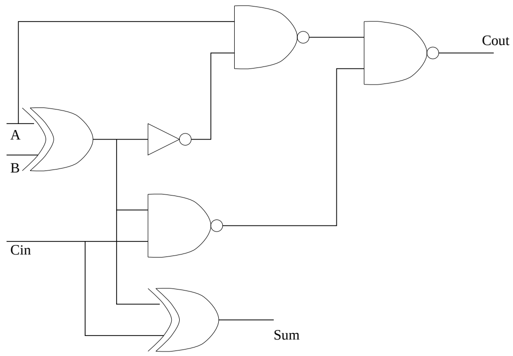

Fig. 4. "Full Adder"

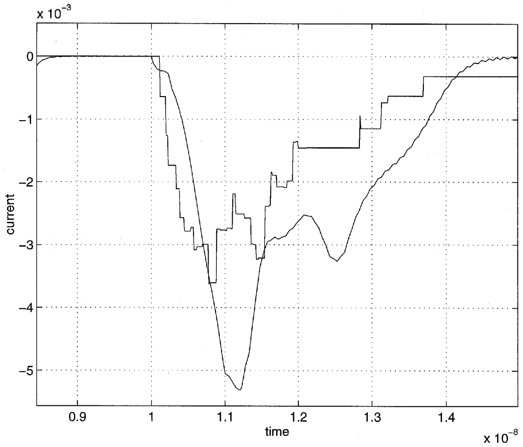

Fig. 5. "Full Adder" simulation results at the '100→110' and '110→010' input transition

B.3 The 8-bit Carry-Select Adder

The largest circuits used to test Dumitru's model is the 8 bit "Carry Select Adder" (CSA). The CSA is larger then the other two testcircuits and is used to determine the accuracy of the model fro larger circuits. The circuit has relatively large critical paths due to the propagating carry-signal within the circuit. The adder was built using the full adder from section II-B.2. The worst-case delay that can occur in this circuit is when a carry propagation occurs though the longest critical path, which runs through 4 full adders.

Figure 6 shows a cut from the current waveform. We zoomed in to a specific output transistion to magnify the results. As can be seen in the figure the delay and amplitude of the model are much too different from the HSpice results. The shape of the current waveform is fortunately quite similar to the HSpice waveform.

[2] For the sake of simplicity the circuit current is used instead of instantanious power consumption. Because the supply voltage is considered constant througout the circuit this is a valid approach.

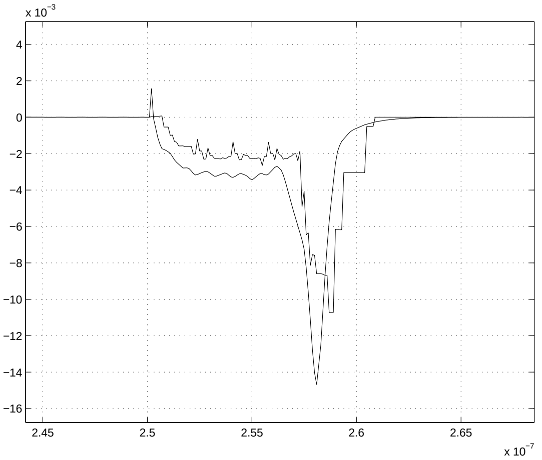

Fig. 6. "Carry Select Adder" simulation results at maximum adder delay due to carry propagation

TABLE II
Simulation results using Dumitru's model

	nand gate	full adder	8 bit csa
CPU time VHDL	0.20s	0.30s	0.983s
CPU time HSpice	3.85s	12.96s	47m11s
HSpice	25.6 pJ	393.3 pJ	1732.0 pJ
VHDL	22.3 pJ	340.8 pJ	2046.1 pJ
Error	12.9%	13.3%	15.3 %

C. *Discussion*

As can be seen from table II and the corresponding figures the results from the VHDL model are a reasonable approximation of the HSpice simulations in shape and delay but the accuracy is not within 10% of the HSpice results. For all three circuits the delay and amplitude as estimated by Dumitru's model should be more accurate to give good power and delay estimation for larger circuits. The shape of the signals is similar, but there are still a few shortcomings that need to be addressed.

Some improvable features of the current model are:

- The capacitive load on the output of a gate is declared as a Generic and is therefore a constant for all gates. It can be manually adjusted for each gate but this is cumbersome work for larger circuits. Because the load depends heavily on the number of connected gates, this is not an accurate approximation.
- The model uses seven rectangles to approximate the exponential current pulses.
- No component specific current waveforms. The model groups all currents into one global signal.
- The chosen VHDL implementation causes compatibility problems with most VHDL simulators when dealing with vector signals.
- Because wire capacitance is not modeled, there can be small differences in delay approximation between the SPICE and VHDL simulations.
- No modeling of glitches[3]. As shown in [2] a significant part of the total circuit power is dissipated during glitches. Figure 7 shows an output glitch as encountered while testing the 2-input nand from section II-B.1.
- No standard format for the used parameters. A generic file format for the cell-parameters, together with an automated parameter generator would improve the portability of the model. E.g. a SDF-type file to parameter convertor.

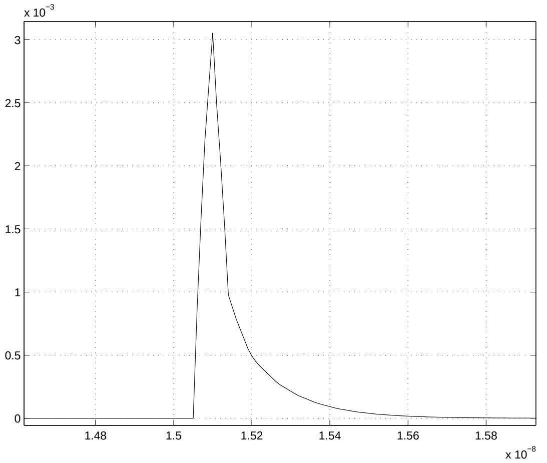

Fig. 7. Output glitch from the 2-input nand gate

III. Improving the model

A. *Introduction*

As shown in the previous section some improvements can still be made to improve the accuracy. While testing the model we concluded that the accuracy can be improved if a number of the shortcomings are eliminated. In this section I propose two improvements, better "current modeling" and "glitch modeling".

B. *Current modeling*

The current implementation models the short-circuit current I_{sc} which appears during the transition of the

[3] See section III-C

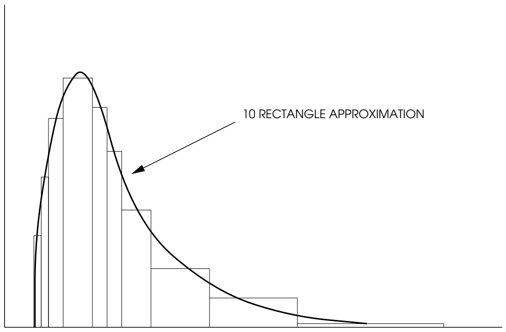

Fig. 8. An ideal invertor current pulse with 10 rectangles as approximation

output signal with seven rectangular shapes (see the example in figure 8). This closely models the peak value of I_{sc} but causes increasing inaccuracies with larger circuits when rectangles from different gates partly overlap as can be seen in figure 6.

A better approximation is to use more rectangular shapes where the derivative of the current pulse is high and less rectangles where it is lower. We have implemented a 10 rectangle approximation of the ideal current pulse.

C. Glitches

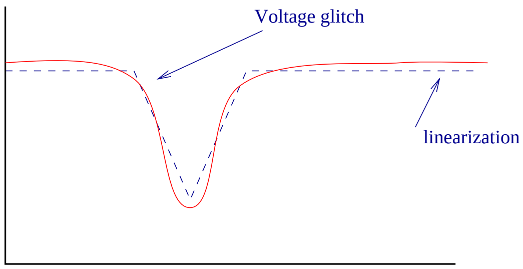

Fig. 9. Linearized output transition

Figure 9 shows a simplified incomplete signal transistion, usually called a glitch. An incomplete signal transistion can occur as the result of two colliding output waveforms with opposite directions which are caused by two different input transitions. Eg. a 2-input nand gate with two inputs switching almost simultaniously will show a glitch on the output. Also an invertor can show a glitch on the output when the input signal does not cross the threshold voltage needed to switch the logic value of the output.

When one of the inputs of a multi-input CMOS gate changes but the logic value of the output remains the same the output of a gate can, similar to the colliding waveform glitch, display a partial signal transition due to the nature of the transistors used. Figure 7 shows a glitch on the output of the 2-input nand gate. When a glitch occurs the fanout capacitance C_l of the CMOS gate is not fully charged or discharged. The power consumed when C_l is charged or discharged is given as

$$P = \frac{1}{2} \cdot C_l \cdot V_{dd}^2 \tag{3}$$

When C_l is not fully charged and discharged (or vice versa) we can write this as:

$$P = \frac{1}{2} \cdot C_l \cdot V_{dd} \cdot \lim_{T \to \infty} \frac{\sum_i |\Delta V_i|}{T} \tag{4}$$

We can model the power dissipation of an output glitch by using 4 parameters. We can linearize the signal as seen in figure 9 by using the peak glitch voltage ΔV, the glitch peak time t_g, the initial delay t_d and the end time t_e, as can be seen in figure 10.

We considered two different kinds of input glitches but modeling these seperately we need 4 sets of parameters (16) for each of the nand2, nor2 and exor2 gates (2 logic values and two types of glitches) and 2 sets of parameters (8) for the buffer and invertor gates. By using one model for both types of glitches and using the parameters to average the power dissipated during a glitch we can reduce the number of parameters to 8 for the two-input gates and 8 for the single-input gates. By averaging the HSpice simulation results when determining the parameters the error made averages out for larger circuits.

We can rewrite the power dissipation given by equation 4 as:

$$\text{Added energy} = \frac{(t_e - t_d) \cdot V_{dd} \cdot \Delta V}{2 \cdot (t_g - t_d) \cdot (t_e - t_g)} \cdot C_l \tag{5}$$

The four parameters t_d, t_g, t_e and ΔV have been determined for the existing library cells for the different logic values and have been added to the model. Three HSpice simulations were done for each gate to determine the parameters.

IV. Testing the new model

A. Introduction

The two improvements suggested in the previous section have been implemented in the existing VHDL model. This section presents the simulation results from the new model and compares them to the previous version.

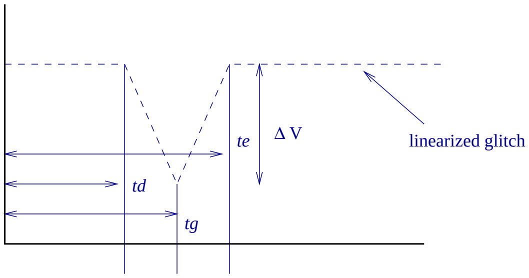

Fig. 10. Parameter estimation for (linearized) glitches

TABLE III
Simulation results for the improved model

	nand gate	full adder	8 bit csa
CPU time VHDL	0.33s	0.35s	1.07s
CPU time HSpice	3.85s	12.96s	47m11s
HSpice	25.6 pJ	393.3 pJ	1732.0 pJ
VHDL	28.2 pJ	428.6 pJ	1846.7 pJ
Error	9.2%	8.2%	6.2 %

B. Results

To visualize the improvements in the model we tested the improved model on the same circuits as in section II. Table III show the results compared to the HSpice simulations. As can be seen from table III the results from the improved model are closer to the HSpice results than the original model.

B.1 The 2-input NAND gate

When we compare the simulation from figure 3 to the results from the improved version (figure 12) we see that the amplitude and delay inaccuracies are still present. The error made is smaller though because the total power dissipated by the nand (area under the curve) is modeled more accurately. The peak value of the current is still not accurately modeled.

Figures 12 and 13 show the HSpice glitches on the output compared to the model. The modeling is not accurate for the peak value but the estimation of the energy contained in the glitch is within 10%. When comapring the two figures we see that on the 1-input change glitch the modeling "overestimates" the consumed energy and that on the 2-input change (colliding waveforms) the energy consumption is "underestimated".

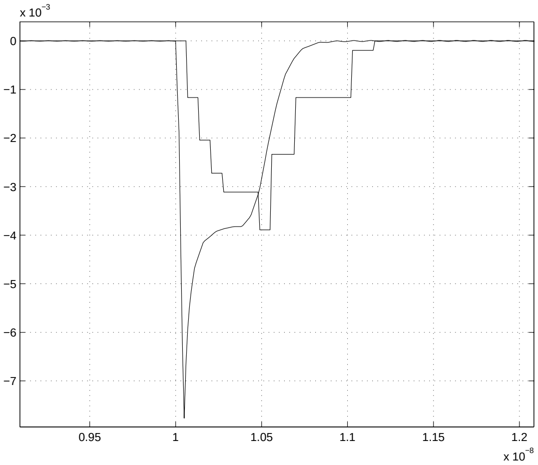

Fig. 11. "Nand" simulation results at the '11→00' transition

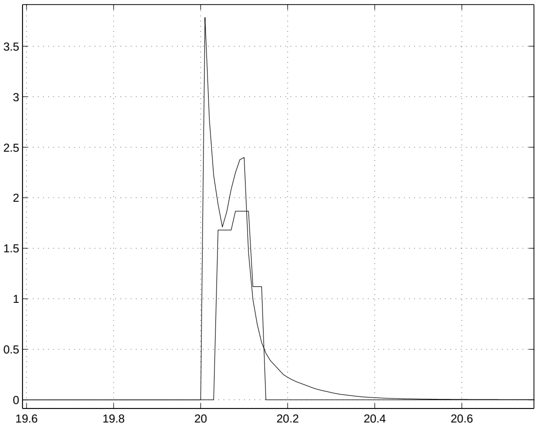

Fig. 12. "Nand" output glitch model, colliding waveforms glitch

B.2 The Full-Adder

Figure 14 show the HSpice and model current waveforms for the full adder. Inaccuracies occur around $12.5ns$, which might be caused by a wrong estimation of the fan-out capacitance C_l.

B.3 The 8-bit Carry-Select Adder

The Carry-Select Adder is the largest circuits tested with the model. As can be seen in figure 15 the modeling of the current is quite accurate. Only at $106.7ns$ there is a glitch that does not occur in the HSpice results. This might be caused by a partial overlap of the rectangles

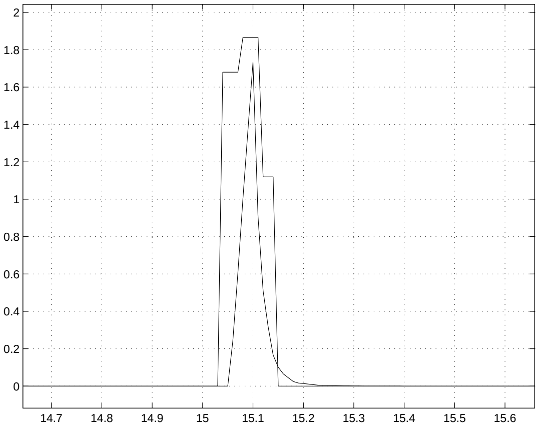

Fig. 13. "Nand" output glitch model, one input change glitch

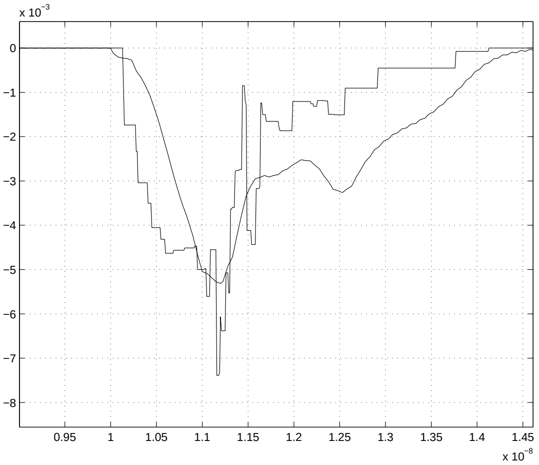

Fig. 14. "Full Adder" simulation results for the improved model at a single output transition

V. Conclusions

Power and delay modeling using VHDL is a good alternative for SPICE simulations. Especially when designing large circuits, which we are unable to test with circuit simulators, we benefit from the large speedup experienced with VHDL simulation.

We have improved the model as developed by Dumitru [1] to more closely match real world simulation results. The model now takes glitches into account, both for colliding waveforms as well as glitches caused by input changes that should not affect the output.

We have shown that even for large circuits the model retains its validity and closely matches the output generated by sophisticated circuit simulators. We now have a VHDL power and delay model whose results lie within 10% of SPICE's results.

There is still room for improvements though. There is no standard file format for the cell parameters. An application was developed to determine the parameters for the different cells but a transition of the model to a different technology is not straitforward and very time consuming. Also, a solution has to be found for improving the capacitive load coupling at the output of the gates. The model could be adapted to a "two pass" system where the load on the gates would be determined in a different run than the actual VHDL simulation. Also we need to determine the accuracy of the model for really large circuits (thousands of gates).

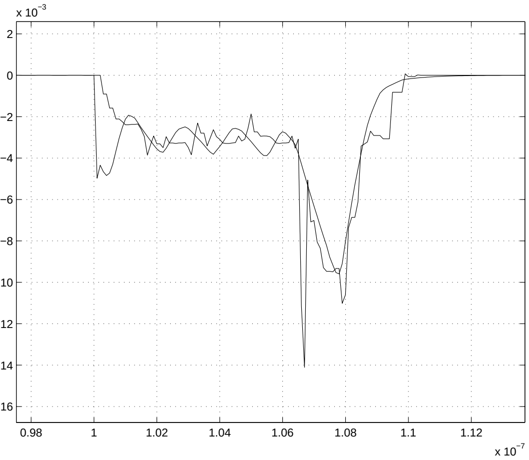

Fig. 15. "Carry Select Adder" simulation results for the improved model for a single output transition

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