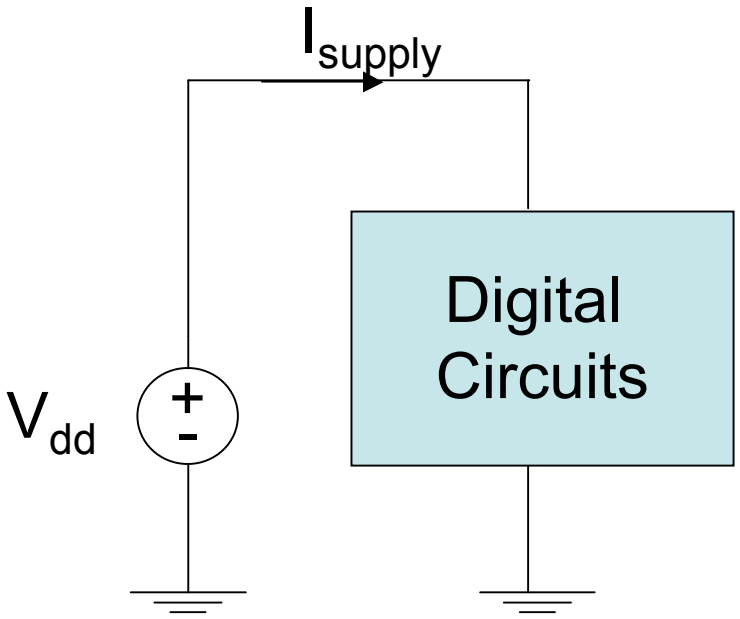
Power Estimation in Digital Circuits

ECE4420

Reading 5.8

Average Power Consumption Over a Clock Period



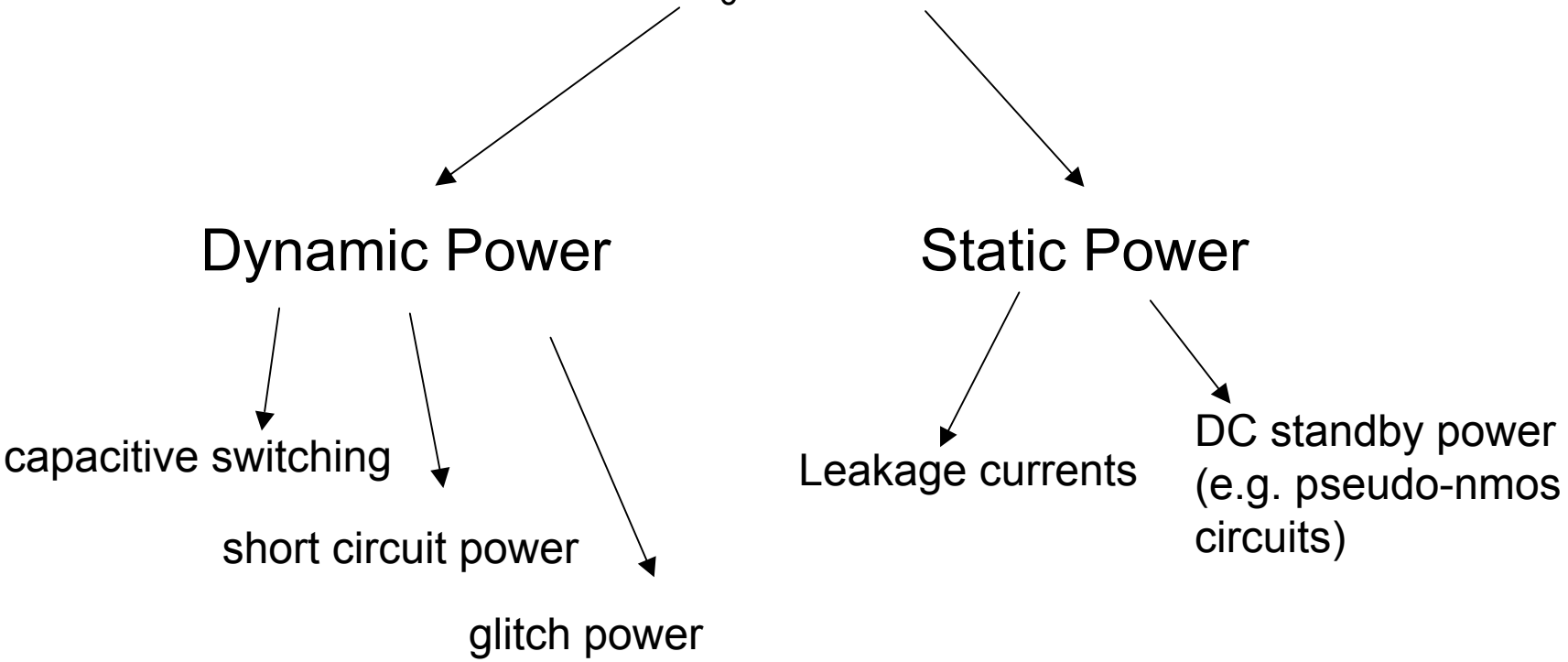
Understand instantaneous power vs. average power concept!

$$\overline{P}_{switching} = \frac{1}{T_{clk}} \int_0^{T_{clk}} V_{dd} * I_{\text{supply}}(t)dt = f_{clk} \int_0^{T_{clk}} V_{dd} * I_{\text{supply}}(t)dt$$

Average power per clock period

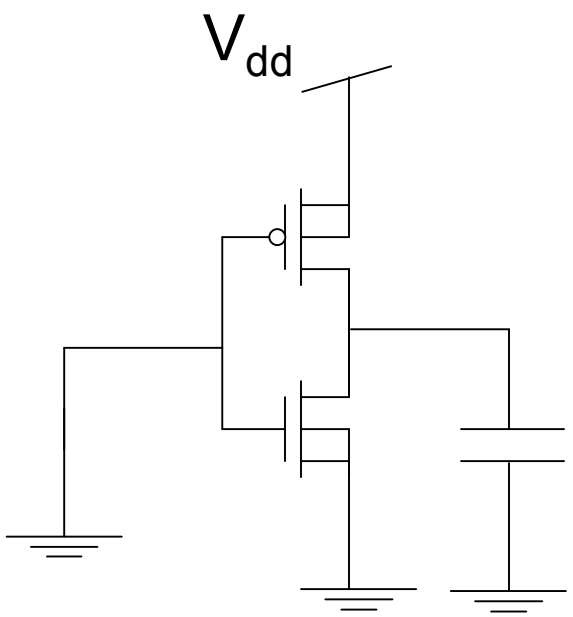
Power Components

$$\overline{P} = f_{clk} \int_0^{T_{clk}} Vdd * I_{supply} dt$$

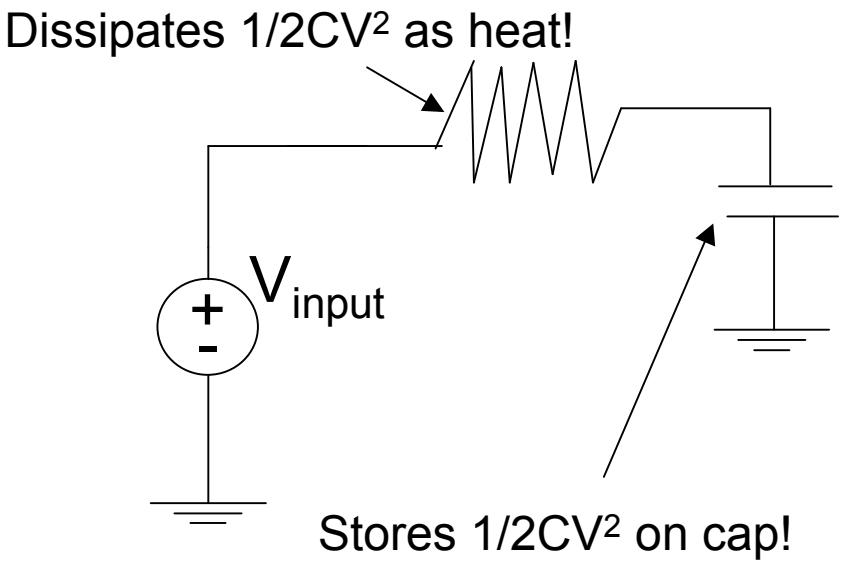


Dynamic Power: Capacitive Switching

Due to charging and discharging of capacitors!

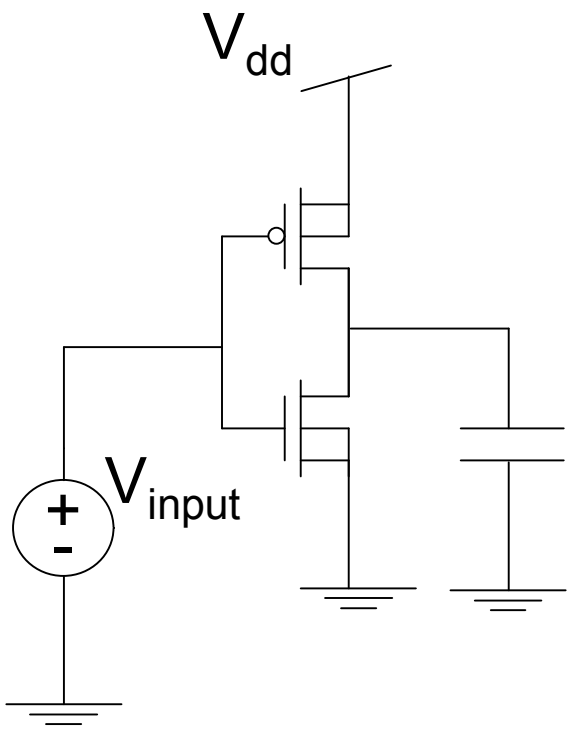


RC model



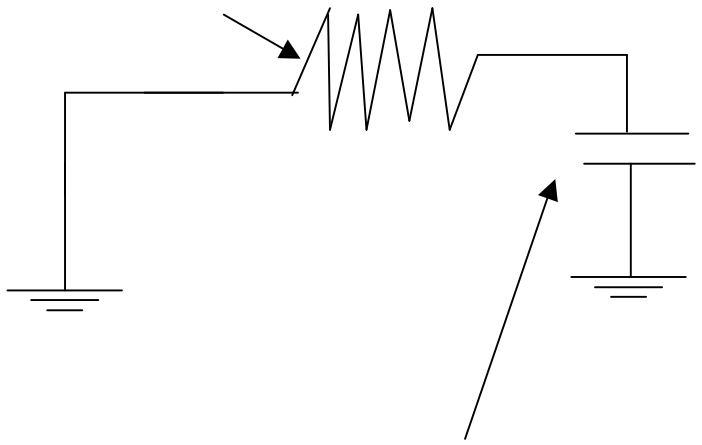
Dynamic Power: Capacitive Switching

During discharge event cap energy dissipates as heat through resistor!



RC model

Dissipates $1/2CV^2$ as heat!



Cap is initially charge!

Dynamic Power: Capacitive Switching

During a single binary transition dissipates $1/2CV^2$ energy as heat!

To reduce power dissipation… *Reduce capacitance*

$$\overline{P_{dyn}} = \frac{1}{2} C V_{dd}^2 f_{clk}$$

Reduce supply voltage *Reduce clock frequency*

NOTE: I will generally just refer to this component as just the "dynamic power".

Dynamic Power:Capacitive Switching

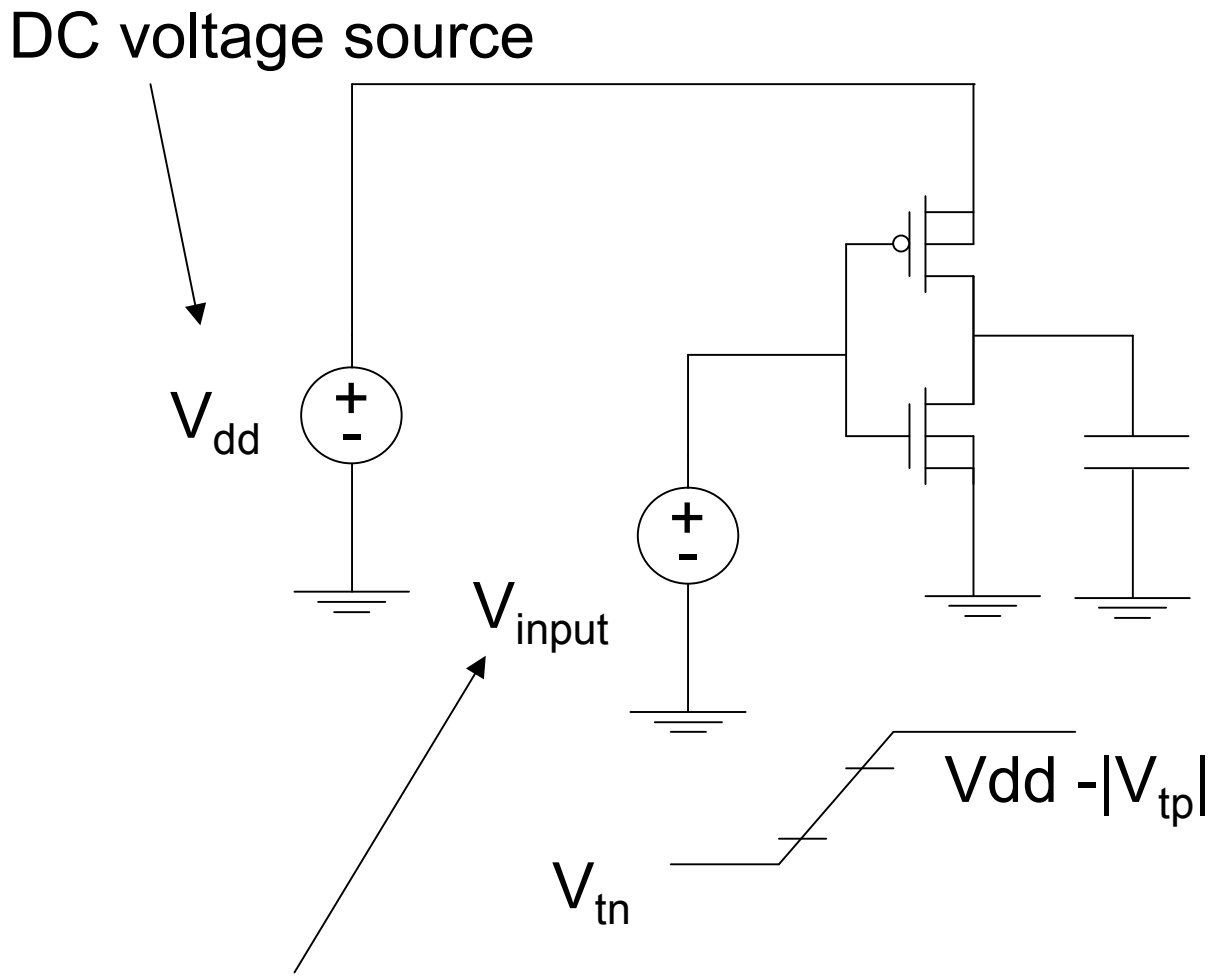
Activity factor 1: fraction of clock periods where output has a binary transition

$$\overline{P} = a\frac{1}{2}CV_{dd}^2 f_{clk}$$

Activity factor 2: fraction of clock periods where the output is switching low-to-high

$$\overline{P} = \alpha_{0\to 1} CV_{dd}^2 f_{clk}$$

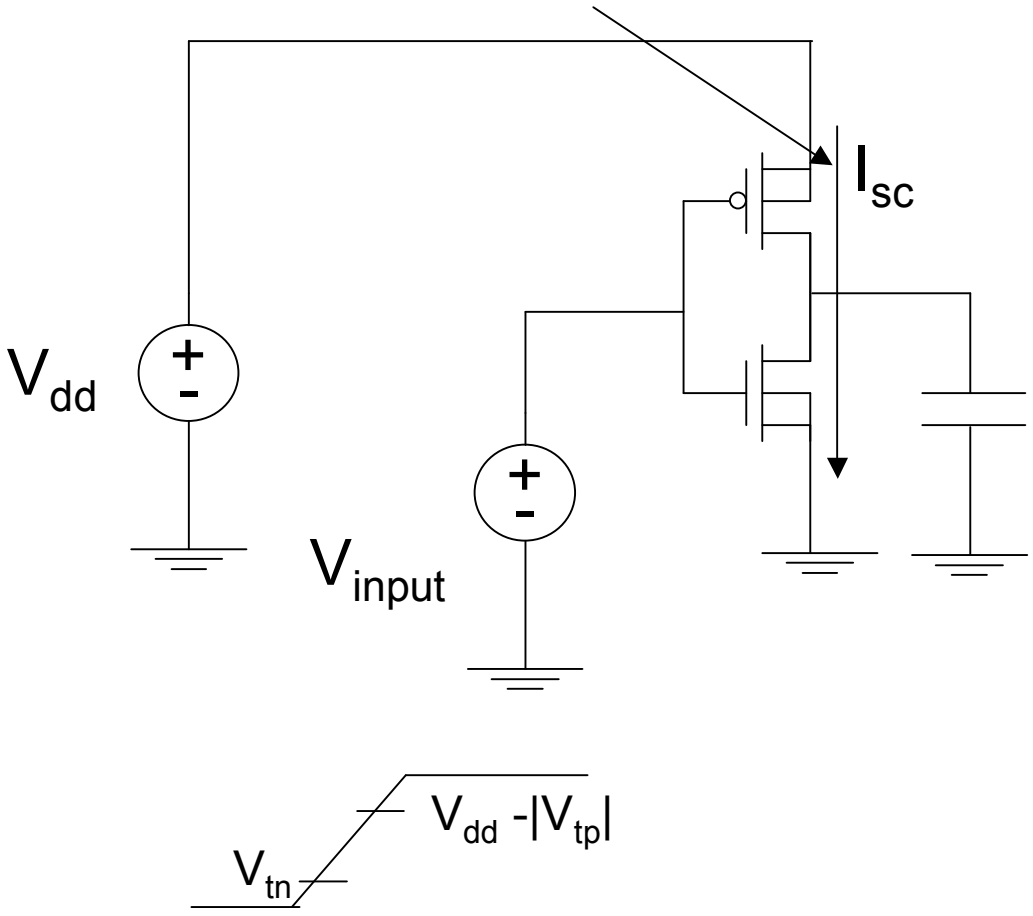
Short Circuit Power Dissipation



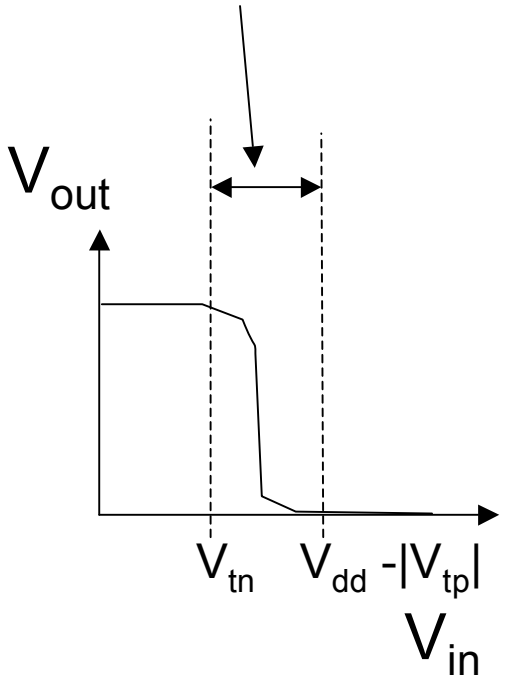
Pulse input voltage source with finite risetime, T_{rise}

Short Circuit (SC) Power Dissipation

I_{sc} = short circuit =a.k.a "crowbar current"



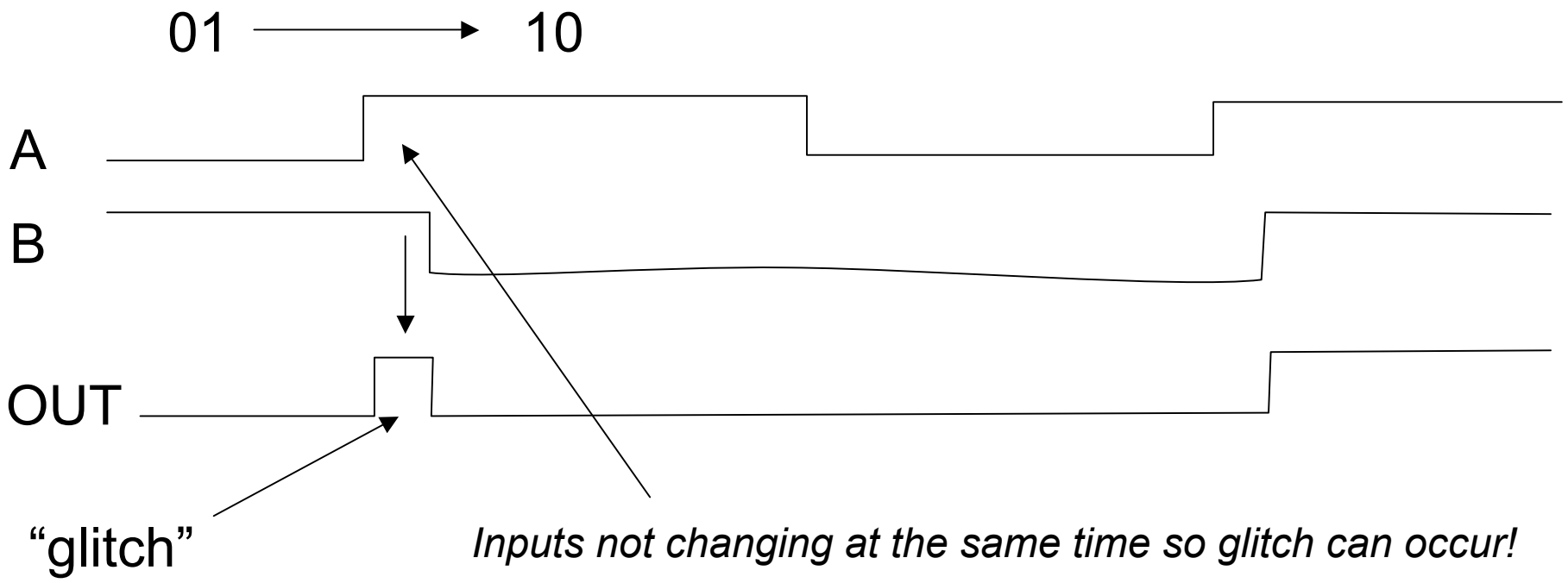
Both nFET and pFET are conducting when input voltage is in the range.



Fast rise and fall times (i.e. "edge rates") can reduce SC power

Definition/Causes of Glitches

- Glitches are caused by having inputs that are not switching simultaneously.
- Glitches occur when the output node temporarily has a value that is not the steady-state value.
- Example: Consider OUT=AB when going 01->10 the following could occur if both inputs do not change simultaneously



Dynamic Power Glitches

- Glitches can cause significant dynamic power dissipation because they represent at least two binary transitions per clock period.
- Designer should minimize glitches to minimize dynamic power dissipation.
- To minimize glitches one must have signals arrive at roughly the same time.
- Designing equal rise and fall times helps to control this because this CAN help to synchronize signal arrival times.

Static Power

Subthreshold leakage currents are the dominate source (also pn junction leakage)

$$I_{leak} \propto \frac{W}{L} \qquad I_{leak} \propto (1 - e^{\frac{-V_{DS}}{kT/q}})$$

$$I_{leak} \propto e^{-\frac{V_{Tn}}{kT/q}}$$

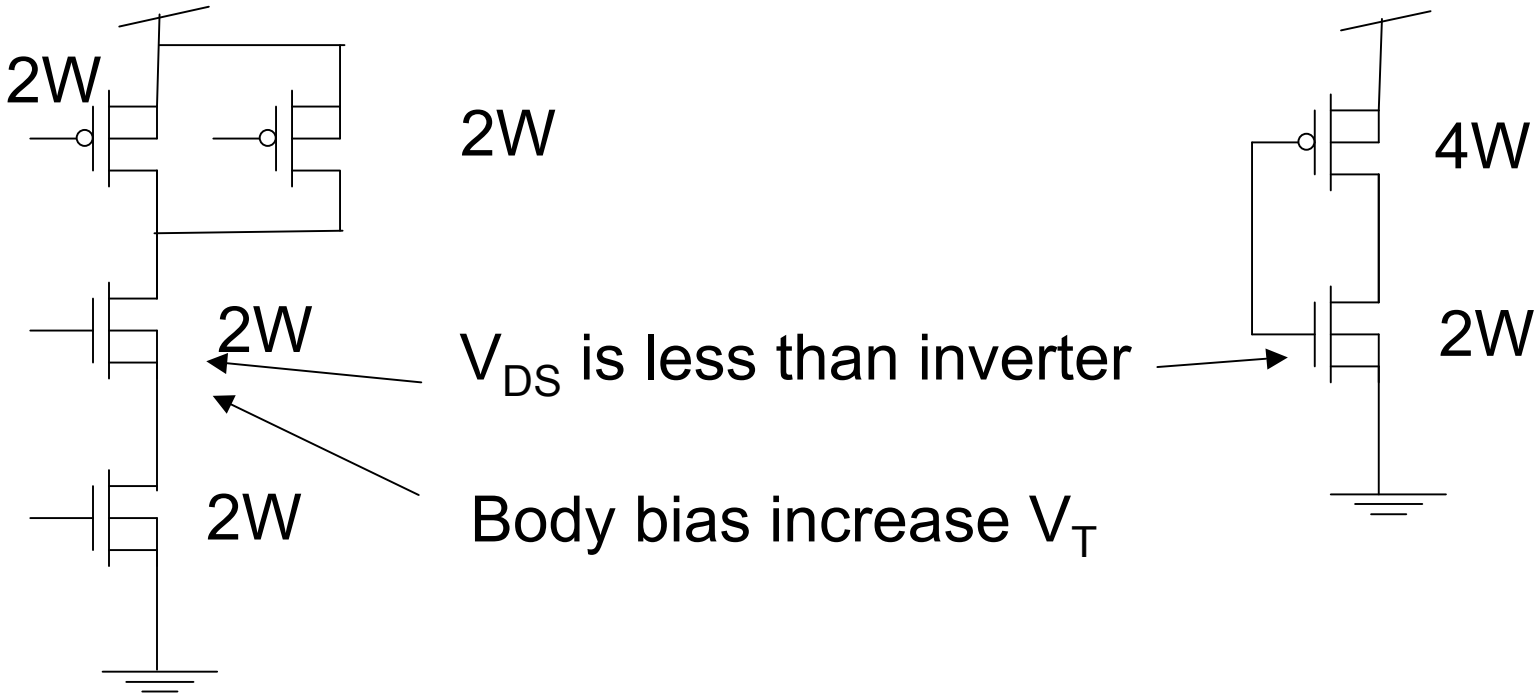
- high V_T (more like dual V_T)
- Cool transistors (not practical?)
- Minimize size of transistors

Static Power

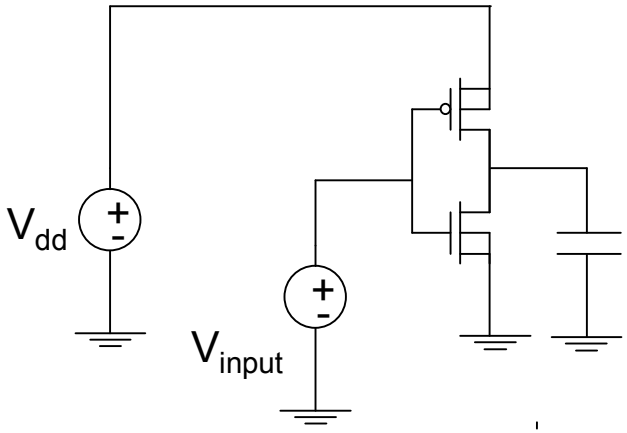
$$I_{leak} \propto \frac{W}{L} \qquad I_{leak} \propto e^{-\frac{V_{Tn}}{kT/q}} \qquad I_{leak} \propto (1 - e^{\frac{-V_{DS}}{kT/q}})$$

High V_{DS} ↑es I_{leak}!

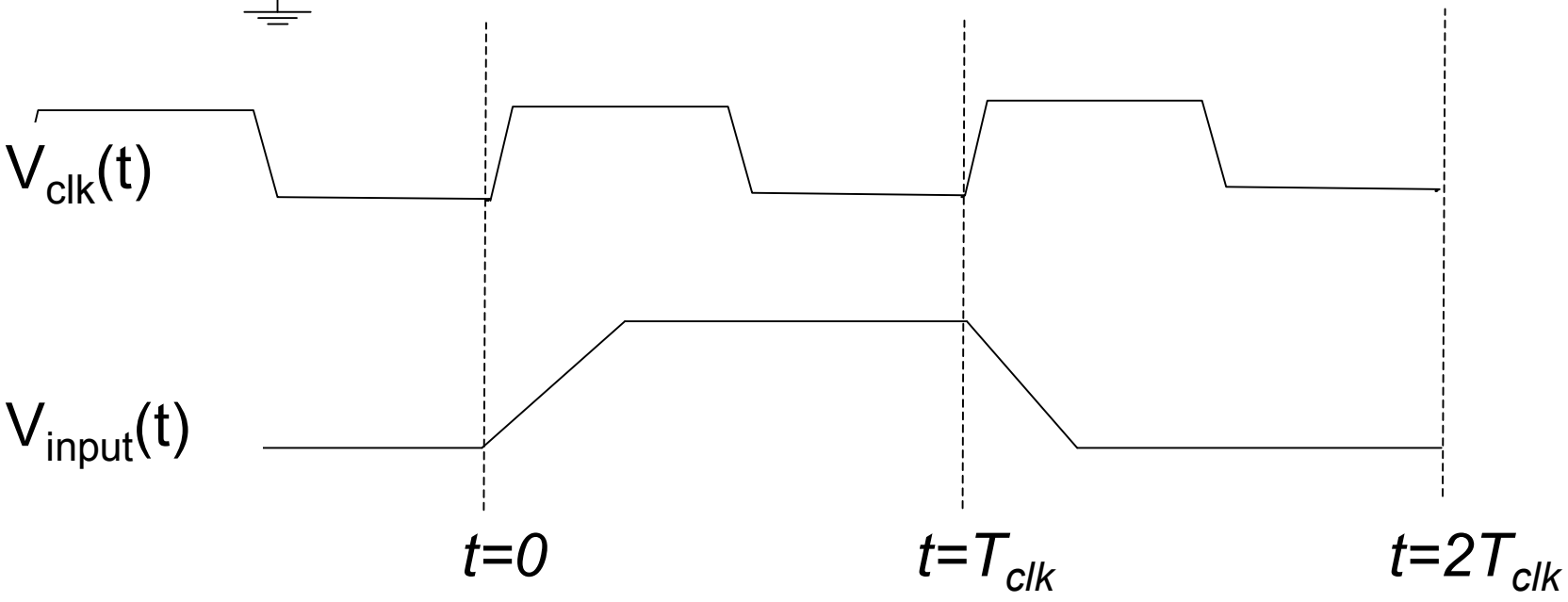
Which has more leakage?



Clock Period/Switching Assumption

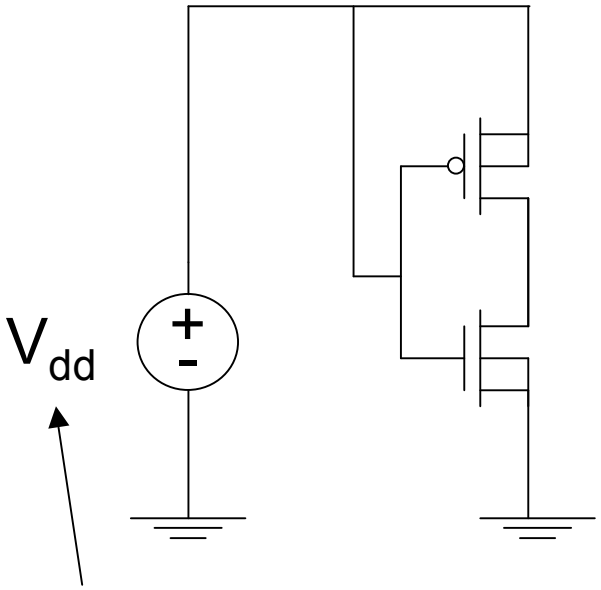


The following slides assume that we have one binary transition during a clock period (i.e. glitch free).

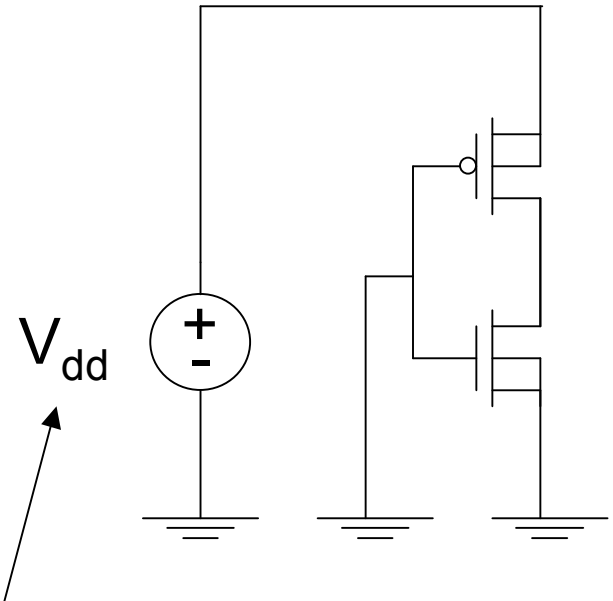


Static Power Measurements in HSPICE

Static power low output



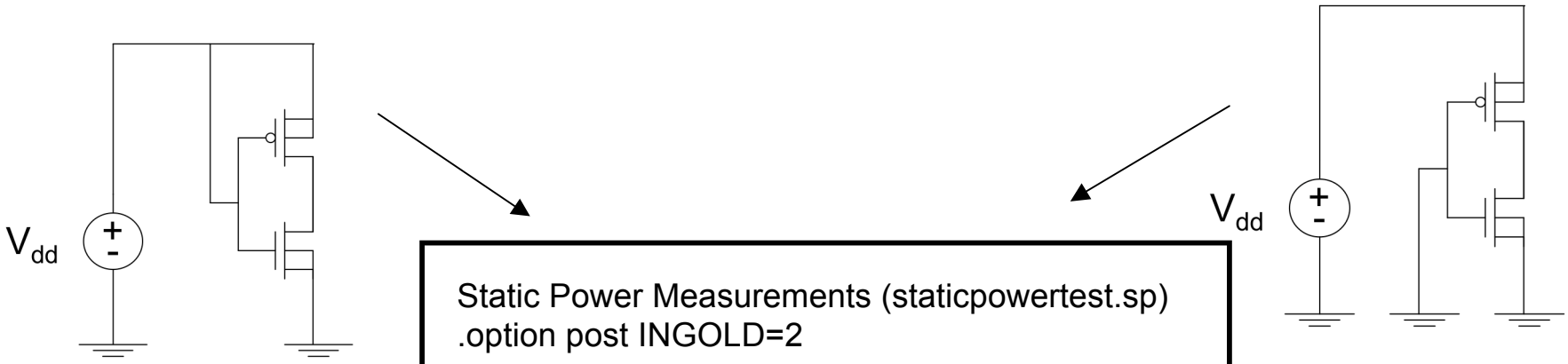
Static power high output



make these DC voltage sources

Static power low output

Static power high output




```
Static Power Measurements (staticpowertest.sp)
.option post INGOLD=2
.op
.lib 'mos.lib' PMOS130nm
.lib 'mos.lib' NMOS130nm
.param supply = 1.3
Vlowoutput 1 0 'supply'
Vhighoutput  3 0 'supply'
*low output
mn 2 1 0 0 n l=0.130u w=2.0u
mp 2 1 1 1 p l=0.130u w=3.0u
*low input
mn2 4 0 0 0 n l=0.130u w=2.0u
mp2 4 0 3 3 p l=0.130u w=3.0u
.end
```

For this case, I have put in both circuits in one file so I have specified TWO supply voltages!

If you use the command : *hspice staticpowertest.sp > log*

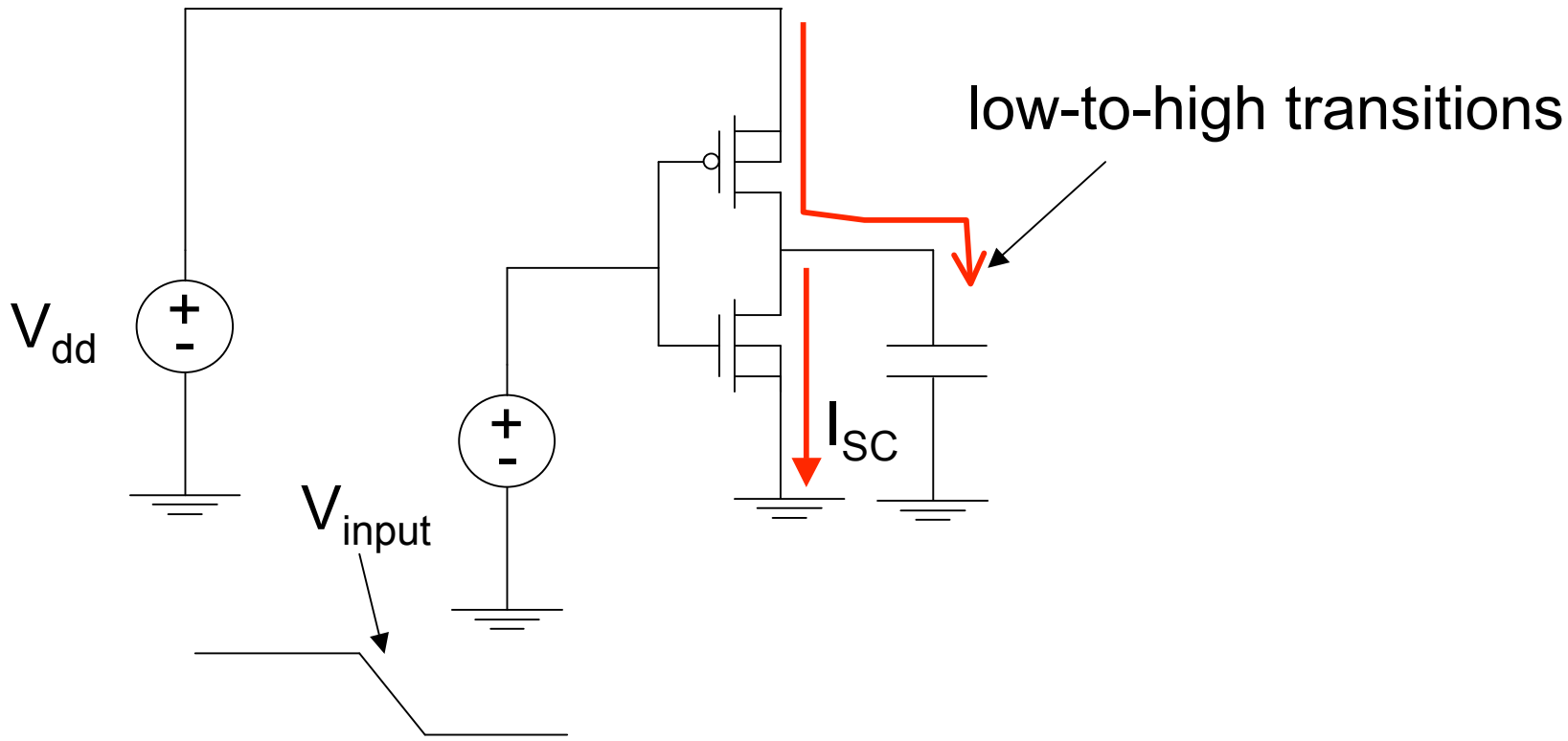
The power supplied by each voltage source is in the ‘log’ file.

Search for the text in ‘log’ “operating point” and you will find the data you require.

(NOTE: In vi use in command mode type *‘/operating point <return>’* and it will take you to this next occurrence.)

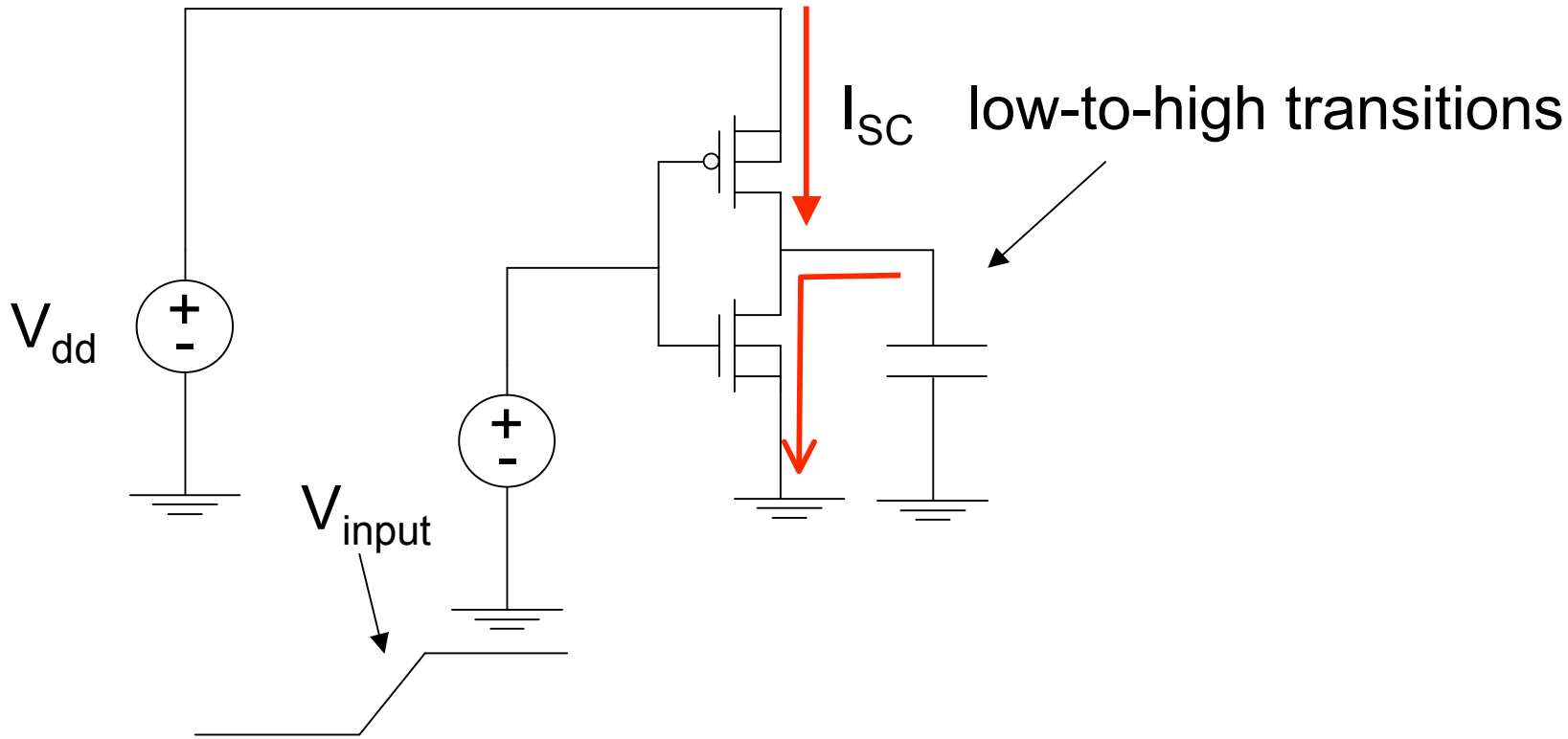
```
static power measurements
 ******  operating point information      tnom=  25.000 temp=  25.000
******
***** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:1       = 1.300e+00 0:2       = 1.472e-07 0:3       = 1.300e+00
+0:4       = 1.300e+00


****  voltage sources

subckt
element  0:vlowoutp 0:vhighout
 volts    1.300e+00  1.300e+00
 current -3.737e-10 -1.440e-11
 power    4.858e-10  1.872e-11
```

Low-to-High SC Power



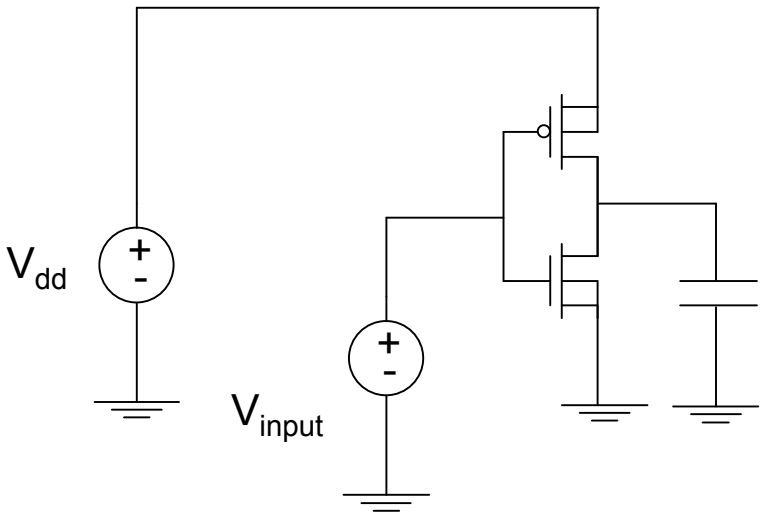
For this case the short circuit current can be determined from the nFET.

High-to-Low SC Power



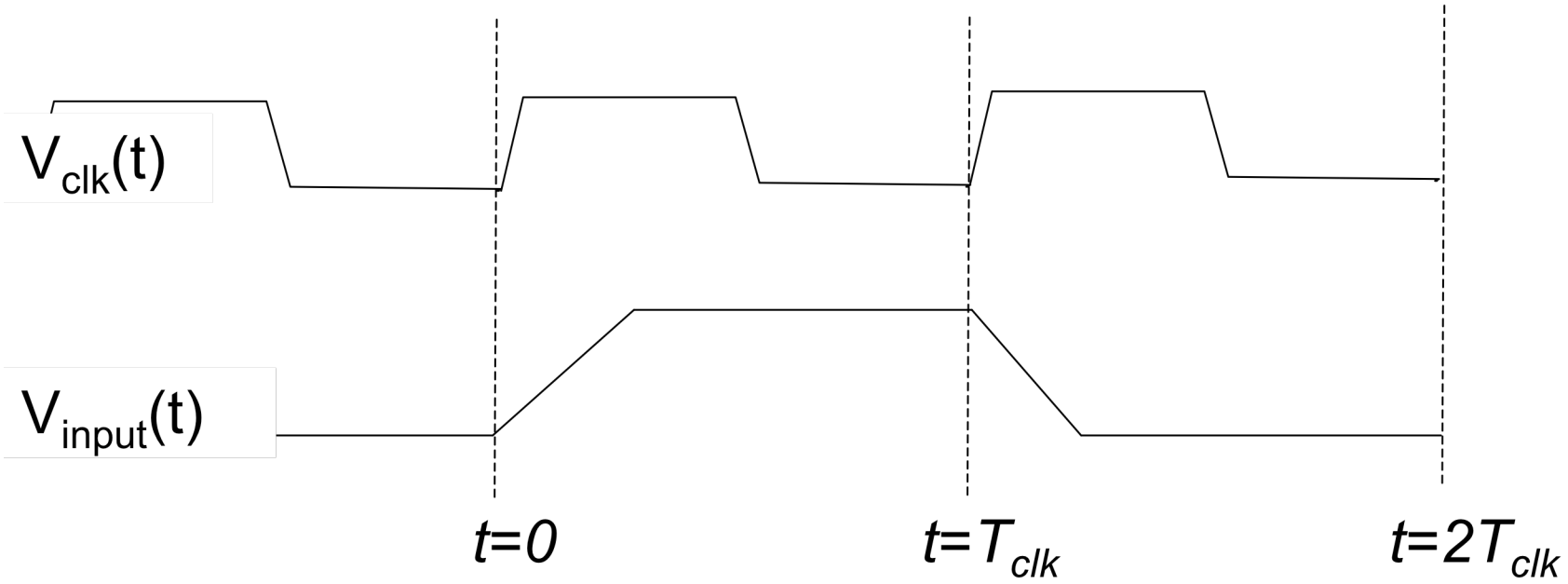
For this case the short circuit current can be determined from the pFET.

HSPICE simulation



$$E_{scHL} = V_{dd} \int_{0}^{T_{clk}} i(m_p)dt$$

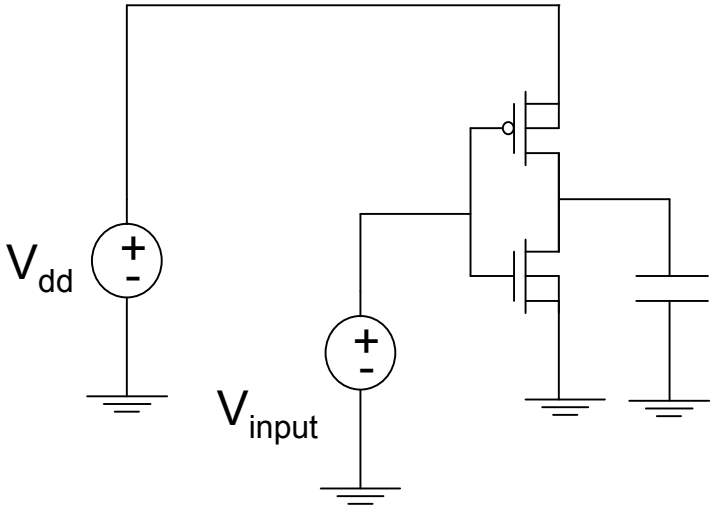
$$E_{scLH} = V_{dd} \int_{T_{clk}}^{2T_{clk}} i(m_n)dt$$

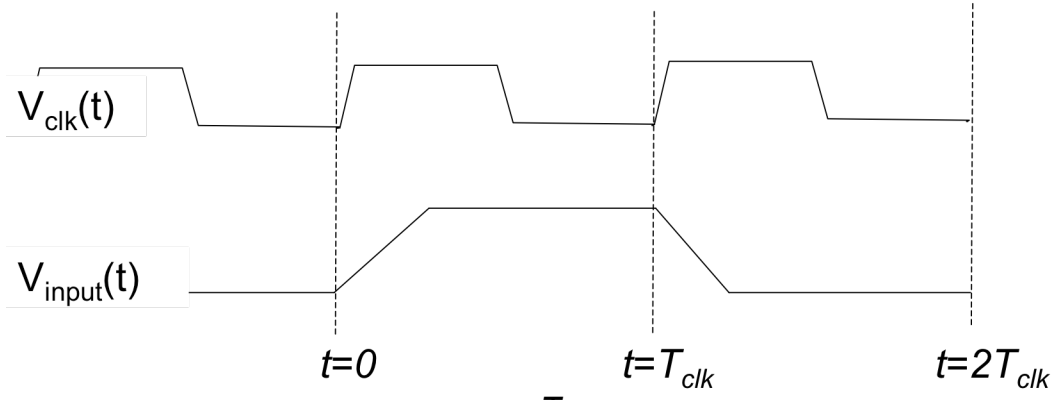


HSPICE Sample Code

```
Short Circuit Power Measurements

.option post INGOLD=2
.lib 'mos.lib' PMOS130nm
.lib 'mos.lib' NMOS130nm
.param supply = 1.3
Vsupply Vdd 0 'supply'
Vinput 1 0 pulse (0 'supply' 0 30p 30p 1n 2n)

mn 2 1 0 0 n l=0.130u w=2.0u
mp 2 1 Vdd Vdd  p l=0.130u w=4.0u

Cout 2 0 100f

.tran 1p 3n

**measure the high-to-low transition
.measure tran Q_HL integral i(mp) FROM = 0 TO= 1n
.measure high_low_SCenergy param = 'supply*Q_HL'

**measure the low-to-high transition
.measure tran Q_LH integral i(mn) FROM = 1n TO= 2n
.measure Low_to_high_SCenergy param = 'supply*Q_LH'

.end
```

Average Binary Switching Energy per Clock Period





$$E_{total\_HL} = V_{dd} \int_{0}^{T_{clk}} i(V_{dd})dt$$

$$E_{total\_LH} = V_{dd} \int_{T_{clk}}^{2T_{clk}} i(V_{dd})dt$$

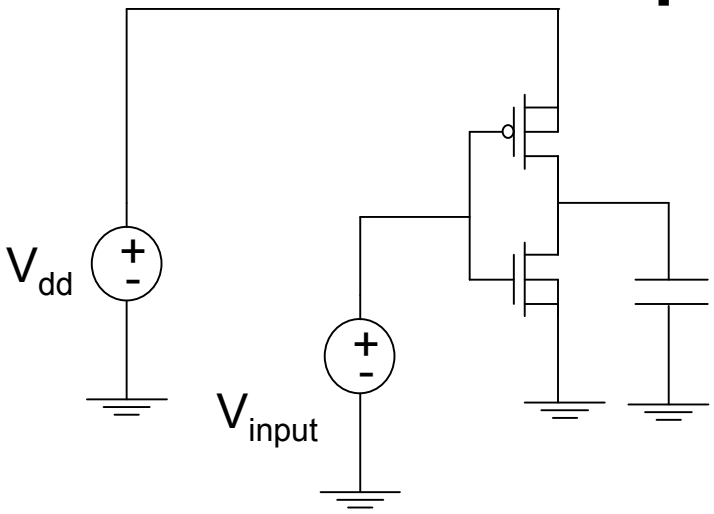
This represents total energy supplied by power supply during these time intervals!

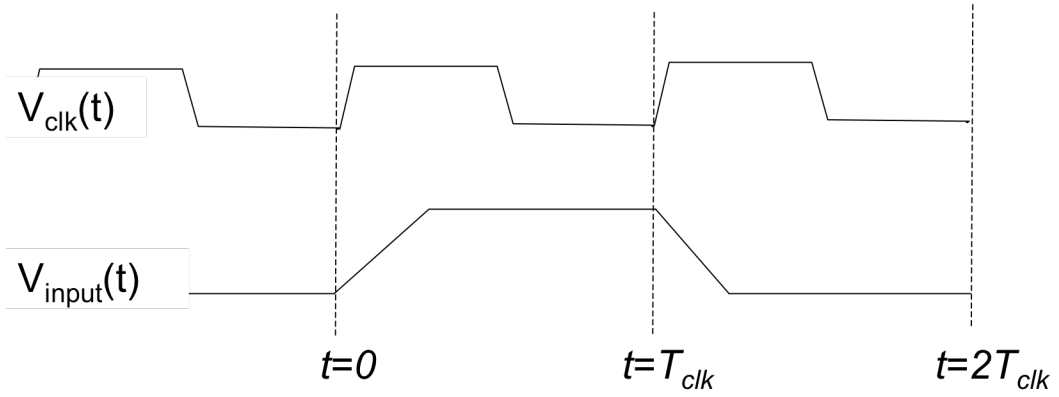
$$\overline{E}_{total} = \frac{E_{total\_HL} + E_{total\_LH}}{2}$$

HL and LH are from the perspective of the output!

Because we are focused on the output, for this calculation we are ignoring energy from V_{input}.

Average Binary Switching Power per Clock Period





$$\overline{E}_{total} = \frac{E_{total\_HL} + E_{total\_LH}}{2}$$

$$\overline{P} = \frac{\overline{E}_{total}}{T_{clk}}$$

For this calculation we are ignoring energy from V_{input}.

HSPICE Code

```
Total Power Measurements
.option post INGOLD=2

.lib 'mos.lib' PMOS130nm
.lib 'mos.lib' NMOS130nm

.param supply = 1.3

Vsupply Vdd 0 'supply'
Vinput 1 0 pulse (0 'supply' 0 30p 30p 1n 2n)

mn 2 1 0 0 n l=0.130u w=2.0u
mp 2 1 Vdd Vdd  p l=0.130u w=4.0u

Cout 2 0 100f IC = ‘supply’

.tran 1p 3n

**measure the high-to-low transition
.measure tran Q_HL integral i(Vsupply) FROM = 0 TO= 1n
.measure high_low_total_energy param = 'supply*Q_HL'

**measure the low-to-high transition
.measure tran Q_LH integral i(Vsupply) FROM = 1n TO= 2n
.measure Low_to_high_total_energy param = 'supply*Q_LH'

.print tran v(1) v(2)

.end
```

Note: The words in bold are keywords in HSPICE!

Results

Total Energy

E_{total_HL} = 5.127fJ

E_{total_LH} = 0.1851pJ

Short Circuit Energy

E_{SC_HL} = 5.690fJ

E_{SC_LH} = 3.265fJ

Leakage Power

P_{low} = 485.8pW

P_{high} = 18.72pW

Calculation of Dynamic Energy with HSPICE

You cannot measure the dynamic power directly with HSPICE; however, you can solve for dynamic components because all OTHER components are known.

$$E_{total\_LH} = E_{SC\_LH} + E_{dyn\_LH} + E_{static\_H}$$

$$E_{total\_HL} = E_{SC\_HL} + E_{dyn\_HL} + E_{static\_L}$$

Average Dynamic Binary Switching Energy per Clock Period

$$E_{dyn\_LH} = E_{total\_LH} - E_{SC\_LH} - E_{static\_H}$$

$$E_{dyn\_HL} = E_{total\_HL} - E_{SC\_HL} - E_{static\_L}$$

$$\overline{E}_{dyn} = \frac{E_{dyn\_HL} + E_{dyn\_LH}}{2}$$

Calculation of Dynamic Energy with HSPICE

$$E_{total\_LH} = E_{SC\_LH} + E_{dyn\_LH} + P_{static\_high} T_{clk}$$

$$0.1851\text{pJ} = 3.265\text{fJ} + E_{dyn\_LH} + (18.72\text{pW})1ns$$

$$E_{dyn\_LH} = 181.83fF$$

How does this compare to $1/2CV^2$

$$E_{dyn\_LH} = 181.83fF$$

$$\frac{1}{2}CV_{dd}^2 = 0.5(100fF)(1.3)^2 = 84.5fJ$$

Because we ignored drain areas in the HSPICE simulation this should be approximately 1/2 Edyn_LH… and it is!

Calculation of Dynamic Energy with HSPICE

$$E_{total\_HL} = E_{SC\_HL} + E_{dyn\_HL} + P_{low} T_{CLK}$$

$$5.127\text{fJ} = 5.690\text{fJ} + E_{dyn\_HL} + (485.8\text{pW})1ns$$

$$E_{dyn\_HL} = -0.563fJ$$

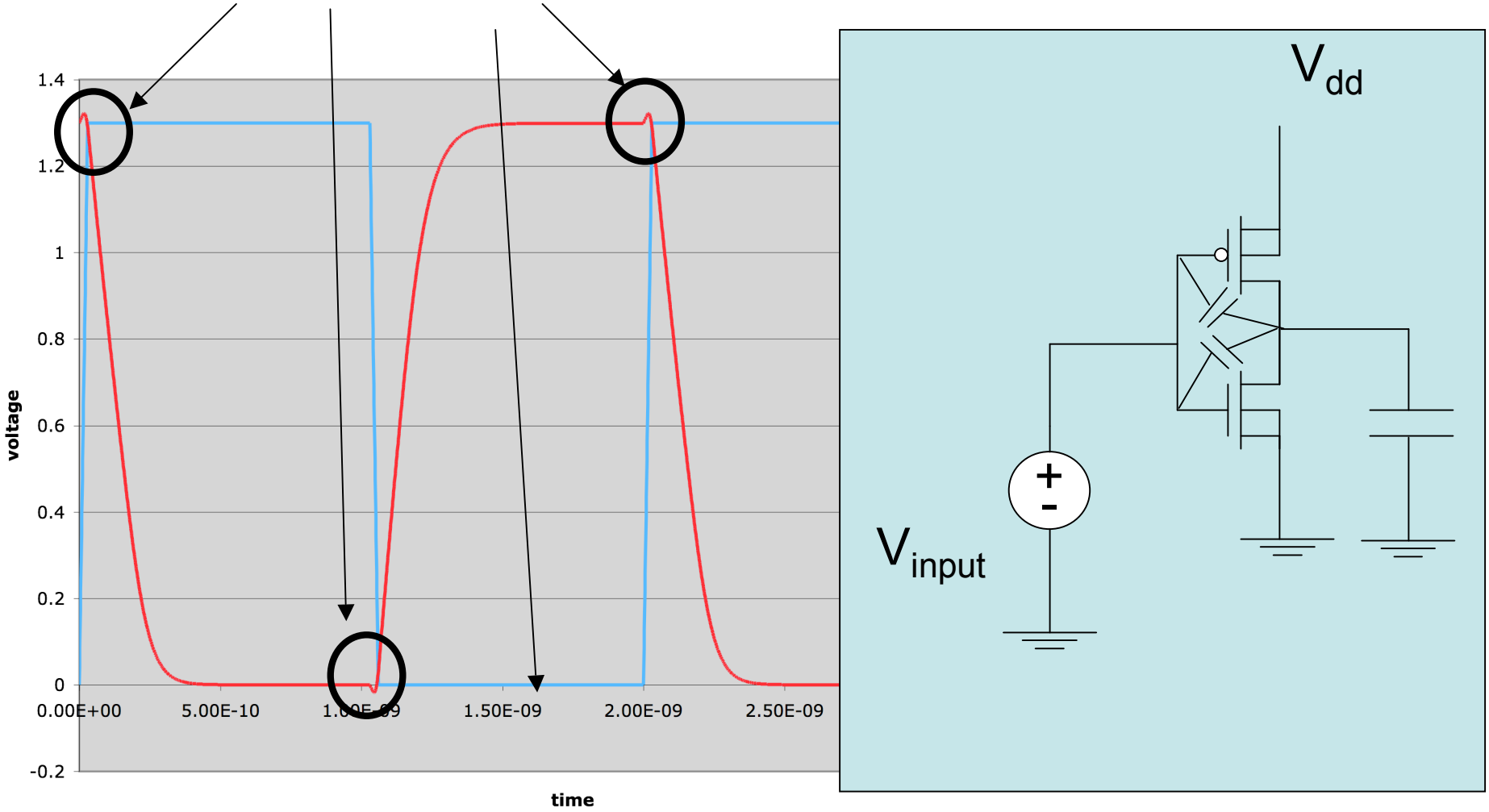
This should be much smaller than the $1/2CV_{dd}$ (and it is!) because the power supply is not providing energy to the circuit.. The circuit is discharging energy stored in capacitive node!

WHY IS THIS NEGATIVE? This is due to the feedthrough current that is provided by V_{input}! (see next page)

Feedthrough Current

"feedthrough current" = capacitive current from gate to drain!

"feedthrough current" cause voltage over/undershoot!



Average Power Calculation

$$\overline{P}_{total} = \frac{E_{total\_LH} + E_{total\_HL}}{2}$$

$$\overline{P}_{total} = \frac{5.127fJ + 185.1fJ}{2} \frac{1}{1e-9} = 95.11\mu W$$