An Efficient Hybrid Power Modeling Approach for Accurate Gate-Level Power Estimation*

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***Abstract*—This paper presents a hybrid power modeling approach based on an efficient library characterization methodology and an effective power estimation flow to accurately assess gate-level power consumption in a faster way. As a case study, we apply the proposed approach on *28nm Fully-Depleted Silicon On Insulator* technology.**

***Index Terms*—FDSOI Technology, Hybrid Power Model, Library Characterization, Power Estimation Technique.**

I. Introduction

High power consumption is a key concern in the design phase of digital circuits. It may cause chip failure, performance issues or an increment in cost or area. To reduce the power consumed by a chip, power optimization techniques are implemented at high abstraction levels. Generally, power estimation at these levels is based on a macro-modeling approach, in which a power model is created using pre-characterized power values as reference.

Usually, chip design uses several high-level components called Intellectual Property (IP), in which general information is saved regarding IP functionality, timing and power information. Mostly, power models are created by computing power consumption at different levels of abstraction [1]. However, in some cases the assessment is not completely reliable as the estimation methodology does not fit the IP characteristics and a detailed information of power consumption per component cannot not be obtained. In addition, time-dependent power consumption is modeled based only on average power results, leaving out the real impact of the instantaneous power dissipation thus reducing the efficacy of the created power model. To ensure the accuracy of these models, power estimation is done at lower levels of the design phase. Then IP power models based on gate-level power estimation are necessary.

Several works have been proposed at gate-level to assess power consumption per component, such as dynamic, short-circuit or leakage power. For instance, the work in [2] presents current/power simulation flow to compute dynamic power. They model the gate current as a triangle shape taking into account different operational conditions (supply voltage, ground voltage) and input switching conditions (rise, fall, static). Their results shows good accuracy with transistor level simulations. However, their assumptions does not fit quite well in sub-nanometer technologies, due to the impact of non-linear parameters on the current profile. Current-based approaches have been applied to compute short-circuit power by taking into account extra current components due to instantaneous switching currents [3], [4]. Other works consider different conditions independently for power analysis like: under noisy input waveforms, temperature variations [5] or supply variations [6]. Most of these techniques envisage a partial solution to compute accurate power consumption, as they are focused on only one power component and on some simplistic assumptions, i.e. Single-Input Switching (SIS) at gate inputs. Nevertheless, this is not a realistic scenario for almots all the circuits. Regarding the leakage component, the work in [7] developed a probabilistic power model taking into account the transistor-level behavior under static conditions. However, they target obly spatial and temporal independence at the input pins analysis.

In order to handle the above mention issues, we propose a hybrid power model and an effective power estimation flow at gate-level, in which, we are able to exploit the run-time efficiency of logic simulation and the physical accuracy of the transistor-level simulation. In this paper, we present the phases of the characterization methodology and the power estimation flow. We use as case study a 28 nm Full-Depleted Silicon on Insulator (FDSOI) technology from STMicroelectronics [8]. The main contributions of this paper are as follows:

- We present an effective characterization methodology that takes into account multiple conditions at the same time.
- We analyze the use of the characterization results to reconstruct circuit-level current/power trace in an efficient way.
- We study the power consumption of standard cells on a *28nm FDSOI* technology per component, i.e. dynamic, short-circuit, leakage power.

This paper is organized as follows. In section II, the details of our library characterization methodology is described. In Section III, we present the basis of our effective power estimation flow. In Section IV, we present the experimental analysis at gate and circuit-level for the technology under study. Section V, concludes this paper.

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II. Library Characterization Methodology

In a library characterization, a detailed analysis of basic components of the standard-cell is executed. The characterization results are often saved in a standard maner, like in Liberty (**lib**) format. Generally, it is provided by the foundry and it contains physical, timing and power information for each standard cell. The stored information is then used by the power estimation engine to compute average energy/power per component.

Usually, there is no knowledge about the characterization conditions and if the designer team choose to have its own cell library, then accuracy must be ensured [9]. In addition, lib information is obtained for a small subset of the whole parameter conditions, e.g. only SIS events. Even though, it is a faster analysis at run-time, in some cases it lacks of accuracy.

We propose an effective characterization methodology, based on the physical description of standard cells. With this methodology, we aim to ensure the reliability of data results and to increase the accuracy on the assessment of power consumption. We take into consideration several gate-level parameters that impact the current/power estimation, i.e. Multiple-Input Switching (MIS) events under different environmental and load conditions.

To ensure the quality of the characterization methodology, we need to consider the following aspects: (1) the parameter selection, to include the ones that directly impact the power consumption; (2) the parameter ranges, to highlight non-linear effects on the current trace. (3) How the parameters are set on the electrical simulator, to ensure realistic-case conditions for each gate. In our case, we have analyzed which parameters constraint directly current waveforms, hence the power consumption. Based on a complete analysis of standard cells characteristics, we determine three groups of parameters:

- **Environmental conditions:** Supply Voltage (V_{DD}), Ground Voltage (GND), Body Biasing (BB) and Temperature (T) .
- **Input pin information:** Activity Information of the input pins, i.e. transition type (rise, fall, stable), input transition times (slew rate) and signal arrival times.
- **Output pin information:** Capacitance value of the output pin that takes into account the gates connected to it, i.e. fan-out capacitance.

The characterization methodology is divided into two main phases: a data measurement phase, to create our gate-level current database. And a modeling extraction phase, to develop different models based on current characteristics. We developed an automated characterization flow to set all the parameters, run the simulations and recollect the desired data (Figure 1). As simulation results we obtain current and timing information. The saved currents are: the supply current ($i_{dd}(t)$) and the capacitor current ($i_{cc}(t)$). And the timing information: the propagation delay and the output transition time (slew rate).

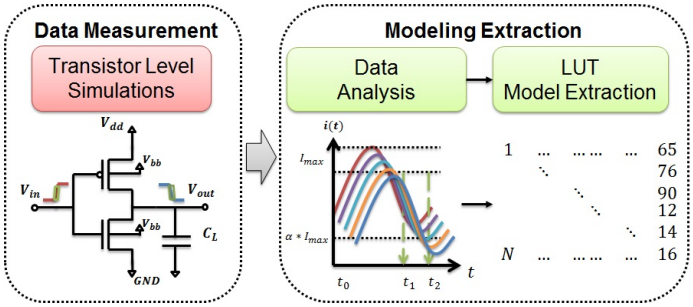

Figure 1: Library Characterization Methodology.

A. Data Measurement

In the first phase of our methodology, we create spice-like decks in which we set all the parameters. We determine how parameters are applied, to ensure that our results are obtained based on conditions close to real circuit scenarios. And we set all simulator parameters, to highlight non-linear behavior of the current profiles, e.g. we save the current values each one picosecond.

To model the input signals, we are able to choose different gate types on the input pins of the gates under analysis. In addition to the current and timing information, a mapping file is also created with the simulated conditions of all the parameters. This file will be used as reference point for the second phase. One of the main advantages of this step, is that we are able to identify and classify all power components at the same time, i.e. we separately are able to compute the dynamic, the short circuit, and the leakage component in a single run.

It is needed to accurately measure the timing characteristics of each gate as this will have a direct impact on the current selection, hence on the power estimation. We use as reference points to compute the slew rate 20-80% and for the propagation delay 40-60%. In our case, we can analyze and save timing information at the same time that our current-characterization, hence there is no increment on the characterization run-time.

B. Modeling Extraction

The modeling extraction phase is subdivided in two steps. In the first one, we analyze all the gate current database and select which information must be conserved. Based on this analysis, we determine characteristics like: current peak value, peak time, current duration time, and then we filter all the extra current information that is not relevant for each condition. In this case, we represent the currents in Look-Up Tables (LUT) for a defined time window, based on the current-trace considering the complete dynamic behavior of the current waveforms. We realize that our LUT are created without any optimization method since our main objective is to show the feasibility of our methodology and their used on the estimation flow. Further effort will be focused on the optimization of the LUT currents and the construction of an equation-based methods.

III. Power Consumption Assessment Flow

To assess the power consumed by a gate or a circuit we use the estimation flow depicted on Figure 2. As input data the following information is necessary: (1) the synthesized gate-level netlist (Verilog format); (2) the activity information of all the internal nodes (VCD File); (3) the input pin capacitance information; and (4) the LUT gate-level current and timing, which are obtained based on the proposed library characterization phase.

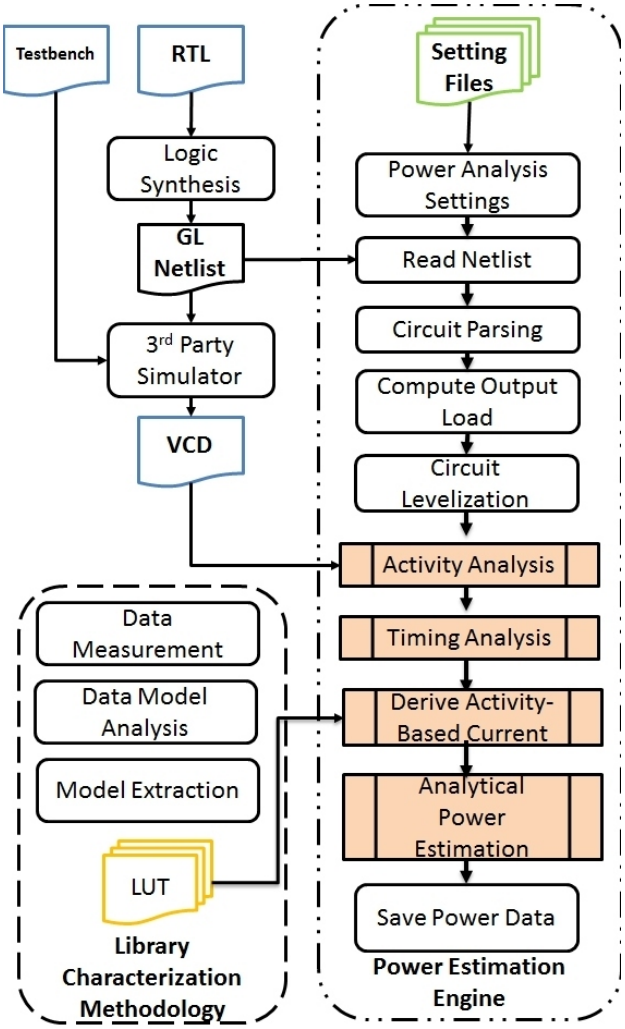

Figure 2: Hybrid Power Estimation Flow.

The estimation engine starts by parsing the circuit to determine the structural information that surrounds every gate, i.e. driving cells and cells driven by each gate. Then, output node capacitance is estimated based on fan-out information and parasitic information if it is available. Afterwards, we run a circuit levelization algorithm to determine the order in which each gate will be analyze and how the timing propagation will be done.

Once we have ordered the gates, we proceed to determine all the switching activity information per net. Then, based on the transition type the slew rate information it is propagated from primary inputs to primary outputs. Once all the require information is completed, we select the current that is drawn by each gate and add it based on the activation times. Finally, the average power is computed taking into account the simulation period and the derived circuit current.

IV. Experimental Results

In this section, we present experimental results of applying our library characterization methodology and estimation flow on a 28nm FDSOI technology. All the reference simulations are done based on SPECTRE simulator by Cadence [10].

We automate our library characterization using PERL language. We applied it under the same conditions than the ones in the lib file, to directly correlate our results with it. We implemented the power estimation flow presented on last section in C++ and we call it Hybrid Power Estimation Tool (HPET). Using HPET we can easily analyze current/power trace at gate and circuit level. All the analysis are performed on a Linux x86 64bit server with 48 sockets, 1 core per socket, and 158GB of available memory.

A. Validation of the Library Characterization

For the validation phase, we compared the current/power results using our power estimation flow and LUT with the results obtained using the commercial tool PrimeTime-PX [11], in which, dynamic power is computed based on the output load capacitance and the average activity information. Short-circuit power is computed based on liberty data and a single energy value per characterized condition. Leakage power is computed based on a probabilistic approach about the time each net is on a static condition.

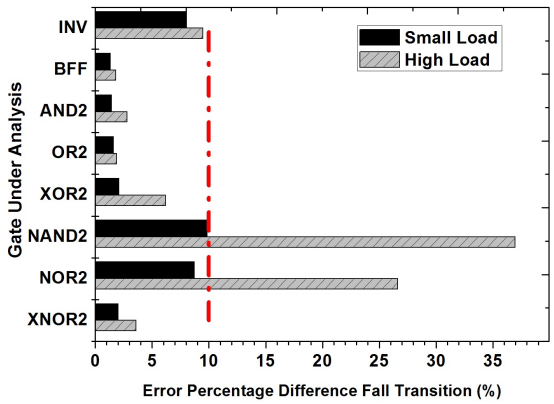

Figure 3: Short-Circuit Power Mean Error.

Dynamic and leakage power are accurately computed based on our characterization results, as mean error difference for both components is lower than 2% for the studied standard cells. On the other hand, we observed a higher difference between our results and the liberty data for short-circuit power component. In general, the mean error percentage is lower than 10% for different gate types and only for two cases we obtained higher differences (Figure 3).

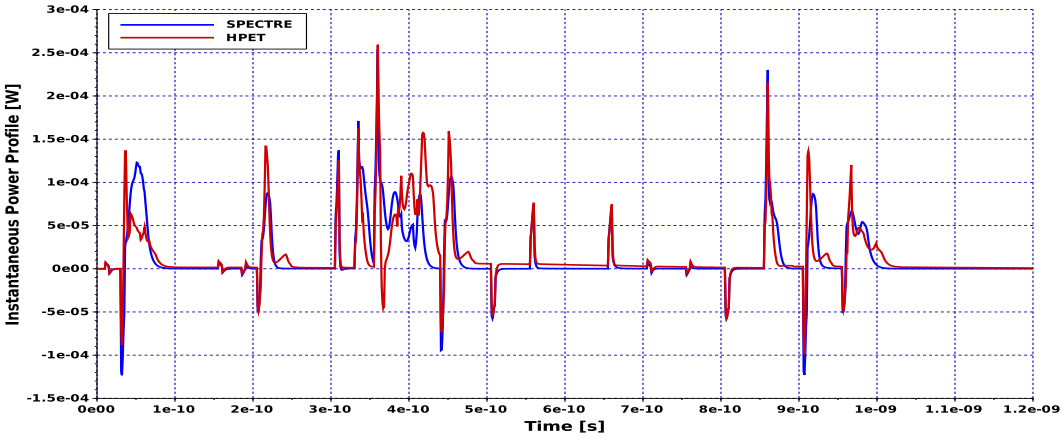

Figure 4: Estimated vs Simulated Current Profile ISCAS C17

We determined that it can be different sources for the obtained percentage error. The main one is that we cannot ensure that simulation conditions were the same than those used to compute the liberty data information. For instance, the use of a different simulator, different driver gate, and different parameter application, will have a direct impact on the current profile when performing the characterization procedure.

Even though we perform the characterization of each gate only once and then use it as many times as necessary, we give some run-time simulation for each gate. In average, for leakage component the LUT creation took less than 5 minutes. For SIS currents, average simulation time was about 1:30h, and for MIS currents it took about 45 minutes.

B. Instantaneous Current Profile Verification

Once our characterization results are validated, we synthesized different circuits using a 28nm technology. As case study, we present the results of the ISCAS85 benchmark circuit C17 to envisage the advantages of the presented work. We derive the current profile using the proposed flow and we compare it with SPECTRE simulation. Estimated versus simulated current profile is presented in Figure 4. Using the Normalized Root Mean Square Deviation (NRMSD) formula, we are able to identify the degree of similarity of the two waveforms, in this case we obtain a 3.4% of difference with a speed-up in computational time of about 5X.

Similar results are obtained on other benchmark circuits with thousands of gates and higher complexity. This demonstrate that we can compute current/power in an efficient way. Future work will be done in ensuring the accuracy of our estimation flow with regard to SPECTRE simulation for instantaneous and average results. And, the complete analysis on real industrial test circuits.

V. Conclusion and Future Work

In this paper, we proposed a hybrid power model that uses transistor-level current information and gate-level logic simulation, to enhance the power estimation flow. The modeling approach is based on efficient library characterization methodology, in which, we save the current waveforms for multiple parameters conditions at the same time. With this approach we aim to speed-up the estimation run-time while having transistor-like accuracy. Further work will be focused on the LUT improvement and the use of activity information from RTL simulation.

References

[1] D. Elléouet, N. Julien, and D. Houzet, "A high level SoC power estimation based on IP modeling," *20th International Parallel and Distributed Processing Symposium, IPDPS 2006*, vol. 2006, pp. 6–9, 2006.

[2] A. Bogliolo, L. Benini, G. De Micheli, and B. Riccò, "Gate-level power and current simulation of CMOS integrated circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 5, no. 4, pp. 473–488, 1997.

[3] H. Fatemi, S. Nazarian, and M. Pedram, "A current-based method for short circuit power calculation under noisy input waveforms," *Proceedings of the Asia and South Pacific Design Automation Conference, ASP-DAC*, pp. 774–779, 2007.

[4] S.-Y. K. Seung-Ho Jung, Jong-Humm Baek, "Short Circuit Power Estimation of Static CMOS Circuits," in *Design Automation Conference, 2001. Proceedings of the ASP-DAC 2001. Asia and South Pacific*, no. 2, 2001, pp. 545–549.

[5] S. Gupta and S. S. Sapatnekar, "Compact Current Source Models for Timing Analysis Under Temperature and Body Bias Variations," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 20, no. 11, pp. 2104–2117, 2012.

[6] C. Knoth, H. Jedda, and U. Schlichtmann, "Current Source Modeling for Power and Timing Analysis at Different Supply Voltages," in *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2012, pp. 923–928.

[7] X. Zhao and K. Wang, "A leakage power estimation method for standard cell based design," *IEEE Conference on Electron Devices and Solid-State Circuits*, pp. 821–824, 2005.

[8] B. S. a. Vitale, P. W. Wyatt, M. Ieee, N. Checka, J. Kedzierski, and C. L. Keast, "FDSOI Process Technology for Ultralow-Power Electronics," *Proceedings of the IEEE*, vol. 98, pp. 333–342, 2010.

[9] J. Jiang, M. Liang, L. Wang, and Y. Zhou, "An effective timing characterization method for an accuracy-proved VLSI standard cell library," *Journal of Semiconductors*, vol. 35, no. 2, 2014.

[10] Cadence, "Cadence® spectre® circuit simulator," 2014.

[11] Synopsys, "Primetime px: Signoff power analysis." 2014.