



**BL808**

数据手册

*Version: 1.1*

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## Features

- 无线（业内顶尖射频性能）
  - 2.4GHz 射频收发器
  - Wi-Fi 802.11 b/g/n
  - Bluetooth® 5.x Dual-mode (BT+BLE)
  - Zigbee / IEEE 802.15.4
  - Wi-Fi/蓝牙/zigbee 共存
  - 集成 balun, PA/LNA
  - 支持外部 PA/LNA
- 微控制器子系统
  - 多核 RISC-V CPUs (Max Freq 480MHz)
  - RTC 定时器最长计数周期为 1 年
  - 通用定时器
  - DMA 通道
  - JTAG 开发支持
  - XIP QSPI 闪存支持
- 音频编解码器
  - ADC\*2 (MIC\*2 or MIC\*1+Line-in)
  - DAC\*1 (Speaker)
  - 采样率 8~192 KHz, 24bit
- Video/Image/Display
  - MJPEG , H264 (Baseline/Main)
  - 最大分辨率: 2M(1920x1080)
  - 视频编码格式:
    - \* MJPEG and H264 (Baseline/Main)
    - \* 1920x1080 @ 30fps + 640x480 @ 30fps
    - \* 高达 8-ROI(region-of-interest)
- Camera Sensor 接口: DVP 和 MIPI-CSI
- 显示接口: SPI、DBI、DPI(RGB)、MIPI-DSI
- AI NN 通用硬件加速器
  - NPU BLAI-100 (BLAI engine) 用于视频/音频检测/识别
- Memory
  - 内嵌 32/64MB DRAM
  - 支持最大 128MB SPI-Nor Flash
  - 支持最大 256MB SPI-NAND Flash
- 安全
  - 安全启动、安全调试
  - XIP QSPI On-The-Fly AES 解密 (OTFAD)
  - 支持 RISC-V 安全 zone 分区
  - AES-CBC/GCM/XTS 模式
  - MD5, SHA-1/224/256/384/512
  - TRNG（真随机数生成器）
  - 用于 RSA/ECC 的 PKA（公钥加速器）
- 外设
  - USB 2.0 HS OTG
  - 以太网 RMII 接口
  - SD 卡接口
  - 4 个 UART 接口（支持 RS485、ISO 17987-8、ISO 11898-1）
  - 2 个 SPI 接口 (Max Freq 80MHz)
  - 4 个 I2C 接口
  - 8 个 PWM 通道
  - I2S 接口

- PDM 接口
  - 关闭 (~1uA)、休眠
- 通用 ADC
  - 断电睡眠
- 通用 DAC
  - 时钟
    - 支持 XTAL 24/26/32/38.4/40 MHz
    - 支持 XTAL 32/32.768 KHz
    - 内部 RC 32KHz/32MHz 振荡器
    - 内部系统 PLL
- 通用模拟比较器 (ACOMP)
  - 支持 XTAL 32/32.768 KHz
- PIR（被动红外）检测
  - 内部 RC 32KHz/32MHz 振荡器
- IR remote 硬件加速器
  - 内部系统 PLL
- 支持 12 通道 Touch
  - 封装类型
    - 88 pin QFN
- 可配置的 36 或 40 个 GPIO
- 功耗（超低功耗模式）

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BL808 是高度集成的 AIoT 芯片组，具有 Wi-Fi/BT/BLE/Zigbee 等无线互联单元，包含多个 CPU 以及音频编码译码器、视频编码译码器和 AI 硬件加速器，适用于各种高性能和低功耗应用领域。

BL808 系列芯片主要包含无线和多媒体两个子系统。

无线子系统包含一颗 RISC-V 32-bit 高性能 CPU，集成 Wi-Fi/BT/Zigbee 无线子系统，可以实现多种无线连接和数据传输，提供多样化的连接与传输体验。

多媒体子系统包含一颗 RISC-V 64-bit 超高性能 CPU，集成 DVP/CSI/ H264/NPU 等视频处理模块，可以广泛应用于视频监控/智能音箱等多种 AI 领域。

多媒体子系统组成部分如下：

- NPU HW NN 协处理器 (BLAI-100)，适用于人工智能应用领域
- 摄像头接口
- 音频编码译码器
- 视频编码解码器
- 传感器
- 显示接口

电源管理单元控制低功耗模式。此外，还支持各种安全功能。

外围接口包括 USB2.0、Ethernet、SD/MMC、SPI、UART、I2C、I2S、PWM、GPDAC/GPADC、ACOMP、PIR、Touch、IR remote、Display 和 GPIO。

支持灵活的 GPIO 配置，BL808 最多可达 40 个 GPIO。

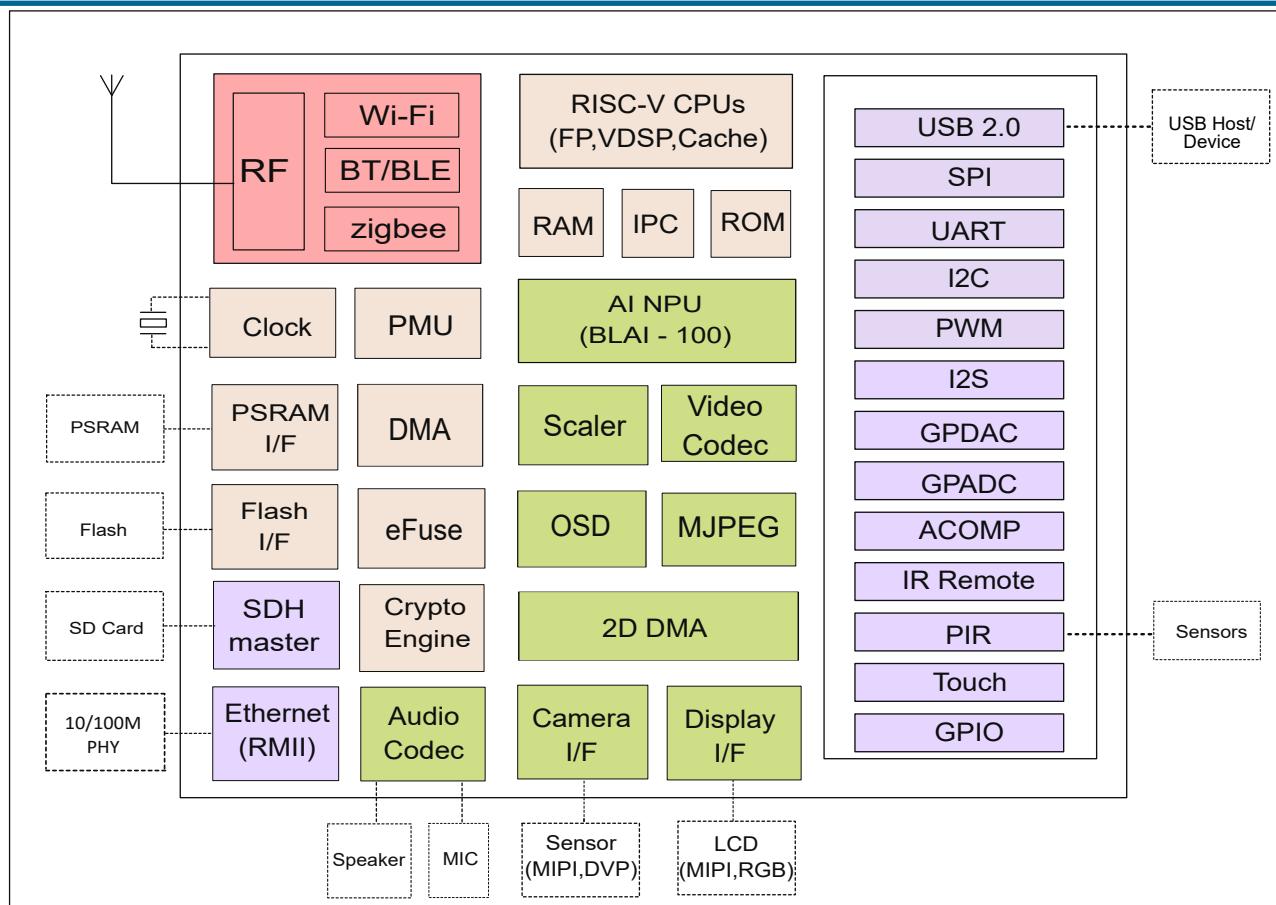


图 1.1: 功能框图

BL808 系统框图如下所示:

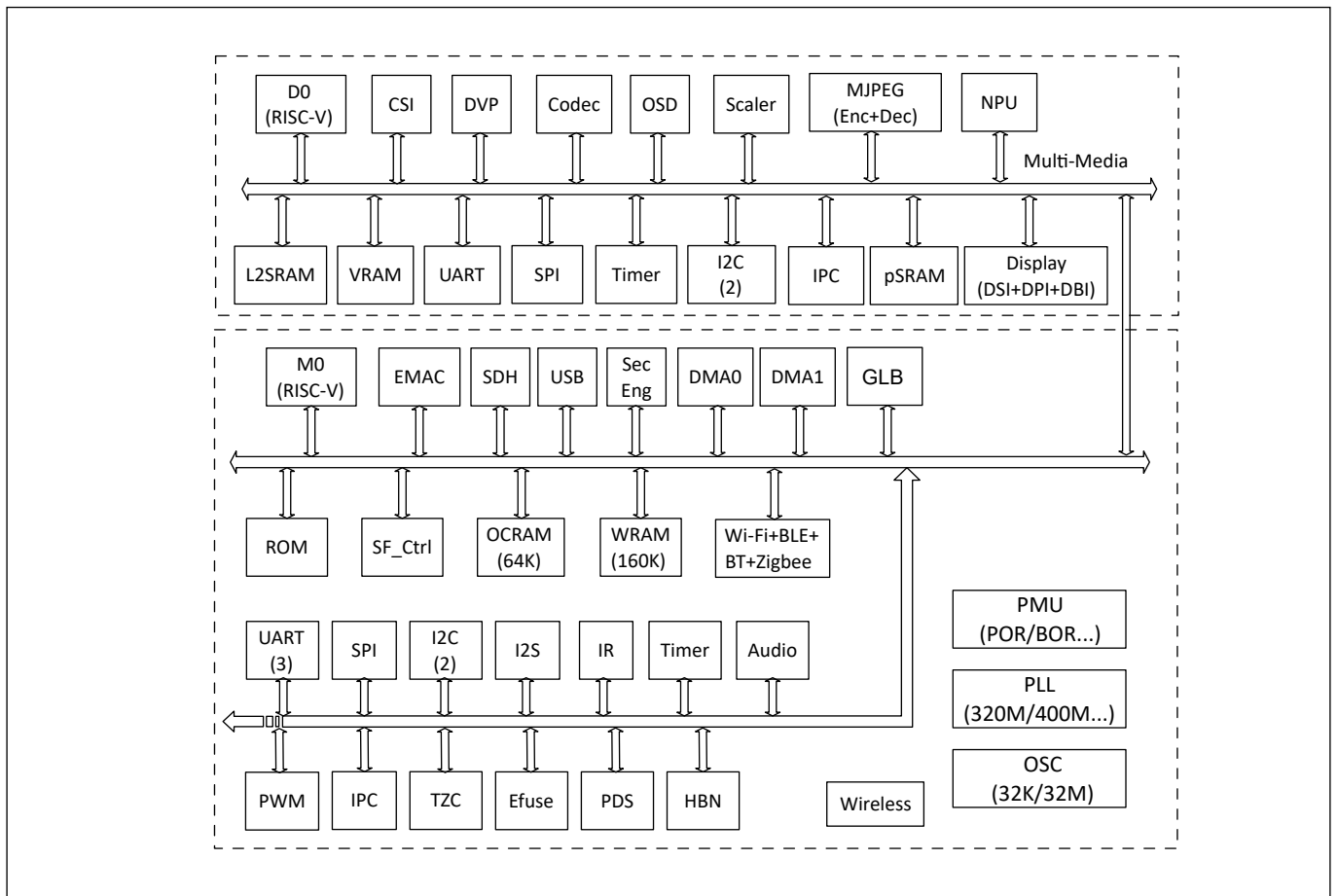


图 2.1: 系统框图

## 2.1 CPU

BL808 芯片内部包含多个 RISC-V 处理器。M0 是一颗 32-bit RISC-V CPU，采用 5 级流水线结构，支持 RISC-V 32/16 位混编指令集，包含 64 个外部中断源，有 4 个 bits 可以用于配置中断优先级。D0 是一颗 64-bit RISC-V CPU，采用 5 级流水线结构，支持 RISC-V RV64IMAFCV 指令架构，包含 67 个外部中断源，有 3 个 bits 可以用于配置中断优先级。

## 2.2 缓存

BL808 的缓存提高了 CPU 访问外部存储器的效能。M0 包含 32K 指令 cache 和 16K 数据 cache；D0 包含 32K 指令 cache 和 32K 数据 cache。

## 2.3 内存

BL808 存储器包括：片上零延迟 SRAM 存储器，只读存储器，一次写入存储器，嵌入式闪存（可选），嵌入式 pSRAM（可选）。

## 2.4 DMA 控制器

BL808 DMA（直接存储器访问）控制器具有 20 个专用通道（DMA0 和 DMA2 分别有 8 个通道，DMA1 有 4 个通道），用于管理外设和存储器之间的数据传输，以提高 CPU /总线效率。DMA 有四种传输类型，内存到内存，内存到外设、外设到内存以及外设到外设四种模式。

DMA 还支持 LLI（链接列表项）功能，该链表由一系列链接列表预定义多个传输，然后硬件会根据每个 LLI 的大小和地址自动完成所有传输。DMA 支持的外设包括 UART、I2C、SPI、ADC、IR、GPIO、Audio、I2S、PDM、DBI、DSI。

## 2.5 地址映射

表 2.1: 内存地址映射

模块	大小	开始地址 ( M0 )		开始地址 ( D0 )	
		Cache	Non-cache	Cache	Non-cache
OCRAM(MCU)	64KB	0x62020000	0x22020000	-	0x22020000
WRAM(MCU)	160KB	0x62030000	0x22030000	-	0x22030000
DRAM(MM)	512KB	-	0x3EF80000	0x3EF80000	-
VRAM(MM)	32KB	-	0x3F000000	0x3F000000	-

OCRAM 和 WRAM 既可以通过 AHB 总线访问，也可以通过 AXI 访问，当 CPU 使用 0x62020000 地址访问 OCRM 时，会经过内部 Cache 并通过 AXI 转 AHB 实现对 OCRM 的访问，当 CPU 使用 0x22020000 地址访问 OCRM 时，不会经过内部 Cache 并且直接通过 AHB 总线访问 OCRM。

表 2.2: 地址映射

模块	目标	开始地址	大小	描述
pSRAM	pSRAM	0x50000000	64MB	pSRAM 存储器地址空间，实际大小取决于芯片型号
FLASH	FlashA	0x58000000	64MB	应用程序地址空间，实际大小取决于芯片型号
MMPERI	TIMER1	0x30009000	4KB	TIMER1 控制寄存器
	SPI1	0x30008000	4KB	SPI1 控制寄存器
	MM_GLB	0x30007000	4KB	Multimedia 侧全局寄存器
	DMA2D	0x30006000	4KB	DMA2D 控制寄存器
	I2C3	0x30004000	4KB	I2C3 控制寄存器
	I2C2	0x30003000	4KB	I2C2 控制寄存器
	UART3	0x30002000	4KB	UART3 控制寄存器
	DMA2	0x30001000	4KB	DMA2 控制寄存器
MCUPERI	DMA1	0x20071000	4KB	DMA1 控制寄存器
	EMAC	0x20070000	4KB	EMAC 控制寄存器
	AUDIO	0x20055000	4KB	Audio 控制寄存器
	USB	0x20072000	4KB	USB 控制寄存器
	HBN	0x2000F000	4KB	深度睡眠控制（休眠）寄存器
	PDS	0x2000E000	4KB	睡眠控制（掉电睡眠）寄存器
	DMA0	0x2000C000	4KB	DMA0 控制寄存器
	I2S	0x2000AB00	256B	I2S 控制寄存器
	ISO11898 UART2	0x2000AA00	256B	ISO11898 总线控制寄存器
		0x2000AA00	256B	UART2 控制寄存器
	I2C1	0x2000A900	256B	I2C1 控制寄存器
	IR	0x2000A600	256B	IR 控制寄存器
	TIMER0	0x2000A500	256B	TIMER0 控制寄存器
	PWM	0x2000A400	256B	PWM 控制寄存器
	I2C0	0x2000A300	256B	I2C0 控制寄存器
	SPI0	0x2000A200	256B	SPI0 控制寄存器
	UART1	0x2000A100	256B	UART1 控制寄存器
	UART0	0x2000A000	256B	UART0 控制寄存器
	eFuse	0x20056000	4KB	eFuse 存储器控制寄存器
	TZ	0x20005000	4KB	安全 Zone 分区
	SEC_ENG	0x20004000	4KB	安全引擎控制寄存器
	GPIP	0x20002000	1KB	通用 DAC / ADC / ACOMP 接口控制寄存器
	GLB	0x20000000	4KB	全局控制寄存器
ROM	ROM	0x90000000	128KB	Bootrom 区域地址空间

表 2.3: DRAM/VRAM 地址空间

DRAM/VRAM		Configure(reg_h2pf_sram_rel , reg_vram_sram_sel , reg_ispl_sram_rel , reg_blai_sram_rel)							
		0, 0, 0, 0	0, 0, 0, 1	1, 0, 0, 0	3, 0, 0, 0	0, 0, 1, 0	0, 1, 0, 0	2, 0, 0, 1	3, 1, 1, 1
DRAM	0x3EF80000 - 0x3EF8FFFF	-	-	-	-	-	-	-	64K
	0x3EF90000 - 0x3EF9FFFF	-	-	-	-	-	-	-	64K
	0x3EFA0000 - 0x3EFAFFFF	-	-	-	-	-	-	-	64K
	0x3EFB0000 - 0x3EFBFFFF	-	-	-	-	-	-	64K	64K
	0x3EFC0000 - 0x3EFCFFFF	-	-	-	64K	-	-	64K	64K
	0x3EFD0000 - 0x3EFDFFFF	-	64K	-	64K	-	-	64K	64K
	0x3EFE0000 - 0x3EFEFFFF	-	64K	64K	64K	64K	64K	64K	64K
	0x3EFF0000 - 0x3EFFFFFF	64K	64K	64K	64K	64K	64K	64K	64K
VRAM	0x3F000000 - 0x3F007FFF	32K	32K	32K	32K	32K	32K	32K	32K
	0x3F008000 - 0x3F017FFF	64K	64K	64K	64K	64K	-	64K	-

## 2.6 中断

BL808 支持内部 RTC 时钟唤醒、外部中断唤醒，以实现低功耗睡眠唤醒功能。

CPU 中断控制器支持 UART 中断、I2C 中断、SPI 中断、定时器中断、DMA 中断等在内的共 131 个可屏蔽中断触发源。

所有 I/O 引脚都可以配置为外部中断输入模式，外部中断支持同步高/低电平触发、同步上升沿/下降沿触发、异步高/低电平触发、异步上升沿/下降沿触发和同步双边沿触发共 9 种触发类型。

## 2.7 启动选项

BL808 支持多种启动选项，可选择从 UART、USB、Flash 闪存启动。

表 2.4: 启动模式

启动引脚	电平	描述
GPIO39	1	从 UART(GPIO20/21)/USB 启动，该模式主要用于 Flash 下载或者下载镜像到 RAM 执行
	0	从 Flash 启动应用镜像

## 2.8 电源管理单元

电源管理单元（PMU）管理整个芯片的电源，可分为运行、空闲、睡眠、休眠和电源关闭模式。软件可配置进入睡眠模式时，通过 RTC 定时器或 EINT 来唤醒，以达到低功耗电源管理。睡眠模式非常灵活，可以使应用配置为最低功耗。

## 2.9 时钟架构

时钟控制单元为核心 MCU 和外围 SOC 设备生成时钟。时钟源可以是 XTAL，PLL 或 RC 振荡器。通过适当的配置（例如 sel, div, en 等）来动态节省功耗。

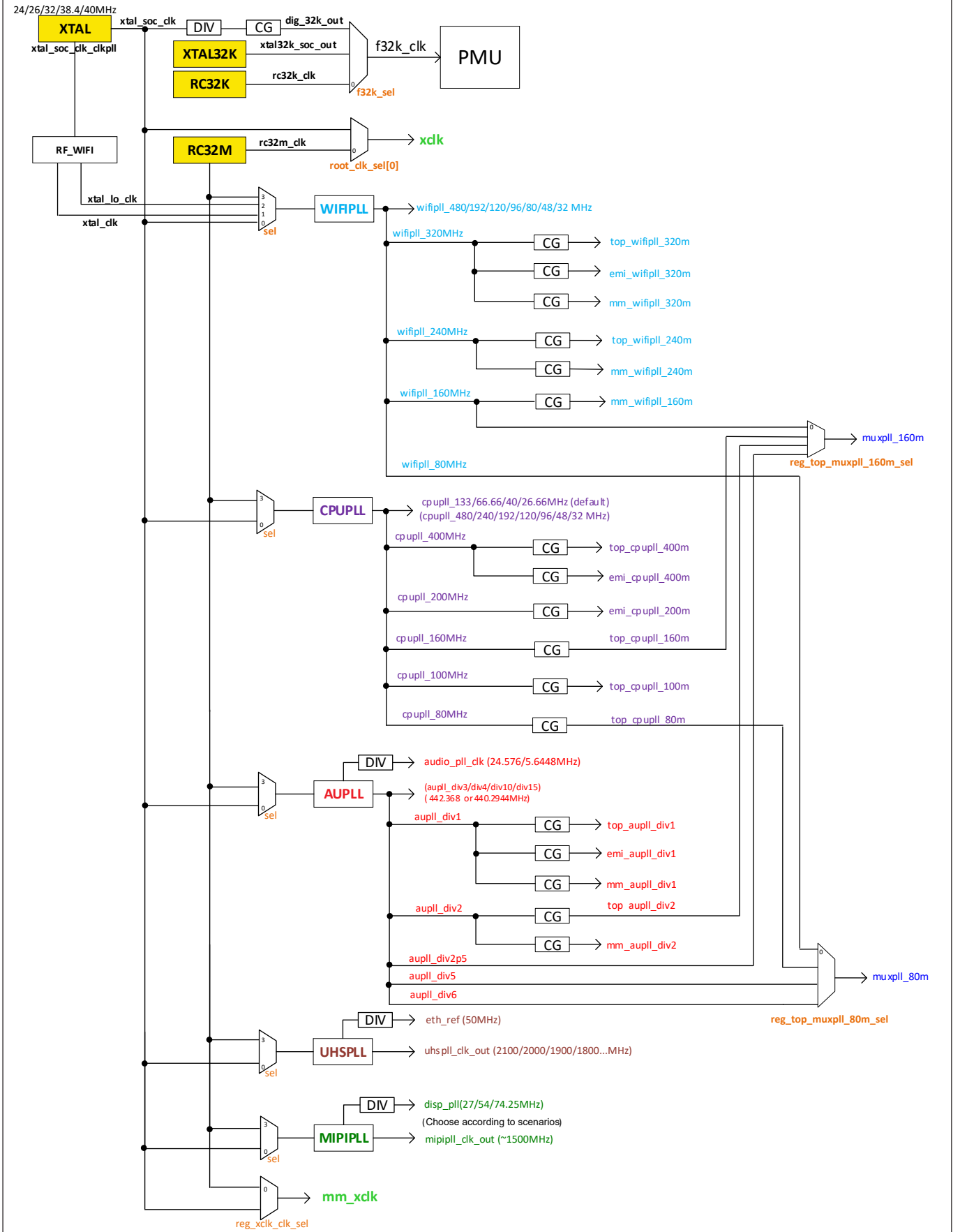


图 2.2: 系统时钟架构



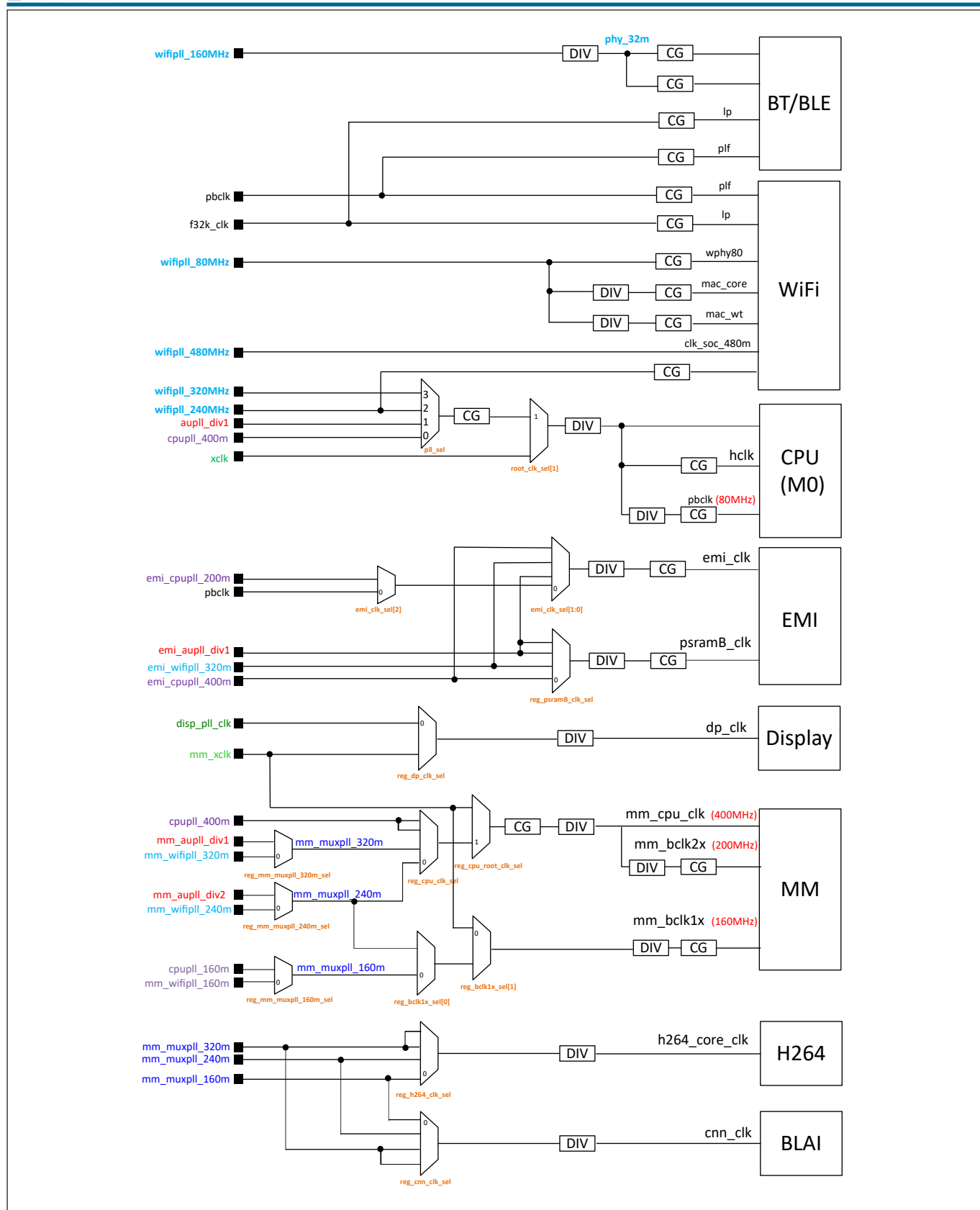


图 2.3: 模块时钟架构

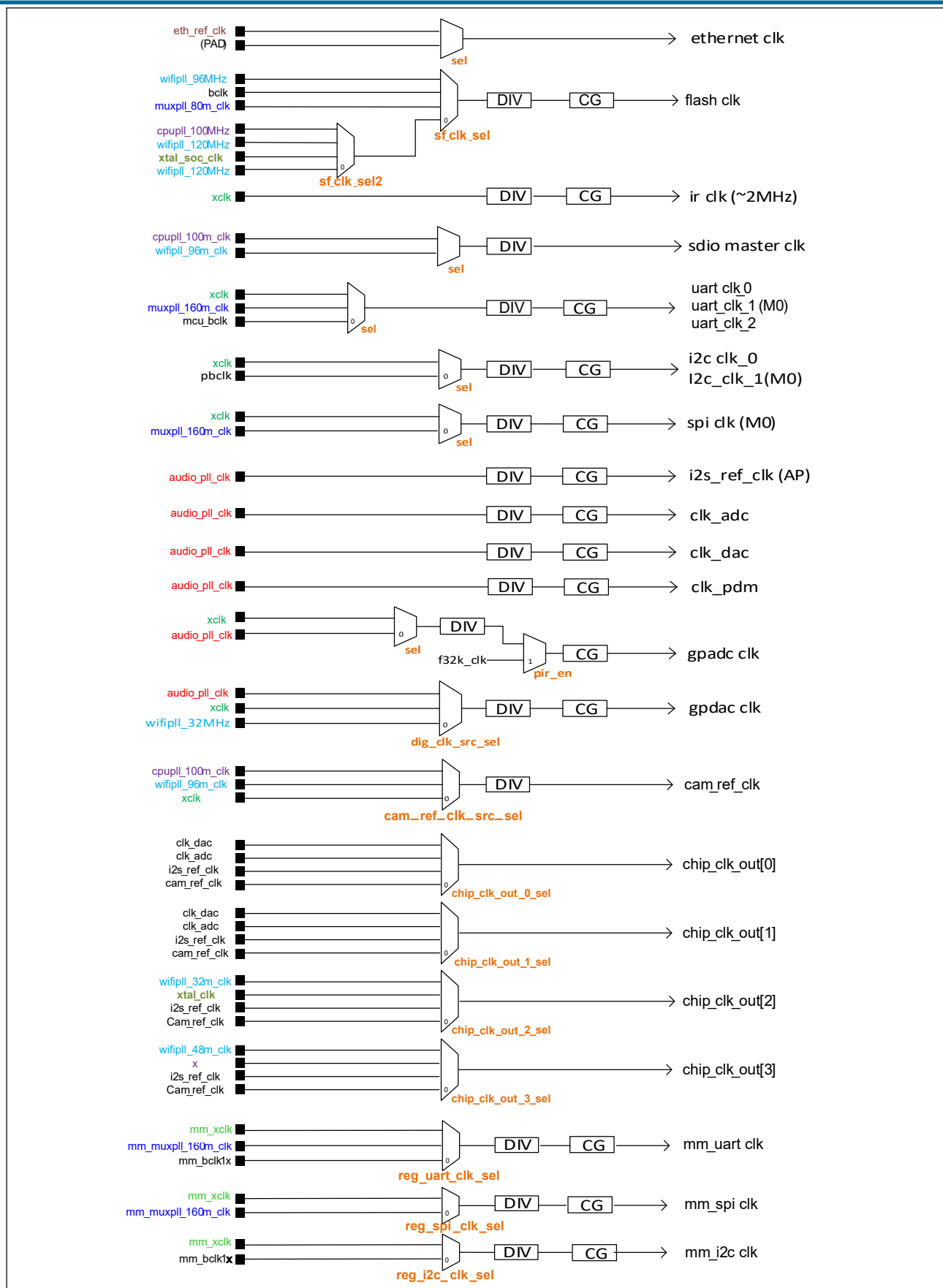


图 2.4: 外设时钟架构

## 2.10 外设

外设包括 USB2.0、Ethernet、SD/MMC、SPI、UART、I2C、I2S、PWM、GPDAC/GPADC、ACOMP、PIR、Touch、IR remote、Display 和 GPIO。

### 2.10.1 GPIO

BL808C 最多可达 40 个 GPIO，BL808D 最多可达 36 个 GPIO，具有以下特性：

- 每个 GPIO 都可用作通用输入和输出功能，上拉/下拉/浮空可由软件配置
- 每个 GPIO 都支持中断功能，中断支持同步高/低电平触发、同步上升沿/下降沿触发、异步高/低电平触发、异步上升沿/下降沿触发和同步双边沿触发
- 每个 GPIO 均可设置为高阻态，用于低功耗模式

### 2.10.2 UART

芯片内置四个通用异步串行收发器 (UART0/1/2/3)，具有以下特性：

- 支持硬件的 CTS 和 RTS 流控
- 支持 LIN 主/从功能
- 可配置的数据位、停止位和奇偶校验位
- 支持普通/固定字符的自动波特率检测
- 工作时钟可以选择为 BCLK、XCLK 或 160MHz，波特率最大支持 10Mbps
- TX 和 RX 具有独立 FIFO，FIFO 深度为 32 字节，支持 DMA 功能

### 2.10.3 SPI

芯片内置两个 SPI，可以配置为主机模式或者从机模式，SPI 模块时钟是 XCLK 或 160MHz，具有以下特性：

- 主机模式下，时钟频率最高为 80 MHz
- 从机模式下，允许主机最大的时钟频率为 80 MHz
- 每帧的位宽可以配置为 8 位/ 16 位/ 24 位/ 32 位
- 自适应的 FIFO 深度变化特性，适配高性能的场景应用
  - 当位宽为 32 位时，FIFO 的深度为 8
  - 当位宽为 24 位时，FIFO 的深度为 8
  - 当位宽为 16 位时，FIFO 的深度为 16
  - 当位宽为 8 位时，FIFO 的深度为 32

- 支持 DMA 传输模式

#### 2.10.4 I2C

芯片内置四个 I2C 接口，具有以下特性：

- 支持多主机模式和仲裁功能
- 工作时钟可以选择为 BCLK 或者 XCLK
- 具有器件地址寄存器，寄存器地址寄存器，寄存器地址长度可设置为 1 字节/ 2 字节/ 3 字节/ 4 字节
- I2C 具有独立收发 FIFO，FIFO 深度为 2 words
- 支持 DMA 功能

#### 2.10.5 I2S

芯片内置一个 I2S 接口，具有以下特性：

- 支持主模式以及从模式
- 支持 Left-justified/ Right-justified/ DSP 等数据格式，数据宽度可配置为 8/16/24/32 比特
- 工作时钟可以选择为 BCLK 或者 XCLK
- 除单声道/双声道模式之外，同时支持四声道与六声道模式
- 支持播放单声道音频复制为双声道模式
- 支持动态静音切换功能
- I2S 具有独立收发 FIFO，FIFO 深度为 16 words
- 支持 DMA 功能

#### 2.10.6 EMAC

EMAC 模块是一个兼容 IEEE 802.3 的 10/100Mbps 以太网 MAC(Ethernet Media Access Controller)，具有以下特性：

- 兼容 IEEE 802.3 定义的 MAC 层功能
- 支持 IEEE 802.3 定义的 MII/RMII 接口的 PHY
- 通过 MDIO 接口与 PHY 交互
- 支持 10Mbps 与 100Mbps 以太网
- 支持半双工与全双工
- 在全双工模式下，支持自动流控及生成控制帧
- 在半双工模式下，支持碰撞检测及重传

- 支持 CRC 的生成及校验
- 数据帧前导生成及移除
- 发送时，自动扩展短的数据帧
- 检测过长或过短的数据帧 (长度限制)
- 可传输长数据帧 (> 标准以太帧长度)
- 自动丢弃重发次数超限或帧间隙过小的数据包
- 广播包过滤
- 用于保存多达 128 个 BD(Buffer Descriptor) 的内部 RAM
- 在发送时，支持将一个数据包分拆配置到多个连续的 BD
- 发送/接收的各种事件标志
- 在事件发生时产生对应中断

EMAC 时序图如下所示：

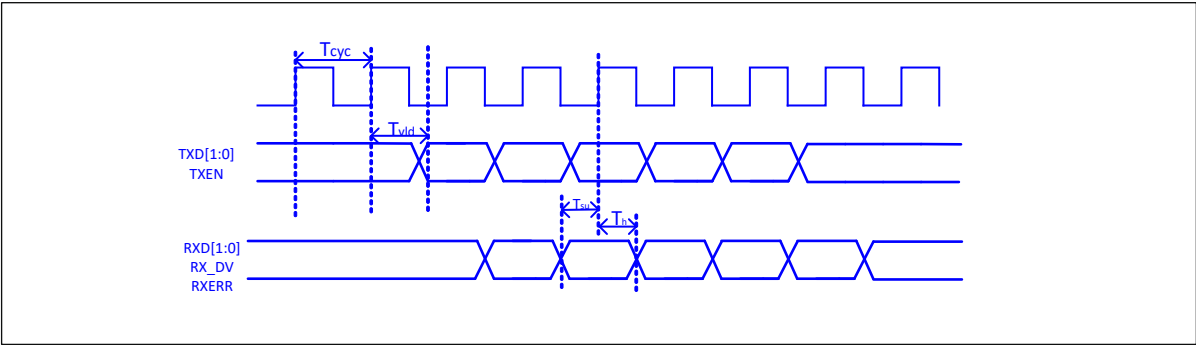


图 2.5: EMAC 时序图

表 2.5: 使用 RX Clock 对应的时序条件

将寄存器 eth_cfg0 对应的位设置为：cfg_inv_eth_rx_clk = 1, cfg_inv_eth_tx_clk = 0, cfg_sel_eth_ref_clk_o = 0						
时序参数 ( 1.8V, Load = 20PF )		最小值	典型值	最大值	单位	备注
T <sub>cyc</sub>	Clock Cycle	-	20	-	ns	Clock From ETH PHY
T <sub>vld</sub>	Output Valid Delay	10.37	-	22	ns	TXD/TX_EN
T <sub>su</sub>	Input Setup Time	6	-	-	ns	RXD/RX_DV/RXERR
T <sub>h</sub>	Input Hold Time	0	-	-	ns	RXD/RX_DV/RXERR

表 2.6: 不使用 RX Clock 对应的时序条件

将寄存器 eth_cfg0 对应的位设置为：cfg_inv_eth_rx_clk = 0, cfg_inv_eth_tx_clk = 0, cfg_sel_eth_ref_clk_o = 0						
时序参数 ( 1.8V, Load = 20PF )		最小值	典型值	最大值	单位	备注
T <sub>cyc</sub>	Clock Cycle	-	20	-	ns	Clock From ETH PHY
T <sub>vid</sub>	Output Valid Delay	10.374	-	22	ns	TXD/TX_EN
T <sub>su</sub>	Input Setup Time	5	-	-	ns	RXD/RX_DV/RXERR
T <sub>h</sub>	Input Hold Time	3	-	-	ns	RXD/RX_DV/RXERR

## 2.10.7 TIMER

芯片内置两个 32-bit 通用定时器和一个看门狗定时器，具有以下特性：

- 通用定时器的时钟源可以选择 FCLK/32K/XTAL，看门狗定时器的时钟源可以选择 FCLK/32K/XTAL
- 每个计数器都有 8-bit 分频器
- 每组通用定时器都包含三个比较寄存器，支持比较中断，计数模式支持 FreeRun 模式和 PreLoad 模式
- 16-bit 看门狗定时器，支持中断或复位两种看门狗溢出方式

## 2.10.8 PWM

芯片内置 2 组 PWM 信号，每组包含 4 通道 PWM 信号输出，每通道可以设置为 2 路互补 PWM，具有以下特性：

- 三种时钟源 BCLK/XCLK/32K 可供选择
- 分频寄存器和周期寄存器位宽为 16-bit
- 每通道 PWM 都支持输出极性可调，双门限值设定，增加脉冲输出灵活性
- 每通道 PWM 都有独立的死区时间设定
- 每路 PWM 都有独立的连接开关用来选择是否与内部计数器相连，并可设定不连接时的默认输出电平
- 软件刹车和外部刹车信号可以将 PWM 输出电平置于预先设定的状态
- 多达 11 种可用于触发 ADC 转换的触发源

### 2.10.9 IR(IR-remote)

芯片内置一个红外遥控，具有以下特性：

- 支持发送和接收两种模式
- 在非自由模式下发送最多支持 128-bit 数据位，自由模式下可连续发送任意长度数据
- 既支持以固定协议 NEC、RC-5 接收数据，也支持以脉冲宽度计数方式接收任意格式数据
- 时钟源为 XCLK，最高工作频率为 32MHz，具有强大的红外波形编辑能力，可发出符合各种协议的波形，发射功率有 15 档可调
- 接收 FIFO 深度为 128 字节，发送 FIFO 深度为 16 字节
- 发送支持 DMA 模式

### 2.10.10 PDM

芯片内置一个 PDM 音频处理模块，具有以下特性：

- 集成 3 路数字滤波器，可支持 3 路数字麦输入
  - 采样率：8k~48k
  - 信噪比 > 110dB
  - 数据有效位宽 20 bit
  - 数字增益：-95.5 ~ +32.5dB, 0.5dB 一档
- 独立可调的三通道高通滤波器
- 复用 GPIO 输入（1 个时钟输出，2 个数据输入）
- 发送 FIFO 位宽 32bit，深度 48
- 支持 DMA 传输模式

## 2.11 视频编码

### 2.11.1 简介

VENC 采用 H264 视频编码标准，主要是以预测及运动补偿等方式进行压缩，并以环路滤波提升画质，兼顾码流传输和图像品质要求。

### 2.11.2 主要特点

- 1920x1080p @ 30fps + 640x480 @ 30fps, BP/MP
- 输入: Semi-Planar YCbCr 4:2:0
- 输出: NALU(Network Abstract Layer Uint) in byte stream format
- CBR/VBR mode
- 最大 8 个 ROI
- 最大 16 个 OSD 编码区域
- 支持软件模式和连动模式
- 可动态配置最大/最小量化参数
- 可动态配置 I/P 帧目标位元
- 可动态配置 I 帧距离

## 2.12 与传感器和显示接口

### 2.12.1 与传感器

- MIPI-CSI
  1. 支持 1-/2-lane 模式
  2. 支持硬件解码 (RAW8/10/12/14, RGB565/888, YUV422 8-/10-bit) 或是软件解码
- DVP
  1. 支持 RAW 12-bit data
  2. 支持 YUV/RGB 8-bit 格式
  3. 支持影像压缩模式

### 2.12.2 与显示器

- MIPI-DSI
  1. 支持 1-/2-/4-lane 模式
  2. 支持 RGB565/666/888 以及 YUV422 8-bit 格式
  3. 支持 Sync Event Mode 或 Sync Pulse Mode
  4. 支持 Escape Mode, 且可搭配 DMA 功能使用
- MIPI-DBI



1. 支持 Type-B (8-bit)、Type-C Option 1 (3-wire) 以及 Type-C Option 3 (4-wire) 模式
  2. 支持 RGB565/666/888 格式
  3. 内建 YUV2RGB 转换模块
  4. 支持 DMA 功能
- MIPI-DPI
    1. 支持 data 16-bit 模式
    2. 支持 RGB565 格式
  - QSPI
    1. CMD/ADDR/DATA 可任意选择 1-/4-wire 模式，因此 QSPI 111/114/144/444 模式皆可支持
    2. 支持 RGB565/666/888 格式
    3. 内建 YUV2RGB 转换模块
    4. 支持 DMA 功能

BL808C 88-pin 封装包括固定电源接口 26 个、固定模拟接口 22 个、以及富含弹性的 GPIO 接口 40 个供应用选择。

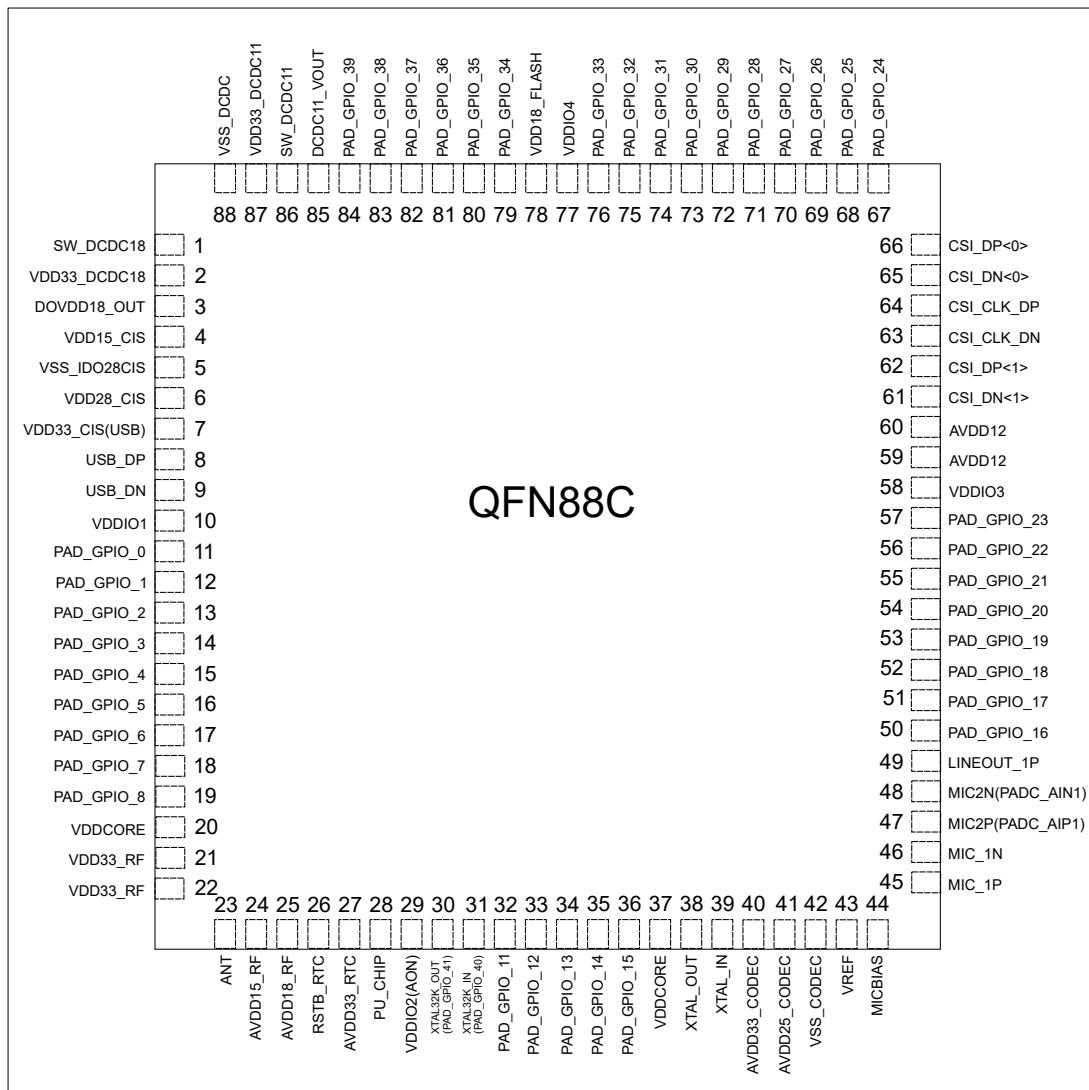


图 3.1: BL808C 管脚布局

BL808D 88-pin 封装包括固定电源接口 27 个、固定模拟接口 25 个、以及富含弹性的 GPIO 接口 36 个供应用选择。

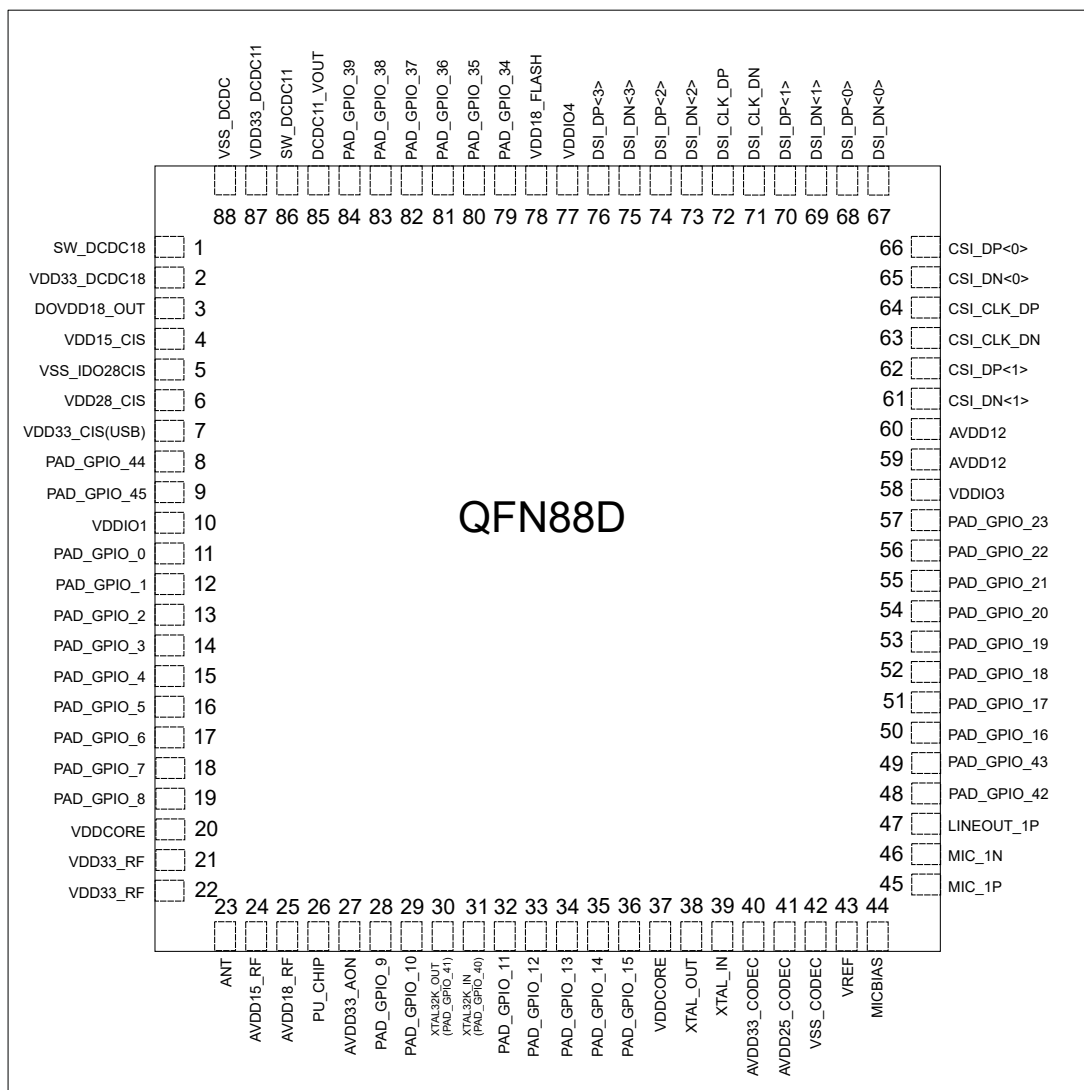


图 3.2: BL808D 管脚布局

表 3.1: 管脚定义

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
1	1	-	Power	SW_DCDC18	-	-	SW_DCDC18	DCDC switch output, connected to power inductor
2	2	-	Power	VDD33_DCDC18	-	-	VDD33_DCDC18	DCDC power input, 3.3V
3	3	-	Power	DOVDD18_OUT	-	-	DOVDD18_OUT	DCDC mode, feedback voltage input, 1.8V LDO mode, power output, 1.8V
4	4	-	Power	VDD15_CIS	-	-	VDD15_CIS	Integrated LDO output to power the image sensor digital power DVDD
5	5	-	Power	VSS_IDO28CIS	-	-	VSS_IDO28CIS	Connect to the image sensor analog ground AGND
6	6	-	Power	VDD28_CIS	-	-	VDD28_CIS	Integrated LDO output to power the image sensor analog power supply AVDD
7	7	-	Power	VDD33_CIS(USB)	-	-	VDD33_CIS(USB)	Integrated LDO VDD28_CIS input, 3.3V
8	-	VDDIO_1	DI/DO	USB_DP	-	-	USB_DP	USB2.0 differential data cable+
9	-	VDDIO_1	DI/DO	USB_DN	-	-	USB_DN	USB2.0 differential data cable

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	8	VDDIO_1	DI/DO	PAD_GPIO_44	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_8_sel=0	UART0_RTS	UART0_RTS
						uart_sig_8_sel=1	UART0_CTS	UART0_CTS
						uart_sig_8_sel=2	UART0_TXD	UART0_TXD
						uart_sig_8_sel=3	UART0_RXD	UART0_RXD
						uart_sig_8_sel=4	UART1_RTS	UART1_RTS
						uart_sig_8_sel=5	UART1_CTS	UART1_CTS
						uart_sig_8_sel=6	UART1_TXD	UART1_TXD
						uart_sig_8_sel=7	UART1_RXD	UART1_RXD
						uart_sig_8_sel=8	UART2_RTS	UART2_RTS
						uart_sig_8_sel=9	UART2_CTS	UART2_CTS
						uart_sig_8_sel=10	UART2_TXD	UART2_TXD
						uart_sig_8_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPI044	SWGPI044
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CS <sub>n</sub>	DBI_CS <sub>n</sub>
					24	-	-	-
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	9	VDDIO_1	DI/DO	PAD_GPIO_45	0	-	-	-
					1	-	SPI_MOSI <sup>1</sup>	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_9_sel=0	UART0_RTS	UART0_RTS
						uart_sig_9_sel=1	UART0_CTS	UART0_CTS
						uart_sig_9_sel=2	UART0_TXD	UART0_TXD
						uart_sig_9_sel=3	UART0_RXD	UART0_RXD
						uart_sig_9_sel=4	UART1_RTS	UART1_RTS
						uart_sig_9_sel=5	UART1_CTS	UART1_CTS
						uart_sig_9_sel=6	UART1_TXD	UART1_TXD
						uart_sig_9_sel=7	UART1_RXD	UART1_RXD
						uart_sig_9_sel=8	UART2_RTS	UART2_RTS
						uart_sig_9_sel=9	UART2_CTS	UART2_CTS
						uart_sig_9_sel=10	UART2_TXD	UART2_TXD
						uart_sig_9_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPI045	SWGPI045
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI
10	10	-	Power	VDDIO1	-	-	VDDIO1	GPIO0~8, GPIO44~45 power supply, 3.3V/1.8V

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
11	11	VDDIO_1	DI/DO	PAD_GPIO_0	0	-	SDH_CLK	SDH_CLK
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
						uart_sig_0_sel=4	UART1_RTS	UART1_RTS
						uart_sig_0_sel=5	UART1_CTS	UART1_CTS
						uart_sig_0_sel=6	UART1_TXD	UART1_TXD
						uart_sig_0_sel=7	UART1_RXD	UART1_RXD
						uart_sig_0_sel=8	UART2_RTS	UART2_RTS
						uart_sig_0_sel=9	UART2_CTS	UART2_CTS
						uart_sig_0_sel=10	UART2_TXD	UART2_TXD
						uart_sig_0_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	USB20_RREF_EXT	USB20_RREF_EXT
					11	-	SWGPI00	SWGPI00
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CS <sub>n</sub>	DBI_CS <sub>n</sub>
					24	-	-	-
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

**表 3.1: 管脚定义 (continued)**

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
12	12	VDDIO_1	DI/DO	PAD_GPIO_1	0	-	SDH_CMD	SDH_CMD
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
						uart_sig_1_sel=4	UART1_RTS	UART1_RTS
						uart_sig_1_sel=5	UART1_CTS	UART1_CTS
						uart_sig_1_sel=6	UART1_TXD	UART1_TXD
						uart_sig_1_sel=7	UART1_RXD	UART1_RXD
						uart_sig_1_sel=8	UART2_RTS	UART2_RTS
						uart_sig_1_sel=9	UART2_CTS	UART2_CTS
						uart_sig_1_sel=10	UART2_TXD	UART2_TXD
						uart_sig_1_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPI01	SWGPI01
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

**表 3.1: 管脚定义 (continued)**

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
13	13	VDDIO_1	DI/DO	PAD_GPIO_2	0	-	SDH_DAT0	SDH_DAT0
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
						uart_sig_2_sel=4	UART1_RTS	UART1_RTS
						uart_sig_2_sel=5	UART1_CTS	UART1_CTS
						uart_sig_2_sel=6	UART1_TXD	UART1_TXD
						uart_sig_2_sel=7	UART1_RXD	UART1_RXD
						uart_sig_2_sel=8	UART2_RTS	UART2_RTS
						uart_sig_2_sel=9	UART2_CTS	UART2_CTS
						uart_sig_2_sel=10	UART2_TXD	UART2_TXD
						uart_sig_2_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO2	SWGPIO2
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS



**表 3.1: 管脚定义 (continued)**

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
14	14	VDDIO_1	DI/DO	PAD_GPIO_3	0	-	SDH_DAT1	SDH_DAT1
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
						uart_sig_3_sel=4	UART1_RTS	UART1_RTS
						uart_sig_3_sel=5	UART1_CTS	UART1_CTS
						uart_sig_3_sel=6	UART1_TXD	UART1_TXD
						uart_sig_3_sel=7	UART1_RXD	UART1_RXD
						uart_sig_3_sel=8	UART2_RTS	UART2_RTS
						uart_sig_3_sel=9	UART2_CTS	UART2_CTS
						uart_sig_3_sel=10	UART2_TXD	UART2_TXD
						uart_sig_3_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO3	SWGPIO3
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
15	15	VDDIO_1	DI/DO	PAD_GPIO_4	0	-	SDH_DAT2	SDH_DAT2
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_4_sel=0	UART0_RTS	UART0_RTS
						uart_sig_4_sel=1	UART0_CTS	UART0_CTS
						uart_sig_4_sel=2	UART0_TXD	UART0_TXD
						uart_sig_4_sel=3	UART0_RXD	UART0_RXD
						uart_sig_4_sel=4	UART1_RTS	UART1_RTS
						uart_sig_4_sel=5	UART1_CTS	UART1_CTS
						uart_sig_4_sel=6	UART1_TXD	UART1_TXD
						uart_sig_4_sel=7	UART1_RXD	UART1_RXD
						uart_sig_4_sel=8	UART2_RTS	UART2_RTS
						uart_sig_4_sel=9	UART2_CTS	UART2_CTS
						uart_sig_4_sel=10	UART2_TXD	UART2_TXD
						uart_sig_4_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH2	ADC_CH2
					11	-	SWGPIO4	SWGPIO4
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CS <sub>n</sub>	DBI_CS <sub>n</sub>
					24	-	-	-
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
16	16	VDDIO_1	DI/DO	PAD_GPIO_5	0	-	SDH_DAT3	SDH_DAT3
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_5_sel=0	UART0_RTS	UART0_RTS
						uart_sig_5_sel=1	UART0_CTS	UART0_CTS
						uart_sig_5_sel=2	UART0_TXD	UART0_TXD
						uart_sig_5_sel=3	UART0_RXD	UART0_RXD
						uart_sig_5_sel=4	UART1_RTS	UART1_RTS
						uart_sig_5_sel=5	UART1_CTS	UART1_CTS
						uart_sig_5_sel=6	UART1_TXD	UART1_TXD
						uart_sig_5_sel=7	UART1_RXD	UART1_RXD
						uart_sig_5_sel=8	UART2_RTS	UART2_RTS
						uart_sig_5_sel=9	UART2_CTS	UART2_CTS
						uart_sig_5_sel=10	UART2_TXD	UART2_TXD
						uart_sig_5_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH1	ADC_CH1
					11	-	SWGPIOS	SWGPIOS
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
17	17	VDDIO_1	DI/DO	PAD_GPIO_6	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_6_sel=0	UART0_RTS	UART0_RTS
						uart_sig_6_sel=1	UART0_CTS	UART0_CTS
						uart_sig_6_sel=2	UART0_TXD	UART0_TXD
						uart_sig_6_sel=3	UART0_RXD	UART0_RXD
						uart_sig_6_sel=4	UART1_RTS	UART1_RTS
						uart_sig_6_sel=5	UART1_CTS	UART1_CTS
						uart_sig_6_sel=6	UART1_TXD	UART1_TXD
						uart_sig_6_sel=7	UART1_RXD	UART1_RXD
						uart_sig_6_sel=8	UART2_RTS	UART2_RTS
						uart_sig_6_sel=9	UART2_CTS	UART2_CTS
						uart_sig_6_sel=10	UART2_TXD	UART2_TXD
						uart_sig_6_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH4	ADC_CH4
					11	-	SWGPIO6	SWGPIO6
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
18	18	VDDIO_1	DI/DO	PAD_GPIO_7	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_7_sel=0	UART0_RTS	UART0_RTS
						uart_sig_7_sel=1	UART0_CTS	UART0_CTS
						uart_sig_7_sel=2	UART0_TXD	UART0_TXD
						uart_sig_7_sel=3	UART0_RXD	UART0_RXD
						uart_sig_7_sel=4	UART1_RTS	UART1_RTS
						uart_sig_7_sel=5	UART1_CTS	UART1_CTS
						uart_sig_7_sel=6	UART1_TXD	UART1_TXD
						uart_sig_7_sel=7	UART1_RXD	UART1_RXD
						uart_sig_7_sel=8	UART2_RTS	UART2_RTS
						uart_sig_7_sel=9	UART2_CTS	UART2_CTS
						uart_sig_7_sel=10	UART2_TXD	UART2_TXD
						uart_sig_7_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO7	SWGPIO7
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
19	19	VDDIO_1	DI/DO	PAD_GPIO_8	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_8_sel=0	UART0_RTS	UART0_RTS
						uart_sig_8_sel=1	UART0_CTS	UART0_CTS
						uart_sig_8_sel=2	UART0_TXD	UART0_TXD
						uart_sig_8_sel=3	UART0_RXD	UART0_RXD
						uart_sig_8_sel=4	UART1_RTS	UART1_RTS
						uart_sig_8_sel=5	UART1_CTS	UART1_CTS
						uart_sig_8_sel=6	UART1_TXD	UART1_TXD
						uart_sig_8_sel=7	UART1_RXD	UART1_RXD
						uart_sig_8_sel=8	UART2_RTS	UART2_RTS
						uart_sig_8_sel=9	UART2_CTS	UART2_CTS
						uart_sig_8_sel=10	UART2_TXD	UART2_TXD
						uart_sig_8_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO8	SWGPIO8
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CS <sub>n</sub>	DBI_CS <sub>n</sub>
					24	-	-	-
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK
20	20	-	Power	VDDCORE	-	-	VDDCORE	Core power, 1.1V
21	21	-	Power	VDD33_RF	-	-	VDD33_RF	RF transmitter power supply, 3.3V
22	22	-	Power	VDD33_RF	-	-	VDD33_RF	RF transmitter power supply, 3.3V
23	23	AVDD15	Analog	ANT	-	-	ANT	RF signal pin
24	24	-	Power	AVDD15_RF	-	-	AVDD15_RF	Integrated LDO output, RF circuit power supply, 1.5V, connected to decoupling capacitors
25	25	-	Power	AVDD18_RF	-	-	AVDD18_RF	Integrated LDO input, 1.8V (connected to the third pin VDD18_OUT)/3.3V
26	-	-	Power	RSTB_RTC	-	-	RSTB_RTC	Real-time clock circuit reset, active low
28	26	AVDD33	Analog	PU_CHIP	-	-	PU_CHIP	Chip enable, active high
27	-	-	Power	AVDD33_RTC	-	-	AVDD33_RTC	Real-time clock circuit power supply, 3.3V
29	27	-	Power	VDDIO2(AON)	-	-	VDDIO2(AON)	GPIO11~15, GPIO40~41 and AON circuit power input, 3.3V

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	28	AVDD33	DI/DO	PAD_GPIO_9	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_9_sel=0	UART0_RTS	UART0_RTS
						uart_sig_9_sel=1	UART0_CTS	UART0_CTS
						uart_sig_9_sel=2	UART0_TXD	UART0_TXD
						uart_sig_9_sel=3	UART0_RXD	UART0_RXD
						uart_sig_9_sel=4	UART1_RTS	UART1_RTS
						uart_sig_9_sel=5	UART1_CTS	UART1_CTS
						uart_sig_9_sel=6	UART1_TXD	UART1_TXD
						uart_sig_9_sel=7	UART1_RXD	UART1_RXD
						uart_sig_9_sel=8	UART2_RTS	UART2_RTS
						uart_sig_9_sel=9	UART2_CTS	UART2_CTS
						uart_sig_9_sel=10	UART2_TXD	UART2_TXD
						uart_sig_9_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPI09	SWGPI09
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	29	AVDD33	DI/DO	PAD_GPIO_10	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_10_sel=0	UART0_RTS	UART0_RTS
						uart_sig_10_sel=1	UART0_CTS	UART0_CTS
						uart_sig_10_sel=2	UART0_TXD	UART0_TXD
						uart_sig_10_sel=3	UART0_RXD	UART0_RXD
						uart_sig_10_sel=4	UART1_RTS	UART1_RTS
						uart_sig_10_sel=5	UART1_CTS	UART1_CTS
						uart_sig_10_sel=6	UART1_TXD	UART1_TXD
						uart_sig_10_sel=7	UART1_RXD	UART1_RXD
						uart_sig_10_sel=8	UART2_RTS	UART2_RTS
						uart_sig_10_sel=9	UART2_CTS	UART2_CTS
						uart_sig_10_sel=10	UART2_TXD	UART2_TXD
						uart_sig_10_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPI010	SWGPI010
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS



表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
30	30	AVDD33	Clock	XTAL32K_OUT	-	XTAL32K_OUT	XTAL32K_OUT	Connect to RTC passive crystal/active clock
		VDDIO_2	DI/DO	PAD_GPIO_41	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_5_sel=0	UART0_RTS	UART0_RTS
						uart_sig_5_sel=1	UART0_CTS	UART0_CTS
						uart_sig_5_sel=2	UART0_TXD	UART0_TXD
						uart_sig_5_sel=3	UART0_RXD	UART0_RXD
						uart_sig_5_sel=4	UART1_RTS	UART1_RTS
						uart_sig_5_sel=5	UART1_CTS	UART1_CTS
						uart_sig_5_sel=6	UART1_TXD	UART1_TXD
						uart_sig_5_sel=7	UART1_RXD	UART1_RXD
						uart_sig_5_sel=8	UART2_RTS	UART2_RTS
						uart_sig_5_sel=9	UART2_CTS	UART2_CTS
						uart_sig_5_sel=10	UART2_TXD	UART2_TXD
						uart_sig_5_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPI041	SWGPI041
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
31	31	AVDD33	Clock	XTAL32K_IN	-	XTAL32K_IN	XTAL32K_IN	Connect to RTC passive crystal
		VDDIO_2	DI/DO	PAD_GPIO_40	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_4_sel=0	UART0_RTS	UART0_RTS
						uart_sig_4_sel=1	UART0_CTS	UART0_CTS
						uart_sig_4_sel=2	UART0_TXD	UART0_TXD
						uart_sig_4_sel=3	UART0_RXD	UART0_RXD
						uart_sig_4_sel=4	UART1_RTS	UART1_RTS
						uart_sig_4_sel=5	UART1_CTS	UART1_CTS
						uart_sig_4_sel=6	UART1_TXD	UART1_TXD
						uart_sig_4_sel=7	UART1_RXD	UART1_RXD
						uart_sig_4_sel=8	UART2_RTS	UART2_RTS
						uart_sig_4_sel=9	UART2_CTS	UART2_CTS
						uart_sig_4_sel=10	UART2_TXD	UART2_TXD
						uart_sig_4_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH5	ADC_CH5
					11	-	SWGPI040	SWGPI040
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	DBI_RDn	DBI_RDn
					23	-	DBI_CSn	DBI_CSn
					24	-	-	-
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
32	32	VDDIO_2	DI/DO	PAD_GPIO_11	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_11_sel=0	UART0_RTS	UART0_RTS
						uart_sig_11_sel=1	UART0_CTS	UART0_CTS
						uart_sig_11_sel=2	UART0_TXD	UART0_TXD
						uart_sig_11_sel=3	UART0_RXD	UART0_RXD
						uart_sig_11_sel=4	UART1_RTS	UART1_RTS
						uart_sig_11_sel=5	UART1_CTS	UART1_CTS
						uart_sig_11_sel=6	UART1_TXD	UART1_TXD
						uart_sig_11_sel=7	UART1_RXD	UART1_RXD
						uart_sig_11_sel=8	UART2_RTS	UART2_RTS
						uart_sig_11_sel=9	UART2_CTS	UART2_CTS
						uart_sig_11_sel=10	UART2_TXD	UART2_TXD
						uart_sig_11_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH3	ADC_CH3
					11	-	SWGPIIO11	SWGPIIO11
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	DBI_CS <sub>n</sub>	DBI_CS <sub>n</sub>
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
33	33	VDDIO_2	DI/DO	PAD_GPIO_12	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
						uart_sig_0_sel=4	UART1_RTS	UART1_RTS
						uart_sig_0_sel=5	UART1_CTS	UART1_CTS
						uart_sig_0_sel=6	UART1_TXD	UART1_TXD
						uart_sig_0_sel=7	UART1_RXD	UART1_RXD
						uart_sig_0_sel=8	UART2_RTS	UART2_RTS
						uart_sig_0_sel=9	UART2_CTS	UART2_CTS
						uart_sig_0_sel=10	UART2_TXD	UART2_TXD
						uart_sig_0_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH6	ADC_CH6
					11	-	SWGPIO12	SWGPIO12
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	DBI_DCn	DBI_DCn
					23	-	DBI_CSn	DBI_CSn
					24	-	DPI_VS	DPI_VS
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
34	34	VDDIO_2	DI/DO	PAD_GPIO_13	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
						uart_sig_1_sel=4	UART1_RTS	UART1_RTS
						uart_sig_1_sel=5	UART1_CTS	UART1_CTS
						uart_sig_1_sel=6	UART1_TXD	UART1_TXD
						uart_sig_1_sel=7	UART1_RXD	UART1_RXD
						uart_sig_1_sel=8	UART2_RTS	UART2_RTS
						uart_sig_1_sel=9	UART2_CTS	UART2_CTS
						uart_sig_1_sel=10	UART2_TXD	UART2_TXD
						uart_sig_1_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH7	ADC_CH7
					11	-	SWGPIO13	SWGPIO13
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	DBI_WRn	DBI_WRn
					23	-	DBI_DCn	DBI_DCn
					24	-	DPI_HS	DPI_HS
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
35	35	VDDIO_2	DI/DO	PAD_GPIO_14	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
						uart_sig_2_sel=4	UART1_RTS	UART1_RTS
						uart_sig_2_sel=5	UART1_CTS	UART1_CTS
						uart_sig_2_sel=6	UART1_TXD	UART1_TXD
						uart_sig_2_sel=7	UART1_RXD	UART1_RXD
						uart_sig_2_sel=8	UART2_RTS	UART2_RTS
						uart_sig_2_sel=9	UART2_CTS	UART2_CTS
						uart_sig_2_sel=10	UART2_TXD	UART2_TXD
						uart_sig_2_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPI014	SWGPI014
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
36	36	VDDIO_2	DI/DO	PAD_GPIO_15	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
						uart_sig_3_sel=4	UART1_RTS	UART1_RTS
						uart_sig_3_sel=5	UART1_CTS	UART1_CTS
						uart_sig_3_sel=6	UART1_TXD	UART1_TXD
						uart_sig_3_sel=7	UART1_RXD	UART1_RXD
						uart_sig_3_sel=8	UART2_RTS	UART2_RTS
						uart_sig_3_sel=9	UART2_CTS	UART2_CTS
						uart_sig_3_sel=10	UART2_TXD	UART2_TXD
						uart_sig_3_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO15	SWGPIO15
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO
37	37	-	Power	VDDCORE	-	-	VDDCORE	Core Power, 1.1V
38	38	AVDD33	Clock	XTAL_OUT	-	-	XTAL_OUT	Connect high frequency passive crystal
39	39	AVDD33	Clock	XTAL_IN	-	-	XTAL_IN	Connect high frequency passive crystal/active clock
40	40	-	Power	AVDD33_CODEC	-	-	AVDD33_CODEC	Integrated LDO input, 3.3V
41	41	-	Power	AVDD25_CODEC	-	-	AVDD25_CODEC	Integrated LDO output, audio codec circuit power supply, 2.5V, connected to decoupling capacitors
42	42	-	Power	VSS_CODEC	-	-	VSS_CODEC	Audio codec circuit ground pin
43	43	-	Power	VREF	-	-	VREF	Audio codec circuit reference voltage, connected to decoupling capacitors
44	44	-	Power	MICBIAS	-	-	MICBIAS	Microphone Bias/Power
45	45	AVDD33/25	Analog	MIC_1P	-	-	MIC_1P	Microphone 1 differential input+
46	46	AVDD33/25	Analog	MIC_1N	-	-	MIC_1N	Microphone 1 differential input-
47	-	AVDD33/25	Analog	MIC2P(PADC_AIP1)	-	-	MIC2P(PADC_AIP1)	Microphone 2 differential input+
48	-	AVDD33/25	Analog	MIC2N(PADC_AIN1)	-	-	MIC2N(PADC_AIN1)	Microphone 2 differential input-
49	47	AVDD33/25	Analog	LINEOUT_1P	-	-	LINEOUT_1P	Line 1 single-ended output

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	48	VDDIO_3	DI/DO	PAD_GPIO_42	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_6_sel=0	UART0_RTS	UART0_RTS
						uart_sig_6_sel=1	UART0_CTS	UART0_CTS
						uart_sig_6_sel=2	UART0_TXD	UART0_TXD
						uart_sig_6_sel=3	UART0_RXD	UART0_RXD
						uart_sig_6_sel=4	UART1_RTS	UART1_RTS
						uart_sig_6_sel=5	UART1_CTS	UART1_CTS
						uart_sig_6_sel=6	UART1_TXD	UART1_TXD
						uart_sig_6_sel=7	UART1_RXD	UART1_RXD
						uart_sig_6_sel=8	UART2_RTS	UART2_RTS
						uart_sig_6_sel=9	UART2_CTS	UART2_CTS
						uart_sig_6_sel=10	UART2_TXD	UART2_TXD
						uart_sig_6_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPI042	SWGPI042
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS



**表 3.1: 管脚定义 (continued)**

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	49	VDDIO_3	DI/DO	PAD_GPIO_43	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_7_sel=0	UART0_RTS	UART0_RTS
						uart_sig_7_sel=1	UART0_CTS	UART0_CTS
						uart_sig_7_sel=2	UART0_TXD	UART0_TXD
						uart_sig_7_sel=3	UART0_RXD	UART0_RXD
						uart_sig_7_sel=4	UART1_RTS	UART1_RTS
						uart_sig_7_sel=5	UART1_CTS	UART1_CTS
						uart_sig_7_sel=6	UART1_TXD	UART1_TXD
						uart_sig_7_sel=7	UART1_RXD	UART1_RXD
						uart_sig_7_sel=8	UART2_RTS	UART2_RTS
						uart_sig_7_sel=9	UART2_CTS	UART2_CTS
						uart_sig_7_sel=10	UART2_TXD	UART2_TXD
						uart_sig_7_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO43	SWGPIO43
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
50	50	VDDIO_3	DI/DO	PAD_GPIO_16	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_4_sel=0	UART0_RTS	UART0_RTS
						uart_sig_4_sel=1	UART0_CTS	UART0_CTS
						uart_sig_4_sel=2	UART0_TXD	UART0_TXD
						uart_sig_4_sel=3	UART0_RXD	UART0_RXD
						uart_sig_4_sel=4	UART1_RTS	UART1_RTS
						uart_sig_4_sel=5	UART1_CTS	UART1_CTS
						uart_sig_4_sel=6	UART1_TXD	UART1_TXD
						uart_sig_4_sel=7	UART1_RXD	UART1_RXD
						uart_sig_4_sel=8	UART2_RTS	UART2_RTS
						uart_sig_4_sel=9	UART2_CTS	UART2_CTS
						uart_sig_4_sel=10	UART2_TXD	UART2_TXD
						uart_sig_4_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	CAM_HSYNC	CAM_HSYNC
					10	-	ADC_CH8	ADC_CH8
					11	-	SWGPI016	SWGPI016
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	DBI_DB_0	DBI_DB_0
					23	-	DBI_CS <sub>n</sub>	DBI_CS <sub>n</sub>
					24	-	DPI_PCLK	DPI_PCLK
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
51	51	VDDIO_3	DI/DO	PAD_GPIO_17	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_5_sel=0	UART0_RTS	UART0_RTS
						uart_sig_5_sel=1	UART0_CTS	UART0_CTS
						uart_sig_5_sel=2	UART0_TXD	UART0_TXD
						uart_sig_5_sel=3	UART0_RXD	UART0_RXD
						uart_sig_5_sel=4	UART1_RTS	UART1_RTS
						uart_sig_5_sel=5	UART1_CTS	UART1_CTS
						uart_sig_5_sel=6	UART1_TXD	UART1_TXD
						uart_sig_5_sel=7	UART1_RXD	UART1_RXD
						uart_sig_5_sel=8	UART2_RTS	UART2_RTS
						uart_sig_5_sel=9	UART2_CTS	UART2_CTS
						uart_sig_5_sel=10	UART2_TXD	UART2_TXD
						uart_sig_5_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	CAM_VSYNC	CAM_VSYNC
					10	-	ADC_CH0	ADC_CH0
					11	-	SWGPI017	SWGPI017
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	DBI_DB_1	DBI_DB_1
					23	-	DBI_DCn	DBI_DCn
					24	-	DPI_DATA[0]	DPI_DATA[0]
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

**表 3.1: 管脚定义 (continued)**

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
52	52	VDDIO_3	DI/DO	PAD_GPIO_18	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_6_sel=0	UART0_RTS	UART0_RTS
						uart_sig_6_sel=1	UART0_CTS	UART0_CTS
						uart_sig_6_sel=2	UART0_TXD	UART0_TXD
						uart_sig_6_sel=3	UART0_RXD	UART0_RXD
						uart_sig_6_sel=4	UART1_RTS	UART1_RTS
						uart_sig_6_sel=5	UART1_CTS	UART1_CTS
						uart_sig_6_sel=6	UART1_TXD	UART1_TXD
						uart_sig_6_sel=7	UART1_RXD	UART1_RXD
						uart_sig_6_sel=8	UART2_RTS	UART2_RTS
						uart_sig_6_sel=9	UART2_CTS	UART2_CTS
						uart_sig_6_sel=10	UART2_TXD	UART2_TXD
						uart_sig_6_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	PIX_DAT8	PIX_DAT8
					10	-	ADC_CH9	ADC_CH9
					11	-	SWGPI018	SWGPI018
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	DBI_DB_2	DBI_DB_2
					23	-	DBI_SCL	DBI_SCL
					24	-	DPI_DATA[1]	DPI_DATA[1]
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

**表 3.1: 管脚定义 (continued)**

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
53	53	VDDIO_3	DI/DO	PAD_GPIO_19	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_7_sel=0	UART0_RTS	UART0_RTS
						uart_sig_7_sel=1	UART0_CTS	UART0_CTS
						uart_sig_7_sel=2	UART0_TXD	UART0_TXD
						uart_sig_7_sel=3	UART0_RXD	UART0_RXD
						uart_sig_7_sel=4	UART1_RTS	UART1_RTS
						uart_sig_7_sel=5	UART1_CTS	UART1_CTS
						uart_sig_7_sel=6	UART1_TXD	UART1_TXD
						uart_sig_7_sel=7	UART1_RXD	UART1_RXD
						uart_sig_7_sel=8	UART2_RTS	UART2_RTS
						uart_sig_7_sel=9	UART2_CTS	UART2_CTS
						uart_sig_7_sel=10	UART2_TXD	UART2_TXD
						uart_sig_7_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	PIX_DAT9	PIX_DAT9
					10	-	ADC_CH10	ADC_CH10
					11	-	SWGPIO19	SWGPIO19
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	DBI_DB_3	DBI_DB_3
					23	-	DBI_SDA	DBI_SDA
					24	-	DPI_DATA[2]	DPI_DATA[2]
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
54	54	VDDIO_3	DI/DO	PAD_GPIO_20	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_8_sel=0	UART0_RTS	UART0_RTS
						uart_sig_8_sel=1	UART0_CTS	UART0_CTS
						uart_sig_8_sel=2	UART0_TXD	UART0_TXD
						uart_sig_8_sel=3	UART0_RXD	UART0_RXD
						uart_sig_8_sel=4	UART1_RTS	UART1_RTS
						uart_sig_8_sel=5	UART1_CTS	UART1_CTS
						uart_sig_8_sel=6	UART1_TXD	UART1_TXD
						uart_sig_8_sel=7	UART1_RXD	UART1_RXD
						uart_sig_8_sel=8	UART2_RTS	UART2_RTS
						uart_sig_8_sel=9	UART2_CTS	UART2_CTS
						uart_sig_8_sel=10	UART2_TXD	UART2_TXD
						uart_sig_8_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	PIX_DAT10	PIX_DAT10
					10	-	-	-
					11	-	SWGPI020	SWGPI020
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	DBI_DB_4	DBI_DB_4
					23	-	DBI_CS <sub>n</sub>	DBI_CS <sub>n</sub>
					24	-	DPI_DATA[3]	DPI_DATA[3]
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
55	55	VDDIO_3	DI/DO	PAD_GPIO_21	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_9_sel=0	UART0_RTS	UART0_RTS
						uart_sig_9_sel=1	UART0_CTS	UART0_CTS
						uart_sig_9_sel=2	UART0_TXD	UART0_TXD
						uart_sig_9_sel=3	UART0_RXD	UART0_RXD
						uart_sig_9_sel=4	UART1_RTS	UART1_RTS
						uart_sig_9_sel=5	UART1_CTS	UART1_CTS
						uart_sig_9_sel=6	UART1_TXD	UART1_TXD
						uart_sig_9_sel=7	UART1_RXD	UART1_RXD
						uart_sig_9_sel=8	UART2_RTS	UART2_RTS
						uart_sig_9_sel=9	UART2_CTS	UART2_CTS
						uart_sig_9_sel=10	UART2_TXD	UART2_TXD
						uart_sig_9_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	PIX_DAT11	PIX_DAT11
					10	-	-	-
					11	-	SWGPI021	SWGPI021
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	DBI_DB_5	DBI_DB_5
					23	-	DBI_DCn	DBI_DCn
					24	-	DPI_DATA[4]	DPI_DATA[4]
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
56	56	VDDIO_3	DI/DO	PAD_GPIO_22	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_10_sel=0	UART0_RTS	UART0_RTS
						uart_sig_10_sel=1	UART0_CTS	UART0_CTS
						uart_sig_10_sel=2	UART0_TXD	UART0_TXD
						uart_sig_10_sel=3	UART0_RXD	UART0_RXD
						uart_sig_10_sel=4	UART1_RTS	UART1_RTS
						uart_sig_10_sel=5	UART1_CTS	UART1_CTS
						uart_sig_10_sel=6	UART1_TXD	UART1_TXD
						uart_sig_10_sel=7	UART1_RXD	UART1_RXD
						uart_sig_10_sel=8	UART2_RTS	UART2_RTS
						uart_sig_10_sel=9	UART2_CTS	UART2_CTS
						uart_sig_10_sel=10	UART2_TXD	UART2_TXD
						uart_sig_10_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	CAM_HSYNC	CAM_HSYNC
					10	-	-	-
					11	-	SWGPIO22	SWGPIO22
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	DBI_DB_6	DBI_DB_6
					23	-	DBI_SCL	DBI_SCL
					24	-	DPI_DATA[5]	DPI_DATA[5]
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS



表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
57	57	VDDIO_3	DI/DO	PAD_GPIO_23	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_11_sel=0	UART0_RTS	UART0_RTS
						uart_sig_11_sel=1	UART0_CTS	UART0_CTS
						uart_sig_11_sel=2	UART0_TXD	UART0_TXD
						uart_sig_11_sel=3	UART0_RXD	UART0_RXD
						uart_sig_11_sel=4	UART1_RTS	UART1_RTS
						uart_sig_11_sel=5	UART1_CTS	UART1_CTS
						uart_sig_11_sel=6	UART1_TXD	UART1_TXD
						uart_sig_11_sel=7	UART1_RXD	UART1_RXD
						uart_sig_11_sel=8	UART2_RTS	UART2_RTS
						uart_sig_11_sel=9	UART2_CTS	UART2_CTS
						uart_sig_11_sel=10	UART2_TXD	UART2_TXD
						uart_sig_11_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	CAM_VSYNC	CAM_VSYNC
					10	-	-	-
					11	-	SWGPIO23	SWGPIO23
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	DBI_DB_7	DBI_DB_7
					23	-	DBI_SDA	DBI_SDA
					24	-	DPI_DATA[6]	DPI_DATA[6]
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO
58	58	-	Power	VDDIO3	-	-	VDDIO3	GPIO16~23 and integrated LDO power input, 1.8V (connected to the third pin VDD18_OUT)/3.3V
59	59	-	Power	AVDD12	-	-	AVDD12	Integrated LDO output, on-chip pSRAM power supply, 1.2V, connected to decoupling capacitors
60	60	-	Power	AVDD12	-	-	AVDD12	Integrated LDO output, on-chip pSRAM power supply, 1.2V, connected to decoupling capacitors
61	61	AVDD12_INT (1.2V)	Analog	CSI_DN<1>	-	-	CSI_DN<1>	MIPI CSI data LANE1 differential input-
62	62	AVDD12_INT (1.2V)	Analog	CSI_DP<1>	-	-	CSI_DP<1>	MIPI CSI data LANE1 differential input+
63	63	AVDD12_INT (1.2V)	Analog	CSI_CLK_DN	-	-	CSI_CLK_DN	MIPI CSI clock LANE differential input-
64	64	AVDD12_INT (1.2V)	Analog	CSI_CLK_DP	-	-	CSI_CLK_DP	MIPI CSI clock LANE differential input+
65	65	AVDD12_INT (1.2V)	Analog	CSI_DN<0>	-	-	CSI_DN<0>	MIPI CSI data LANE0 differential input -
66	66	AVDD12_INT (1.2V)	Analog	CSI_DP<0>	-	-	CSI_DP<0>	MIPI CSI data LANE0 differential input+
-	67	AVDD12_INT (1.2V)	Analog	DSI_DN<0>	-	-	DSI_DN<0>	MIPI DSI data LANE0 differential output-

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	68	AVDD12_INT (1.2V)	Analog	DSI_DP<0>	-	-	DSI_DP<0>	MIPI DSI data LANE0 differential output+
-	69	AVDD12_INT (1.2V)	Analog	DSI_DN<1>	-	-	DSI_DN<1>	MIPI DSI data LANE1 differential output-
-	70	AVDD12_INT (1.2V)	Analog	DSI_DP<1>	-	-	DSI_DP<1>	MIPI DSI data LANE1 differential output+
-	71	AVDD12_INT (1.2V)	Analog	DSI_CLK_DN	-	-	DSI_CLK_DN	MIPI DSI clock LANE differential output-
-	72	AVDD12_INT (1.2V)	Analog	DSI_CLK_DP	-	-	DSI_CLK_DP	MIPI DSI clock LANE differential output+
-	73	AVDD12_INT (1.2V)	Analog	DSI_DN<2>	-	-	DSI_DN<2>	MIPI DSI data LANE2 differential output-
-	74	AVDD12_INT (1.2V)	Analog	DSI_DP<2>	-	-	DSI_DP<2>	MIPI DSI data LANE2 differential output+
-	75	AVDD12_INT (1.2V)	Analog	DSI_DN<3>	-	-	DSI_DN<3>	MIPI DSI data LANE3 differential output-
-	76	AVDD12_INT (1.2V)	Analog	DSI_DP<3>	-	-	DSI_DP<3>	MIPI DSI data LANE2 differential output+
67	-	VDDIO_4	DI/DO	PAD_GPIO_24	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
						uart_sig_0_sel=4	UART1_RTS	UART1_RTS
						uart_sig_0_sel=5	UART1_CTS	UART1_CTS
						uart_sig_0_sel=6	UART1_TXD	UART1_TXD
						uart_sig_0_sel=7	UART1_RXD	UART1_RXD
						uart_sig_0_sel=8	UART2_RTS	UART2_RTS
						uart_sig_0_sel=9	UART2_CTS	UART2_CTS
						uart_sig_0_sel=10	UART2_TXD	UART2_TXD
						uart_sig_0_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_REF_CLK	RMII_REF_CLK
					9	-	DVP_CLK	DVP_CLK
					10	-	-	-
					11	-	SWGPIIO24	SWGPIIO24
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CS <sub>n</sub>	DBI_CS <sub>n</sub>
					24	-	DPI_DATA[7]	DPI_DATA[7]
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
68	-	VDDIO_4	DI/DO	PAD_GPIO_25	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
						uart_sig_1_sel=4	UART1_RTS	UART1_RTS
						uart_sig_1_sel=5	UART1_CTS	UART1_CTS
						uart_sig_1_sel=6	UART1_TXD	UART1_TXD
						uart_sig_1_sel=7	UART1_RXD	UART1_RXD
						uart_sig_1_sel=8	UART2_RTS	UART2_RTS
						uart_sig_1_sel=9	UART2_CTS	UART2_CTS
						uart_sig_1_sel=10	UART2_TXD	UART2_TXD
						uart_sig_1_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_TXD[0]	RMII_TXD[0]
					9	-	PIX_DAT0	PIX_DAT0
					10	-	-	-
					11	-	SWGPIO25	SWGPIO25
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	DPI_DATA[8]	DPI_DATA[8]
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
69	-	VDDIO_4	DI/DO	PAD_GPIO_26	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
						uart_sig_2_sel=4	UART1_RTS	UART1_RTS
						uart_sig_2_sel=5	UART1_CTS	UART1_CTS
						uart_sig_2_sel=6	UART1_TXD	UART1_TXD
						uart_sig_2_sel=7	UART1_RXD	UART1_RXD
						uart_sig_2_sel=8	UART2_RTS	UART2_RTS
						uart_sig_2_sel=9	UART2_CTS	UART2_CTS
						uart_sig_2_sel=10	UART2_TXD	UART2_TXD
						uart_sig_2_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_TXD[1]	RMII_TXD[1]
					9	-	PIX_DAT1	PIX_DAT1
					10	-	-	-
					11	-	SWGPI026	SWGPI026
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	DPI_DATA[9]	DPI_DATA[9]
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
70	-	VDDIO_4	DI/DO	PAD_GPIO_27	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
						uart_sig_3_sel=4	UART1_RTS	UART1_RTS
						uart_sig_3_sel=5	UART1_CTS	UART1_CTS
						uart_sig_3_sel=6	UART1_TXD	UART1_TXD
						uart_sig_3_sel=7	UART1_RXD	UART1_RXD
						uart_sig_3_sel=8	UART2_RTS	UART2_RTS
						uart_sig_3_sel=9	UART2_CTS	UART2_CTS
						uart_sig_3_sel=10	UART2_TXD	UART2_TXD
						uart_sig_3_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_RXD[0]	RMII_RXD[0]
					9	-	PIX_DAT2	PIX_DAT2
					10	-	-	-
					11	-	SWGPIO27	SWGPIO27
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	DPI_DATA[10]	DPI_DATA[10]
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
71	-	VDDIO_4	DI/DO	PAD_GPIO_28	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_4_sel=0	UART0_RTS	UART0_RTS
						uart_sig_4_sel=1	UART0_CTS	UART0_CTS
						uart_sig_4_sel=2	UART0_TXD	UART0_TXD
						uart_sig_4_sel=3	UART0_RXD	UART0_RXD
						uart_sig_4_sel=4	UART1_RTS	UART1_RTS
						uart_sig_4_sel=5	UART1_CTS	UART1_CTS
						uart_sig_4_sel=6	UART1_TXD	UART1_TXD
						uart_sig_4_sel=7	UART1_RXD	UART1_RXD
						uart_sig_4_sel=8	UART2_RTS	UART2_RTS
						uart_sig_4_sel=9	UART2_CTS	UART2_CTS
						uart_sig_4_sel=10	UART2_TXD	UART2_TXD
						uart_sig_4_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_RXD[1]	RMII_RXD[1]
					9	-	PIX_DAT3	PIX_DAT3
					10	-	-	-
					11	-	SWGPIO28	SWGPIO28
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CS <sub>n</sub>	DBI_CS <sub>n</sub>
					24	-	DPI_DATA[11]	DPI_DATA[11]
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
72	-	VDDIO_4	DI/DO	PAD_GPIO_29	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_5_sel=0	UART0_RTS	UART0_RTS
						uart_sig_5_sel=1	UART0_CTS	UART0_CTS
						uart_sig_5_sel=2	UART0_TXD	UART0_TXD
						uart_sig_5_sel=3	UART0_RXD	UART0_RXD
						uart_sig_5_sel=4	UART1_RTS	UART1_RTS
						uart_sig_5_sel=5	UART1_CTS	UART1_CTS
						uart_sig_5_sel=6	UART1_TXD	UART1_TXD
						uart_sig_5_sel=7	UART1_RXD	UART1_RXD
						uart_sig_5_sel=8	UART2_RTS	UART2_RTS
						uart_sig_5_sel=9	UART2_CTS	UART2_CTS
						uart_sig_5_sel=10	UART2_TXD	UART2_TXD
						uart_sig_5_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_RXERR	RMII_RXERR
					9	-	PIX_DAT4	PIX_DAT4
					10	-	-	-
					11	-	SWGPI029	SWGPI029
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	DPI_DATA[12]	DPI_DATA[12]
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

**表 3.1: 管脚定义 (continued)**

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
73	-	VDDIO_4	DI/DO	PAD_GPIO_30	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_6_sel=0	UART0_RTS	UART0_RTS
						uart_sig_6_sel=1	UART0_CTS	UART0_CTS
						uart_sig_6_sel=2	UART0_TXD	UART0_TXD
						uart_sig_6_sel=3	UART0_RXD	UART0_RXD
						uart_sig_6_sel=4	UART1_RTS	UART1_RTS
						uart_sig_6_sel=5	UART1_CTS	UART1_CTS
						uart_sig_6_sel=6	UART1_TXD	UART1_TXD
						uart_sig_6_sel=7	UART1_RXD	UART1_RXD
						uart_sig_6_sel=8	UART2_RTS	UART2_RTS
						uart_sig_6_sel=9	UART2_CTS	UART2_CTS
						uart_sig_6_sel=10	UART2_TXD	UART2_TXD
						uart_sig_6_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_TX_EN	RMII_TX_EN
					9	-	PIX_DAT5	PIX_DAT5
					10	-	-	-
					11	-	SWGPI030	SWGPI030
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	DPI_DATA[13]	DPI_DATA[13]
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS



表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
74	-	VDDIO_4	DI/DO	PAD_GPIO_31	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_7_sel=0	UART0_RTS	UART0_RTS
						uart_sig_7_sel=1	UART0_CTS	UART0_CTS
						uart_sig_7_sel=2	UART0_TXD	UART0_TXD
						uart_sig_7_sel=3	UART0_RXD	UART0_RXD
						uart_sig_7_sel=4	UART1_RTS	UART1_RTS
						uart_sig_7_sel=5	UART1_CTS	UART1_CTS
						uart_sig_7_sel=6	UART1_TXD	UART1_TXD
						uart_sig_7_sel=7	UART1_RXD	UART1_RXD
						uart_sig_7_sel=8	UART2_RTS	UART2_RTS
						uart_sig_7_sel=9	UART2_CTS	UART2_CTS
						uart_sig_7_sel=10	UART2_TXD	UART2_TXD
						uart_sig_7_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_RX_DV	RMII_RX_DV
					9	-	PIX_DAT6	PIX_DAT6
					10	-	-	-
					11	-	SWGPIO31	SWGPIO31
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	DPI_DATA[14]	DPI_DATA[14]
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
75	-	VDDIO_4	DI/DO	PAD_GPIO_32	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_8_sel=0	UART0_RTS	UART0_RTS
						uart_sig_8_sel=1	UART0_CTS	UART0_CTS
						uart_sig_8_sel=2	UART0_TXD	UART0_TXD
						uart_sig_8_sel=3	UART0_RXD	UART0_RXD
						uart_sig_8_sel=4	UART1_RTS	UART1_RTS
						uart_sig_8_sel=5	UART1_CTS	UART1_CTS
						uart_sig_8_sel=6	UART1_TXD	UART1_TXD
						uart_sig_8_sel=7	UART1_RXD	UART1_RXD
						uart_sig_8_sel=8	UART2_RTS	UART2_RTS
						uart_sig_8_sel=9	UART2_CTS	UART2_CTS
						uart_sig_8_sel=10	UART2_TXD	UART2_TXD
						uart_sig_8_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_MDC	RMII_MDC
					9	-	PIX_DAT7	PIX_DAT7
					10	-	-	-
					11	-	SWGPI032	SWGPI032
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CS <sub>n</sub>	DBI_CS <sub>n</sub>
					24	-	DPI_DATA[15]	DPI_DATA[15]
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
76	-	VDDIO_4	DI/DO	PAD_GPIO_33	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_9_sel=0	UART0_RTS	UART0_RTS
						uart_sig_9_sel=1	UART0_CTS	UART0_CTS
						uart_sig_9_sel=2	UART0_TXD	UART0_TXD
						uart_sig_9_sel=3	UART0_RXD	UART0_RXD
						uart_sig_9_sel=4	UART1_RTS	UART1_RTS
						uart_sig_9_sel=5	UART1_CTS	UART1_CTS
						uart_sig_9_sel=6	UART1_TXD	UART1_TXD
						uart_sig_9_sel=7	UART1_RXD	UART1_RXD
						uart_sig_9_sel=8	UART2_RTS	UART2_RTS
						uart_sig_9_sel=9	UART2_CTS	UART2_CTS
						uart_sig_9_sel=10	UART2_TXD	UART2_TXD
						uart_sig_9_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_MDIO	RMII_MDIO
					9	-	-	-
					10	-	-	-
					11	-	SWGPI033	SWGPI033
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	DPI_DE	DPI_DE
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI
77	77	-	Power	VDDIO4	-	-	VDDIO4	VDDIO4
78	78	-	Power	VDD18_FLASH	-	-	VDD18_FLASH	VDD18_FLASH

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
79	79	VDDIO_4	DI/DO	PAD_GPIO_34	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	SF2_CLK	SF2_CLK
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_10_sel=0	UART0_RTS	UART0_RTS
						uart_sig_10_sel=1	UART0_CTS	UART0_CTS
						uart_sig_10_sel=2	UART0_TXD	UART0_TXD
						uart_sig_10_sel=3	UART0_RXD	UART0_RXD
						uart_sig_10_sel=4	UART1_RTS	UART1_RTS
						uart_sig_10_sel=5	UART1_CTS	UART1_CTS
						uart_sig_10_sel=6	UART1_TXD	UART1_TXD
						uart_sig_10_sel=7	UART1_RXD	UART1_RXD
						uart_sig_10_sel=8	UART2_RTS	UART2_RTS
						uart_sig_10_sel=9	UART2_CTS	UART2_CTS
						uart_sig_10_sel=10	UART2_TXD	UART2_TXD
						uart_sig_10_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_RXERR	RMII_RXERR
					9	-	-	-
					10	-	ADC_CH11	ADC_CH11
					11	-	SWGPIO34	SWGPIO34
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
80	80	VDDIO_4	DI/DO	PAD_GPIO_35	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	SF2_CS	SF2_CS
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_11_sel=0	UART0_RTS	UART0_RTS
						uart_sig_11_sel=1	UART0_CTS	UART0_CTS
						uart_sig_11_sel=2	UART0_TXD	UART0_TXD
						uart_sig_11_sel=3	UART0_RXD	UART0_RXD
						uart_sig_11_sel=4	UART1_RTS	UART1_RTS
						uart_sig_11_sel=5	UART1_CTS	UART1_CTS
						uart_sig_11_sel=6	UART1_TXD	UART1_TXD
						uart_sig_11_sel=7	UART1_RXD	UART1_RXD
						uart_sig_11_sel=8	UART2_RTS	UART2_RTS
						uart_sig_11_sel=9	UART2_CTS	UART2_CTS
						uart_sig_11_sel=10	UART2_TXD	UART2_TXD
						uart_sig_11_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_TX_EN	RMII_TX_EN
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO35	SWGPIO35
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
81	81	VDDIO_4	DI/DO	PAD_GPIO_36	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	SF2_D0	SF2_D0
					3	-	I2S_BCLK	I2S_BCLK
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
						uart_sig_0_sel=4	UART1_RTS	UART1_RTS
						uart_sig_0_sel=5	UART1_CTS	UART1_CTS
						uart_sig_0_sel=6	UART1_TXD	UART1_TXD
						uart_sig_0_sel=7	UART1_RXD	UART1_RXD
						uart_sig_0_sel=8	UART2_RTS	UART2_RTS
						uart_sig_0_sel=9	UART2_CTS	UART2_CTS
						uart_sig_0_sel=10	UART2_TXD	UART2_TXD
						uart_sig_0_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_RX_DV	RMII_RX_DV
					9	-	-	-
					10	-	-	-
					11	-	SWGPI036	SWGPI036
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CS <sub>n</sub>	DBI_CS <sub>n</sub>
					24	-	-	-
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
82	82	VDDIO_4	DI/DO	PAD_GPIO_37	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	SF2_D1	SF2_D1
					3	-	I2S_FS	I2S_FS
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
						uart_sig_1_sel=4	UART1_RTS	UART1_RTS
						uart_sig_1_sel=5	UART1_CTS	UART1_CTS
						uart_sig_1_sel=6	UART1_TXD	UART1_TXD
						uart_sig_1_sel=7	UART1_RXD	UART1_RXD
						uart_sig_1_sel=8	UART2_RTS	UART2_RTS
						uart_sig_1_sel=9	UART2_CTS	UART2_CTS
						uart_sig_1_sel=10	UART2_TXD	UART2_TXD
						uart_sig_1_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_MDC	RMII_MDC
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO37	SWGPIO37
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

**表 3.1: 管脚定义 (continued)**

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
83	83	VDDIO_4	DI/DO	PAD_GPIO_38	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	SF2_D2	SF2_D2
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
						uart_sig_2_sel=4	UART1_RTS	UART1_RTS
						uart_sig_2_sel=5	UART1_CTS	UART1_CTS
						uart_sig_2_sel=6	UART1_TXD	UART1_TXD
						uart_sig_2_sel=7	UART1_RXD	UART1_RXD
						uart_sig_2_sel=8	UART2_RTS	UART2_RTS
						uart_sig_2_sel=9	UART2_CTS	UART2_CTS
						uart_sig_2_sel=10	UART2_TXD	UART2_TXD
						uart_sig_2_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_MDIO	RMII_MDIO
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO38	SWGPIO38
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS



表 3.1: 管脚定义 (continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
84	84	VDDIO_4	DI/DO	PAD_GPIO_39	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	SF2_D3	SF2_D3
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
						uart_sig_3_sel=4	UART1_RTS	UART1_RTS
						uart_sig_3_sel=5	UART1_CTS	UART1_CTS
						uart_sig_3_sel=6	UART1_TXD	UART1_TXD
						uart_sig_3_sel=7	UART1_RXD	UART1_RXD
						uart_sig_3_sel=8	UART2_RTS	UART2_RTS
						uart_sig_3_sel=9	UART2_CTS	UART2_CTS
						uart_sig_3_sel=10	UART2_TXD	UART2_TXD
						uart_sig_3_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO39	SWGPIO39
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO
85	85	-	Power	DCDC11_VOUT	-	-	DCDC11_VOUT	Feedback voltage input, 1.1V
86	86	-	Power	SW_DCDC11	-	-	SW_DCDC11	DCDC switch output, connected to power inductor
87	87	-	Power	VDD33_DCDC11	-	-	VDD33_DCDC11	DCDC power input, 3.3V
88	88	-	Power	VSS_DCDC11	-	-	VSS_DCDC11	DCDC circuit ground pin

<sup>1</sup> 该功能默认为 SPI\_MOSI，可通过寄存器将该功能转换为 SPI\_MISO。

## 射频特性

射频接收和传输模式的特性，如下表所示：

表 4.1: WLAN TX 射频特性

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
发射功率	11b - 1Mbps			21		dBm
	11b - 11Mbps			21		
	11g - 6Mbps			19		
	11g - 54Mbps			18		
	11n - MCS0			19		
	11n - MCS7			17		

表 4.2: WLAN RX 射频特性

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
RX 灵敏度	11b - 1Mbps			-98		dBm
	11b - 11Mbps			-90		
	11g - 6Mbps			-93		
	11g - 54Mbps			-77		
	11n - MCS0			-93		
	11n - MCS7			-74		

表 4.3: BLE RX 射频特性

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
RX 灵敏度	1Mbps			-99		dBm
	2Mbps			-97		
	S8 (125Kbps)			-105		
	S2 (500Kbps)			-102		

表 4.4: BLE TX 射频特性

模式	备注	Performance @3.3V,25°C			
		最小值	典型值	最大值	单位
TX 发射功率			10	20	dBm

表 4.5: BT TX 射频特性

模式	备注	Performance @3.3V,25°C			
		最小值	典型值	最大值	单位
BR 输出功率			10		dBm
EDR 输出功率			8		dBm
$\Delta f_{1avg}$	BR 1Mbps		159		kHz
$\Delta f_{2max}$			132		
$\Delta f_{2avg}/\Delta f_{1avg}$			0.88		
$\omega_0$	EDR 2Mbps	-3		3	kHz
$\omega_i$		-12		6	
$\omega_i + \omega_0$		-6		3	
RMS DEVM				5	%
99% DEVM				9	
Peak DEVM				10	
$\omega_0$	EDR 3Mbps	-3		3	kHz
$\omega_i$		-12		6	
$\omega_i + \omega_0$		-6		3	
RMS DEVM				5	%
99% DEVM				9	
Peak DEVM				10	

表 4.6: BT RX 射频特性

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
灵敏度	BR 1Mbps	Dirty Off		-94		dBm
最大接收电平						
灵敏度	EDR 2Mbps			-95		
最大接收电平						
灵敏度	EDR 3Mbps			-89		
最大接收电平						

## 5.1 电气特性

表 5.1: 模数转换器电气特性

At 25°C, AVDD25_CODEC= 2.5 V, f <sub>S</sub> = 48kHz, 20-bit audio data (unless otherwise noted)						
参数		测试条件	最小值	典型值	最大值	单位
AUDIO ADC	Input signal full-scale level	Differential input, 0 dB PGA gain		1.8		Vrms
		Single-ended input, 0 dB PGA gain		0.9	1.4	
	Input common-mode voltage	differential/Single-ended input		1.23		
SNR	Signal-to-noise ratio, A-weighted	f <sub>S</sub> = 48 kHz, 0 dB PGA gain, 1kHz full-scale sine-wave input		103		dB
DR	Dynamic range, A-weighted	f <sub>S</sub> = 48 kHz, 0 dB PGA gain, 1kHz -60dB sine-wave input		103		
THD	Total harmonic distortion	f <sub>S</sub> = 48 kHz, 0 dB PGA gain, 1kHz -5dB sine-wave input		-95		
PSRR	Power supply rejection ratio	234 Hz, 100 mVPP on AVDD, single-ended input		-		
		234 Hz, 100 mVPP on AVDD, differential input		-		
Crosstalk	ADC channel separation	0 dB PGA gain, 1kHz full-scale sine-wave input	130			
		36dB PGA gain, 1kHz full-scale sine-wave input	100			
Freq. Response		-5dB 20Hz~24kHz sine-wave input		0.25		
ADC programmable analogue amplifier gain range		Analogue gain resolution = 3dB	0		42	
ADC programmable digital gain range		Digital gain resolution = 0.5dB	-95.5		31.5	

表 5.1: 模数转换器电气特性 (continued)

At 25°C, AVDD25_CODEC= 2.5 V, $f_s$ = 48kHz, 20-bit audio data (unless otherwise noted)					
参数	测试条件	最小值	典型值	最大值	单位
Input resistance	Analogue gain 0dB		16		k $\Omega$
	Analogue gain 6dB~42dB	160		640	
Input capacitance			10		pF
MICROPHONE BIAS	Bias voltage	Programmable settings	1.8	2.5	V
	Current sourcing	2.5V setting, load = 1 K $\Omega$		2.2	mA
	Integrated noise	BW = 20 Hz to 20 kHz, A-weighted, 1 $\mu$ F capacitor between MICBIAS and AGND		1.5	$\mu$ V rms

表 5.2: 数模转换器电气特性

At 25°C, AVDD25_CODEC= 2.5 V, f <sub>S</sub> = 48kHz, 20-bit audio data (unless otherwise noted)						
参数		测试条件	最小值	典型值	最大值	单位
AUDIO DAC	Input signal full-scale level	Differential output, 0 dB line-out gain		1.68		Vrms
		Single-ended output, 0 dB line-out gain		0.84		
	Input common-mode voltage			1.23		
SNR	Signal-to-noise ratio, A-W without Noise Gating	f <sub>S</sub> = 48 kHz, 1kHz full-scale sine-wave output		104		dB
	Signal-to-noise ratio, A-W with Noise Gating	f <sub>S</sub> = 48 kHz, 1kHz full-scale sine-wave output		112		
DR	Dynamic range, A-weighted	f <sub>S</sub> = 48 kHz, 1kHz -60dB sine-wave output		104		
THD	Total harmonic distortion	f <sub>S</sub> = 48 kHz, 1kHz -5dB sine-wave output		-89		
PSRR	Power supply rejection ratio	234 Hz, 100 mVPP on AVDD, single-ended output		-		
		234 Hz, 100 mVPP on AVDD, differential output		-		
Noise Floor		A-weighted without Noise Gating		10		μV rms
Noise Floor		A-weighted with Noise Gating		4.3		
Crosstalk	DAC channel separation	1kHz full-scale sine-wave output	130			dB
Freq. Response		-5dB 20Hz~24kHz sine-wave input		0.25		
DC offset		P/N output DC offset		0.5		mV

表 5.2: 数模转换器电气特性 (continued)

At 25°C, AVDD25_CODEC= 2.5 V, f <sub>S</sub> = 48kHz, 20-bit audio data (unless otherwise noted)					
参数	测试条件	最小值	典型值	最大值	单位
DAC programmable analogue amplifier gain range	Analogue gain resolution = 3dB	-21		0	dB
DAC programmable digital gain range	Digital gain resolution = 0.5dB	-95.5		31.5	

每个电源模式的功耗，如下表所示：

表 6.1: 电源模式 & 整个芯片的电流

模式		备注	Performance @25°C			
			最小值	典型值	最大值	单位
RX		3.3V, RF only		13		mA
TX	11b - 11Mbps @21dBm	3.3V, RF only Duty 99%		295		
HBN	HBN0	Vdd11_aon = 0.9V		7.9		uA
		Vdd11_aon = 1.1V		14.3		
PDS	PDS7	Vdd11_aon = 0.9V		70.8		
		Vdd11_aon = 1.1V		121.7		
Shut-down				<0.5		



## 7.1 绝对最大额定值

表 7.1: 电源的绝对最大额定值

管脚名称	最小值	最大值	单位
VDD33_DCDC18, VDD33_DCDC11	-0.3	3.63	V
VDD33(USB)	-0.3	3.63	V
VDDIO1	-0.3	3.63	V
VDDIO2	-0.3	3.63	V
VDDIO3	-0.3	3.63	V
VDDIO4	-0.3	3.63	V
VDD33_RF	-0.3	3.63	V
AVDD33_CODEC	-0.3	3.63	V

## 7.2 运行条件

### 7.2.1 电源特性

表 7.2: 建议电源值范围

管脚名称	最小值	典型值	最大值	单位
VDD33_DCDC18, VDD33_DCDC11	3	3.3	3.63	V
VDD33(USB)	3	3.3	3.63	V
VDDIO1	3.0/1.62	3.3/1.8	3.63/1.98	V
VDDIO2	3	3.3	3.63	V

表 7.2: 建议电源值范围 (continued)

管脚名称	最小值	典型值	最大值	单位
VDDIO3	3.0/1.62	3.3/1.8	3.63/1.98	V
VDDIO4	3.0/1.62	3.3/1.8	3.63/1.98	V
VDD33_RF	3	3.3	3.63	V
AVDD33_CODEC	3	3.3	3.63	V

## 7.2.2 IO 直流特性

表 7.3: IO 直流特性

符号	描述	条件	最小值	典型值	最大值	单位
VOH	Output voltage high		$0.8 * V_{IO}$			V
VOL	Output voltage low				$0.1 * V_{IO}$	V
VIH	Input voltage high		$0.7 * V_{IO}$		$V_{IO} + 0.3$	V
VIL	Input voltage low		-0.3		$0.3 * V_{IO}$	V

## 7.2.3 上电时序

为确保正常的上电启动，电源、复位、Bootstrap 引脚需要满足相应的时序要求。

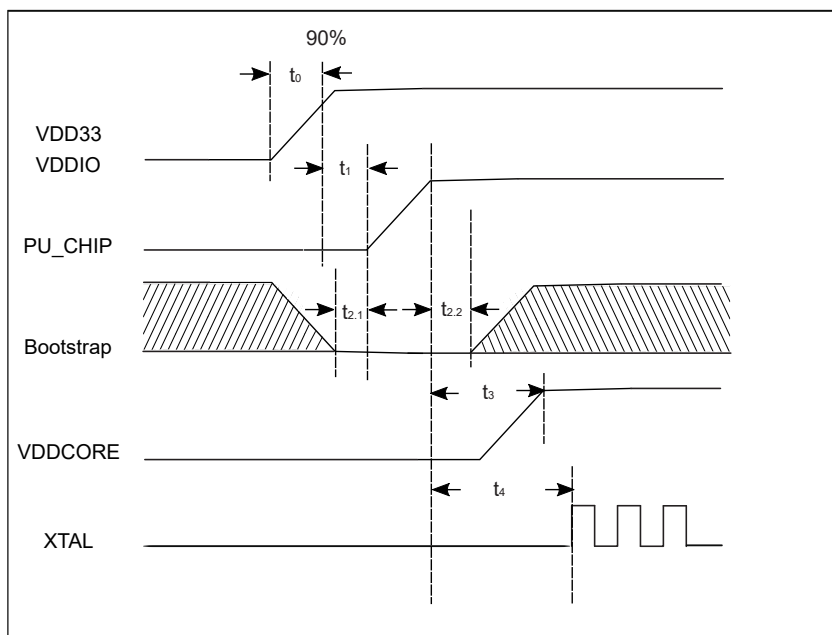


图 7.1: 上电时序

表 7.4: 上电时序参数说明

参数	说明	最小值 (ms)	典型值 (ms)	最大值 (ms)
$t_0$	电源电压到达 90% 的上升时间			2
$t_1$	电源上升完成到 PU_CHIP 拉高前延时	0.1		
$t_{2.1}$	Bootstrap 引脚 <sup>1</sup> 电平在 PU_CHIP 拉高前的建立时间	0		
$t_{2.2}$	Bootstrap 引脚电平在 PU_CHIP 拉高后的保持时间	2		
$t_3$	PU_CHIP 拉高到 VDDCORE 输出		2	
$t_4$	PU_CHIP 拉高到 XTAL 起振		2	

<sup>1</sup> Bootstrap 引脚是 GPIO39。

## 7.2.4 温度特性

表 7.5: 建议温度值范围

项目		最小值	最大值	单位
温度	主芯片	-40	85	°C
	合封多芯片	-40	85	

## 7.2.5 通用工作条件

表 7.6: 一般操作条件

项目	描述	最小值	典型值	最大值	单位
FCPU	CPU 时钟频率 (M0)			320	MHz
	CPU 时钟频率 (D0)			480	

## 8.1 湿敏等级 (MSL)

芯片的湿敏等级为：MSL3。真空包装打开后，在  $\leq 30^{\circ}\text{C}/60\%\text{RH}$  下，需要在 168 小时（7 天）内使用完毕，否则需要烘烤后上线。烘烤温度和时间可参考 IPC/JEDECJ-STD-033B01。

表 8.1: Reference Conditions for Drying Mounted or Unmounted SMD Packages (User Bake: Floor life begins counting at time = 0 after bake)

Package Body	Level	Bake @ $125^{\circ}\text{C}$		Bake @ $90^{\circ}\text{C}$ $\leq 5\%\text{ RH}$		Bake @ $40^{\circ}\text{C}$ $\leq 5\%\text{ RH}$	
		Exceeding Floor Life by $>72\text{ h}$	Exceeding Floor Life by $\leq 72\text{ h}$	Exceeding Floor Life by $>72\text{ h}$	Exceeding Floor Life by $\leq 72\text{ h}$	Exceeding Floor Life by $>72\text{ h}$	Exceeding Floor Life by $\leq 72\text{ h}$
Thickness $\leq 1.4\text{ mm}$	2	5 hours	3 hours	17 hours	11 hours	8 days	5 days
	2a	7 hours	5 hours	23 hours	13 hours	9 days	7 days
	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days
	4	11 hours	7 hours	37 hours	23 hours	15 days	9 days
	5	12 hours	7 hours	41 hours	24 hours	17 days	10 days
	5a	16 hours	10 hours	54 hours	24 hours	22 days	10 days

## 8.2 静电放电 (ESD)

- 人体放电模式 (HBM): 2000V
- 组件充电模式 (CDM): 500V

## 8.3 回流焊接曲线 (Reflow Profile)

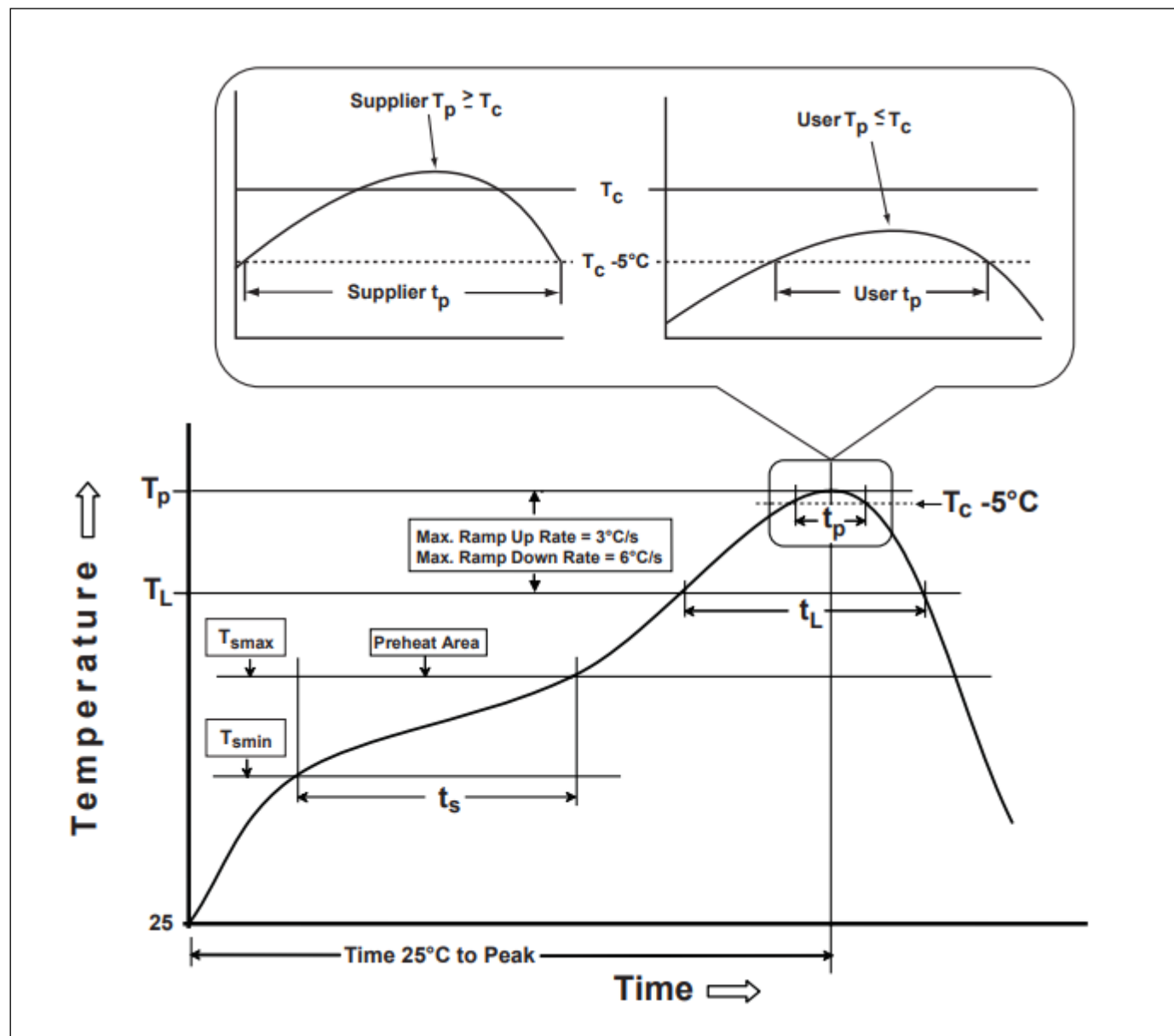


图 8.1: Classification Profile (Not to scale)

表 8.2: Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min ( $T_{smin}$ ) Temperature Max ( $T_{smax}$ ) Time ( $t_s$ ) from ( $T_{smin}$ to $T_{smax}$ )	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Ramp-up rate ( $T_L$ to $T_p$ )	3 °C/second max.	3 °C/second max.
Liquidous temperature ( $T_L$ ) Time ( $t_L$ ) maintained above $T_L$	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature ( $T_p$ )	240 °C+0/-5 °C	250 °C+0/-5 °C
Time ( $t_p$ )* within 5 °C of the specified classification temperature ( $T_c$ )	10-30 seconds	20-40 seconds
Ramp-down rate ( $T_p$ to $T_L$ )	6 °C/second max	6 °C/second max
Time 25 °C to peak temperature	6 minutes max	8 minutes max
- Tolerance for peak profile temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.		

具体可参考 IPC/JEDEC J-STD-020E。



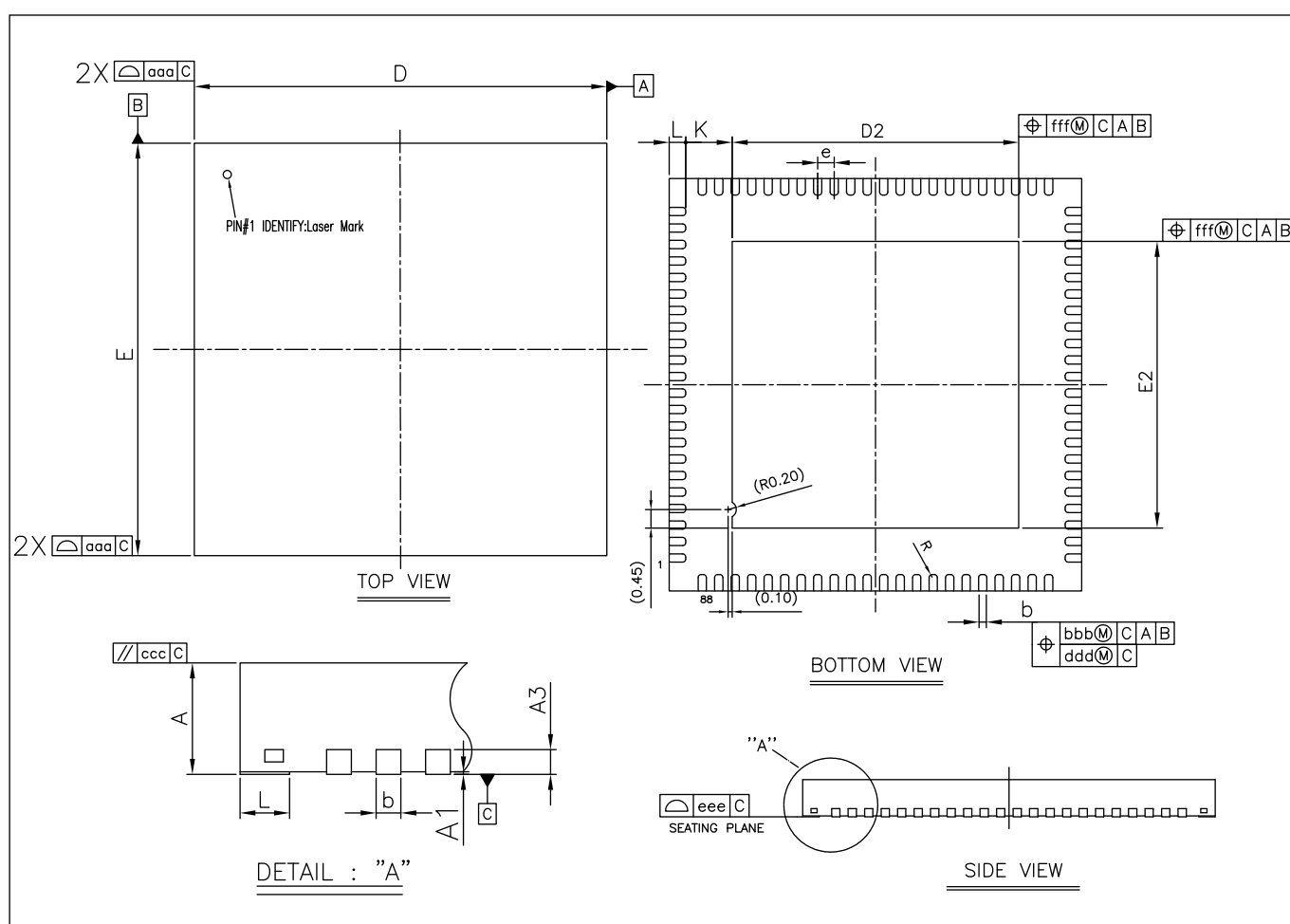


图 10.1: QFN88 封装图



表 10.1: QFN88 尺寸说明

标号	测量单位：毫米			测量单位：英寸		
	最小值	典型值	最大值	最小值	典型值	最大值
A	0.85	0.90	0.95	0.033	0.035	0.037
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D2	6.85	6.95/6.40	7.05	0.270	0.274	0.278
E2	6.85	6.95/6.40	7.05	0.270	0.274	0.278
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	-	-	0.008	-	-
R	0.075	-	0.125	0.003	-	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

注解：控制尺寸：毫米

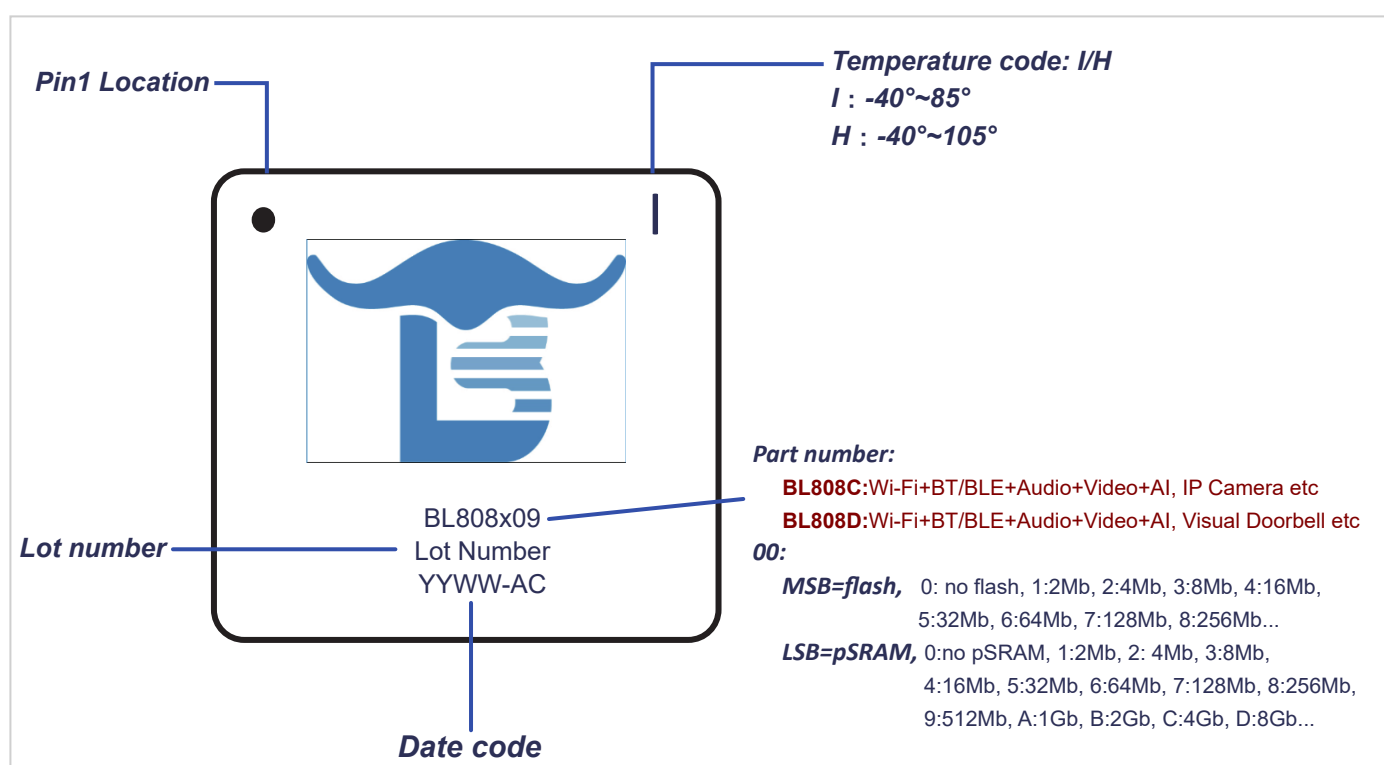


图 11.1: 标志定义

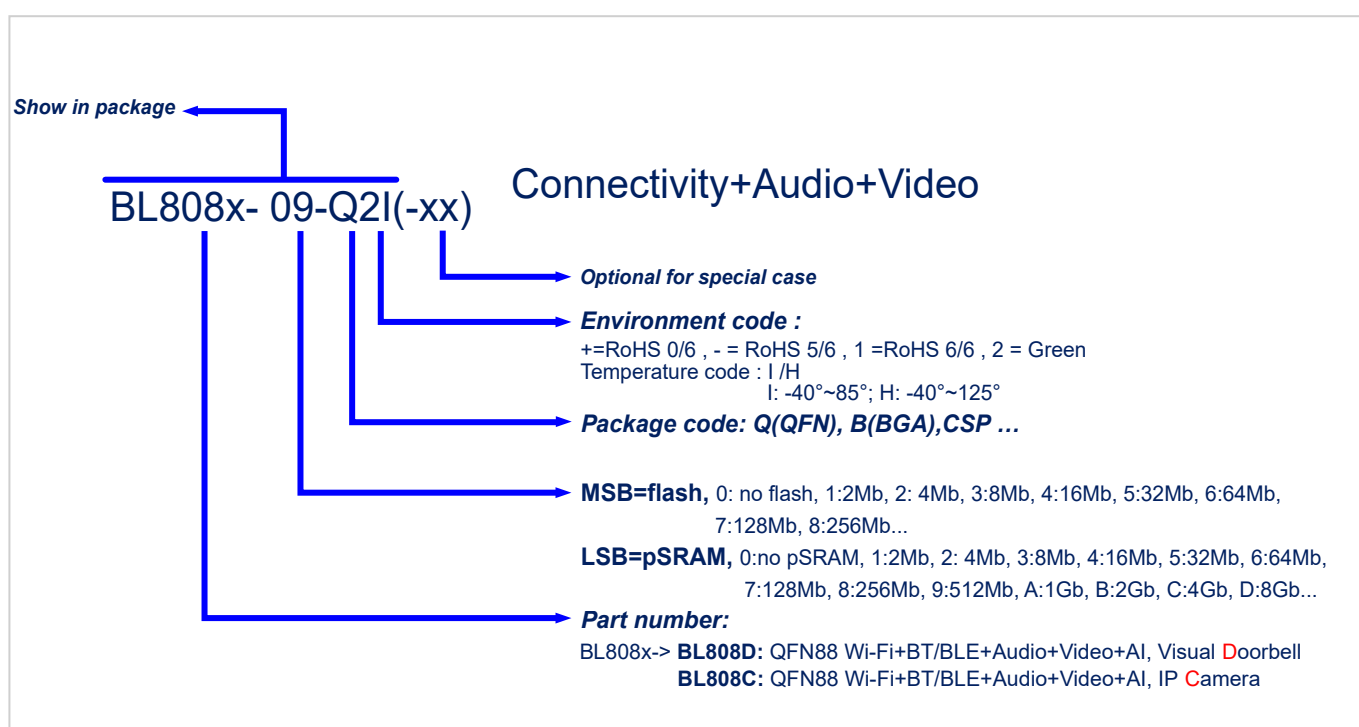


图 12.1: 型号命名

表 12.1: 订购选项

产品编号	描述
BL808D-09-Q2I	Wi-Fi + BT/BLE + Audio + Video + AI, QFN88, no flash, 512Mb pSRAM, 可视对讲门铃 (Doorbell) 等
BL808C-09-Q2I	Wi-Fi + BT/BLE + Audio + Video + AI, QFN88, no flash, 512Mb pSRAM, IPC 等

表 13.1: 修改记录

日期	版本	修改内容
2021/12/17	0.9	初版
2022/1/14	0.95	增加音频特性和射频特性数据
2022/2/10	0.96	增加 BLE 射频特性和电气特性相关数据
2022/3/3	0.97	增加 BT 射频特性数据和 Bootstrap 引脚说明
2022/3/17	0.98	增加功耗数据
2022/5/12	0.99	修改内存地址映射描述, 增加 EMAC 时序说明
2022/6/9	1.0	增加 pinmux function 26 和 27 的说明
2022/8/17	1.1	增加 spi 和 uart function 描述, 型号命名中增加具体温度描述