BL808

Datasheet

Version: 1.1

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Features

- Wireless (Tier-1 RF Performance)
  - 2.4 GHz RF transceiver
  - Wi-Fi 802.11 b/g/n
  - Bluetooth® 5.x Dual-mode (BT+BLE)
  - Zigbee / IEEE 802.15.4
  - Wi-Fi/Bluetooth/Zigbee Coexistence
  - Integrated balun, PA/LNA
  - Support External PA/LNA
- Microcontroller
  - Multi-Core RISC-V CPUs (Max Freq 480MHz)
  - RTC timer up to one year
  - General purpose timers
  - DMA channels
  - JTAG development support
  - XIP QSPI flash support
- Audio Codec
  - ADC*2 (Mic*2 or Mic*1+Line-in)
  - DAC*1 (Speaker)
  - Sample Rate 8~192KHz, 24bit
- Video/Image/Display
  - MJPEG , H264 (Baseline/Main)
  - Maximum resolution:2M(1920x1080)
  - Video encoding format:
    - MJPEG and H264 (Baseline/Main)
    - 1920x1080 @ 30fps + 640x480 @ 30fps
    - Up to 8-ROI(region-of-interest)
  - Camera Sensor interface: DVP and MIPI-CSI
  - Display interface: SPI、DBI、DPI(RGB)、MIPI-DSI
- AI NN general HW Accelerator
  - NPU BLAI-100 (Bouffalo Lab AI engine) For Video/Audio detection/recognition, etc.
- Memory
  - Embedded 32/64MB DRAM
  - Support max 128MB SPI-Nor Flash
  - Support max 256MB SPI-NAND Flash
- Security
  - Secure boot ; Secure debug
  - XIP QSPI On-The-Fly AES Decryption (OTFAD)
  - Support sensitive SW isolation (TrustZone)
  - AES-CBC/CCM/GCM/XTS modes
  - MD5, SHA-1/224/256/384/512
  - TRNG (True Random Number Generator)
  - PKA (Public Key Accelerator) for RSA/ECC
- Peripherals
  - USB 2.0 HS OTG
  - Ethernet RMII Interface
  - SD-card interface
  - Four UART interface
  - Two SPI interface
  - Four I2C interface
  - Eight PWM channels
  - I2S interface
  - PDM interface

  - General-Purpose ADC
  - General-Purpose DAC
  - General analog comparators (ACOMP)
  - PIR (Passive Infra-Red) detection
  - IR remote HW accelerator
  - Support 12-Channel Touch
  - Flexible 36 or 40 GPIOs
- Power Modes (Ultra-low Power modes)
  - Off(~1uA) ; Hibernate
  - Power Down Sleep (flexible)
- Clock
  - Support XTAL 24/26/32/38.4/40 MHz
  - Support XTAL 32/32.768 KHz
  - Internal RC 32KHz/32MHz oscillator
  - Internal System PLLs
- Package Type
  - 88 pin QFN

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1 Overview

BL808 is a highly integrated AIoT chipset with Wi-Fi/BT/BLE/Zigbee, Multi-Core CPUs, Audio Codec , Video Codec and AI HW accelerator for high-performance & low-power application.

BL808 mainly includes two subsystems, wireless and multimedia.

The wireless subsystem includes a RISC-V 32-bit high-performance CPU, integrated Wi-Fi /BT/Zigbee wireless subsystem, which can realize a variety of wireless connections and data transmission, and provide a variety of connection and transmission experiences.

The multimedia subsystem includes a RISC-V 64-bit ultra-high-performance CPU and integrates video processing modules such as DVP/CSI/ H264/NPU, which can be widely used in various AI fields such as video surveillance/smart speakers.

The components of the multimedia subsystem are as follows:

- NPU HW NN co-processor (BLAI-100) generally used for AI applications
- Camera interface
- Audio Codec
- Video Codec
- Sensor
- Display interfaces

Power Management Unit provides low-power modes. Moreover, variety of security features are supported.

Peripheral interfaces include USB2.0, Ethernet, SD/MMC, SPI, UART, I2C, I2S, PWM, GPDAC, GPADC, ACOMP, PIR, Touch, IR remote, Display and GPIOs.

Flexible GPIO configurations are supported. BL808 has total 36 or 40 GPIOs.

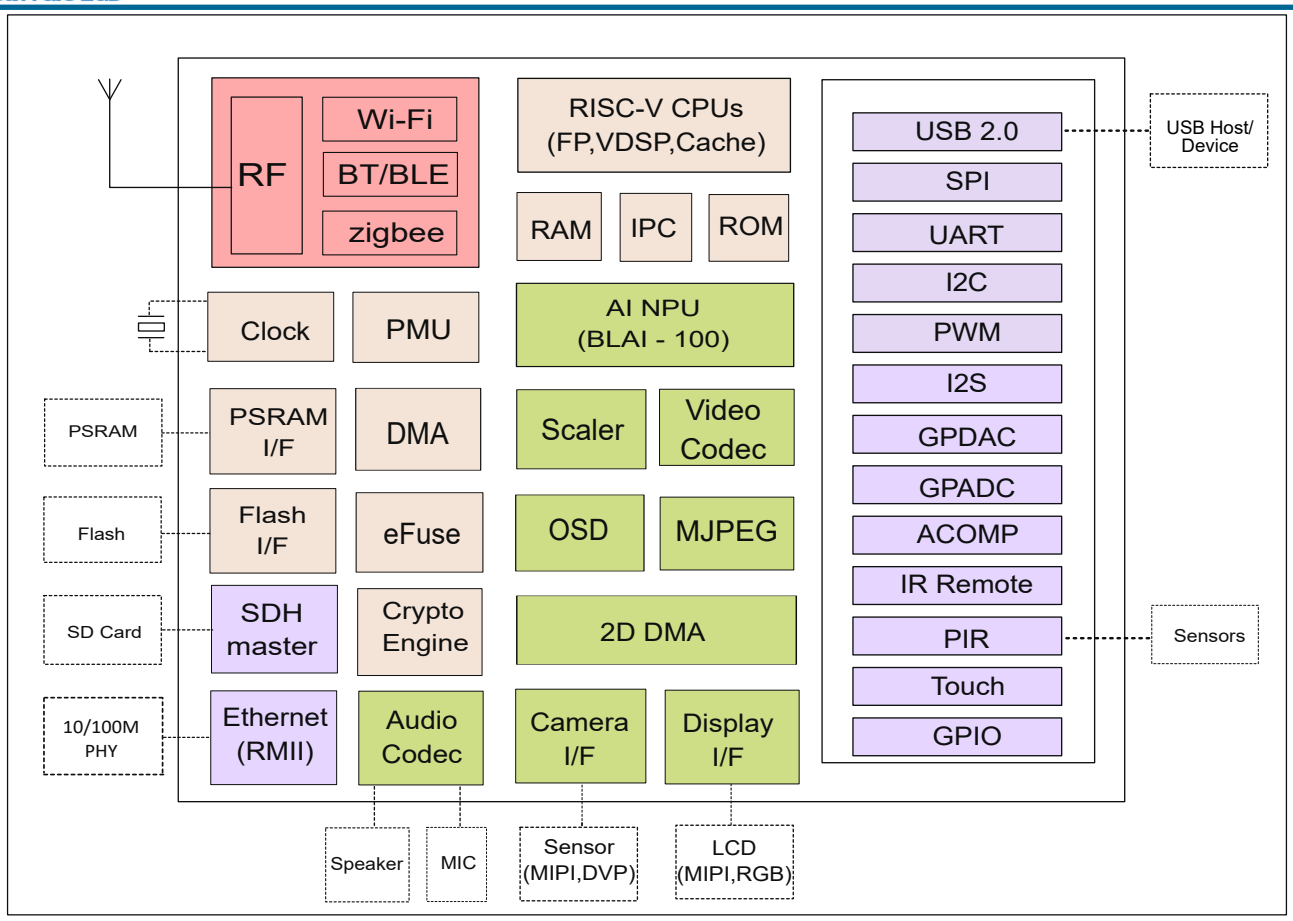

Fig. 1.1: Block Diagram

2 Functional Description

BL808 main functions described as follows:

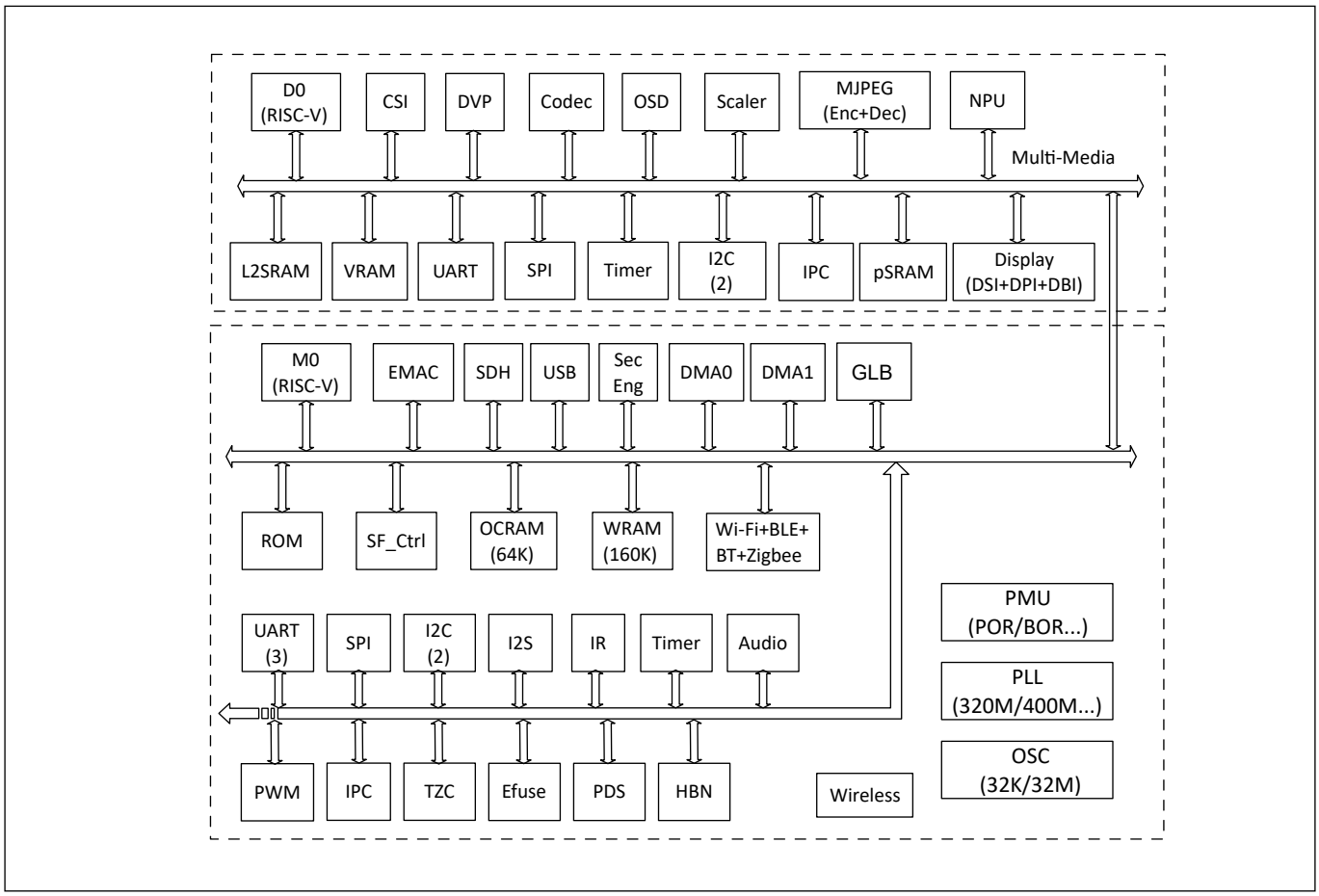

Fig. 2.1: System Architecture

2.1 CPU

BL808 contains multiple RISC-V processors inside.

M0 is a 32-bit RISC-V CPU with a 5-stage pipeline structure, supports RISC-V 32/16-bit mixed instruction set, contains 64 external interrupt sources, and 4 bits can be used to configure interrupt priority.

D0 is a 64-bit RISC-V CPU with a 5-stage pipeline structure, supports the RISC-V RV64IMAFCV instruction architecture, contains 67 external interrupt sources, and 3 bits can be used to configure the interrupt priority.

2.2 Cache

The cache of BL808 improves the performance of CPU accessing external memory. M0 contains 32K instruction cache and 16K data cache; D0 contains 32K instruction cache and 32K data cache.

2.3 Memory

BL808 memory includes: on-chip zero-delay SRAM memory, read-only memory, write-once memory, Embedded flash (optional), embedded pSRAM (optional).

2.4 DMA

The DMA controller has 20 dedicated channels (8 channels each for DMA0 and DMA2, and 4 channels for DMA1) to manage data transfers between peripherals and memory to improve CPU/bus efficiency. DMA has four transfer types, memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral modes.

The DMA also supports the LLI (Linked List Item) feature, which consists of a series of linked lists that predefine multiple transfers, and then the hardware automatically completes all transfers based on the size and address of each LLI. Peripherals supported by DMA include UART, I2C, SPI, ADC, IR, GPIO, Audio, I2S, PDM, DBI, DSI.

2.5 Memory Map

Table 2.1: Memory Map

Module	Size	Base Address(M0)		Base Address(D0)	
		Cache	Non-cache	Cache	Non-cache
OCRAM(MCU)	64KB	0x62020000	0x22020000	-	0x22020000
WRAM(MCU)	160KB	0x62030000	0x22030000	-	0x22030000
DRAM(MM)	512KB	-	0x3EF80000	0x3EF80000	-
VRAM(MM)	32KB	-	0x3F000000	0x3F000000	-

OCRAM and WRAM can be accessed either through AHB bus or through AXI. When the CPU accesses OCRAM

using the address of 0x62020000, it will go through the internal cache and transfer AXI to AHB to achieve access to OCRAM. When the CPU uses the 0x22020000 address to access OCRAM, it does not go through the internal cache and directly accesses OCRAM through the AHB bus.

Table 2.2: Memory Map

Module	Target	Base Address	Size	Description
pSRAM	pSRAM	0x54000000	64MB	pSRAM memory address space, actual size depends on chip model
FLASH	FlashA	0x58000000	64MB	Application address space, the actual size depends on the chip model
MMPERI	TIMER1	0x30009000	4KB	TIMER1 control register
	SPI1	0x30008000	4KB	SPI1 control register
	MM_GLB	0x30007000	4KB	Multimedia side global register
	DMA2D	0x30006000	4KB	DMA2D control register
	I2C3	0x30004000	4KB	I2C3 control register
	I2C2	0x30003000	4KB	I2C2 control register
	UART3	0x30002000	4KB	UART3 control register
	DMA2	0x30001000	4KB	DMA2 control register
MCUPERI	DMA1	0x20071000	4KB	DMA1 control register
	EMAC	0x20070000	4KB	EMAC control register
	AUDIO	0x20055000	4KB	Audio control register
	USB	0x20072000	4KB	USB control register
	HBN	0x2000F000	4KB	Hibernate register
	PDS	0x2000E000	4KB	Power-Down sleep register
	DMA0	0x2000C000	4KB	DMA0 control register
	I2S	0x2000AB00	256B	I2S control register
	ISO11898	0x2000AA00	256B	ISO11898 bus control register
	UART2	0x2000AA00	256B	UART2 control register
	I2C1	0x2000A900	256B	I2C1 control register
	IR	0x2000A600	256B	IR control register
	TIMER0	0x2000A500	256B	TIMER0 control register
	PWM	0x2000A400	256B	PWM control register
	I2C0	0x2000A300	256B	I2C0 control register
	SPI0	0x2000A200	256B	SPI0 control register
	UART1	0x2000A100	256B	UART1 control register
	UART0	0x2000A000	256B	UART0 control register
	eFuse	0x20056000	4KB	eFuse memory control register
	TZ	0x20005000	4KB	Security Zone partition
	SEC_ENG	0x20004000	4KB	Security engine control register
	GPIP	0x20002000	1KB	General purpose DAC/ADC/ACOMP interface control register
	GLB	0x20000000	4KB	Global control register

Table 2.2: Memory Map (continued)

Module	Target	Base Address	Size	Description
ROM	ROM	0x90000000	128KB	Bootrom address space

Table 2.3: MRAM/VRAM address space

MRAM/VRAM		Configure(reg_h2pf_sram_rel , reg_vram_sram_sel , reg_ispl_sram_rel , reg_blai_sram_rel)							
		0 , 0 , 0 , 0	0 , 0 , 0 , 1	1 , 0 , 0 , 0	3 , 0 , 0 , 0	0 , 0 , 1 , 0	0 , 1 , 0 , 0	2 , 0 , 0 , 1	3 , 1 , 1 , 1
MRAM	0x3EF80000 - 0x3EF8FFFF	-	-	-	-	-	-	-	64K
	0x3EF90000 - 0x3EF9FFFF	-	-	-	-	-	-	-	64K
	0x3EFA0000 - 0x3EFAFFFF	-	-	-	-	-	-	-	64K
	0x3EFB0000 - 0x3EFBFFFF	-	-	-	-	-	-	64K	64K
	0x3EFC0000 - 0x3EFCFFFF	-	-	-	64K	-	-	64K	64K
	0x3EFD0000 - 0x3EFDFFFF	-	64K	-	64K	-	-	64K	64K
	0x3EFE0000 - 0x3EFEFFFF	-	64K	64K	64K	64K	64K	64K	64K
	0x3EFF0000 - 0x3EFFFFFF	64K	64K	64K	64K	64K	64K	64K	64K
VRAM	0x3F000000 - 0x3F007FFF	32K	32K	32K	32K	32K	32K	32K	32K

2.6 Interrupt

BL808 supports internal RTC clock wake-up and external interrupt wake-up to realize low-power sleep wake-up function.

The CPU interrupt controller supports a total of 131 maskable interrupt trigger sources including UART interrupt, I2C interrupt, SPI interrupt, timer interrupt, DMA interrupt, etc.

All I/O pins can be configured as external interrupt input mode, the external interrupt supports nine trigger types: synchronous high/low level trigger, synchronous rising/falling edge trigger, asynchronous high/low level trigger, asynchronous rising edge /Falling edge trigger and synchronous double edge trigger.

2.7 Boot

BL808 supports multiple boot options: UART, USB, and Flash.

Table 2.4: Boot mode

Boot pin	Level	Description
GPIO39	1	Boot from UART(GPIO20/21)/USB, this mode is mainly used for Flash download or download image to RAM
	0	Launch application image from Flash

2.8 Power

PMU (power management unit) manages the power of the entire chip and is divided into running, idle, sleep, hibernation and power off modes. The software can be configured to enter sleep mode and wake-up via RTC timer or EINT to achieve low-power sleep and accurate wake-up management.

Power down sleep modes are flexible for applications to configure as the lowest power consumption.

2.9 Clock

Clock control unit generates clocks to the core MCU and the peripheral SOC devices. The root clock source can be XTAL, PLL or RC oscillator. Dynamic power-saved by proper configurations such as sel, div, en, etc.

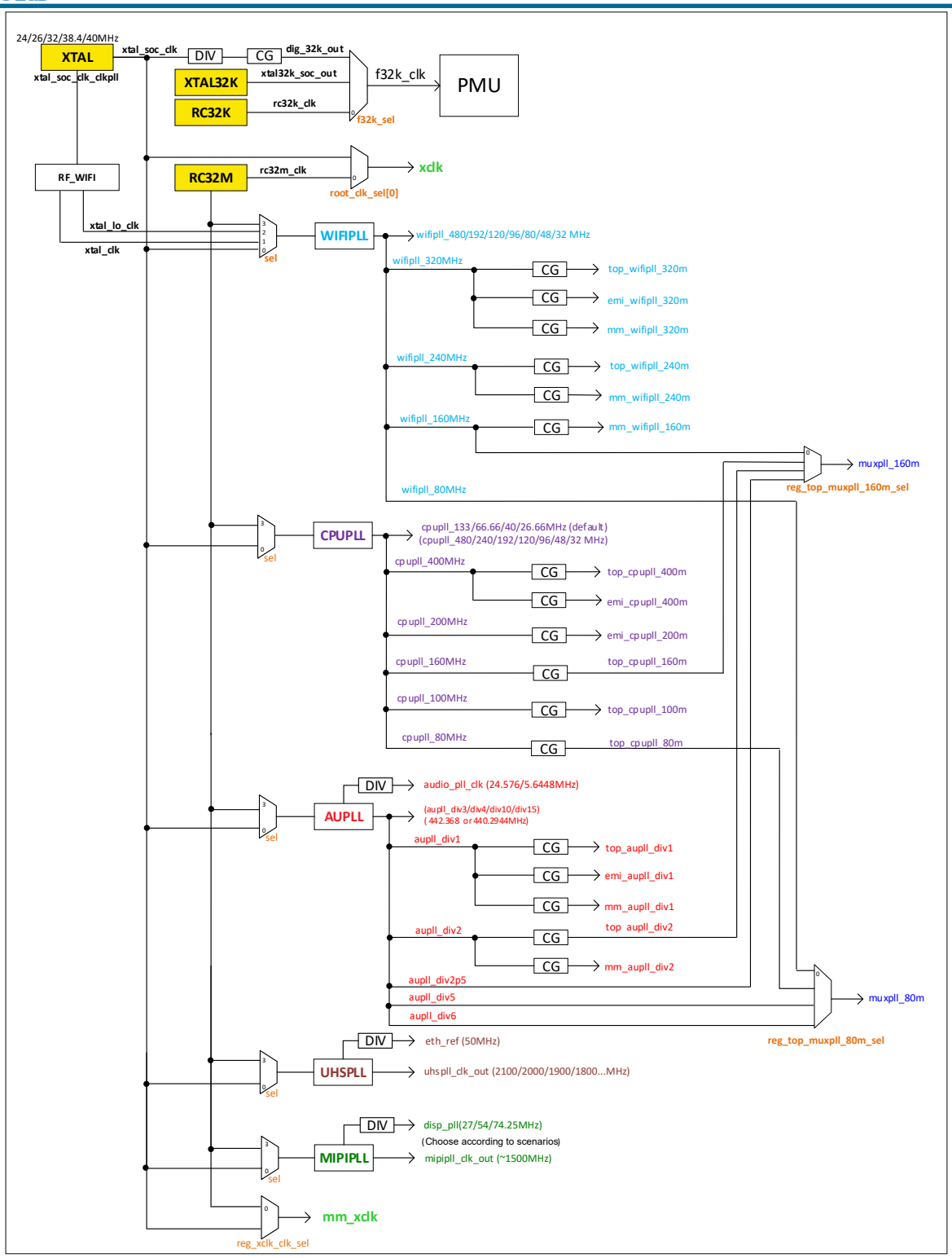

Fig. 2.2: System Clock Architecture

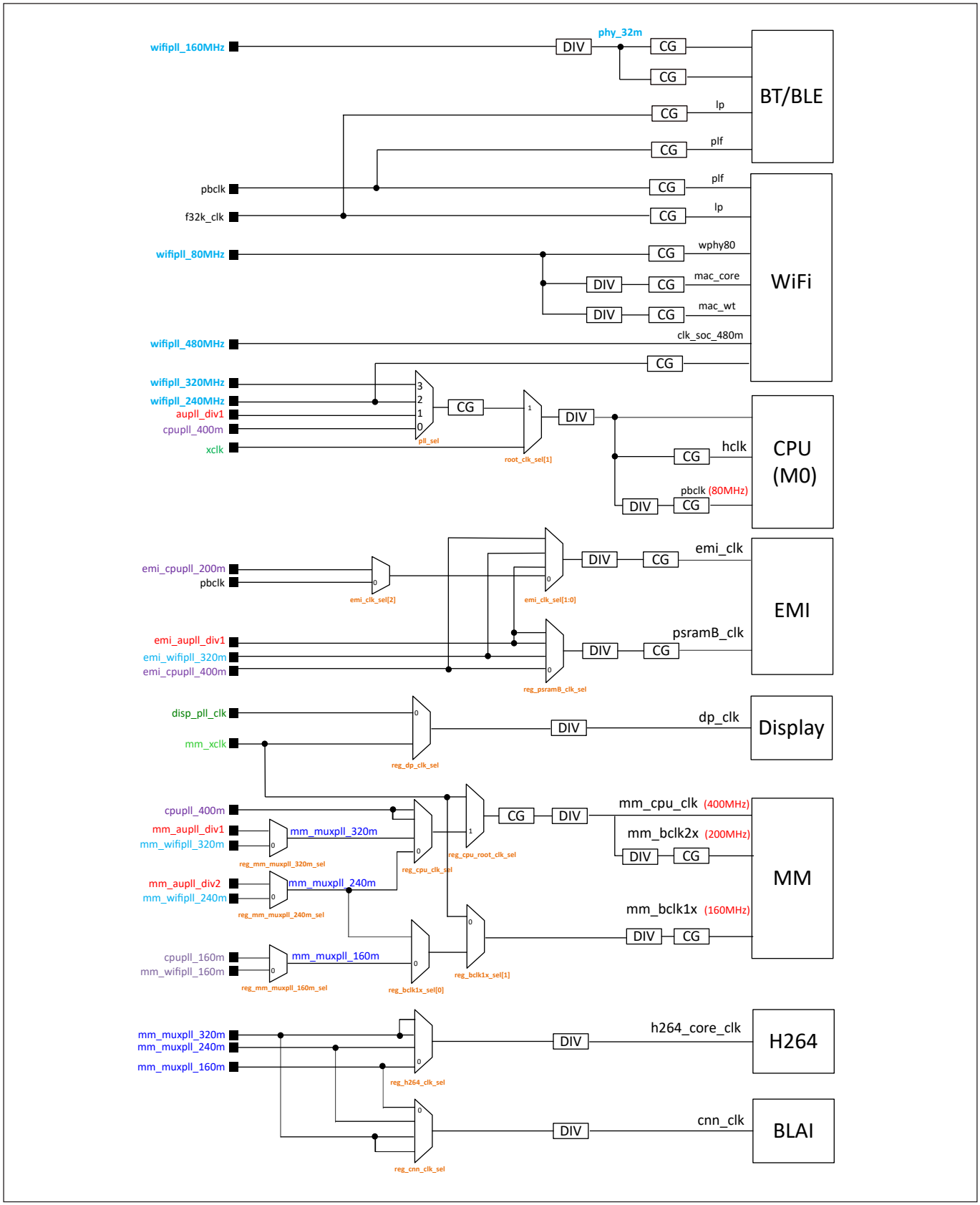

Fig. 2.3: Moudle Clock Architecture

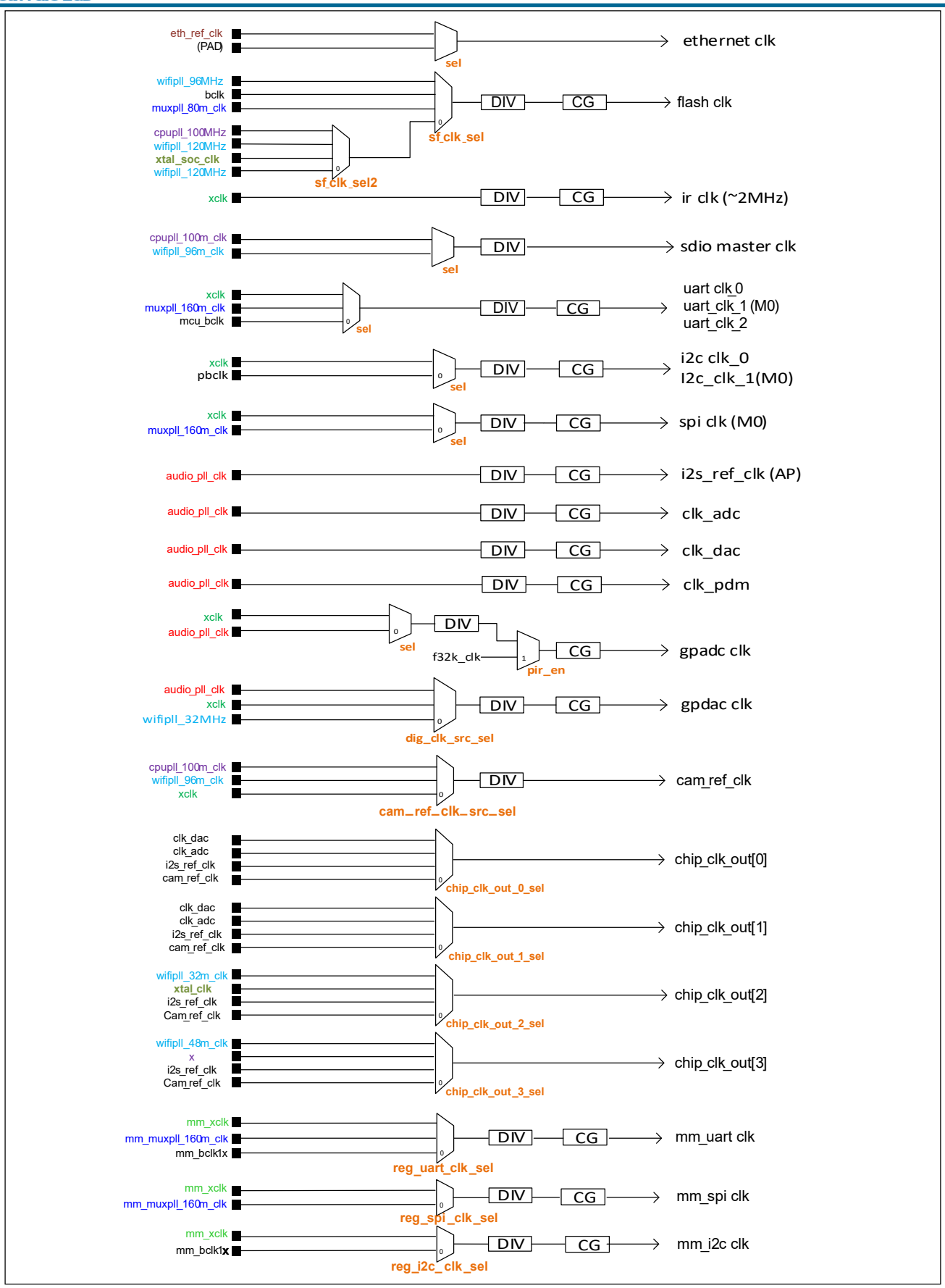

Fig. 2.4: Peripheral Clock Architecture

2.10 Peripheral

Peripherals include USB2.0, Ethernet, SD/MMC, SPI, UART, I2C, I2S, PWM, GPDAC/GPADC/, ACOMP, PIR, Touch, IR remote, Display and GPIO.

2.10.1 GPIO

BL808C can have up to 40 GPIOs, BL808D can have up to 36 GPIOs, with the following features:

- Each GPIO can be used as general purpose input and output function, pull-up/pull-down/float can be configured by software
- Each GPIO supports interrupt function, the interrupt supports synchronous high/low level trigger, synchronous rising/falling edge trigger, asynchronous high/low level trigger, asynchronous rising/falling edge trigger and synchronous double edge trigger
- Each GPIO can be set to high impedance state for low power mode

2.10.2 UART

The chip has four built-in UARTs (UART0/1/2/3) with the following features:

- Supports CTS and RTS flow control in hardware
- Support LIN master/slave function
- Configurable data bits, stop bits and parity bits
- Supports automatic baud rate detection for common/fixed characters
- The working clock can be selected as BCLK, XCLK or 160MHz, the maximum baud rate supports 10Mbps
- TX and RX have independent FIFO, FIFO depth is 32 bytes, support DMA function

2.10.3 SPI

The chip has two built-in SPIs, which can be configured as master mode or slave mode. The SPI module clock is XCLK or 160MHz, and has the following characteristics:

- In master mode, clock frequency up to 80 MHz
- In slave mode, the maximum allowed master clock frequency is 80 MHz
- The bit width of each frame can be configured as 8bit/16bit/24bit/32bit
- Adaptive FIFO depth change characteristics, suitable for high-performance scene applications
  - When the bit width is 32 bits, the depth of the FIFO is 8
  - When the bit width is 24 bits, the depth of the FIFO is 8

  - When the bit width is 16 bits, the depth of the FIFO is 16
  - When the bit width is 8 bits, the depth of the FIFO is 32
- Support DMA transfer mode

2.10.4 I2C

The chip has four built-in I2C interfaces with the following features:

- Support multi-master mode and arbitration function
- The working clock can be selected as BCLK or XCLK
- With device address register, register address register, register address length can be set to 1 byte / 2 bytes / 3 bytes / 4 bytes
- I2C has independent transceiver FIFO, FIFO depth is 2 words
- Support DMA function

2.10.5 I2S

The chip has a built-in I2S interface with the following features:

- Support master mode and slave mode
- Support Left-justified/ Right-justified/ DSP and other data formats, the data width can be configured as 8/16/24/32 bits
- The working clock can be selected as BCLK or XCLK
- Supports both four-channel and six-channel modes in addition to mono/dual-channel mode
- Supports playback of mono audio dubbing to binaural mode
- Support dynamic mute switching function
- I2S has independent transceiver FIFO, FIFO depth is 16 words
- Support DMA function

2.10.6 EMAC

The EMAC module is a 10/100Mbps Ethernet Media Access Controller (Ethernet MAC) compatible with IEEE 802.3, has the following characteristics:

- Compatible with the MAC layer defined by IEEE 802.3
- PHY supporting MII/RMII interface defined by IEEE 802.3
- Interacts with PHY through MDIO interface

- Supports 10 Mbps and 100 Mbps Ethernet
- Supports half-duplex and full-duplex
- Supports automatic flow control and control frame generation in the full-duplex mode
- Supports collision detection and retransmission in the half-duplex mode
- Supports the generation and verification of CRC
- Generates and removes data frame preamble
- Supports automatic extension of short data frames when sending
- Detects too long/short data frames (length limit)
- Transmits long data frames (> standard Ethernet frame length)
- Automatically discards data packets with over-limit retransmission times or too small frame gap
- Broadcast packet filtering
- Internal RAM for storing up to 128 BDs
- Splits and configures a data packet to multiple consecutive Bds when sending
- Various event flags sent or received
- Generates a corresponding interrupt when an event occurs

The EMAC timing diagram is shown below:

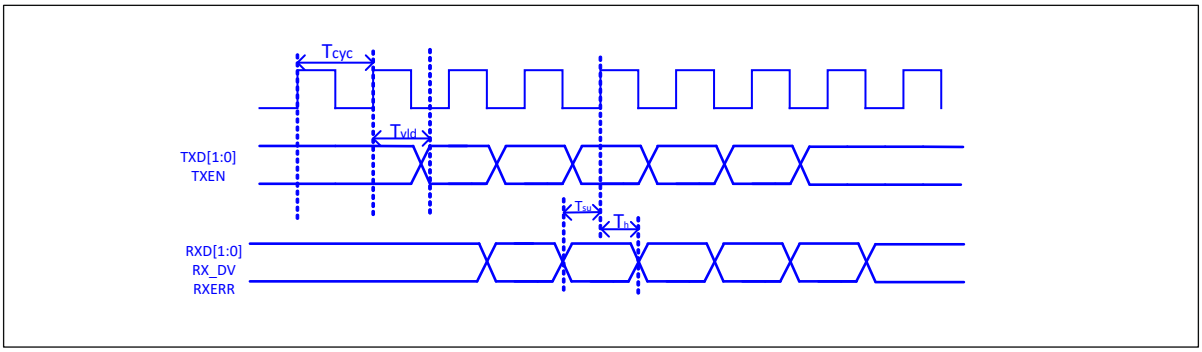

Fig. 2.5: EMAC Timing Diagram

Table 2.5: Timing conditions for using RX Clock

Set the corresponding bit of register eth_cfg0:cfg_inv_eth_rx_clk = 1,cfg_inv_eth_tx_clk = 0,cfg_sel_eth_ref_clk_o = 0						
Timing parameters(1.8V, Load = 20PF)		Min.	Typ	Max.	Unit	Note
T_{cyc}	Clock Cycle	-	20	-	ns	Clock From ETH PHY
T_{vld}	Output Valid Delay	10.37	-	22	ns	TXD/TX_EN

Table 2.5: Timing conditions for using RX Clock(continued)

Set the corresponding bit of register eth_cfg0:cfg_inv_eth_rx_clk = 1,cfg_inv_eth_tx_clk = 0,cfg_sel_eth_ref_clk_o = 0						
Timing parameters(1.8V, Load = 20PF)		Min.	Typ	Max.	Unit	Note
T_{su}	Input Setup Time	6	-	-	ns	RXD/RX_DV/RXERR
T_h	Input Hold Time	0	-	-	ns	RXD/RX_DV/RXERR

Table 2.6: Timing conditions without using RX Clock

Set the corresponding bit of register eth_cfg0:cfg_inv_eth_rx_clk = 0,cfg_inv_eth_tx_clk = 0,cfg_sel_eth_ref_clk_o = 0						
Timing parameters(1.8V, Load = 20PF)		Min.	Typ	Max.	Unit	Note
T_{cyc}	Clock Cycle	-	20	-	ns	Clock From ETH PHY
T_{vld}	Output Valid Delay	10.374	-	22	ns	TXD/TX_EN
T_{su}	Input Setup Time	5	-	-	ns	RXD/RX_DV/RXERR
T_h	Input Hold Time	3	-	-	ns	RXD/RX_DV/RXERR

2.10.7 TIMER

The chip has two built-in 32-bit general-purpose timers and a watchdog timer with the following features:

- The clock source of the general timer can be selected from FCLK/32K/XTAL, and the clock source of the watchdog timer can be selected from FCLK/32K/XTAL
- 8-bit divider for each counter
- Each group of general-purpose timers includes three compare registers, supports compare interrupts, and supports FreeRun mode and PreLoad mode in counting mode
- 16-bit watchdog timer, supports two watchdog overflow methods: interrupt or reset

2.10.8 PWM

The chip has built-in 2 groups of PWM signals, each group contains 4 channels of PWM signal output, each channel can be set to 2 channels of complementary PWM, with the following characteristics:

- Three clock sources BCLK/XCLK/32K
- Frequency divider register and period register are 16-bit wide
- Each channel PWM supports adjustable output polarity, dual threshold setting, increasing the flexibility of pulse output

- Each channel PWM has independent dead time setting
- Each PWM has an independent connection switch to choose whether to connect with the internal counter, and can set the default output level when not connected
- Software brake and external brake signal can put the PWM output level into a preset state
- Up to 11 trigger sources that can be used to trigger ADC conversions

2.10.9 IR(IR-remote)

The chip has a built-in infrared remote control with the following features:

- Support both sending and receiving modes
- Supports up to 128-bit data bits to be sent in non-free mode, and can continuously send data of any length in free mode
- Supports receiving data with fixed protocols NEC, RC-5, and receiving data in any format with pulse width counting
- The clock source is XCLK, and the maximum operating frequency is 32MHz. It has powerful infrared waveform editing capabilities, and can send waveforms that conform to various protocols. The transmit power is adjustable in 15 levels
- Receive FIFO depth is 128 bytes, transmit FIFO depth is 16 bytes
- Transmit supports DMA mode

2.10.10 PDM

The chip has a built-in PDM audio processing module with the following features:

- Integrated 3-channel digital filter, can support 3-channel digital microphone input
  - Sampling rate: 8k~48k
  - SNR > 110dB
  - Data valid bit width 20 bit
  - Digital gain: -95.5 ~ +32.5dB, 0.5dB step
- Independently adjustable three-channel high-pass filter
- Multiplexed GPIO input (1 clock output, 2 data input)
- Transmit FIFO width 32bit, depth 48
- Support DMA transfer mode

2.11 Video encoding

2.11.1 Introduction

VENC adopts the H264 video coding standard, which is mainly compressed by means of prediction and motion compensation, and uses loop filtering to improve the image quality, taking into account the requirements of code stream transmission and image quality.

2.11.2 Features

- 1920x1080p @ 30fps + 640x480 @ 30fps, BP/MP
- Input: Semi-Planar YCbCr 4:2:0
- Output: NALU(Network Abstract Layer Uint) in byte stream format
- CBR/VBR mode
- Up to 8 ROIs
- Up to 16 OSD coding areas
- Support software mode and linkage mode
- Dynamically configurable max/min quantization parameters
- Dynamically configurable I/P frame target bits
- Dynamically configurable I-frame distance

2.12 And sensor and display interface

2.12.1 And sensor

- MIPI-CSI
  1. Support 1-/2-lane mode
  2. Support hardware decoding (RAW8/10/12/14, RGB565/888, YUV422 8-/10-bit) or software decoding
- DVP
  1. Support RAW 12-bit data
  2. Support YUV/RGB 8-bit format
  3. Support image compression mode

2.12.2 And monitor

- MIPI-DSI
  1. Support 1-/2-/4-lane mode
  2. Support RGB565/666/888 and YUV422 8-bit format
  3. Support Sync Event Mode or Sync Pulse Mode
  4. Support Escape Mode, and can be used with DMA function
- MIPI-DBI
  1. Support Type-B (8-bit), Type-C Option 1 (3-wire) and Type-C Option 3 (4-wire) modes
  2. Support RGB565/666/888 format
  3. Built-in YUV2RGB conversion module
  4. Support DMA function
- MIPI-DPI
  1. Support data 16-bit mode
  2. Support RGB565 format
- QSPI
  1. CMD/ADDR/DATA can choose 1-/4-wire mode arbitrarily, so QSPI 111/114/144/444 mode can be supported
  2. Support RGB565/666/888 format
  3. Built-in YUV2RGB conversion module
  4. Support DMA function

3 Pin Definition

BL808C 88-pin package includes 26 power pins, 22 analog pins, and 40 flexible GPIO pins.

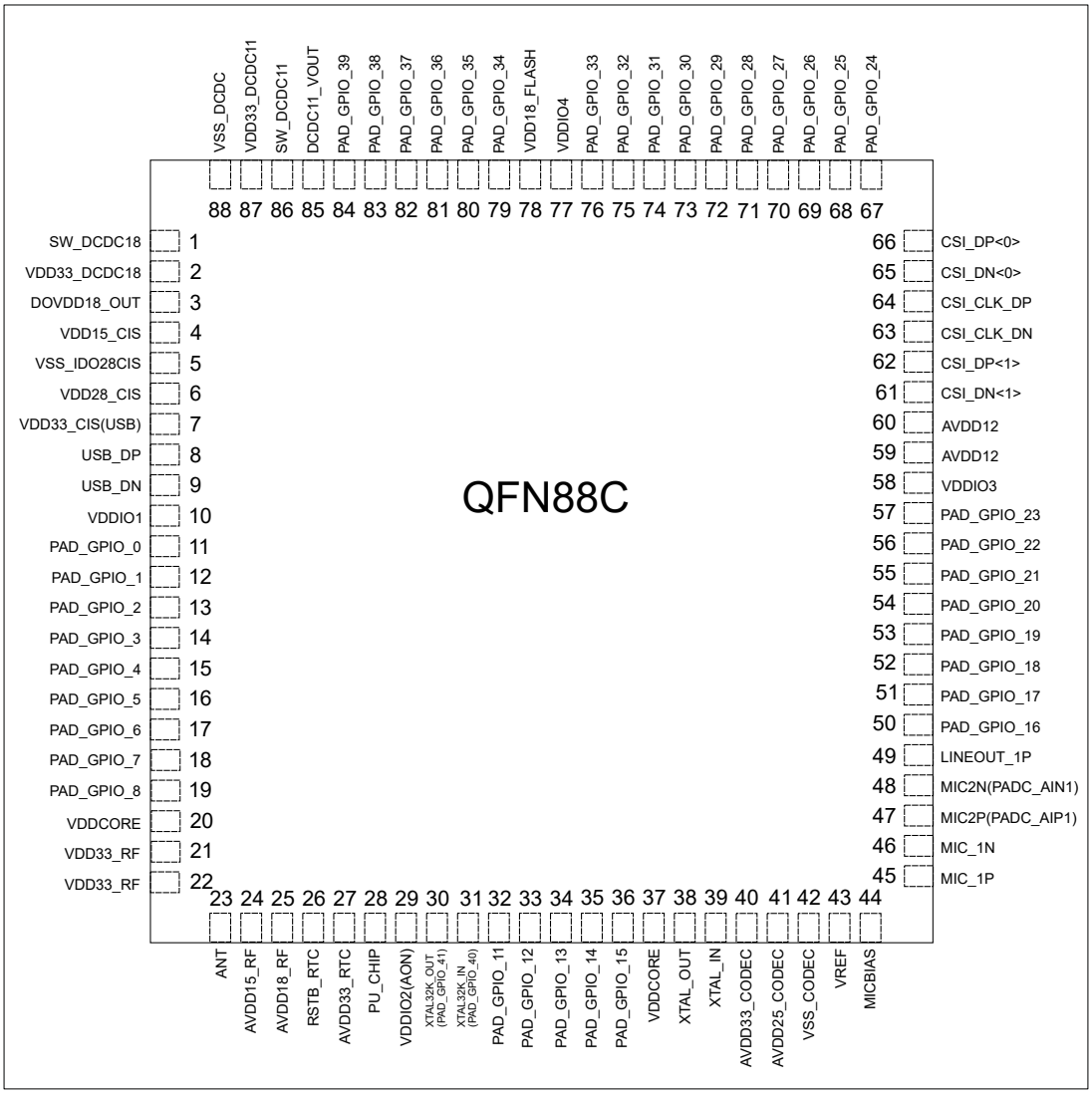

Fig. 3.1: BL808C Pin layout

BL808D 88-pin package includes 27 power pins, 25 analog pins, and 36 flexible GPIO pins.

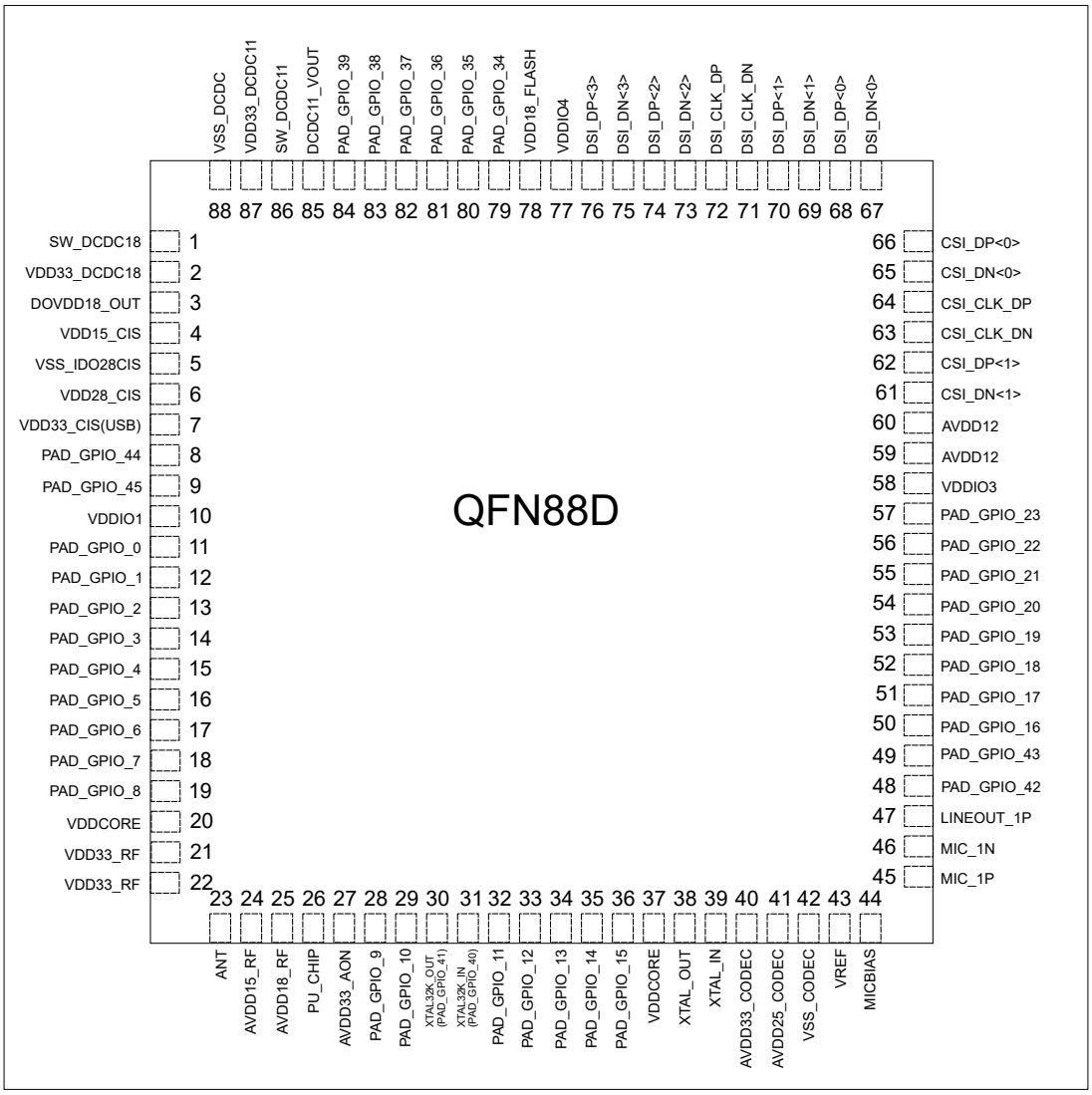

Fig. 3.2: BL808D Pin layout

Table 3.1: Pin Description

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
1	1	-	Power	SW_DCDC18	-	-	SW_DCDC18	DCDC switch output, connected to power inductor
2	2	-	Power	VDD33_DCDC18	-	-	VDD33_DCDC18	DCDC power input, 3.3V
3	3	-	Power	DOVDD18_OUT	-	-	DOVDD18_OUT	DCDC mode, feedback voltage input, 1.8V LDO mode, power output, 1.8V
4	4	-	Power	VDD15_CIS	-	-	VDD15_CIS	Integrated LDO output to power the image sensor digital power DVDD
5	5	-	Power	VSS_IDO28CIS	-	-	VSS_IDO28CIS	Connect to the image sensor analog ground AGND
6	6	-	Power	VDD28_CIS	-	-	VDD28_CIS	Integrated LDO output to power the image sensor analog power supply AVDD
7	7	-	Power	VDD33_CIS(USB)	-	-	VDD33_CIS(USB)	Integrated LDO VDD28_CIS input, 3.3V
8	-	VDDIO_1	DI/DO	USB_DP	-	-	USB_DP	USB2.0 differential data cable+
9	-	VDDIO_1	DI/DO	USB_DN	-	-	USB_DN	USB2.0 differential data cable

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	8	VDDIO_1	DI/DO	PAD_GPIO_44	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_8_sel=0	UART0_RTS	UART0_RTS
						uart_sig_8_sel=1	UART0_CTS	UART0_CTS
						uart_sig_8_sel=2	UART0_TXD	UART0_TXD
						uart_sig_8_sel=3	UART0_RXD	UART0_RXD
						uart_sig_8_sel=4	UART1_RTS	UART1_RTS
						uart_sig_8_sel=5	UART1_CTS	UART1_CTS
						uart_sig_8_sel=6	UART1_TXD	UART1_TXD
						uart_sig_8_sel=7	UART1_RXD	UART1_RXD
						uart_sig_8_sel=8	UART2_RTS	UART2_RTS
						uart_sig_8_sel=9	UART2_CTS	UART2_CTS
						uart_sig_8_sel=10	UART2_TXD	UART2_TXD
						uart_sig_8_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO44	SWGPIO44
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CSn	DBI_CSn
					24	-	-	-
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	9	VDDIO_1	DI/DO	PAD_GPIO_45	0	-	-	-
					1	-	SPI_MOSI [1]	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_9_sel=0	UART0_RTS	UART0_RTS
						uart_sig_9_sel=1	UART0_CTS	UART0_CTS
						uart_sig_9_sel=2	UART0_TXD	UART0_TXD
						uart_sig_9_sel=3	UART0_RXD	UART0_RXD
						uart_sig_9_sel=4	UART1_RTS	UART1_RTS
						uart_sig_9_sel=5	UART1_CTS	UART1_CTS
						uart_sig_9_sel=6	UART1_TXD	UART1_TXD
						uart_sig_9_sel=7	UART1_RXD	UART1_RXD
						uart_sig_9_sel=8	UART2_RTS	UART2_RTS
						uart_sig_9_sel=9	UART2_CTS	UART2_CTS
						uart_sig_9_sel=10	UART2_TXD	UART2_TXD
						uart_sig_9_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO45	SWGPIO45
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI
10	10	-	Power	VDDIO1	-	-	VDDIO1	GPIO0~8, GPIO44~45 power supply, 3.3V/1.8V

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
11	11	VDDIO_1	DI/DO	PAD_GPIO_0	0	-	SDH_CLK	SDH_CLK
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
						uart_sig_0_sel=4	UART1_RTS	UART1_RTS
						uart_sig_0_sel=5	UART1_CTS	UART1_CTS
						uart_sig_0_sel=6	UART1_TXD	UART1_TXD
						uart_sig_0_sel=7	UART1_RXD	UART1_RXD
						uart_sig_0_sel=8	UART2_RTS	UART2_RTS
						uart_sig_0_sel=9	UART2_CTS	UART2_CTS
						uart_sig_0_sel=10	UART2_TXD	UART2_TXD
						uart_sig_0_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	USB20_RREF_EXT	USB20_RREF_EXT
					11	-	SWGPIO0	SWGPIO0
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CSn	DBI_CSn
					24	-	-	-
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
12	12	VDDIO_1	DI/DO	PAD_GPIO_1	0	-	SDH_CMD	SDH_CMD
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
						uart_sig_1_sel=4	UART1_RTS	UART1_RTS
						uart_sig_1_sel=5	UART1_CTS	UART1_CTS
						uart_sig_1_sel=6	UART1_TXD	UART1_TXD
						uart_sig_1_sel=7	UART1_RXD	UART1_RXD
						uart_sig_1_sel=8	UART2_RTS	UART2_RTS
						uart_sig_1_sel=9	UART2_CTS	UART2_CTS
						uart_sig_1_sel=10	UART2_TXD	UART2_TXD
						uart_sig_1_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO1	SWGPIO1
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
13	13	VDDIO_1	DI/DO	PAD_GPIO_2	0	-	SDH_DAT0	SDH_DAT0
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
						uart_sig_2_sel=4	UART1_RTS	UART1_RTS
						uart_sig_2_sel=5	UART1_CTS	UART1_CTS
						uart_sig_2_sel=6	UART1_TXD	UART1_TXD
						uart_sig_2_sel=7	UART1_RXD	UART1_RXD
						uart_sig_2_sel=8	UART2_RTS	UART2_RTS
						uart_sig_2_sel=9	UART2_CTS	UART2_CTS
						uart_sig_2_sel=10	UART2_TXD	UART2_TXD
						uart_sig_2_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO2	SWGPIO2
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
14	14	VDDIO_1	DI/DO	PAD_GPIO_3	0	-	SDH_DAT1	SDH_DAT1
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
						uart_sig_3_sel=4	UART1_RTS	UART1_RTS
						uart_sig_3_sel=5	UART1_CTS	UART1_CTS
						uart_sig_3_sel=6	UART1_TXD	UART1_TXD
						uart_sig_3_sel=7	UART1_RXD	UART1_RXD
						uart_sig_3_sel=8	UART2_RTS	UART2_RTS
						uart_sig_3_sel=9	UART2_CTS	UART2_CTS
						uart_sig_3_sel=10	UART2_TXD	UART2_TXD
						uart_sig_3_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO3	SWGPIO3
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
15	15	VDDIO_1	DI/DO	PAD_GPIO_4	0	-	SDH_DAT2	SDH_DAT2
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_4_sel=0	UART0_RTS	UART0_RTS
						uart_sig_4_sel=1	UART0_CTS	UART0_CTS
						uart_sig_4_sel=2	UART0_TXD	UART0_TXD
						uart_sig_4_sel=3	UART0_RXD	UART0_RXD
						uart_sig_4_sel=4	UART1_RTS	UART1_RTS
						uart_sig_4_sel=5	UART1_CTS	UART1_CTS
						uart_sig_4_sel=6	UART1_TXD	UART1_TXD
						uart_sig_4_sel=7	UART1_RXD	UART1_RXD
						uart_sig_4_sel=8	UART2_RTS	UART2_RTS
						uart_sig_4_sel=9	UART2_CTS	UART2_CTS
						uart_sig_4_sel=10	UART2_TXD	UART2_TXD
						uart_sig_4_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH2	ADC_CH2
					11	-	SWGPIO4	SWGPIO4
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CSn	DBI_CSn
					24	-	-	-
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
16	16	VDDIO_1	DI/DO	PAD_GPIO_5	0	-	SDH_DAT3	SDH_DAT3
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_5_sel=0	UART0_RTS	UART0_RTS
						uart_sig_5_sel=1	UART0_CTS	UART0_CTS
						uart_sig_5_sel=2	UART0_TXD	UART0_TXD
						uart_sig_5_sel=3	UART0_RXD	UART0_RXD
						uart_sig_5_sel=4	UART1_RTS	UART1_RTS
						uart_sig_5_sel=5	UART1_CTS	UART1_CTS
						uart_sig_5_sel=6	UART1_TXD	UART1_TXD
						uart_sig_5_sel=7	UART1_RXD	UART1_RXD
						uart_sig_5_sel=8	UART2_RTS	UART2_RTS
						uart_sig_5_sel=9	UART2_CTS	UART2_CTS
						uart_sig_5_sel=10	UART2_TXD	UART2_TXD
						uart_sig_5_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH1	ADC_CH1
					11	-	SWGPIO5	SWGPIO5
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
17	17	VDDIO_1	DI/DO	PAD_GPIO_6	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_6_sel=0	UART0_RTS	UART0_RTS
						uart_sig_6_sel=1	UART0_CTS	UART0_CTS
						uart_sig_6_sel=2	UART0_TXD	UART0_TXD
						uart_sig_6_sel=3	UART0_RXD	UART0_RXD
						uart_sig_6_sel=4	UART1_RTS	UART1_RTS
						uart_sig_6_sel=5	UART1_CTS	UART1_CTS
						uart_sig_6_sel=6	UART1_TXD	UART1_TXD
						uart_sig_6_sel=7	UART1_RXD	UART1_RXD
						uart_sig_6_sel=8	UART2_RTS	UART2_RTS
						uart_sig_6_sel=9	UART2_CTS	UART2_CTS
						uart_sig_6_sel=10	UART2_TXD	UART2_TXD
						uart_sig_6_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH4	ADC_CH4
					11	-	SWGPIO6	SWGPIO6
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
18	18	VDDIO_1	DI/DO	PAD_GPIO_7	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_7_sel=0	UART0_RTS	UART0_RTS
						uart_sig_7_sel=1	UART0_CTS	UART0_CTS
						uart_sig_7_sel=2	UART0_TXD	UART0_TXD
						uart_sig_7_sel=3	UART0_RXD	UART0_RXD
						uart_sig_7_sel=4	UART1_RTS	UART1_RTS
						uart_sig_7_sel=5	UART1_CTS	UART1_CTS
						uart_sig_7_sel=6	UART1_TXD	UART1_TXD
						uart_sig_7_sel=7	UART1_RXD	UART1_RXD
						uart_sig_7_sel=8	UART2_RTS	UART2_RTS
						uart_sig_7_sel=9	UART2_CTS	UART2_CTS
						uart_sig_7_sel=10	UART2_TXD	UART2_TXD
						uart_sig_7_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO7	SWGPIO7
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
19	19	VDDIO_1	DI/DO	PAD_GPIO_8	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_8_sel=0	UART0_RTS	UART0_RTS
						uart_sig_8_sel=1	UART0_CTS	UART0_CTS
						uart_sig_8_sel=2	UART0_TXD	UART0_TXD
						uart_sig_8_sel=3	UART0_RXD	UART0_RXD
						uart_sig_8_sel=4	UART1_RTS	UART1_RTS
						uart_sig_8_sel=5	UART1_CTS	UART1_CTS
						uart_sig_8_sel=6	UART1_TXD	UART1_TXD
						uart_sig_8_sel=7	UART1_RXD	UART1_RXD
						uart_sig_8_sel=8	UART2_RTS	UART2_RTS
						uart_sig_8_sel=9	UART2_CTS	UART2_CTS
						uart_sig_8_sel=10	UART2_TXD	UART2_TXD
						uart_sig_8_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO8	SWGPIO8
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CSn	DBI_CSn
					24	-	-	-
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK
20	20	-	Power	VDDCORE	-	-	VDDCORE	Core power, 1.1V
21	21	-	Power	VDD33_RF	-	-	VDD33_RF	RF transmitter power supply, 3.3V
22	22	-	Power	VDD33_RF	-	-	VDD33_RF	RF transmitter power supply, 3.3V
23	23	AVDD15	Analog	ANT	-	-	ANT	RF signal pin
24	24	-	Power	AVDD15_RF	-	-	AVDD15_RF	Integrated LDO output, RF circuit power supply, 1.5V, connected to decoupling capacitors
25	25	-	Power	AVDD18_RF	-	-	AVDD18_RF	Integrated LDO input, 1.8V (connected to the third pin VDD18_OUT)/3.3V
26	-	-	Power	RSTB_RTC	-	-	RSTB_RTC	Real-time clock circuit reset, active low
28	26	AVDD33	Analog	PU_CHIP	-	-	PU_CHIP	Chip enable, active high
27	-	-	Power	AVDD33_RTC	-	-	AVDD33_RTC	Real-time clock circuit power supply, 3.3V
29	27	-	Power	VDDIO2(AON)	-	-	VDDIO2(AON)	GPIO11~15, GPIO40~41 and AON circuit power input, 3.3V

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	28	AVDD33	DI/DO	PAD_GPIO_9	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_9_sel=0	UART0_RTS	UART0_RTS
						uart_sig_9_sel=1	UART0_CTS	UART0_CTS
						uart_sig_9_sel=2	UART0_TXD	UART0_TXD
						uart_sig_9_sel=3	UART0_RXD	UART0_RXD
						uart_sig_9_sel=4	UART1_RTS	UART1_RTS
						uart_sig_9_sel=5	UART1_CTS	UART1_CTS
						uart_sig_9_sel=6	UART1_TXD	UART1_TXD
						uart_sig_9_sel=7	UART1_RXD	UART1_RXD
						uart_sig_9_sel=8	UART2_RTS	UART2_RTS
						uart_sig_9_sel=9	UART2_CTS	UART2_CTS
						uart_sig_9_sel=10	UART2_TXD	UART2_TXD
						uart_sig_9_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO9	SWGPIO9
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	29	AVDD33	DI/DO	PAD_GPIO_10	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_10_sel=0	UART0_RTS	UART0_RTS
						uart_sig_10_sel=1	UART0_CTS	UART0_CTS
						uart_sig_10_sel=2	UART0_TXD	UART0_TXD
						uart_sig_10_sel=3	UART0_RXD	UART0_RXD
						uart_sig_10_sel=4	UART1_RTS	UART1_RTS
						uart_sig_10_sel=5	UART1_CTS	UART1_CTS
						uart_sig_10_sel=6	UART1_TXD	UART1_TXD
						uart_sig_10_sel=7	UART1_RXD	UART1_RXD
						uart_sig_10_sel=8	UART2_RTS	UART2_RTS
						uart_sig_10_sel=9	UART2_CTS	UART2_CTS
						uart_sig_10_sel=10	UART2_TXD	UART2_TXD
						uart_sig_10_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO10	SWGPIO10
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
		AVDD33	Clock	XTAL32K_OUT	-	XTAL32K_OUT	XTAL32K_OUT	Connect to RTC passive crystal/active clock
					0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_5_sel=0	UART0_RTS	UART0_RTS
						uart_sig_5_sel=1	UART0_CTS	UART0_CTS
						uart_sig_5_sel=2	UART0_TXD	UART0_TXD
						uart_sig_5_sel=3	UART0_RXD	UART0_RXD
						uart_sig_5_sel=4	UART1_RTS	UART1_RTS
						uart_sig_5_sel=5	UART1_CTS	UART1_CTS
						uart_sig_5_sel=6	UART1_TXD	UART1_TXD
						uart_sig_5_sel=7	UART1_RXD	UART1_RXD
						uart_sig_5_sel=8	UART2_RTS	UART2_RTS
						uart_sig_5_sel=9	UART2_CTS	UART2_CTS
30	30	VDDIO_2	DI/DO	PAD_GPIO_41		uart_sig_5_sel=10	UART2_TXD	UART2_TXD
						uart_sig_5_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO41	SWGPIO41
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
		AVDD33	Clock	XTAL32K_IN	-	XTAL32K_IN	XTAL32K_IN	Connect to RTC passive crystal
31	31	VDDIO_2	DI/DO	PAD_GPIO_40	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_4_sel=0	UART0_RTS	UART0_RTS
						uart_sig_4_sel=1	UART0_CTS	UART0_CTS
						uart_sig_4_sel=2	UART0_TXD	UART0_TXD
						uart_sig_4_sel=3	UART0_RXD	UART0_RXD
						uart_sig_4_sel=4	UART1_RTS	UART1_RTS
						uart_sig_4_sel=5	UART1_CTS	UART1_CTS
						uart_sig_4_sel=6	UART1_TXD	UART1_TXD
						uart_sig_4_sel=7	UART1_RXD	UART1_RXD
						uart_sig_4_sel=8	UART2_RTS	UART2_RTS
						uart_sig_4_sel=9	UART2_CTS	UART2_CTS
						uart_sig_4_sel=10	UART2_TXD	UART2_TXD
						uart_sig_4_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH5	ADC_CH5
					11	-	SWGPIO40	SWGPIO40
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	DBI_RDn	DBI_RDn
					23	-	DBI_CSn	DBI_CSn
					24	-	-	-
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
32	32	VDDIO_2	DI/DO	PAD_GPIO_11	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_11_sel=0	UART0_RTS	UART0_RTS
						uart_sig_11_sel=1	UART0_CTS	UART0_CTS
						uart_sig_11_sel=2	UART0_TXD	UART0_TXD
						uart_sig_11_sel=3	UART0_RXD	UART0_RXD
						uart_sig_11_sel=4	UART1_RTS	UART1_RTS
						uart_sig_11_sel=5	UART1_CTS	UART1_CTS
						uart_sig_11_sel=6	UART1_TXD	UART1_TXD
						uart_sig_11_sel=7	UART1_RXD	UART1_RXD
						uart_sig_11_sel=8	UART2_RTS	UART2_RTS
						uart_sig_11_sel=9	UART2_CTS	UART2_CTS
						uart_sig_11_sel=10	UART2_TXD	UART2_TXD
						uart_sig_11_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH3	ADC_CH3
					11	-	SWGPIO11	SWGPIO11
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	DBI_CSn	DBI_CSn
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
33	33	VDDIO_2	DI/DO	PAD_GPIO_12	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
						uart_sig_0_sel=4	UART1_RTS	UART1_RTS
						uart_sig_0_sel=5	UART1_CTS	UART1_CTS
						uart_sig_0_sel=6	UART1_TXD	UART1_TXD
						uart_sig_0_sel=7	UART1_RXD	UART1_RXD
						uart_sig_0_sel=8	UART2_RTS	UART2_RTS
						uart_sig_0_sel=9	UART2_CTS	UART2_CTS
						uart_sig_0_sel=10	UART2_TXD	UART2_TXD
						uart_sig_0_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH6	ADC_CH6
					11	-	SWGPIO12	SWGPIO12
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	DBI_DCn	DBI_DCn
					23	-	DBI_CSn	DBI_CSn
					24	-	DPI_VS	DPI_VS
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
34	34	VDDIO_2	DI/DO	PAD_GPIO_13	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
						uart_sig_1_sel=4	UART1_RTS	UART1_RTS
						uart_sig_1_sel=5	UART1_CTS	UART1_CTS
						uart_sig_1_sel=6	UART1_TXD	UART1_TXD
						uart_sig_1_sel=7	UART1_RXD	UART1_RXD
						uart_sig_1_sel=8	UART2_RTS	UART2_RTS
						uart_sig_1_sel=9	UART2_CTS	UART2_CTS
						uart_sig_1_sel=10	UART2_TXD	UART2_TXD
						uart_sig_1_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH7	ADC_CH7
					11	-	SWGPIO13	SWGPIO13
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	DBI_WRn	DBI_WRn
					23	-	DBI_DCn	DBI_DCn
					24	-	DPI_HS	DPI_HS
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
35	35	VDDIO_2	DI/DO	PAD_GPIO_14	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
						uart_sig_2_sel=4	UART1_RTS	UART1_RTS
						uart_sig_2_sel=5	UART1_CTS	UART1_CTS
						uart_sig_2_sel=6	UART1_TXD	UART1_TXD
						uart_sig_2_sel=7	UART1_RXD	UART1_RXD
						uart_sig_2_sel=8	UART2_RTS	UART2_RTS
						uart_sig_2_sel=9	UART2_CTS	UART2_CTS
						uart_sig_2_sel=10	UART2_TXD	UART2_TXD
						uart_sig_2_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO14	SWGPIO14
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
36	36	VDDIO_2	DI/DO	PAD_GPIO_15	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
						uart_sig_3_sel=4	UART1_RTS	UART1_RTS
						uart_sig_3_sel=5	UART1_CTS	UART1_CTS
						uart_sig_3_sel=6	UART1_TXD	UART1_TXD
						uart_sig_3_sel=7	UART1_RXD	UART1_RXD
						uart_sig_3_sel=8	UART2_RTS	UART2_RTS
						uart_sig_3_sel=9	UART2_CTS	UART2_CTS
						uart_sig_3_sel=10	UART2_TXD	UART2_TXD
						uart_sig_3_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO15	SWGPIO15
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO
37	37	-	Power	VDDCORE	-	-	VDDCORE	Core Power, 1.1V
38	38	AVDD33	Clock	XTAL_OUT	-	-	XTAL_OUT	Connect high frequency passive crystal
39	39	AVDD33	Clock	XTAL_IN	-	-	XTAL_IN	Connect high frequency passive crystal/active clock
40	40	-	Power	AVDD33_CODEC	-	-	AVDD33_CODEC	Integrated LDO input, 3.3V
41	41	-	Power	AVDD25_CODEC	-	-	AVDD25_CODEC	Integrated LDO output, audio codec circuit power supply, 2.5V,connected to decoupling capacitors
42	42	-	Power	VSS_CODEC	-	-	VSS_CODEC	Audio codec circuit ground pin
43	43	-	Power	VREF	-	-	VREF	Audio codec circuit reference voltage, connected to decoupling capacitors
44	44	-	Power	MICBIAS	-	-	MICBIAS	Microphone Bias/Power
45	45	AVDD33/25	Analog	MIC_1P	-	-	MIC_1P	Microphone 1 differential input+
46	46	AVDD33/25	Analog	MIC_1N	-	-	MIC_1N	Microphone 1 differential input-
47	-	AVDD33/25	Analog	MIC2P(PADC_AIP1)	-	-	MIC2P(PADC_AIP1)	Microphone 2 differential input+
48	-	AVDD33/25	Analog	MIC2N(PADC_AIN1)	-	-	MIC2N(PADC_AIN1)	Microphone 2 differential input-
49	47	AVDD33/25	Analog	LINEOUT_1P	-	-	LINEOUT_1P	Line 1 single-ended output

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	48	VDDIO_3	DI/DO	PAD_GPIO_42	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_6_sel=0	UART0_RTS	UART0_RTS
						uart_sig_6_sel=1	UART0_CTS	UART0_CTS
						uart_sig_6_sel=2	UART0_TXD	UART0_TXD
						uart_sig_6_sel=3	UART0_RXD	UART0_RXD
						uart_sig_6_sel=4	UART1_RTS	UART1_RTS
						uart_sig_6_sel=5	UART1_CTS	UART1_CTS
						uart_sig_6_sel=6	UART1_TXD	UART1_TXD
						uart_sig_6_sel=7	UART1_RXD	UART1_RXD
						uart_sig_6_sel=8	UART2_RTS	UART2_RTS
						uart_sig_6_sel=9	UART2_CTS	UART2_CTS
						uart_sig_6_sel=10	UART2_TXD	UART2_TXD
						uart_sig_6_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO42	SWGPIO42
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	49	VDDIO_3	DI/DO	PAD_GPIO_43	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_7_sel=0	UART0_RTS	UART0_RTS
						uart_sig_7_sel=1	UART0_CTS	UART0_CTS
						uart_sig_7_sel=2	UART0_TXD	UART0_TXD
						uart_sig_7_sel=3	UART0_RXD	UART0_RXD
						uart_sig_7_sel=4	UART1_RTS	UART1_RTS
						uart_sig_7_sel=5	UART1_CTS	UART1_CTS
						uart_sig_7_sel=6	UART1_TXD	UART1_TXD
						uart_sig_7_sel=7	UART1_RXD	UART1_RXD
						uart_sig_7_sel=8	UART2_RTS	UART2_RTS
						uart_sig_7_sel=9	UART2_CTS	UART2_CTS
						uart_sig_7_sel=10	UART2_TXD	UART2_TXD
						uart_sig_7_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO43	SWGPIO43
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
50	50	VDDIO_3	DI/DO	PAD_GPIO_16	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_4_sel=0	UART0_RTS	UART0_RTS
						uart_sig_4_sel=1	UART0_CTS	UART0_CTS
						uart_sig_4_sel=2	UART0_TXD	UART0_TXD
						uart_sig_4_sel=3	UART0_RXD	UART0_RXD
						uart_sig_4_sel=4	UART1_RTS	UART1_RTS
						uart_sig_4_sel=5	UART1_CTS	UART1_CTS
						uart_sig_4_sel=6	UART1_TXD	UART1_TXD
						uart_sig_4_sel=7	UART1_RXD	UART1_RXD
						uart_sig_4_sel=8	UART2_RTS	UART2_RTS
						uart_sig_4_sel=9	UART2_CTS	UART2_CTS
						uart_sig_4_sel=10	UART2_TXD	UART2_TXD
						uart_sig_4_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	CAM_HSYNC	CAM_HSYNC
					10	-	ADC_CH8	ADC_CH8
					11	-	SWGPIO16	SWGPIO16
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	DBI_DB_0	DBI_DB_0
					23	-	DBI_CSn	DBI_CSn
					24	-	DPI_PCLK	DPI_PCLK
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
51	51	VDDIO_3	DI/DO	PAD_GPIO_17	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_5_sel=0	UART0_RTS	UART0_RTS
						uart_sig_5_sel=1	UART0_CTS	UART0_CTS
						uart_sig_5_sel=2	UART0_TXD	UART0_TXD
						uart_sig_5_sel=3	UART0_RXD	UART0_RXD
						uart_sig_5_sel=4	UART1_RTS	UART1_RTS
						uart_sig_5_sel=5	UART1_CTS	UART1_CTS
						uart_sig_5_sel=6	UART1_TXD	UART1_TXD
						uart_sig_5_sel=7	UART1_RXD	UART1_RXD
						uart_sig_5_sel=8	UART2_RTS	UART2_RTS
						uart_sig_5_sel=9	UART2_CTS	UART2_CTS
						uart_sig_5_sel=10	UART2_TXD	UART2_TXD
						uart_sig_5_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	CAM_VSYNC	CAM_VSYNC
					10	-	ADC_CH0	ADC_CH0
					11	-	SWGPIO17	SWGPIO17
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	DBI_DB_1	DBI_DB_1
					23	-	DBI_DCn	DBI_DCn
					24	-	DPI_DATA[0]	DPI_DATA[0]
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
52	52	VDDIO_3	DI/DO	PAD_GPIO_18	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_6_sel=0	UART0_RTS	UART0_RTS
						uart_sig_6_sel=1	UART0_CTS	UART0_CTS
						uart_sig_6_sel=2	UART0_TXD	UART0_TXD
						uart_sig_6_sel=3	UART0_RXD	UART0_RXD
						uart_sig_6_sel=4	UART1_RTS	UART1_RTS
						uart_sig_6_sel=5	UART1_CTS	UART1_CTS
						uart_sig_6_sel=6	UART1_TXD	UART1_TXD
						uart_sig_6_sel=7	UART1_RXD	UART1_RXD
						uart_sig_6_sel=8	UART2_RTS	UART2_RTS
						uart_sig_6_sel=9	UART2_CTS	UART2_CTS
						uart_sig_6_sel=10	UART2_TXD	UART2_TXD
						uart_sig_6_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	PIX_DAT8	PIX_DAT8
					10	-	ADC_CH9	ADC_CH9
					11	-	SWGPIO18	SWGPIO18
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	DBI_DB_2	DBI_DB_2
					23	-	DBI_SCL	DBI_SCL
					24	-	DPI_DATA[1]	DPI_DATA[1]
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
53	53	VDDIO_3	DI/DO	PAD_GPIO_19	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_7_sel=0	UART0_RTS	UART0_RTS
						uart_sig_7_sel=1	UART0_CTS	UART0_CTS
						uart_sig_7_sel=2	UART0_TXD	UART0_TXD
						uart_sig_7_sel=3	UART0_RXD	UART0_RXD
						uart_sig_7_sel=4	UART1_RTS	UART1_RTS
						uart_sig_7_sel=5	UART1_CTS	UART1_CTS
						uart_sig_7_sel=6	UART1_TXD	UART1_TXD
						uart_sig_7_sel=7	UART1_RXD	UART1_RXD
						uart_sig_7_sel=8	UART2_RTS	UART2_RTS
						uart_sig_7_sel=9	UART2_CTS	UART2_CTS
						uart_sig_7_sel=10	UART2_TXD	UART2_TXD
						uart_sig_7_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	PIX_DAT9	PIX_DAT9
					10	-	ADC_CH10	ADC_CH10
					11	-	SWGPIO19	SWGPIO19
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	DBI_DB_3	DBI_DB_3
					23	-	DBI_SDA	DBI_SDA
					24	-	DPI_DATA[2]	DPI_DATA[2]
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
54	54	VDDIO_3	DI/DO	PAD_GPIO_20	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_8_sel=0	UART0_RTS	UART0_RTS
						uart_sig_8_sel=1	UART0_CTS	UART0_CTS
						uart_sig_8_sel=2	UART0_TXD	UART0_TXD
						uart_sig_8_sel=3	UART0_RXD	UART0_RXD
						uart_sig_8_sel=4	UART1_RTS	UART1_RTS
						uart_sig_8_sel=5	UART1_CTS	UART1_CTS
						uart_sig_8_sel=6	UART1_TXD	UART1_TXD
						uart_sig_8_sel=7	UART1_RXD	UART1_RXD
						uart_sig_8_sel=8	UART2_RTS	UART2_RTS
						uart_sig_8_sel=9	UART2_CTS	UART2_CTS
						uart_sig_8_sel=10	UART2_TXD	UART2_TXD
						uart_sig_8_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	PIX_DAT10	PIX_DAT10
					10	-	-	-
					11	-	SWGPIO20	SWGPIO20
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	DBI_DB_4	DBI_DB_4
					23	-	DBI_CSn	DBI_CSn
					24	-	DPI_DATA[3]	DPI_DATA[3]
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
55	55	VDDIO_3	DI/DO	PAD_GPIO_21	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_9_sel=0	UART0_RTS	UART0_RTS
						uart_sig_9_sel=1	UART0_CTS	UART0_CTS
						uart_sig_9_sel=2	UART0_TXD	UART0_TXD
						uart_sig_9_sel=3	UART0_RXD	UART0_RXD
						uart_sig_9_sel=4	UART1_RTS	UART1_RTS
						uart_sig_9_sel=5	UART1_CTS	UART1_CTS
						uart_sig_9_sel=6	UART1_TXD	UART1_TXD
						uart_sig_9_sel=7	UART1_RXD	UART1_RXD
						uart_sig_9_sel=8	UART2_RTS	UART2_RTS
						uart_sig_9_sel=9	UART2_CTS	UART2_CTS
						uart_sig_9_sel=10	UART2_TXD	UART2_TXD
						uart_sig_9_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	PIX_DAT11	PIX_DAT11
					10	-	-	-
					11	-	SWGPIO21	SWGPIO21
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	DBI_DB_5	DBI_DB_5
					23	-	DBI_DCn	DBI_DCn
					24	-	DPI_DATA[4]	DPI_DATA[4]
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
56	56	VDDIO_3	DI/DO	PAD_GPIO_22	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_10_sel=0	UART0_RTS	UART0_RTS
						uart_sig_10_sel=1	UART0_CTS	UART0_CTS
						uart_sig_10_sel=2	UART0_TXD	UART0_TXD
						uart_sig_10_sel=3	UART0_RXD	UART0_RXD
						uart_sig_10_sel=4	UART1_RTS	UART1_RTS
						uart_sig_10_sel=5	UART1_CTS	UART1_CTS
						uart_sig_10_sel=6	UART1_TXD	UART1_TXD
						uart_sig_10_sel=7	UART1_RXD	UART1_RXD
						uart_sig_10_sel=8	UART2_RTS	UART2_RTS
						uart_sig_10_sel=9	UART2_CTS	UART2_CTS
						uart_sig_10_sel=10	UART2_TXD	UART2_TXD
						uart_sig_10_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	CAM_HSYNC	CAM_HSYNC
					10	-	-	-
					11	-	SWGPIO22	SWGPIO22
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	DBI_DB_6	DBI_DB_6
					23	-	DBI_SCL	DBI_SCL
					24	-	DPI_DATA[5]	DPI_DATA[5]
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
57	57	VDDIO_3	DI/DO	PAD_GPIO_23	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_11_sel=0	UART0_RTS	UART0_RTS
						uart_sig_11_sel=1	UART0_CTS	UART0_CTS
						uart_sig_11_sel=2	UART0_TXD	UART0_TXD
						uart_sig_11_sel=3	UART0_RXD	UART0_RXD
						uart_sig_11_sel=4	UART1_RTS	UART1_RTS
						uart_sig_11_sel=5	UART1_CTS	UART1_CTS
						uart_sig_11_sel=6	UART1_TXD	UART1_TXD
						uart_sig_11_sel=7	UART1_RXD	UART1_RXD
						uart_sig_11_sel=8	UART2_RTS	UART2_RTS
						uart_sig_11_sel=9	UART2_CTS	UART2_CTS
						uart_sig_11_sel=10	UART2_TXD	UART2_TXD
						uart_sig_11_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	CAM_VSYNC	CAM_VSYNC
					10	-	-	-
					11	-	SWGPIO23	SWGPIO23
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	DBI_DB_7	DBI_DB_7
					23	-	DBI_SDA	DBI_SDA
					24	-	DPI_DATA[6]	DPI_DATA[6]
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO
58	58	-	Power	VDDIO3	-	-	VDDIO3	GPIO16~23 and integrated LDO power input, 1.8V (connected to the third pin VDD18_OUT)/3.3V
59	59	-	Power	AVDD12	-	-	AVDD12	Integrated LDO output, on-chip pSRAM power supply, 1.2V,connected to decoupling capacitors
60	60	-	Power	AVDD12	-	-	AVDD12	Integrated LDO output, on-chip pSRAM power supply, 1.2V,connected to decoupling capacitors
61	61	AVDD12_INT (1.2V)	Analog	CSI_DN<1>	-	-	CSI_DN<1>	MIPI CSI data LANE1 differential input-
62	62	AVDD12_INT (1.2V)	Analog	CSI_DP<1>	-	-	CSI_DP<1>	MIPI CSI data LANE1 differential input+
63	63	AVDD12_INT (1.2V)	Analog	CSI_CLK_DN	-	-	CSI_CLK_DN	MIPI CSI clock LANE differential input-
64	64	AVDD12_INT (1.2V)	Analog	CSI_CLK_DP	-	-	CSI_CLK_DP	MIPI CSI clock LANE differential input+
65	65	AVDD12_INT (1.2V)	Analog	CSI_DN<0>	-	-	CSI_DN<0>	MIPI CSI data LANE0 differential input -
66	66	AVDD12_INT (1.2V)	Analog	CSI_DP<0>	-	-	CSI_DP<0>	MIPI CSI data LANE0 differential input+
-	67	AVDD12_INT (1.2V)	Analog	DSI_DN<0>	-	-	DSI_DN<0>	MIPI DSI data LANE0 differential output-

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	68	AVDD12_INT (1.2V)	Analog	DSI_DP<0>	-	-	DSI_DP<0>	MIPI DSI data LANE0 differential output+
-	69	AVDD12_INT (1.2V)	Analog	DSI_DN<1>	-	-	DSI_DN<1>	MIPI DSI data LANE1 differential output-
-	70	AVDD12_INT (1.2V)	Analog	DSI_DP<1>	-	-	DSI_DP<1>	MIPI DSI data LANE1 differential output+
-	71	AVDD12_INT (1.2V)	Analog	DSI_CLK_DN	-	-	DSI_CLK_DN	MIPI DSI clock LANE differential output-
-	72	AVDD12_INT (1.2V)	Analog	DSI_CLK_DP	-	-	DSI_CLK_DP	MIPI DSI clock LANE differential output+
-	73	AVDD12_INT (1.2V)	Analog	DSI_DN<2>	-	-	DSI_DN<2>	MIPI DSI data LANE2 differential output-
-	74	AVDD12_INT (1.2V)	Analog	DSI_DP<2>	-	-	DSI_DP<2>	MIPI DSI data LANE2 differential output+
-	75	AVDD12_INT (1.2V)	Analog	DSI_DN<3>	-	-	DSI_DN<3>	MIPI DSI data LANE3 differential output-
-	76	AVDD12_INT (1.2V)	Analog	DSI_DP<3>	-	-	DSI_DP<3>	MIPI DSI data LANE2 differential output+
67	-	VDDIO_4	DI/DO	PAD_GPIO_24	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
						uart_sig_0_sel=4	UART1_RTS	UART1_RTS
						uart_sig_0_sel=5	UART1_CTS	UART1_CTS
						uart_sig_0_sel=6	UART1_TXD	UART1_TXD
						uart_sig_0_sel=7	UART1_RXD	UART1_RXD
						uart_sig_0_sel=8	UART2_RTS	UART2_RTS
						uart_sig_0_sel=9	UART2_CTS	UART2_CTS
						uart_sig_0_sel=10	UART2_TXD	UART2_TXD
						uart_sig_0_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_REF_CLK	RMII_REF_CLK
					9	-	DVP_CLK	DVP_CLK
					10	-	-	-
					11	-	SWGPIO24	SWGPIO24
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CSn	DBI_CSn
					24	-	DPI_DATA[7]	DPI_DATA[7]
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
68	-	VDDIO_4	DI/DO	PAD_GPIO_25	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
						uart_sig_1_sel=4	UART1_RTS	UART1_RTS
						uart_sig_1_sel=5	UART1_CTS	UART1_CTS
						uart_sig_1_sel=6	UART1_TXD	UART1_TXD
						uart_sig_1_sel=7	UART1_RXD	UART1_RXD
						uart_sig_1_sel=8	UART2_RTS	UART2_RTS
						uart_sig_1_sel=9	UART2_CTS	UART2_CTS
						uart_sig_1_sel=10	UART2_TXD	UART2_TXD
						uart_sig_1_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_TXD[0]	RMII_TXD[0]
					9	-	PIX_DAT0	PIX_DAT0
					10	-	-	-
					11	-	SWGPIO25	SWGPIO25
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	DPI_DATA[8]	DPI_DATA[8]
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
69	-	VDDIO_4	DI/DO	PAD_GPIO_26	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
						uart_sig_2_sel=4	UART1_RTS	UART1_RTS
						uart_sig_2_sel=5	UART1_CTS	UART1_CTS
						uart_sig_2_sel=6	UART1_TXD	UART1_TXD
						uart_sig_2_sel=7	UART1_RXD	UART1_RXD
						uart_sig_2_sel=8	UART2_RTS	UART2_RTS
						uart_sig_2_sel=9	UART2_CTS	UART2_CTS
						uart_sig_2_sel=10	UART2_TXD	UART2_TXD
						uart_sig_2_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_TXD[1]	RMII_TXD[1]
					9	-	PIX_DAT1	PIX_DAT1
					10	-	-	-
					11	-	SWGPIO26	SWGPIO26
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	DPI_DATA[9]	DPI_DATA[9]
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
70	-	VDDIO_4	DI/DO	PAD_GPIO_27	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
						uart_sig_3_sel=4	UART1_RTS	UART1_RTS
						uart_sig_3_sel=5	UART1_CTS	UART1_CTS
						uart_sig_3_sel=6	UART1_TXD	UART1_TXD
						uart_sig_3_sel=7	UART1_RXD	UART1_RXD
						uart_sig_3_sel=8	UART2_RTS	UART2_RTS
						uart_sig_3_sel=9	UART2_CTS	UART2_CTS
						uart_sig_3_sel=10	UART2_TXD	UART2_TXD
						uart_sig_3_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_RXD[0]	RMII_RXD[0]
					9	-	PIX_DAT2	PIX_DAT2
					10	-	-	-
					11	-	SWGPIO27	SWGPIO27
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	DPI_DATA[10]	DPI_DATA[10]
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
71	-	VDDIO_4	DI/DO	PAD_GPIO_28	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_4_sel=0	UART0_RTS	UART0_RTS
						uart_sig_4_sel=1	UART0_CTS	UART0_CTS
						uart_sig_4_sel=2	UART0_TXD	UART0_TXD
						uart_sig_4_sel=3	UART0_RXD	UART0_RXD
						uart_sig_4_sel=4	UART1_RTS	UART1_RTS
						uart_sig_4_sel=5	UART1_CTS	UART1_CTS
						uart_sig_4_sel=6	UART1_TXD	UART1_TXD
						uart_sig_4_sel=7	UART1_RXD	UART1_RXD
						uart_sig_4_sel=8	UART2_RTS	UART2_RTS
						uart_sig_4_sel=9	UART2_CTS	UART2_CTS
						uart_sig_4_sel=10	UART2_TXD	UART2_TXD
						uart_sig_4_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_RXD[1]	RMII_RXD[1]
					9	-	PIX_DAT3	PIX_DAT3
					10	-	-	-
					11	-	SWGPIO28	SWGPIO28
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CSn	DBI_CSn
					24	-	DPI_DATA[11]	DPI_DATA[11]
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
72	-	VDDIO_4	DI/DO	PAD_GPIO_29	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_5_sel=0	UART0_RTS	UART0_RTS
						uart_sig_5_sel=1	UART0_CTS	UART0_CTS
						uart_sig_5_sel=2	UART0_TXD	UART0_TXD
						uart_sig_5_sel=3	UART0_RXD	UART0_RXD
						uart_sig_5_sel=4	UART1_RTS	UART1_RTS
						uart_sig_5_sel=5	UART1_CTS	UART1_CTS
						uart_sig_5_sel=6	UART1_TXD	UART1_TXD
						uart_sig_5_sel=7	UART1_RXD	UART1_RXD
						uart_sig_5_sel=8	UART2_RTS	UART2_RTS
						uart_sig_5_sel=9	UART2_CTS	UART2_CTS
						uart_sig_5_sel=10	UART2_TXD	UART2_TXD
						uart_sig_5_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_RXERR	RMII_RXERR
					9	-	PIX_DAT4	PIX_DAT4
					10	-	-	-
					11	-	SWGPIO29	SWGPIO29
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	DPI_DATA[12]	DPI_DATA[12]
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
73	-	VDDIO_4	DI/DO	PAD_GPIO_30	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_6_sel=0	UART0_RTS	UART0_RTS
						uart_sig_6_sel=1	UART0_CTS	UART0_CTS
						uart_sig_6_sel=2	UART0_TXD	UART0_TXD
						uart_sig_6_sel=3	UART0_RXD	UART0_RXD
						uart_sig_6_sel=4	UART1_RTS	UART1_RTS
						uart_sig_6_sel=5	UART1_CTS	UART1_CTS
						uart_sig_6_sel=6	UART1_TXD	UART1_TXD
						uart_sig_6_sel=7	UART1_RXD	UART1_RXD
						uart_sig_6_sel=8	UART2_RTS	UART2_RTS
						uart_sig_6_sel=9	UART2_CTS	UART2_CTS
						uart_sig_6_sel=10	UART2_TXD	UART2_TXD
						uart_sig_6_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_TX_EN	RMII_TX_EN
					9	-	PIX_DAT5	PIX_DAT5
					10	-	-	-
					11	-	SWGPIO30	SWGPIO30
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	DPI_DATA[13]	DPI_DATA[13]
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
74	-	VDDIO_4	DI/DO	PAD_GPIO_31	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_7_sel=0	UART0_RTS	UART0_RTS
						uart_sig_7_sel=1	UART0_CTS	UART0_CTS
						uart_sig_7_sel=2	UART0_TXD	UART0_TXD
						uart_sig_7_sel=3	UART0_RXD	UART0_RXD
						uart_sig_7_sel=4	UART1_RTS	UART1_RTS
						uart_sig_7_sel=5	UART1_CTS	UART1_CTS
						uart_sig_7_sel=6	UART1_TXD	UART1_TXD
						uart_sig_7_sel=7	UART1_RXD	UART1_RXD
						uart_sig_7_sel=8	UART2_RTS	UART2_RTS
						uart_sig_7_sel=9	UART2_CTS	UART2_CTS
						uart_sig_7_sel=10	UART2_TXD	UART2_TXD
						uart_sig_7_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_RX_DV	RMII_RX_DV
					9	-	PIX_DAT6	PIX_DAT6
					10	-	-	-
					11	-	SWGPIO31	SWGPIO31
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	DPI_DATA[14]	DPI_DATA[14]
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
75	-	VDDIO_4	DI/DO	PAD_GPIO_32	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	-	-
					3	-	I2S_BCLK	I2S_BCLK
					4	-	-	-
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_8_sel=0	UART0_RTS	UART0_RTS
						uart_sig_8_sel=1	UART0_CTS	UART0_CTS
						uart_sig_8_sel=2	UART0_TXD	UART0_TXD
						uart_sig_8_sel=3	UART0_RXD	UART0_RXD
						uart_sig_8_sel=4	UART1_RTS	UART1_RTS
						uart_sig_8_sel=5	UART1_CTS	UART1_CTS
						uart_sig_8_sel=6	UART1_TXD	UART1_TXD
						uart_sig_8_sel=7	UART1_RXD	UART1_RXD
						uart_sig_8_sel=8	UART2_RTS	UART2_RTS
						uart_sig_8_sel=9	UART2_CTS	UART2_CTS
						uart_sig_8_sel=10	UART2_TXD	UART2_TXD
						uart_sig_8_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_MDC	RMII_MDC
					9	-	PIX_DAT7	PIX_DAT7
					10	-	-	-
					11	-	SWGPIO32	SWGPIO32
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0_CH0P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CSn	DBI_CSn
					24	-	DPI_DATA[15]	DPI_DATA[15]
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
76	-	VDDIO_4	DI/DO	PAD_GPIO_33	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	-	-
					3	-	I2S_FS	I2S_FS
					4	-	-	-
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_9_sel=0	UART0_RTS	UART0_RTS
						uart_sig_9_sel=1	UART0_CTS	UART0_CTS
						uart_sig_9_sel=2	UART0_TXD	UART0_TXD
						uart_sig_9_sel=3	UART0_RXD	UART0_RXD
						uart_sig_9_sel=4	UART1_RTS	UART1_RTS
						uart_sig_9_sel=5	UART1_CTS	UART1_CTS
						uart_sig_9_sel=6	UART1_TXD	UART1_TXD
						uart_sig_9_sel=7	UART1_RXD	UART1_RXD
						uart_sig_9_sel=8	UART2_RTS	UART2_RTS
						uart_sig_9_sel=9	UART2_CTS	UART2_CTS
						uart_sig_9_sel=10	UART2_TXD	UART2_TXD
						uart_sig_9_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_MDIO	RMII_MDIO
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO33	SWGPIO33
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0_CH0N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	DPI_DE	DPI_DE
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI
77	77	-	Power	VDDIO4	-	-	VDDIO4	VDDIO4
78	78	-	Power	VDD18_FLASH	-	-	VDD18_FLASH	VDD18_FLASH

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
79	79	VDDIO_4	DI/DO	PAD_GPIO_34	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	SF2_CLK	SF2_CLK
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_10_sel=0	UART0_RTS	UART0_RTS
						uart_sig_10_sel=1	UART0_CTS	UART0_CTS
						uart_sig_10_sel=2	UART0_TXD	UART0_TXD
						uart_sig_10_sel=3	UART0_RXD	UART0_RXD
						uart_sig_10_sel=4	UART1_RTS	UART1_RTS
						uart_sig_10_sel=5	UART1_CTS	UART1_CTS
						uart_sig_10_sel=6	UART1_TXD	UART1_TXD
						uart_sig_10_sel=7	UART1_RXD	UART1_RXD
						uart_sig_10_sel=8	UART2_RTS	UART2_RTS
						uart_sig_10_sel=9	UART2_CTS	UART2_CTS
						uart_sig_10_sel=10	UART2_TXD	UART2_TXD
						uart_sig_10_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_RXERR	RMII_RXERR
					9	-	-	-
					10	-	ADC_CH11	ADC_CH11
					11	-	SWGPIO34	SWGPIO34
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0_CH1P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
80	80	VDDIO_4	DI/DO	PAD_GPIO_35	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	SF2_CS	SF2_CS
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_11_sel=0	UART0_RTS	UART0_RTS
						uart_sig_11_sel=1	UART0_CTS	UART0_CTS
						uart_sig_11_sel=2	UART0_TXD	UART0_TXD
						uart_sig_11_sel=3	UART0_RXD	UART0_RXD
						uart_sig_11_sel=4	UART1_RTS	UART1_RTS
						uart_sig_11_sel=5	UART1_CTS	UART1_CTS
						uart_sig_11_sel=6	UART1_TXD	UART1_TXD
						uart_sig_11_sel=7	UART1_RXD	UART1_RXD
						uart_sig_11_sel=8	UART2_RTS	UART2_RTS
						uart_sig_11_sel=9	UART2_CTS	UART2_CTS
						uart_sig_11_sel=10	UART2_TXD	UART2_TXD
						uart_sig_11_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_TX_EN	RMII_TX_EN
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO35	SWGPIO35
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0_CH1N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
81	81	VDDIO_4	DI/DO	PAD_GPIO_36	0	-	-	-
					1	-	SPI_SS	SPI_SS
					2	-	SF2_D0	SF2_D0
					3	-	I2S_BCLK	I2S_BCLK
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
						uart_sig_0_sel=4	UART1_RTS	UART1_RTS
						uart_sig_0_sel=5	UART1_CTS	UART1_CTS
						uart_sig_0_sel=6	UART1_TXD	UART1_TXD
						uart_sig_0_sel=7	UART1_RXD	UART1_RXD
						uart_sig_0_sel=8	UART2_RTS	UART2_RTS
						uart_sig_0_sel=9	UART2_CTS	UART2_CTS
						uart_sig_0_sel=10	UART2_TXD	UART2_TXD
						uart_sig_0_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_RX_DV	RMII_RX_DV
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO36	SWGPIO36
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0_CH0P
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0_CH2P
					17	reg_pwm2_io_sel=0	PWM1_CH0P	PWM1_CH0P
						reg_pwm2_io_sel=1	PWM0_BREAK_EXT	PWM0_BREAK_EXT
					18	-	MM_SPI_SS	MM_SPI_SS
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_TXD	MM_UART_TXD
					22	-	-	-
					23	-	DBI_CSn	DBI_CSn
					24	-	-	-
					26	-	M0_JTAG_TCLK	M0_JTAG_TCLK
					27	-	D0_JTAG_TCK	D0_JTAG_TCK

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
82	82	VDDIO_4	DI/DO	PAD_GPIO_37	0	-	-	-
					1	-	SPI_MOSI	SPI_MOSI
					2	-	SF2_D1	SF2_D1
					3	-	I2S_FS	I2S_FS
					4	-	PDM_1_IN	PDM_1_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
						uart_sig_1_sel=4	UART1_RTS	UART1_RTS
						uart_sig_1_sel=5	UART1_CTS	UART1_CTS
						uart_sig_1_sel=6	UART1_TXD	UART1_TXD
						uart_sig_1_sel=7	UART1_RXD	UART1_RXD
						uart_sig_1_sel=8	UART2_RTS	UART2_RTS
						uart_sig_1_sel=9	UART2_CTS	UART2_CTS
						uart_sig_1_sel=10	UART2_TXD	UART2_TXD
						uart_sig_1_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_MDC	RMII_MDC
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO37	SWGPIO37
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0_CH1P
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0_CH2N
					17	reg_pwm2_io_sel=0	PWM1_CH1P	PWM1_CH1P
						reg_pwm2_io_sel=1	PWM0_CH0P	PWM0_CH0P
					18	-	MM_SPI_MOSI	MM_SPI_MOSI
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_RXD	MM_UART_RXD
					22	-	-	-
					23	-	DBI_DCn	DBI_DCn
					24	-	-	-
					26	-	M0_JTAG_TDI	M0_JTAG_TDI
					27	-	D0_JTAG_TDI	D0_JTAG_TDI

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
83	83	VDDIO_4	DI/DO	PAD_GPIO_38	0	-	-	-
					1	-	SPI_MISO	SPI_MISO
					2	-	SF2_D2	SF2_D2
					3	-	I2S_DI/I2S_RCLK_O	I2S_DI/I2S_RCLK_O
					4	-	PDM_CLK_O	PDM_CLK_O
					5	-	I2C0_SCL	I2C0_SCL
					6	-	I2C1_SCL	I2C1_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
						uart_sig_2_sel=4	UART1_RTS	UART1_RTS
						uart_sig_2_sel=5	UART1_CTS	UART1_CTS
						uart_sig_2_sel=6	UART1_TXD	UART1_TXD
						uart_sig_2_sel=7	UART1_RXD	UART1_RXD
						uart_sig_2_sel=8	UART2_RTS	UART2_RTS
						uart_sig_2_sel=9	UART2_CTS	UART2_CTS
						uart_sig_2_sel=10	UART2_TXD	UART2_TXD
						uart_sig_2_sel=11	UART2_RXD	UART2_RXD
					8	-	RMII_MDIO	RMII_MDIO
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO38	SWGPIO38
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0_CH2P
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0_CH3P
					17	reg_pwm2_io_sel=0	PWM1_CH2P	PWM1_CH2P
						reg_pwm2_io_sel=1	PWM0_CH1P	PWM0_CH1P
					18	-	MM_SPI_MISO	MM_SPI_MISO
					19	-	MM_I2C0_SCL	MM_I2C0_SCL
					20	-	MM_I2C1_SCL	MM_I2C1_SCL
					21	-	MM_UART_RTS	MM_UART_RTS
					22	-	-	-
					23	-	DBI_SCL	DBI_SCL
					24	-	-	-
					26	-	M0_JTAG_TMS	M0_JTAG_TMS
					27	-	D0_JTAG_TMS	D0_JTAG_TMS

Table 3.1: Pin Description(continued)

BL808C	BL808D	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
84	84	VDDIO_4	DI/DO	PAD_GPIO_39	0	-	-	-
					1	-	SPI_SCLK	SPI_SCLK
					2	-	SF2_D3	SF2_D3
					3	-	I2S_DO/I2S_RCLK_O	I2S_DO/I2S_RCLK_O
					4	-	PDM_0_IN	PDM_0_IN
					5	-	I2C0_SDA	I2C0_SDA
					6	-	I2C1_SDA	I2C1_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
						uart_sig_3_sel=4	UART1_RTS	UART1_RTS
						uart_sig_3_sel=5	UART1_CTS	UART1_CTS
						uart_sig_3_sel=6	UART1_TXD	UART1_TXD
						uart_sig_3_sel=7	UART1_RXD	UART1_RXD
						uart_sig_3_sel=8	UART2_RTS	UART2_RTS
						uart_sig_3_sel=9	UART2_CTS	UART2_CTS
						uart_sig_3_sel=10	UART2_TXD	UART2_TXD
						uart_sig_3_sel=11	UART2_RXD	UART2_RXD
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO39	SWGPIO39
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0_CH3P
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0_CH3N
					17	reg_pwm2_io_sel=0	PWM1_CH3P	PWM1_CH3P
						reg_pwm2_io_sel=1	PWM0_CH2P	PWM0_CH2P
					18	-	MM_SPI_SCLK	MM_SPI_SCLK
					19	-	MM_I2C0_SDA	MM_I2C0_SDA
					20	-	MM_I2C1_SDA	MM_I2C1_SDA
					21	-	MM_UART_CTS	MM_UART_CTS
					22	-	-	-
					23	-	DBI_SDA	DBI_SDA
					24	-	-	-
					26	-	M0_JTAG_TDO	M0_JTAG_TDO
					27	-	D0_JTAG_TDO	D0_JTAG_TDO
85	85	-	Power	DCDC11_VOUT	-	-	DCDC11_VOUT	Feedback voltage input, 1.1V
86	86	-	Power	SW_DCDC11	-	-	SW_DCDC11	DCDC switch output, connected to power inductor
87	87	-	Power	VDD33_DCDC11	-	-	VDD33_DCDC11	DCDC power input, 3.3V
88	88	-	Power	VSS_DCDC11	-	-	VSS_DCDC11	DCDC circuit ground pin

[1] This function defaults to SPI_MOSI, which can be converted to SPI_MISO through a register.

4 RF Characteristsic

RF Characteristics of Receiving and Transmitting modes.

Table 4.1: WLAN TX RF characteristics

Mode		Note	Performance @3.3V,25°C			
			Min.	Typ	Max.	Unit
TX power	11b - 1Mbps			21		dBm
	11b - 11Mbps			21		
	11g - 6Mbps			19		
	11g - 54Mbps			18		
	11n - MCS0			19		
	11n - MCS7			17		

Table 4.2: WLAN RX RF characteristics

Mode		Note	Performance @3.3V,25°C			
			Min.	Typ	Max.	Unit
RX sensitivity	11b - 1Mbps			-98		dBm
	11b - 11Mbps			-90		
	11g - 6Mbps			-93		
	11g - 54Mbps			-77		
	11n - MCS0			-93		
	11n - MCS7			-74		

Table 4.3: BLE RX RF characteristics

Mode		Note	Performance @3.3V,25°C			
			Min.	Typ	Max.	Unit
RX sensitivity	1Mbps			-99		dBm
	2Mbps			-97		
	S8 (125Kbps)			-105		
	S2 (500Kbps)			-102		

Table 4.4: BLE TX RF characteristics

Mode	Note	Performance @3.3V,25°C			
		Min.	Typ	Max.	Unit
TX power			10	20	dBm

Table 4.5: BT TX RF characteristics

Mode	Note	Performance @3.3V,25°C			
		Min.	Typ	Max.	Unit
BR output power			10		dBm
EDR output power			8		dBm
Δf1avg	BR 1Mbps		159		kHz
Δf2max			132		
Δf2avg/Δf1avg			0.88		
ω0	EDR 2Mbps	-3		3	kHz
ωi		-12		6	
ωi+ω0		-6		3	
RMS DEVM				5	%
99% DEVM				9	
Peak DEVM				10	
ω0	EDR 3Mbps	-3		3	kHz
ωi		-12		6	
ωi+ω0		-6		3	
RMS DEVM				5	%
99% DEVM				9	
Peak DEVM				10	

Table 4.6: BT RX RF Characteristics

Mode		Note	Performance @3.3V,25℃			
			Min.	Typ	Max.	Unit
Sensitivity	BR 1Mbps	Dirty Off		-94		dBm
Maximum reception level						
Sensitivity	EDR 2Mbps			-95		
Maximum reception level						
Sensitivity	EDR 3Mbps			-89		
Maximum reception level						

5 Audio characteristic

5.1 Electrical characteristics

Table 5.1: Analog-to-Digital converter electrical characteristics

At 25°C, AVDD25_CODEC= 2.5 V, f_S= 48kHz, 20-bit audio data (unless otherwise noted)						
Parameter		Conditions	Min.	Typ	Max.	Unit
AUDIO ADC	Input signal full-scale level	Differential input，0 dB PGA gain		1.8		Vrms
		Single-ended input，0 dB PGA gain		0.9	1.4	
	Input common-mode voltage	differential/Single-ended input		1.23		
SNR	Signal-to-noise ratio, A-weighted	f_S= 48 kHz, 0 dB PGA gain, 1kHz full-scale sine-wave input		103		dB
DR	Dynamic range, A-weighted	f_S= 48 kHz, 0 dB PGA gain, 1kHz -60dB sine-wave input		103		
THD	Total harmonic distortion	f_S= 48 kHz, 0 dB PGA gain, 1kHz -5dB sine-wave input		-95		
PSRR	Power supply rejection ratio	234 Hz, 100 mVPP on AVDD, single-ended input		-		
		234 Hz, 100 mVPP on AVDD, differential input		-		
Crosstalk	ADC channel separation	0 dB PGA gain, 1kHz full-scale sine-wave input	130			
		36dB PGA gain, 1kHz full-scale sine-wave input	100			
Freq. Response		-5dB 20Hz~24kHz sine-wave input		0.25		
ADC programmable analogue amplifier gain range		Analogue gain resolution = 3dB	0		42	
ADC programmable digital gain range		Digital gain resolution = 0.5dB	-95.5		31.5	

Table 5.1: Analog-to-Digital converter electrical characteristics(continued)

At 25°C, AVDD25_CODEC= 2.5 V, f_S= 48kHz, 20-bit audio data (unless otherwise noted)						
Parameter		Conditions	Min.	Typ	Max.	Unit
Input resistance		Analogue gain 0dB		16		kΩ
		Analogue gain 6dB~42dB	160		640	
Input capacitance				10		pF
MICROPHONE BIAS	Bias voltage	Programmable settings	1.8		2.5	V
	Current sourcing	2.5V setting, load = 1 KΩ		2.2		mA
	Integrated noise	BW = 20 Hz to 20 kHz, A-weighted, 1μF capacitor between MICBIAS and AGND		1.5		μV rms

Table 5.2: Digital-to-Analog converter electrical characteristics

At 25°C, AVDD25_CODEC= 2.5 V, f_S= 48kHz, 20-bit audio data (unless otherwise noted)						
Parameter		Conditions	Min.	Typ	Max.	Unit
AUDIO DAC	Input signal full-scale level	Differential output，0 dB line-out gain		1.68		Vrms
		Single-ended output，0 dB line-out gain		0.84		
	Input common-mode voltage			1.23		
SNR	Signal-to-noise ratio, A-W without Noise Gating	f_S= 48 kHz, 1kHz full-scale sine-wave output		104		dB
	Signal-to-noise ratio, A-W with Noise Gating	f_S= 48 kHz, 1kHz full-scale sine-wave output		112		
DR	Dynamic range, A-weighted	f_S= 48 kHz, 1kHz -60dB sine-wave output		104		
THD	Total harmonic distortion	f_S= 48 kHz, 1kHz -5dB sine-wave output		-89		
PSRR	Power supply rejection ratio	234 Hz, 100 mVPP on AVDD, single-ended output		-		
		234 Hz, 100 mVPP on AVDD, differential output		-		
Noise Floor		A-weighted without Noise Gating		10		μV rms
Noise Floor		A-weighted with Noise Gating		4.3		
Crosstalk	DAC channel separation	1kHz full-scale sine-wave output	130			dB
Freq. Response		-5dB 20Hz~24kHz sine-wave input		0.25		
DC offset		P/N output DC offset		0.5		mV

Table 5.2: Digital-to-Analog converter electrical characteristics(continued)

At 25°C, AVDD25_CODEC= 2.5 V, f_S= 48kHz, 20-bit audio data (unless otherwise noted)					
Parameter	Conditions	Min.	Typ	Max.	Unit
DAC programmable analogue amplifier gain range	Analogue gain resolution = 3dB	-21		0	dB
DAC programmable digital gain range	Digital gain resolution = 0.5dB	-95.5		31.5	

6 Power Consumption

Power Consumption of each power mode.

Table 6.1: Power Modes & Whole-chip Current

Mode		Conditions	Performance @25℃			
			Min.	Typ	Max.	Unit
RX		3.3V，RF only		13		mA
TX	11b - 11Mbps @21dBm	3.3V，RF only Duty 99%		295		
HBN	HBN0	Vdd11_aon = 0.9V		7.9		uA
		Vdd11_aon = 1.1V		14.3		
PDS	PDS7	Vdd11_aon = 0.9V		70.8		
		Vdd11_aon = 1.1V		121.7		
Shut-down				<0.5		

7 Electrical Specifications

7.1 Absolute Maximum Rating

Table 7.1: Absolute Maximum Rating

Pin Name	Min.	Max.	Unit
VDD33_DCDC18, VDD33_DCDC11	-0.3	3.63	V
VDD33(USB)	-0.3	3.63	V
VDDIO1	-0.3	3.63	V
VDDIO2	-0.3	3.63	V
VDDIO3	-0.3	3.63	V
VDDIO4	-0.3	3.63	V
VDD33_RF	-0.3	3.63	V
AVDD33_CODEC	-0.3	3.63	V

7.2 Operating Condition

7.2.1 Power characteristics

Table 7.2: Recommended Power Operating Range

Pin Name	Min.	Typ	Max.	Unit
VDD33_DCDC18, VDD33_DCDC11	3	3.3	3.63	V
VDD33(USB)	3	3.3	3.63	V
VDDIO1	3.0/1.62	3.3/1.8	3.63/1.98	V
VDDIO2	3	3.3	3.63	V

Table 7.2: Recommended Power Operating Range(continued)

Pin Name	Min.	Typ	Max.	Unit
VDDIO3	3.0/1.62	3.3/1.8	3.63/1.98	V
VDDIO4	3.0/1.62	3.3/1.8	3.63/1.98	V
VDD33_RF	3	3.3	3.63	V
AVDD33_CODEC	3	3.3	3.63	V

7.2.2 IO DC characteristics

Table 7.3: IO DC characteristics

Symbol	Description	Conditions	Min.	Typ	Max.	Unit
VOH	Output voltage high		0.8 * VIO			V
VOL	Output voltage low				0.1 * VIO	V
VIH	Input voltage high		0.7 * VIO		VIO + 0.3	V
VIL	Input voltage low		-0.3		0.3 * VIO	V

7.2.3 Power-on sequence

In order to ensure normal power-on startup, the power, reset and Bootstrap pins need to meet the corresponding timing requirements.

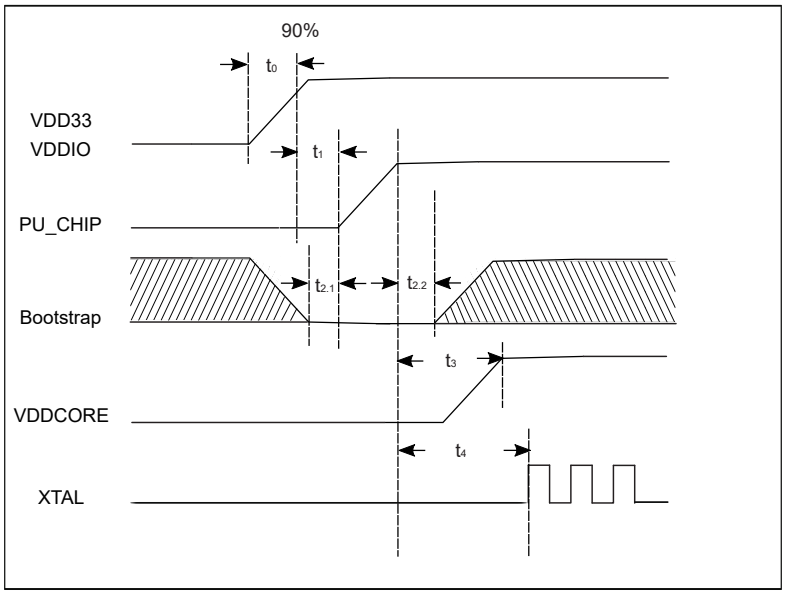

Fig. 7.1: Power-on sequence

Table 7.4: Power-on sequence parameters

Parameters	Description	Min.(ms)	Typ(ms)	Max.(ms)
t_0	Rise time for supply voltage to reach 90%			2
t_1	Delay time before power rises until PU_CHIP is pulled high	0.1		
$t_{2.1}$	Bootstrap pin [1] level setup time before PU_CHIP is pulled high	0		
$t_{2.2}$	Hold time of Bootstrap pin level after PU_CHIP is pulled high	2		
t_3	The time that PU_CHIP is pulled high to VDDCORE output		2	
t_4	The time when PU_CHIP is pulled high until XTAL starts to vibrate		2	

[1] Bootstrap pin is GPIO39.

7.2.4 Temperature sensor characteristics

Table 7.5: Recommended Temperature Operating Range

Item		Min.	Max.	Unit
Temperature	Main Die	-40	85	°C
	Multi-Die SiP	-40	85	

7.2.5 General operating conditions

Table 7.6: General Operating Conditions

Item	Description	Min.	Typ	Max.	Unit
FCPU	CPU clock frequency (M0)			320	MHz
	CPU clock frequency (D0)			480	

8 Product use

8.1 Moisture Sensitivity Level(MSL)

The moisture sensitivity level of the chip is: MSL3. After the vacuum package is opened, it needs to be used up within 168 hours (7 days) at ≤30°C/60%RH, otherwise it needs to be baked and put online.

For baking temperature and time, please refer to IPC/JEDECJ-STD-033B01.

Table 8.1: Reference Conditions for Drying Mounted or Unmounted SMD Packages (User Bake: Floor life begins counting at time = 0 after bake)

Package Body	Level	Bake @ 125°C		Bake @ 90°C ≤5% RH		Bake @ 40°C ≤5% RH	
		Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h
Thickness ≤1.4 mm	2	5 hours	3 hours	17 hours	11 hours	8 days	5 days
	2a	7 hours	5 hours	23 hours	13 hours	9 days	7 days
	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days
	4	11 hours	7 hours	37 hours	23 hours	15 days	9 days
	5	12 hours	7 hours	41 hours	24 hours	17 days	10 days
	5a	16 hours	10 hours	54 hours	24 hours	22 days	10 days

8.2 Electro-Static discharge（ESD）

- Human Body Model(HBM): 2000V
- Charged-Device Model(CDM): 500V

8.3 Reflow Profile

For details, please refer to IPC/JEDEC J-STD-020E.

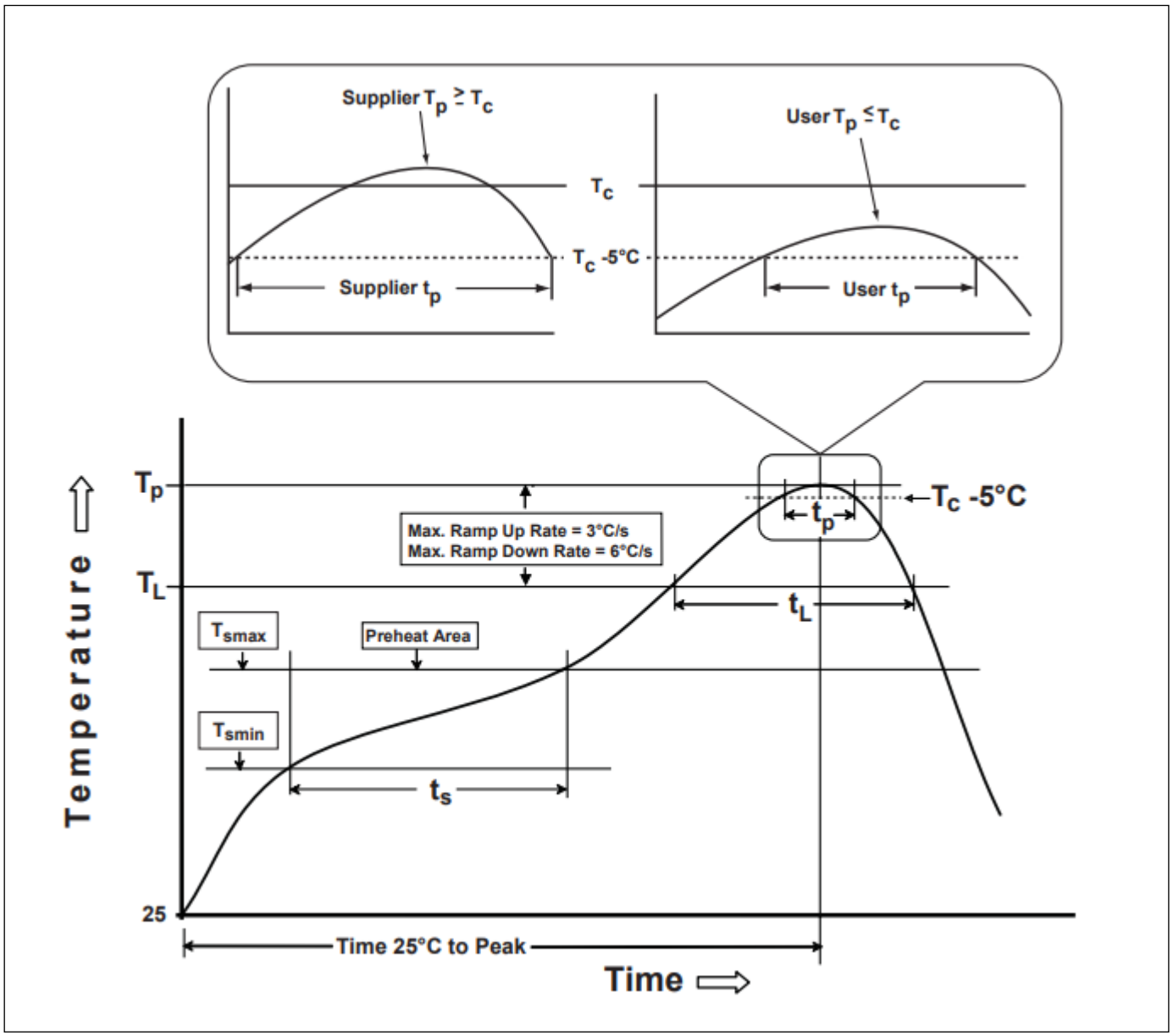

Fig. 8.1: Classification Profile (Not to scale)

Table 8.2: Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	240 °C+0/-5 °C	250 °C+0/-5 °C
Time (t_p)* within 5 °C of the specified classification temperature (T_c)	10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)	6 °C/second max	6 °C/second max
Time 25 °C to peak temperature	6 minutes max	8 minutes max
- Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.		

9 Reference Design

10 Package Information(QFN88)

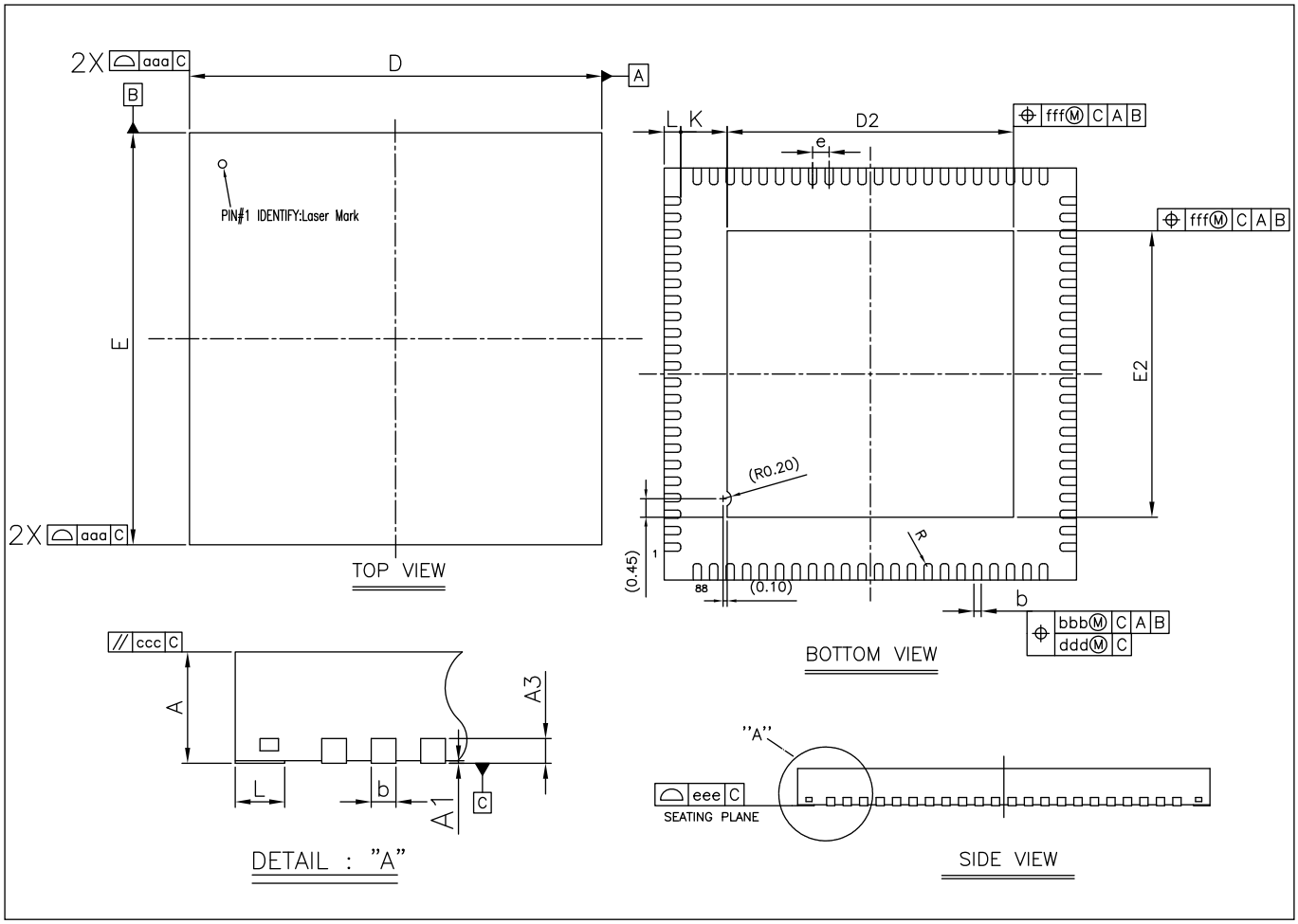

Fig. 10.1: QFN88 Package drawing

Table 10.1: QFN88 Size Description

SYMBOL	UNIT OF MEASURE = MILLIMETER			UNIT OF MEASURE = INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.90	0.95	0.033	0.035	0.037
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D2	6.85	6.95/6.40	7.05	0.270	0.274	0.278
E2	6.85	6.95/6.40	7.05	0.270	0.274	0.278
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	-	-	0.008	-	-
R	0.075	-	0.125	0.003	-	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

Note: Control size: millimeter

11 Top Marking Definition

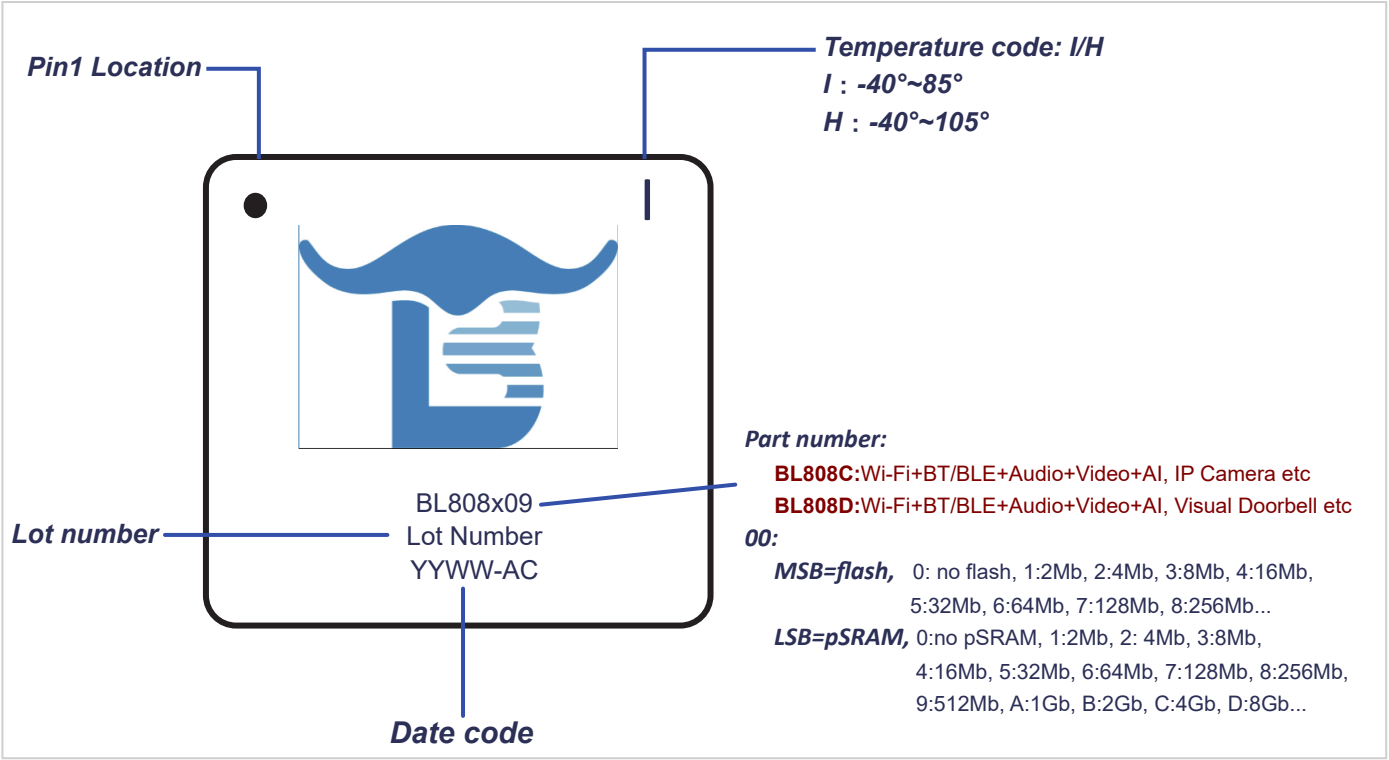

Fig. 11.1: Top Marking Definition

12 Ordering Information

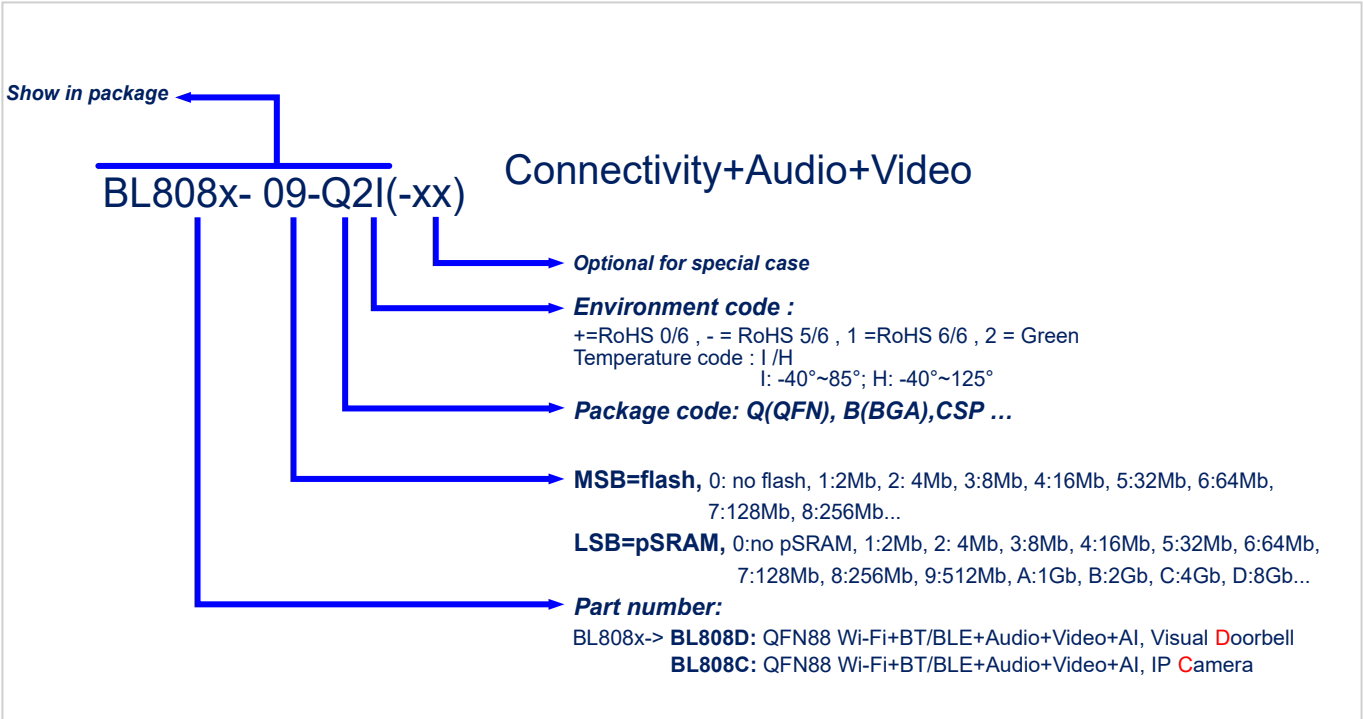

Table 12.1: Part Order Options

Product No.	Description
BL808D-09-Q2I	Wi-Fi + BT/BLE + Audio + Video + AI, QFN88, no flash, 512Mb pSRAM, Doorbell
BL808C-09-Q2I	Wi-Fi + BT/BLE + Audio + Video + AI, QFN88, no flash, 512Mb pSRAM, IPC

13 Revision history

Table 13.1: Document revision history

Date	Revision	Changes
2021/12/17	0.9	Initial release
2022/1/14	0.95	Add audio characteristics and RF characteristics data
2022/2/10	0.96	Add BLE RF characteristics and electrical characteristics
2022/3/3	0.97	Add BT RF characteristics and Bootstrap pin description
2022/3/17	0.98	Add power consumption data
2022/5/12	0.99	Modify memory map and add EMAC timing description
2022/6/9	1.0	Add pinmux function 26 and 27
2022/8/17	1.1	Add spi and uart function descriptions, and add temperature descriptions