

|      |      |      |      |      |      |      |      |      |                   |                  |                   |                  |             |             |               |               |
|------|------|------|------|------|------|------|------|------|-------------------|------------------|-------------------|------------------|-------------|-------------|---------------|---------------|
| RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD              | RSVD             | RSVD              | RSVD             | RSVD        | RSVD        | RSVD          |               |
| 31   | 30   | 29   | 28   | 27   | 26   | 25   | 24   | 23   | 22                | 21               | 20                | 19               | 18          | 17          | 16            |               |
| 15   | 14   | 13   | 12   | 11   | 10   | 9    | 8    | 7    | 6                 | 5                | 4                 | 3                | 2           | 1           | 0             |               |
| RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | rx_fifo_underflow | rx_fifo_overflow | tx_fifo_underflow | tx_fifo_overflow | rx_fifo_clr | tx_fifo_clr | i2c_dma_rx_en | i2c_dma_tx_en |