External 5V

J1

D1

TP38 TP39 TP40 TP41

GND

USB-C

J5

R1 5k1

R3 5k1

R68 0

USB_CONN_P

USB_CONN_N

+5VUSB

GND

Routing note:
- REV2: by USB standard, USB signals must be 90Ω differential to each other, and 45Ω each to Signal Ground

Current Input

J3

Current_In

JP1

J4

Vcm_Buf

Routing note:
- Test Point should be directly in the track
- Place solder bridge as close as possible to the junction

Routing note:
- REV2: Footprints of both the coax and triax MUST BE on top of each other (so that the user can choose themself which one they want to use)
- Add Vcm_Buf shield around Current_In as well as a Vcm_Buf plane below it
- Input area should be as short and small as possible

Power Supply & USB

+5VEXT
+5VUSB
+5V
+3V3A
+3V3D
+2V5
+1V2
FPGA_TXD
FPGA_RXD
FPGA_PROG{SCK MOSI MISO SS_B CDONE CRESET}
USB_CONN_N
USB_CONN_P
3V3_REFD
3V_REFD
MCU_TXD
MCU_RXD
DTRD
GND

File: Power Supply.kicad_sch

ACCURATE ASIC

+3V3D
+3V3A
3V3_REF
3V_REF
Comp[1..4]
Current_In
ACCURATE_RESET
FPGA_CLK
GND
FPGA_SCL
FPGA_SDA
ADC_Ready
MCU_SCL
MCU_SDA
Vcm_Buf

File: ACCURATE ASIC.kicad_sch

FPGA

+1V2
+2V5
+3V3A
+3V3D
FPGA_FTDI_UART_TX
FPGA_FTDI_UART_RX
FPGA_PROG{SCK MOSI MISO SS_B CDONE CRESET}
FPGA_MCU_UART_TX
FPGA_MCU_UART_RX
ACCURATE_RESET
FPGA_CLK
ADC_Ready
FPGA_SDA
FPGA_SCL
Enable{High, Medium, Low}
Comp[1..4]
GND

File: FPGA.kicad_sch

MCU

+3V3D
+5V
MCU_TX
MCU_RX
DTR
MCU_SDA
MCU_SCL
MCU_FPGA_RX
MCU_FPGA_TX
GND

File: MCU.kicad_sch

Display

+3V3D
MCU_SDA
MCU_SCL
GND

File: Display.kicad_sch

Project/Equipment: **CROME**

KiCad E.D.A. 8.99.0-2230-g1cc11bc589

Document

RP-IL

ACCURATE 2 Evaluation Board

/

Designer	
Drawn by	Liverud, Consani
Checked by	
Last Mod.	2025-01-20
File: Accurate_Eval.kicad_sch	
Sheet: 1 of 6	

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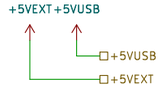
CH-1211 Genève 23 – Switzerland

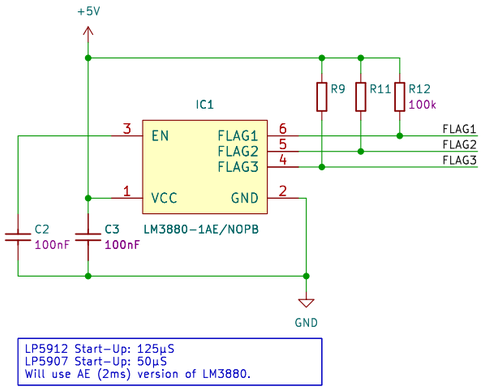
A3 A

Power Ports

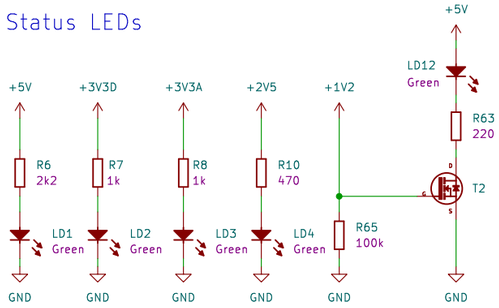


Inputs

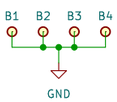
PSU Sequencer



Status LEDs

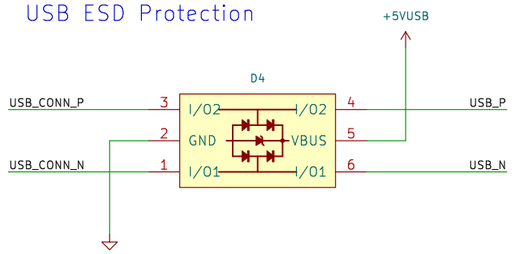


Mounting Holes

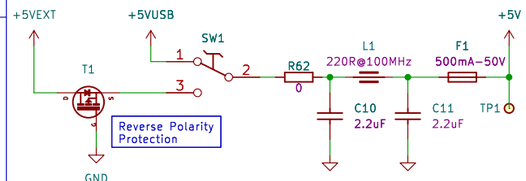


Fiducial Targets

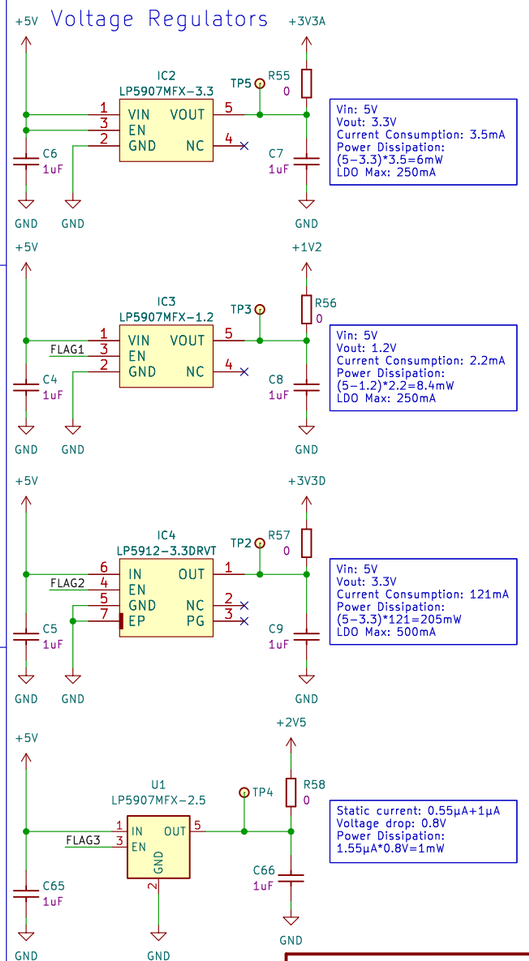
USB ESD Protection



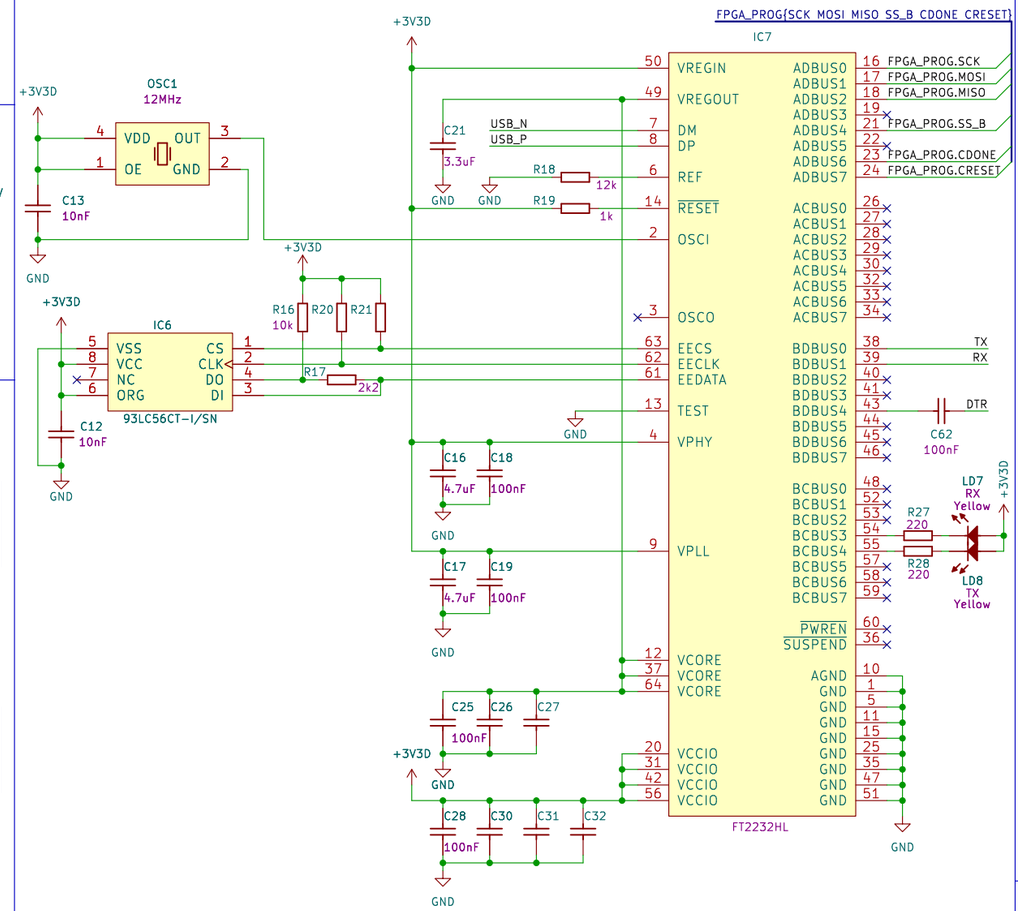
Input Filtering



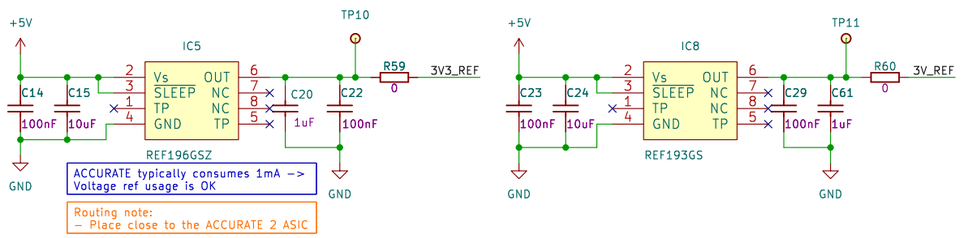
Voltage Regulators



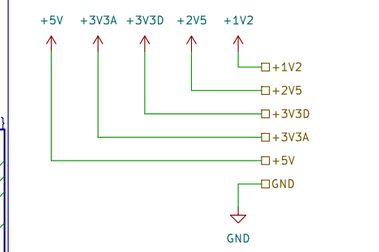
USB-To-Serial

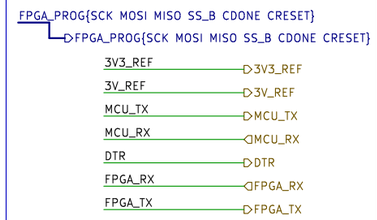


Voltage References

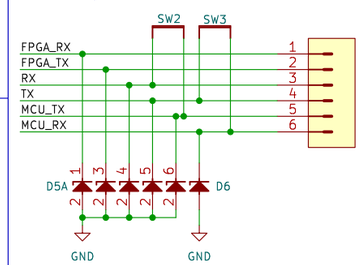


Outputs





FPGA/MCU UART Header



Project/Equipment: **CROME**

KiCad E.D.A. 8.99.0-2230-g1cc11bc589

Document

RP-IL

ACCURATE 2 Evaluation Board

/Power Supply & USB/

Designer	
Drawn by	Liverud, Consani
Checked by	
Last Mod.	2025-01-20
File: Power Supply.kicad_sch	
Sheet: 2 of 6	

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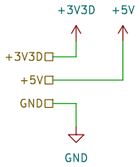
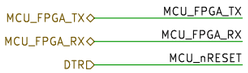
A3 A

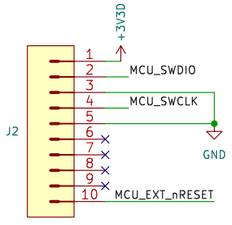
Power Ports

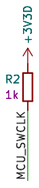


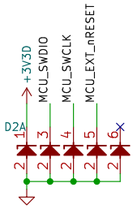
Inputs



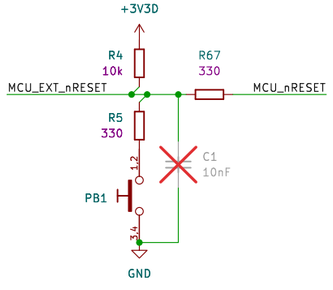
Programming Header





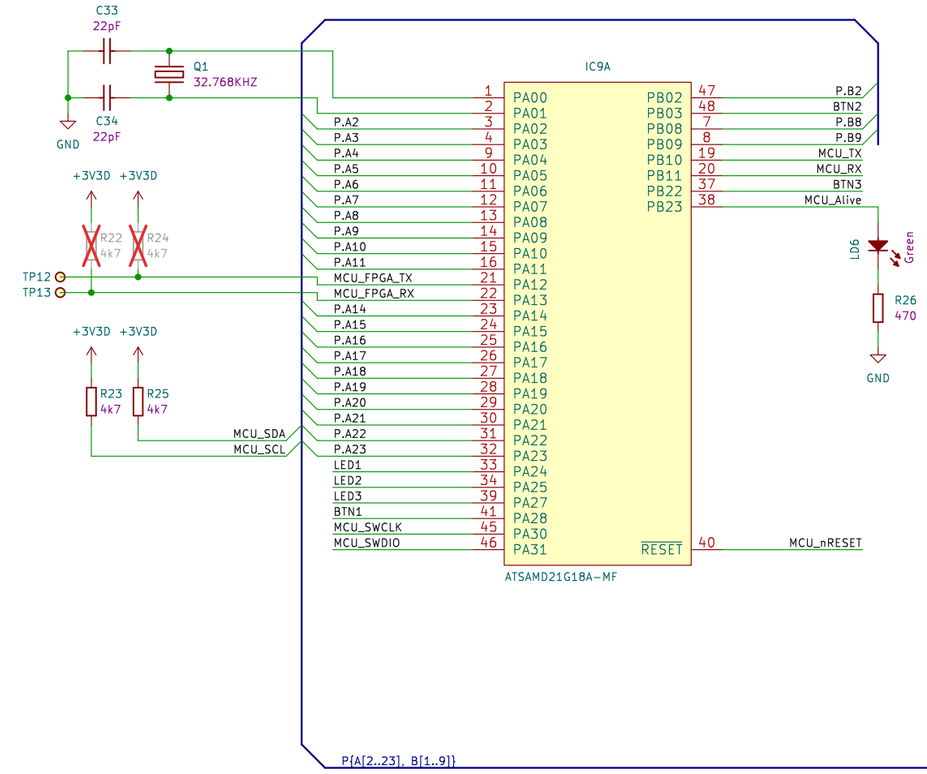


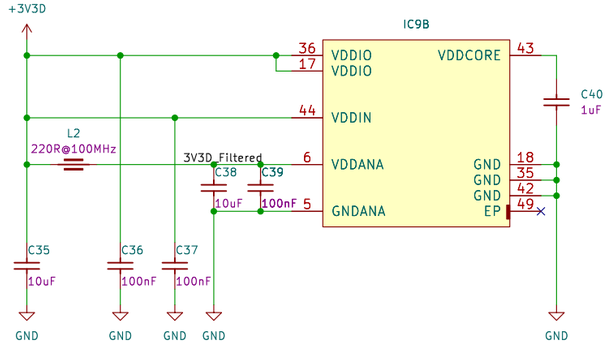
TO CHECK:



ATSAMD21 MCU

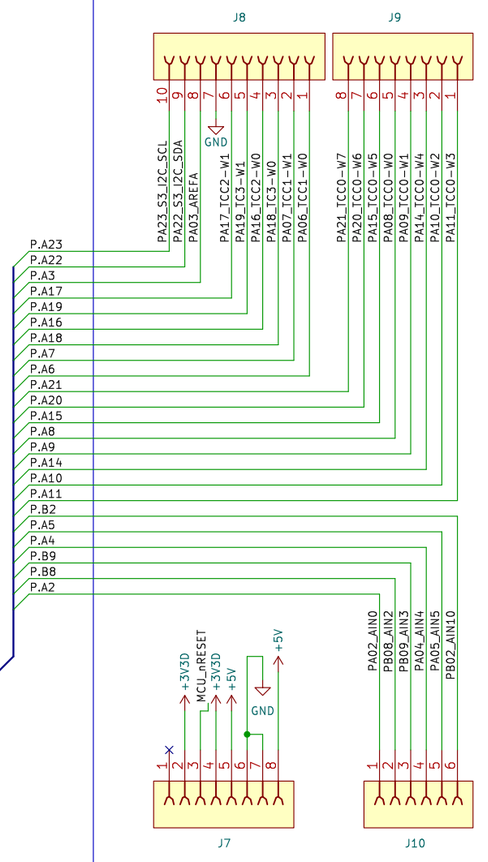
Calculation of crystal load capacitors:
CLOAD = ([CXIN + CLEXT] * [CXOUT + CLEXT]) / ([CXIN + CLEXT + CLEXT + CXOUT]) + CSTRAY
CLOAD = 12.0pF (from crystal datasheet)
CXIN32 = 3.1pF (from MCU datasheet)
CXOUT = 3.3pF (from MCU datasheet)
CSTRAY = 0.5pF (estimate)
CLEXT = 19.8pF



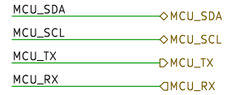


Arduino Header

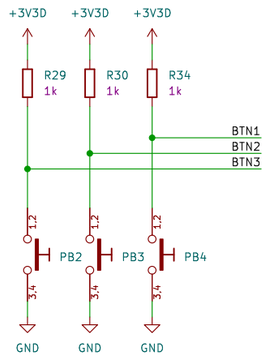
Routing note:
– Placement of female headers must match Arduino Zero Shield



Outputs

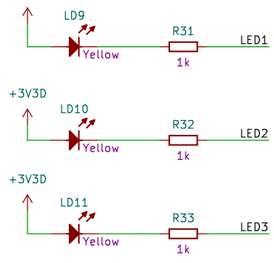


Buttons



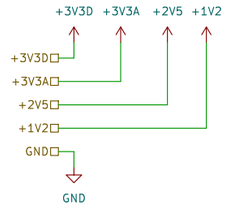
Routing note:
– REV2: Place BTN1 (PB4) rightmost, then BTN2 and BTN3 leftmost

LEDs

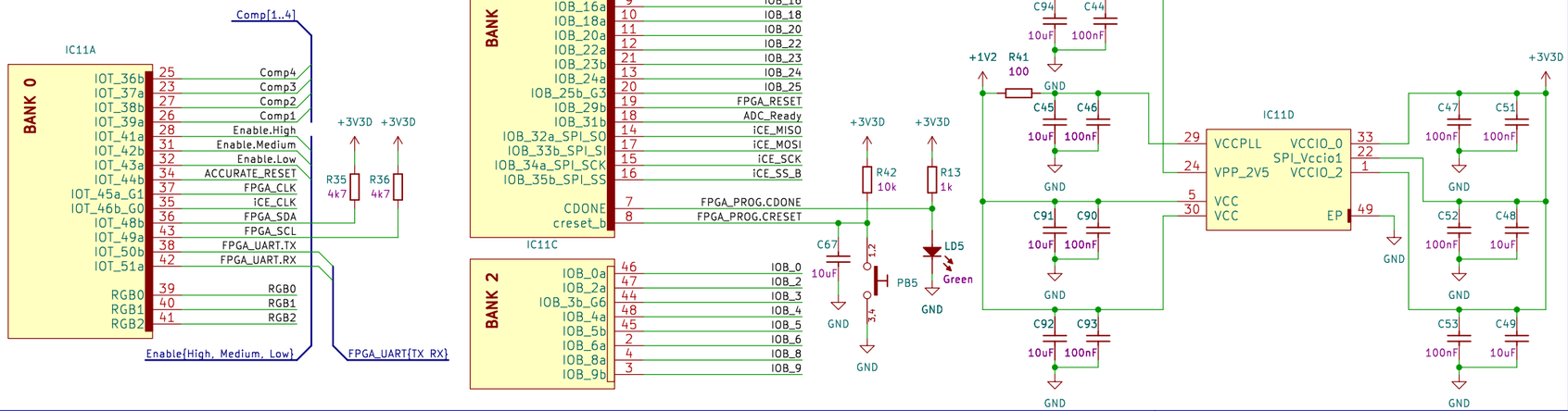


Project/Equipment:	**CROME**
	KiCad E.D.A. 8.99.0–2230–g1cc11bc589
Document	**ACCURATE 2 Evaluation Board** /MCU/
RP-IL	
Designer	
Drawn by	Liverud, Consani
Checked by	
Last Mod.	2025–01–20
File:	MCU.kicad_sch
Sheet:	3 of 6
European Organization for Nuclear Research CH–1211 Genève 23 – Switzerland	A3 A

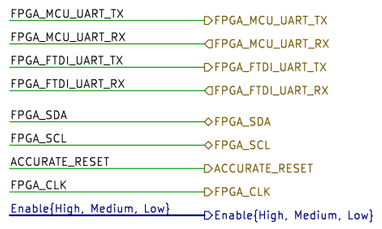
Power Ports



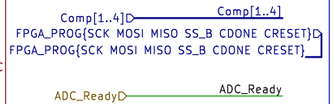
iCE40 Ultra FPGA



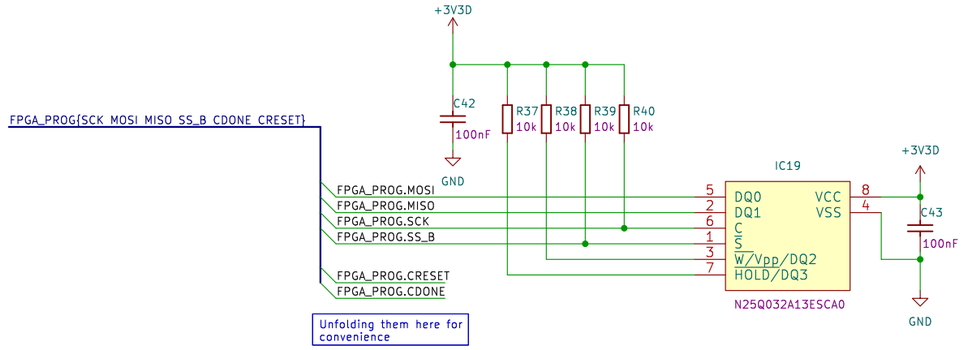
Outputs



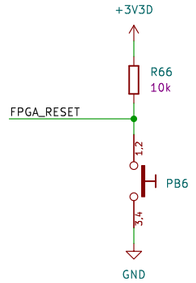
Inputs



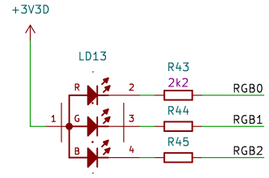
Flash



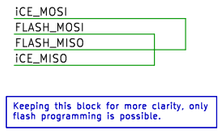
FPGA Reset



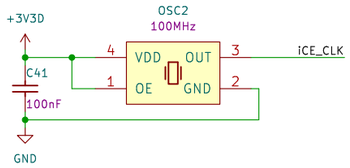
RGB LED



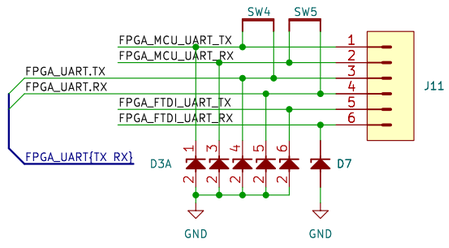
Flash/iCE Header



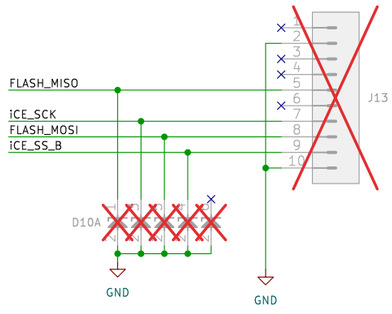
Oscillator



FTDI/MCU UART Header

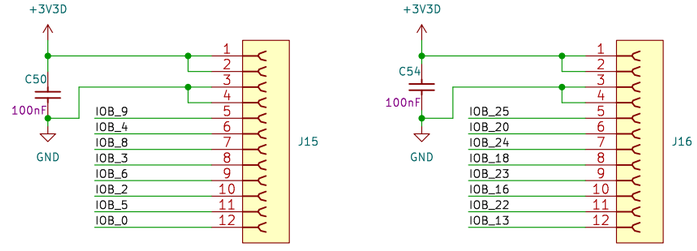


Programming Connector



PMOD Connectors

Routing note:
– Place by board edge



Project/Equipment: **CROME**

KiCad E.D.A. 8.99.0–2230–g1cc11bc589

Document

RP–IL

ACCURATE 2 Evaluation Board

/FPGA/

Designer	
Drawn by	Liverud, Consani
Checked by	
Last Mod.	2025–01–20
File: FPGA.kicad_sch	
Sheet: 4 of 6	

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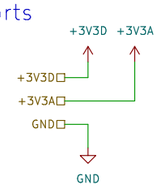
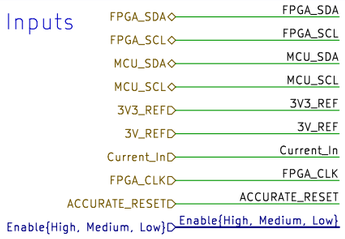
A3 A

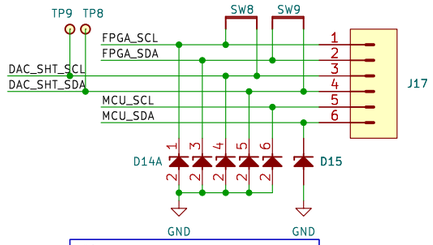
Power Ports



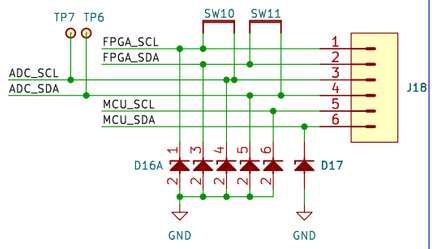
Inputs



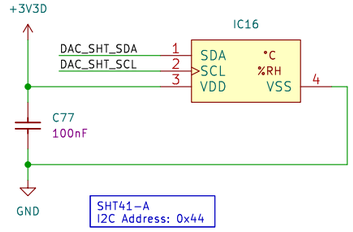
FPGA/MCU I2C Headers



J12:
|| Use I2C from FPGA (Default)
. .
. .
|| Use I2C from MCU



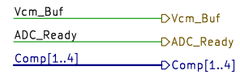
Humidity and Temperature sensor



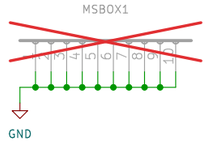
SHT41-A
I2C Address: 0x44

Routing note:
– Place close to ACCURATE2 ASIC

Outputs



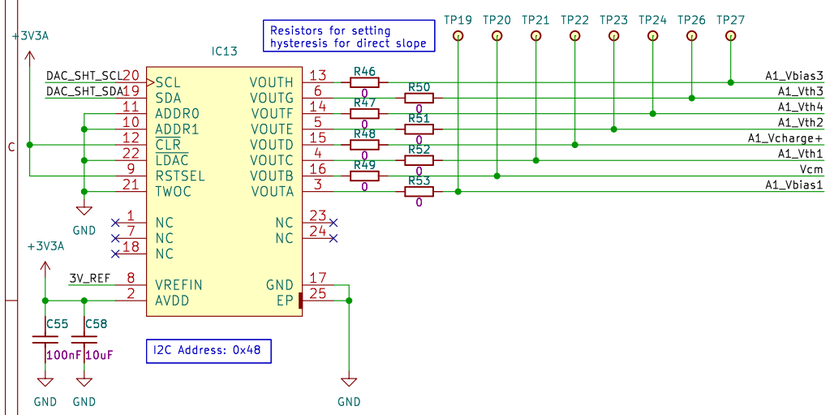
Shielding box



Routing note:
– Add shielding guard similar to Lambda1 board (EDA-03726-V3-0)
– Place J3 and J4 connectors inside shield box on bottom side of board
– Every component on this sheet except for headers should be below the shield

DACs

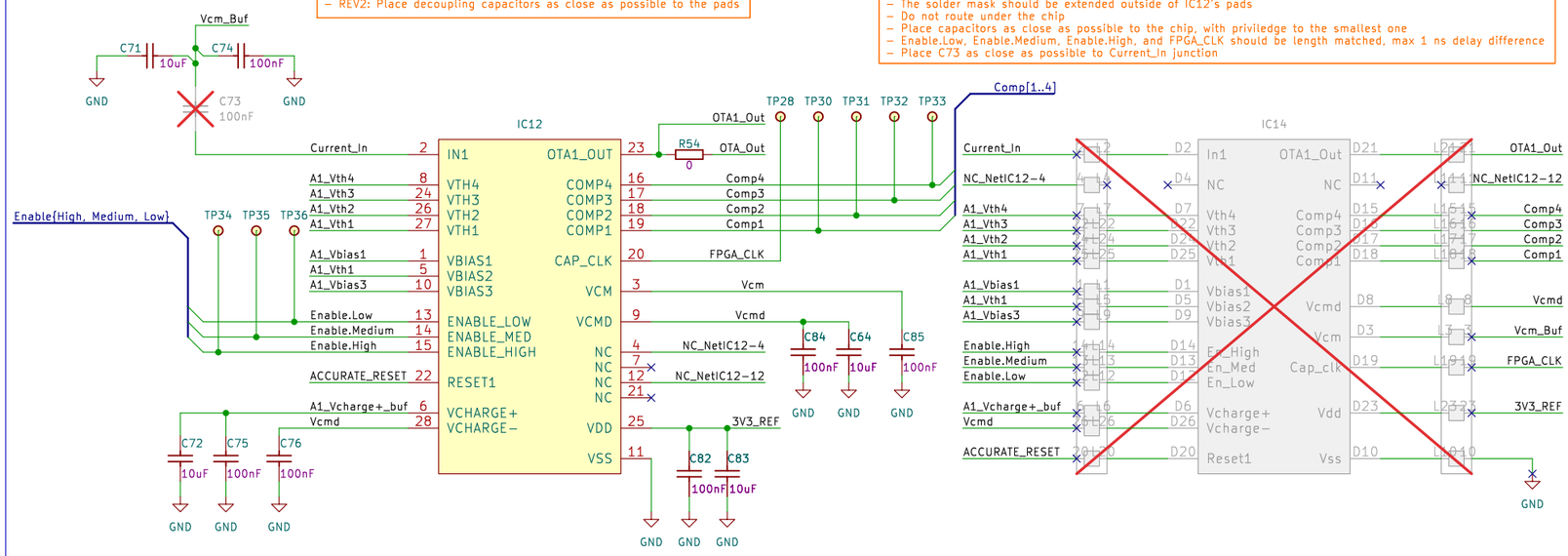
Routing note:
– Place capacitors close to the destination
– Possible to swap signals for easier routing



Accurate ASIC

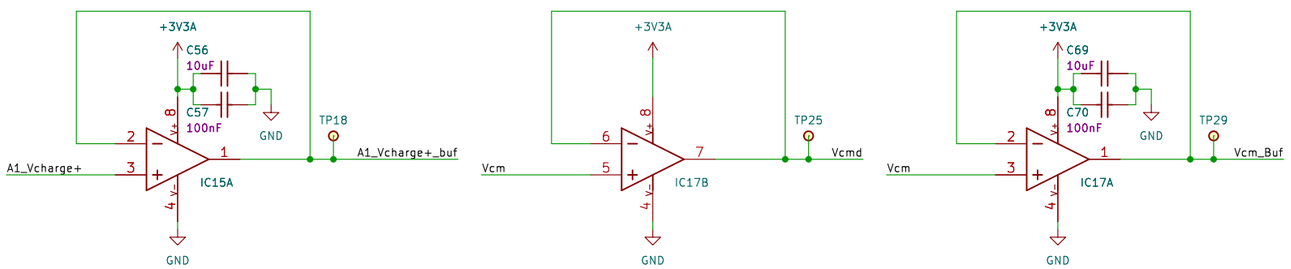
Routing note:
– REV2: Put solder mask on input lines
– REV2: Smaller capacitors must be placed closest to chip
– REV2: Place decoupling capacitors as close as possible to the pads

Routing note:
– IC14 shall be placed in the middle of IC12. The PCB-pads of IC14 shall be deleted in the layout. This is to have both the option of the packaged and bonded version of the ASIC
– The solder mask should be extended outside of IC12's pads
– Do not route under the chip
– Place capacitors as close as possible to the chip, with priviledge to the smallest one
– Enable.Low, Enable.Medium, Enable.High, and FPGA_CLK should be length matched, max 1 ns delay difference
– Place C73 as close as possible to Current_In junction

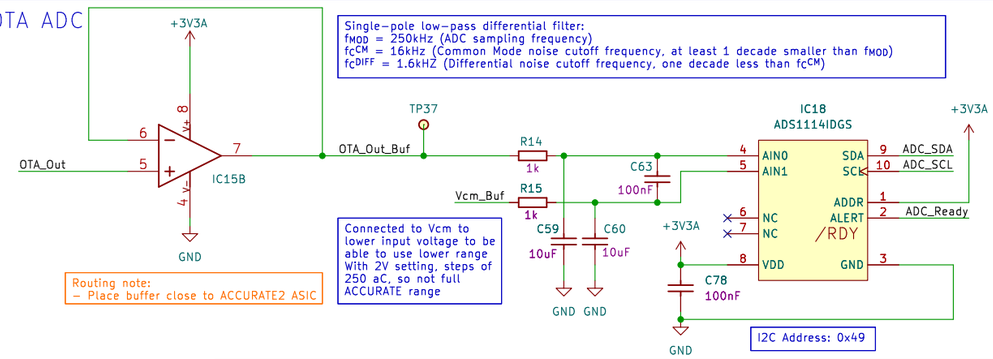


Buffers

Buffers required due to dynamic loads which needs large bypass caps to drive.



OTA ADC



Routing note:
– Place buffer close to ACCURATE2 ASIC

Connected to Vcm to lower input voltage to be able to use lower range With 2V setting, steps of 250 aC, so not full ACCURATE range

I2C Address: 0x49

Project/Equipment:	**CROME**
	KiCad E.D.A. 8.99.0-2230-g1cc11bc589
Document	**ACCURATE 2 Evaluation Board**
	/ACCURATE ASIC/
Designer	
Drawn by	Liverud, Consani
Checked by	
Last Mod.	2025-01-20
File:	ACCURATE ASIC.kicad_sch
Sheet:	5 of 6
RP-IL	
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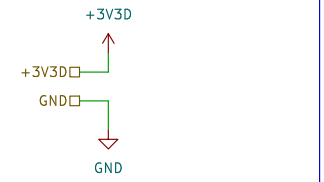
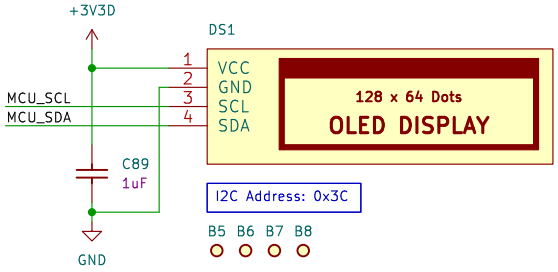
A3	A

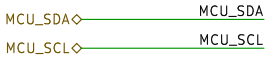
Power Ports



OLED Display



Inputs



Project/Equipment: **CROME**

KiCad E.D.A. 8.99.0–2230–g1cc11bc589

Document

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ACCURATE 2 Evaluation Board

/Display/

Designer	
Drawn by	Håkon Liverud
Checked by	
Last Mod.	2025–01–20
File: Display.kicad_sch	
Sheet: 6 of 6	

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Text