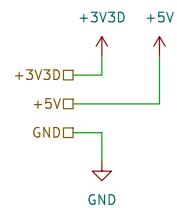


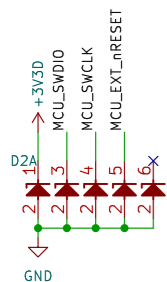
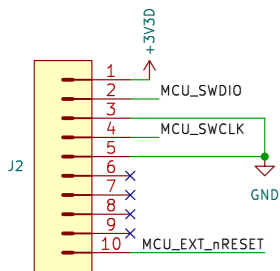
## Power Ports



## Inputs

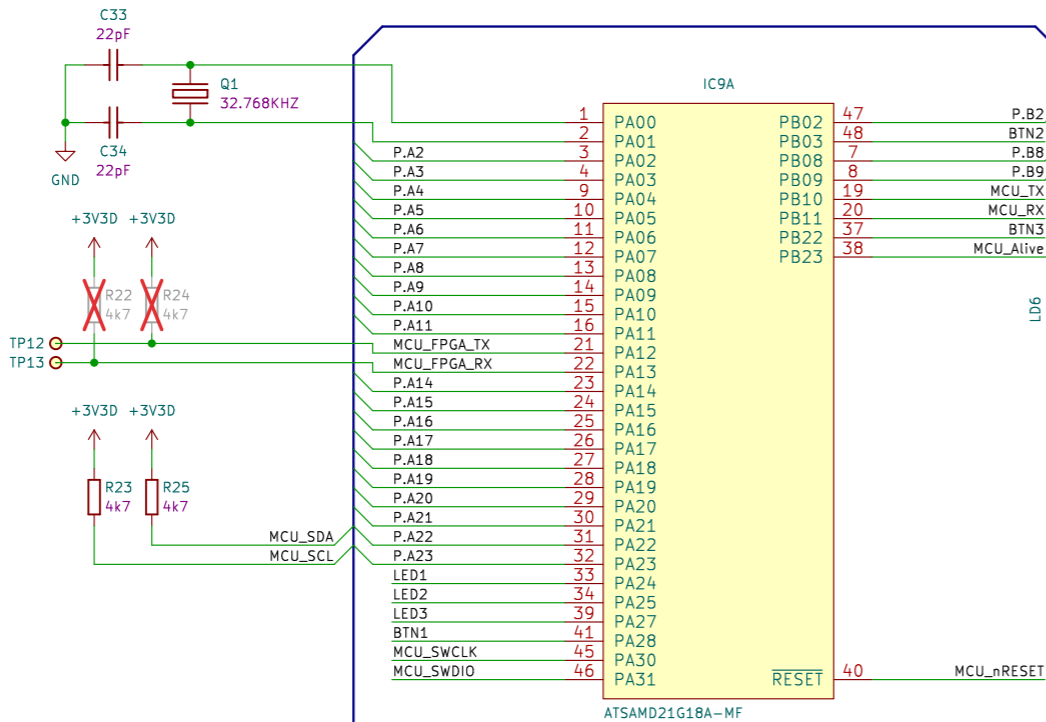


## Programming Header

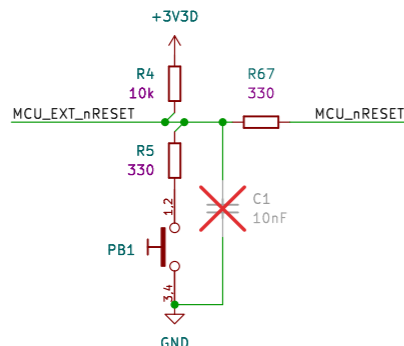


## ATSAMD21 MCU

Calculation of crystal load capacitors:  
 $C_{LOAD} = \frac{([C_{XIN} + C_{LEXT}] * [C_{XOUT} + C_{LEXT}])}{([C_{XIN} + C_{LEXT} + C_{LEXT} + C_{XOUT}]) + C_{STRAY}}$   
 $C_{LOAD} = 12.0pF$  (from crystal datasheet)  
 $C_{XIN32} = 3.1pF$  (from MCU datasheet)  
 $C_{XOUT} = 3.3pF$  (from MCU datasheet)  
 $C_{STRAY} = 0.5pF$  (estimate)  
 $C_{LEXT} = 19.8pF$



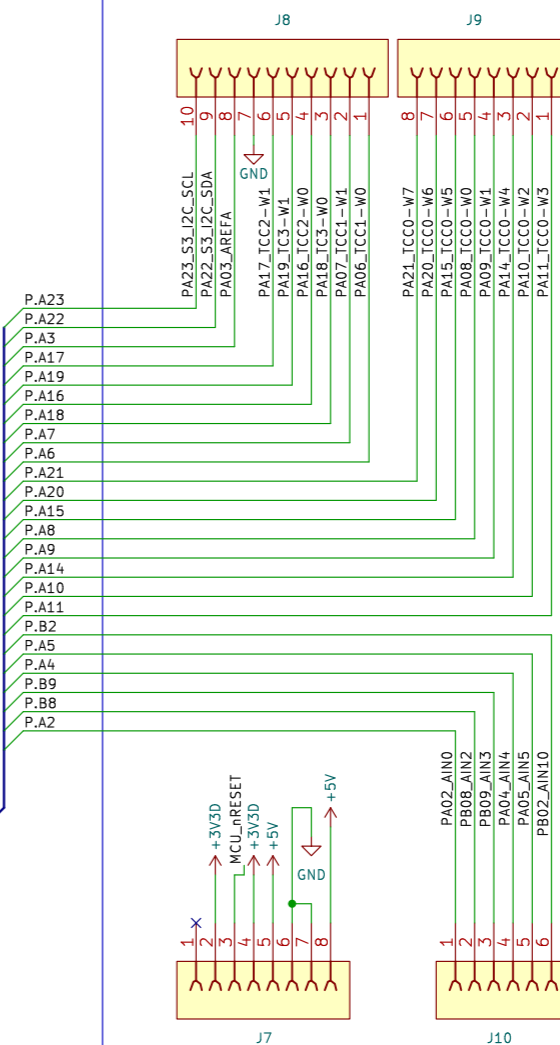
## MCU Reset:



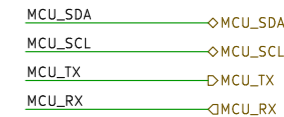
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## Arduino Header

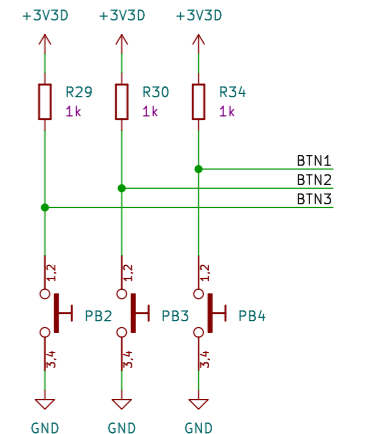
Routing note:  
 – Placement of female headers must match Arduino Zero Shield



## Outputs

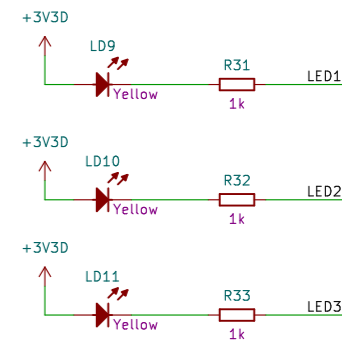


## Buttons



Routing note:  
 – REV2: Place BTN1 (PB4) rightmost, then BTN2 and BTN3 leftmost

## LEDs



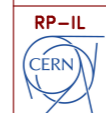
Project/Equipment: CROME

KiCad E.D.A. 8.99.0–2230–g1cc11bc589

Document

**ACCURATE 2 Evaluation Board**  
 /MCU/

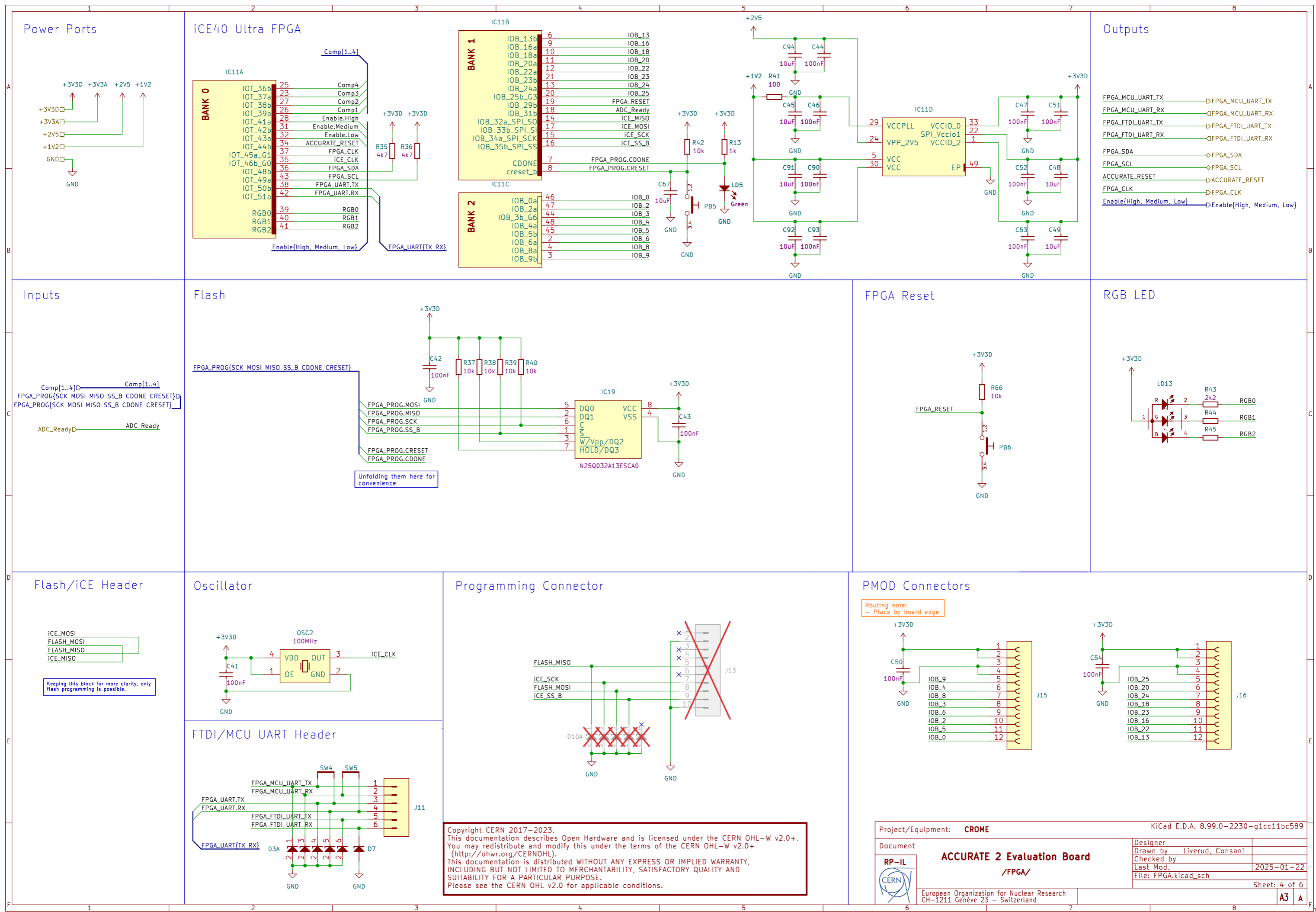
Designer  
 Drawn by Liverud, Consani  
 Checked by  
 Last Mod. 2025–01–22  
 File: MCU.kicad\_sch



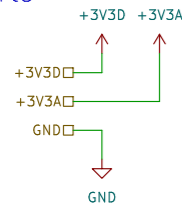
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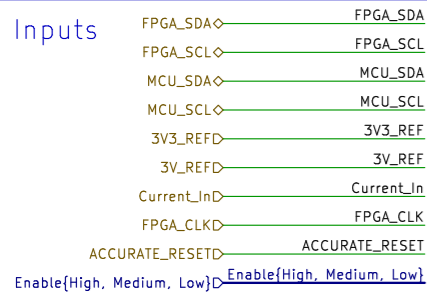
A3 A



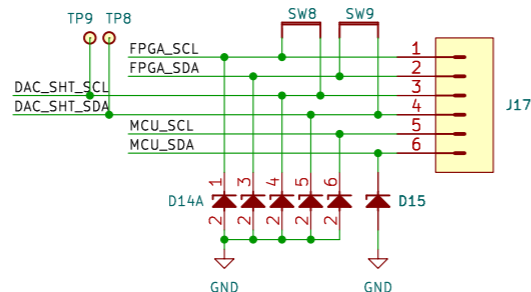
## Power Ports



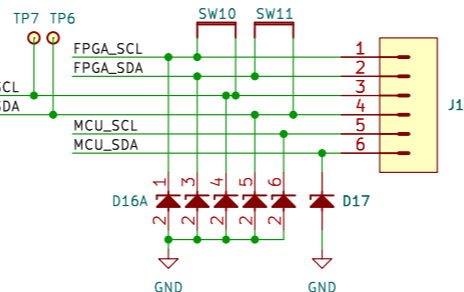
## Inputs



## FPGA/MCU I2C Headers

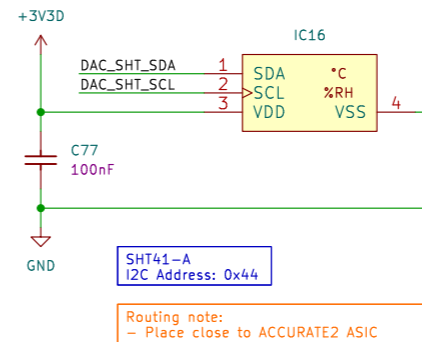


J17 (board oriented with ACCURATE up):  
 || Use I2C from FPGA (Default)  
 ..  
 || Use I2C from MCU



J18 (board oriented with ACCURATE up):  
 || Use I2C from FPGA (Default)  
 ..  
 || Use I2C from MCU

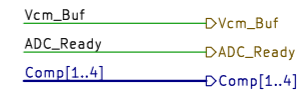
## Humidity and Temperature sensor



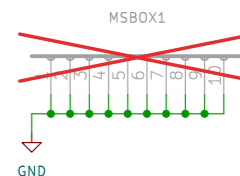
SHT41-A  
 I2C Address: 0x44

Routing note:  
 - Place close to ACCURATE2 ASIC

## Outputs



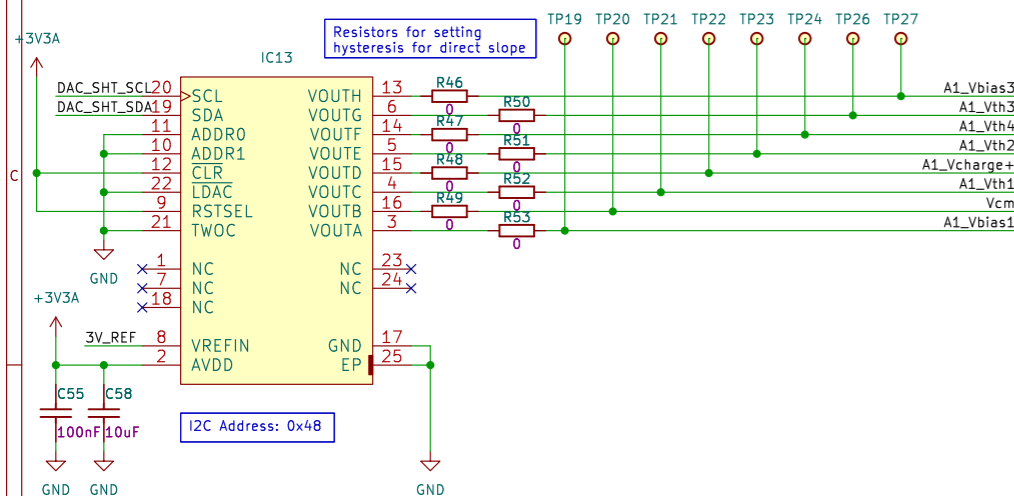
## Shielding box



Routing note:  
 - Add shielding guard similar to Lambda1 board (EDA-03726-V3-0)  
 - Place J3 and J4 connectors inside shield box on bottom side of board  
 - Every component on this sheet except for headers should be below the shield

## DACs

Routing note:  
 - Place capacitors close to the destination  
 - Possible to swap signals for easier routing

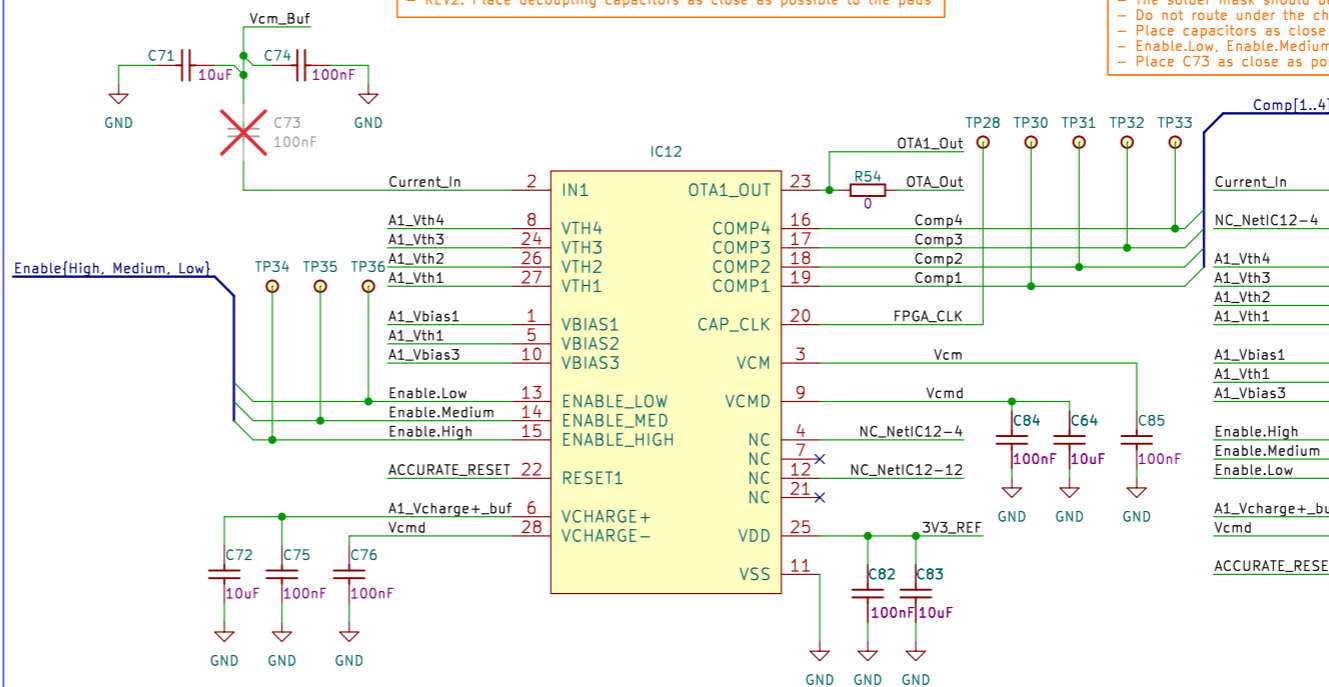


Resistors for setting hysteresis for direct slope

I2C Address: 0x48

## Accurate ASIC

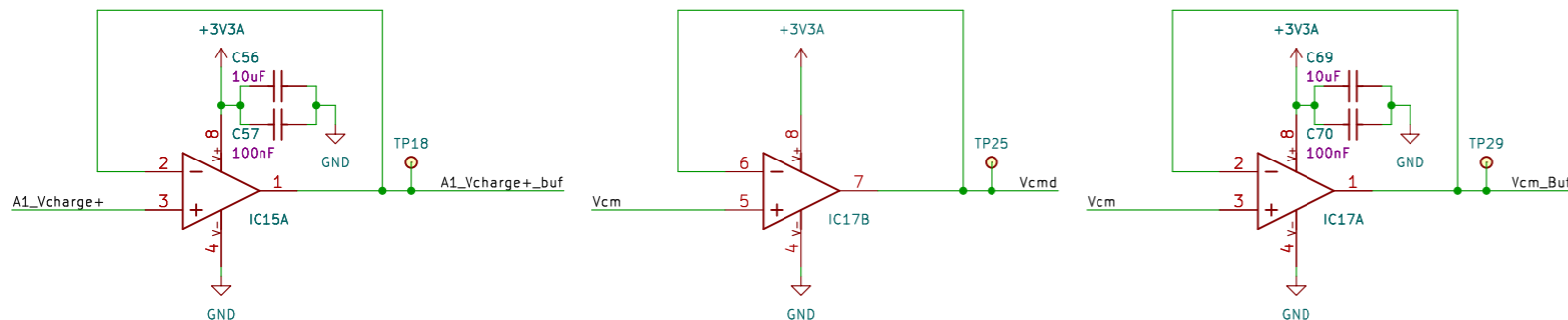
Routing note:  
 - REV2: Put solder mask on input lines  
 - REV2: Smaller capacitors must be placed closest to chip  
 - REV2: Place decoupling capacitors as close as possible to the pads



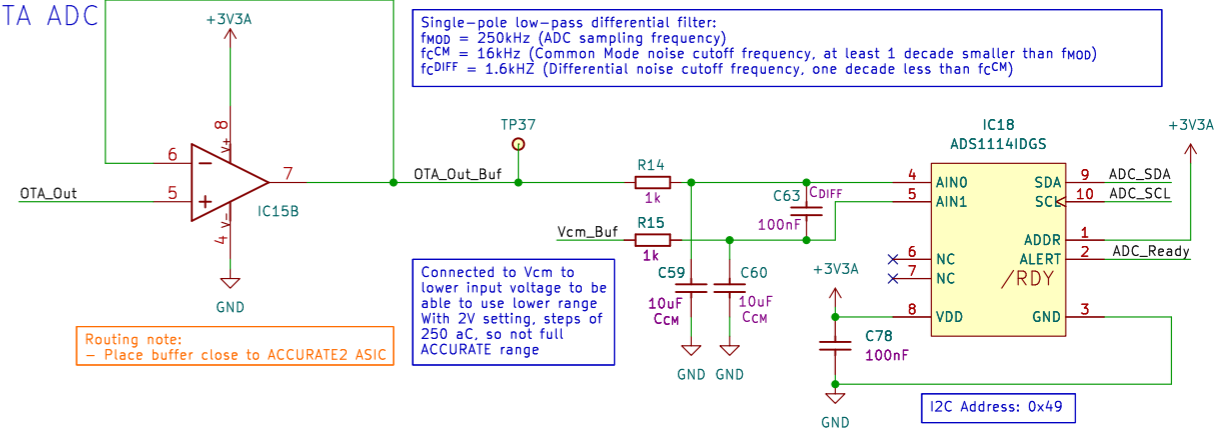
Routing note:  
 - IC14 shall be placed in the middle of IC12. The PCB-pads of IC14 shall be deleted in the layout. This is to have both the option of the packaged and bonded version of the ASIC  
 - The solder mask should be extended outside of IC12's pads  
 - Do not route under the chip  
 - Place capacitors as close as possible to the chip, with privilege to the smallest one  
 - Enable.Low, Enable.Medium, Enable.High, and FPGA\_CLK should be length matched, max 1 ns delay difference  
 - Place C73 as close as possible to Current\_In junction

## Buffers

Buffers required due to dynamic loads which needs large bypass caps to drive.



## OTA ADC



Single-pole low-pass differential filter:  
 $f_{\text{MD}} = 250\text{kHz}$  (ADC sampling frequency)  
 $f_{\text{CM}} = 16\text{kHz}$  (Common Mode noise cutoff frequency, at least 1 decade smaller than  $f_{\text{MD}}$ )  
 $f_{\text{DIFF}} = 1.6\text{kHz}$  (Differential noise cutoff frequency, one decade less than  $f_{\text{CM}}$ )

Connected to Vcm to lower input voltage to be able to use lower range  
 With 2V setting, steps of 250 aC, so not full ACCURATE range

I2C Address: 0x49

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Project/Equipment: CROME

KiCad E.D.A. 8.99.0–2230–g1cc11bc589

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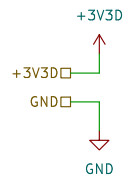
ACCURATE 2 Evaluation Board  
 /ACCURATE ASIC/

Designer  
 Drawn by Liverud, Consani  
 Checked by  
 Last Mod. 2025–01–22  
 File: ACCURATE ASIC.kicad\_sch

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 A3 A

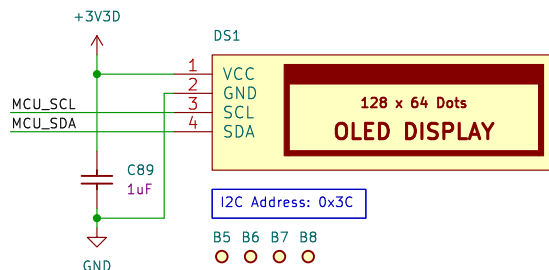
## Power Ports



## Inputs



## OLED Display



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Project/Equipment: **CROME**

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**ACCURATE 2 Evaluation Board**

**/Display/**

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Drawn by	Håkon Liverud
Checked by	
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**A4** **A**