


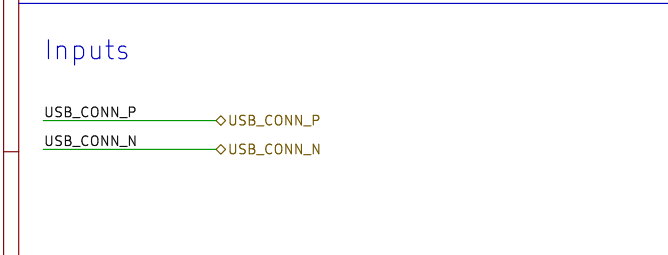
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Power Ports

+5VEXT +5VUSB

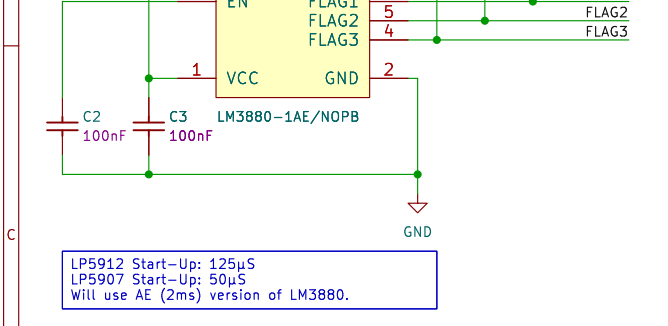


A

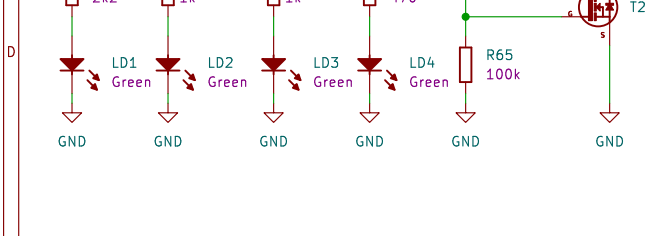


PSU Sequencer

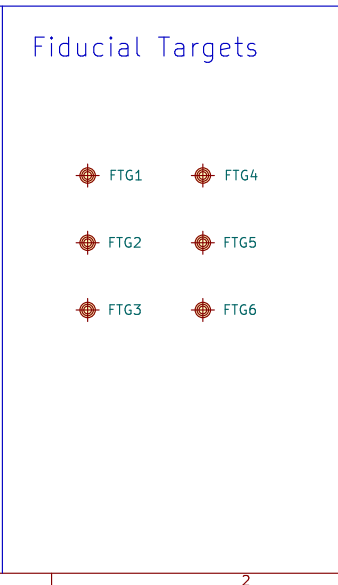
The diagram shows a circuit for a PSU Sequencer. A +5V supply is connected to the EN pin of IC1 (pin 3) and to a network of resistors R9, R11, and R12 (all 100k) connected to pins 6 and FLAG1. The FLAG1 pin is also connected to the +5V supply.



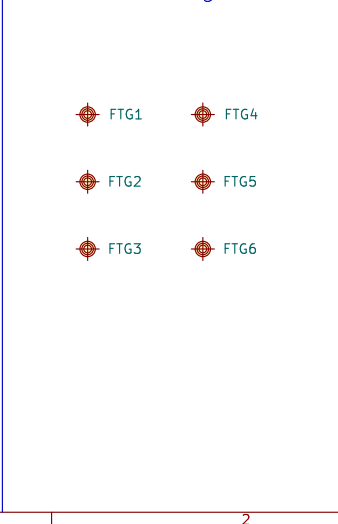
Status LEDs



Mounting Holes



The diagram illustrates the layout of six footcandle gauges (FTG1 through FTG6) positioned around a central point. The gauges are arranged in a 3x2 grid. Each gauge is represented by a red crosshair symbol. The labels FTG1, FTG2, and FTG3 are in green, while FTG4, FTG5, and FTG6 are in red. A scale bar at the bottom indicates a distance of 10 feet.

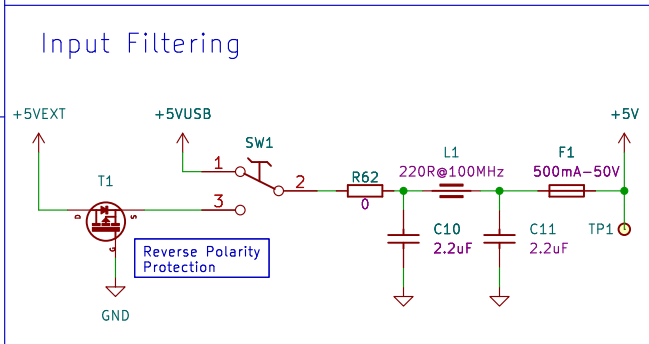


USB ESD Protection

The diagram illustrates the internal structure of a USB ESD protection diode array (D4). It features a central yellow box representing the diode array, with four diodes connected in a bridge configuration. The pins are labeled as follows:

- Pin 1 (USB_CONN_N):** Connected to the bottom-left terminal (I/O1) of the diode array.
- Pin 2 (GND):** Connected to the bottom-right terminal (VBUS) of the diode array.
- Pin 3 (USB_CONN_P):** Connected to the top-left terminal (I/O2) of the diode array.
- Pin 4 (USB_P):** Connected to the top-right terminal (I/O2) of the diode array.
- Pin 5 (+5VUSB):** Connected to the bottom-right terminal (VBUS) of the diode array.
- Pin 6 (USB_N):** Connected to the bottom-left terminal (I/O1) of the diode array.

The diode array (D4) is shown with its internal structure, including the diodes and the central VBUS and I/O1/I/O2 terminals. The pins are numbered 1 through 6, corresponding to the labels on the right. The connections show that the USB_CONN_P and USB_CONN_N pins are connected to the I/O1 and I/O2 terminals, while the GND and +5VUSB pins are connected to the VBUS terminal. The USB_P and USB_N pins are also connected to the I/O1 and I/O2 terminals, respectively.



Voltage Regulators

IC2
LP5907MFX-3.3

VIN VOUT
EN NC
GND

C6 1µF

TP5 R55 0

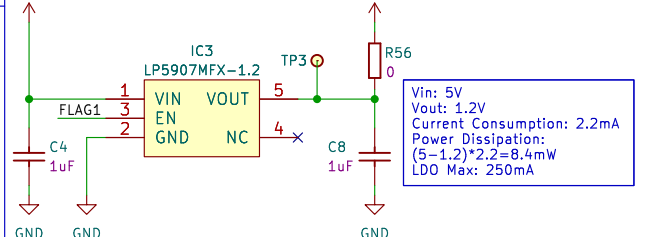
C7 1µF

+5V +3V3A

GND GND

+5V +1V2

Vin: 5V
Vout: 3.3V
Current Consumption: 3.5mA
Power Dissipation:
 $(5-3.3) \times 3.5 = 6\text{mW}$
LDO Max: 250mA



IC4
LP5912-3.3DRVT

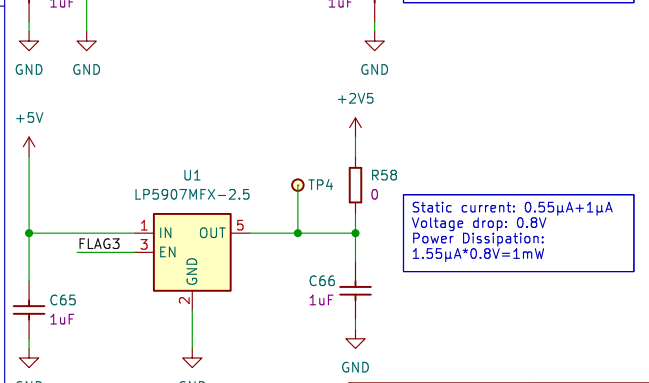
IN 6
EN 4
GND 5
EP 7

OUT 1
NC 2
PG 3

FLAG2
C5
C9

+5V
+3V3D
R57
TP2

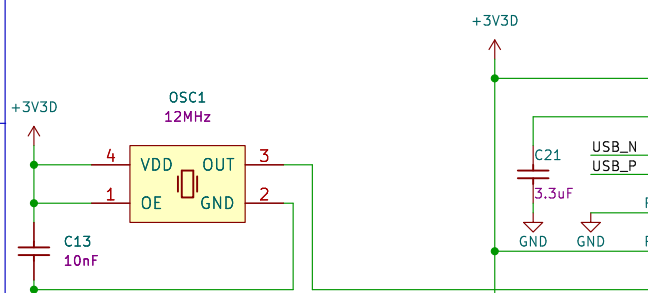
Vin: 5V
Vout: 3.3V
Current Consumption: 121mA
Power Dissipation:
(5-3.3) * 121 = 205mW
LDO Max: 500mA



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$\frac{1}{2}$ $\frac{4}{5}$



Voltage References

The diagram illustrates a voltage reference circuit. A +5V supply is connected to the TP pin of the REF196GSZ IC (IC5) through a 100nF capacitor (C14). The SLEEP pin is connected to the same +5V supply through a 10uF capacitor (C15). The NC pin is connected to the TP pin through a 10uF capacitor (C15). The GND pin is connected to ground. The OUT pin is connected to the TP10 output through a 1uF capacitor (C20). The TP10 output is connected to the 3V3_REF output through a resistor (R59, 0 ohms). The circuit is powered by a +5V supply and grounded.

IC5

REF196GSZ

TP10

3V3_REF

+5V

GND

C14 100nF

C15 10uF

C20 1uF

R59 0

Vs SLEEP TP GND

OUT NC TP

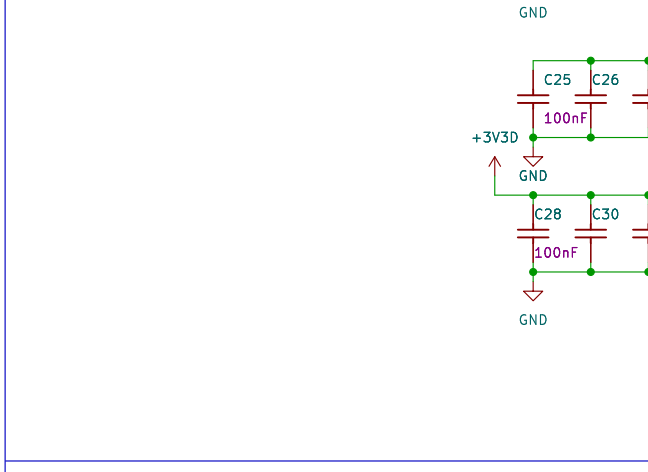
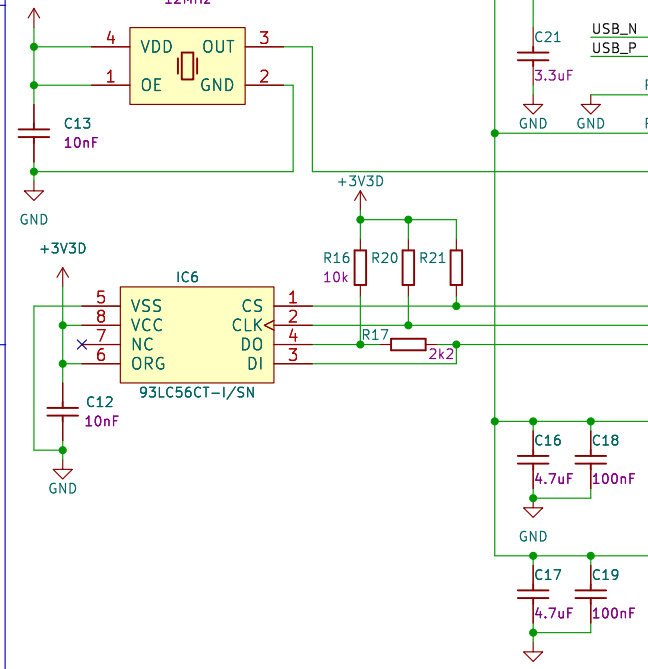
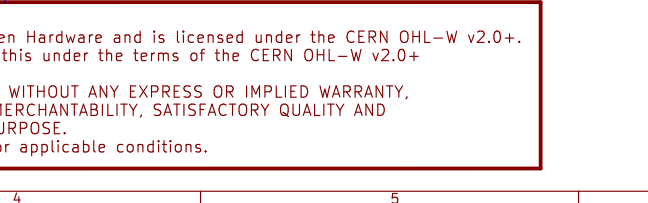
6 7 8 5

2 3 4

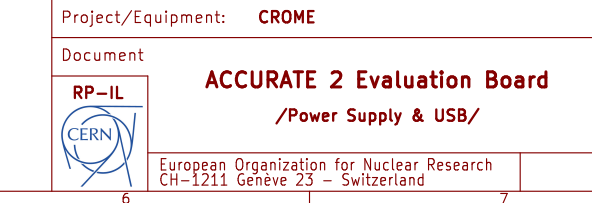
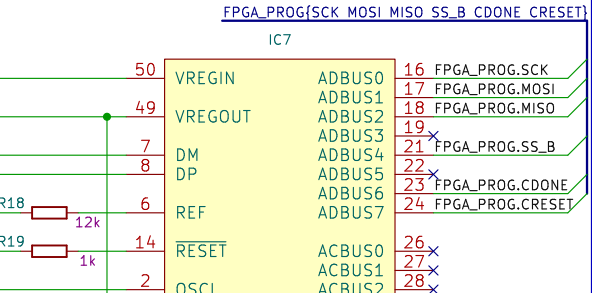
100nF 10uF 1uF

ACCURATE typically consumes 1mA -> Voltage ref usage is OK

Routing note:
- Place close to the ACCURATE 2 ASIC



6		7	
IC7			
50	VREGIN	ADBUS0	16 FPGA_PROG.SCK
49	VREGOUT	ADBUS1	17 FPGA_PROG.MOSI
		ADBUS2	18 FPGA_PROG.MISO

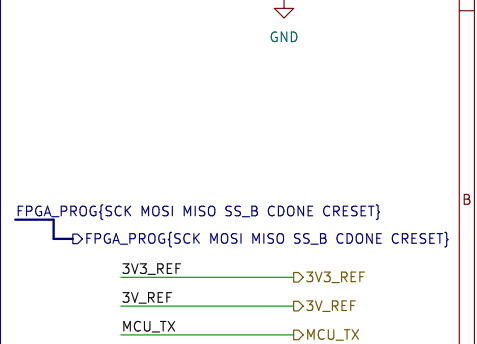


Outputs

Diagram illustrating the output stage of a 741 op-amp. The outputs are labeled as follows:

- +5V
- +3V3A
- +3V3D
- +2V5
- +1V2

The output pins are connected to a common GND pin.



FPGA/MCU UART Header

FPGA_RX
FPGA_TX
RX
TX
MCU_TX
MCU_RX

SW2 SW3

1
2
3
4
5
6

J6

D5A D5B D5C D5D D5E D5F

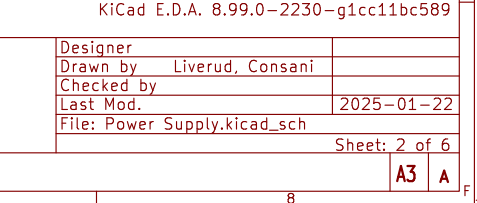
GND GND

J6 (board oriented with ACCURATE up):

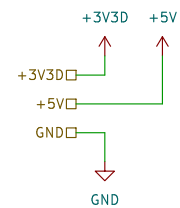
|| Use UART from FPGA

|| Use UART from MCU (Default)

Rx and Tx switched for MCU



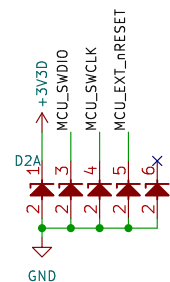
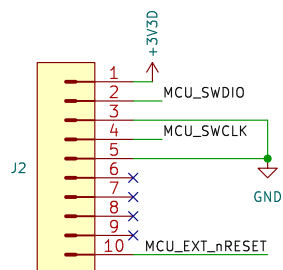
Power Ports



Inputs

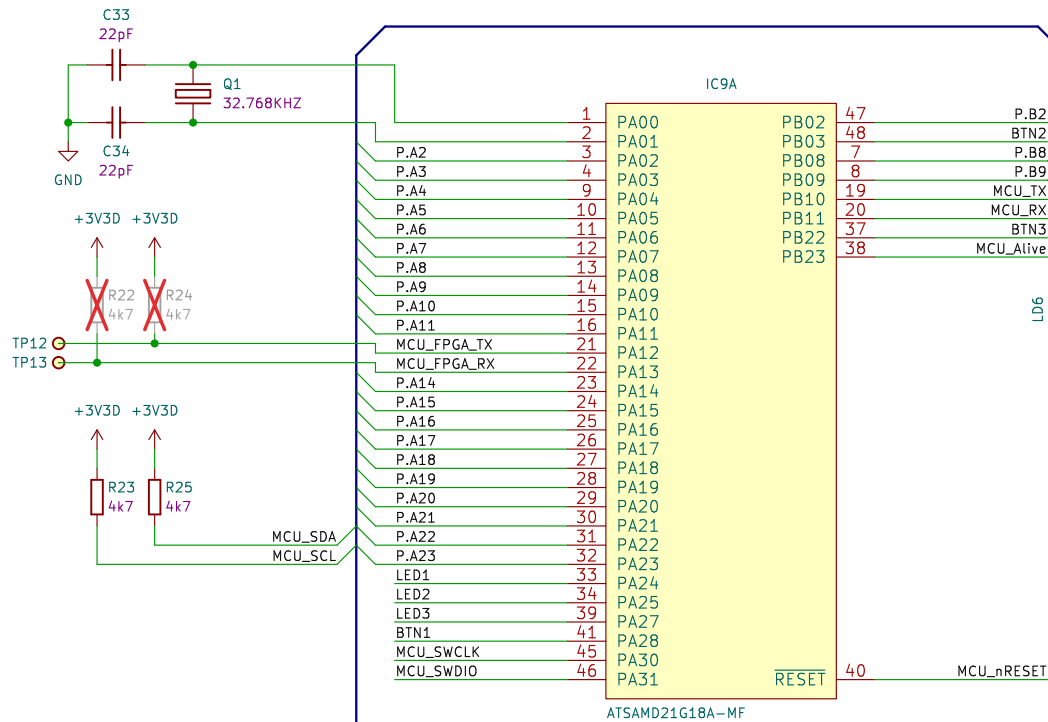


Programming Header

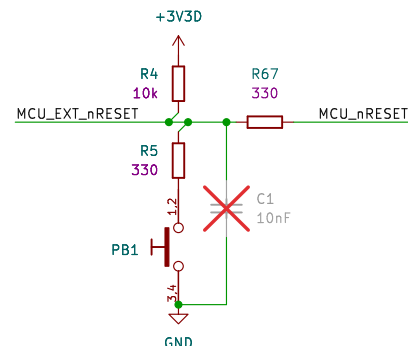


ATSAMD21 MCU

Calculation of crystal load capacitors:
 $C_{LOAD} = \frac{([C_{XIN} + C_{LEXT}] * [C_{XOUT} + C_{LEXT}])}{([C_{XIN} + C_{LEXT} + C_{LEXT} + C_{XOUT}]) + C_{STRAY}}$
 $C_{LOAD} = 12.0pF$ (from crystal datasheet)
 $C_{XIN32} = 3.1pF$ (from MCU datasheet)
 $C_{XOUT} = 3.3pF$ (from MCU datasheet)
 $C_{STRAY} = 0.5pF$ (estimate)
 $C_{LEXT} = 19.8pF$



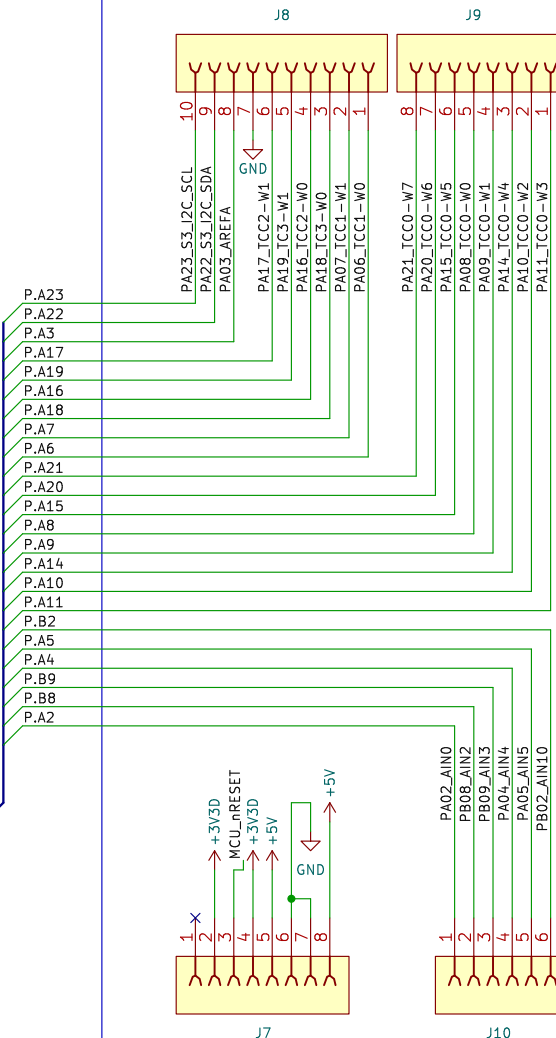
MCU Reset:



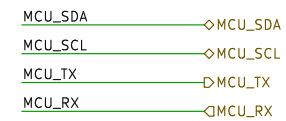
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Arduino Header

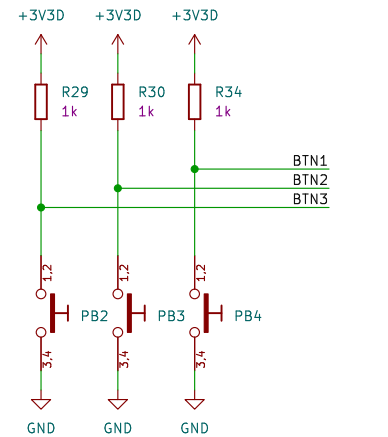
Routing note:
 – Placement of female headers must match Arduino Zero Shield



Outputs

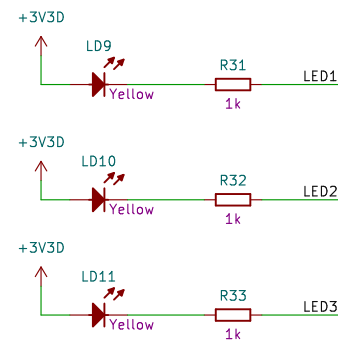


Buttons



Routing note:
 – REV2: Place BTN1 (PB4) rightmost, then BTN2 and BTN3 leftmost

LEDs



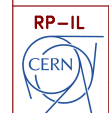
Project/Equipment: CROME

KiCad E.D.A. 8.99.0–2230–g1cc11bc589

Document

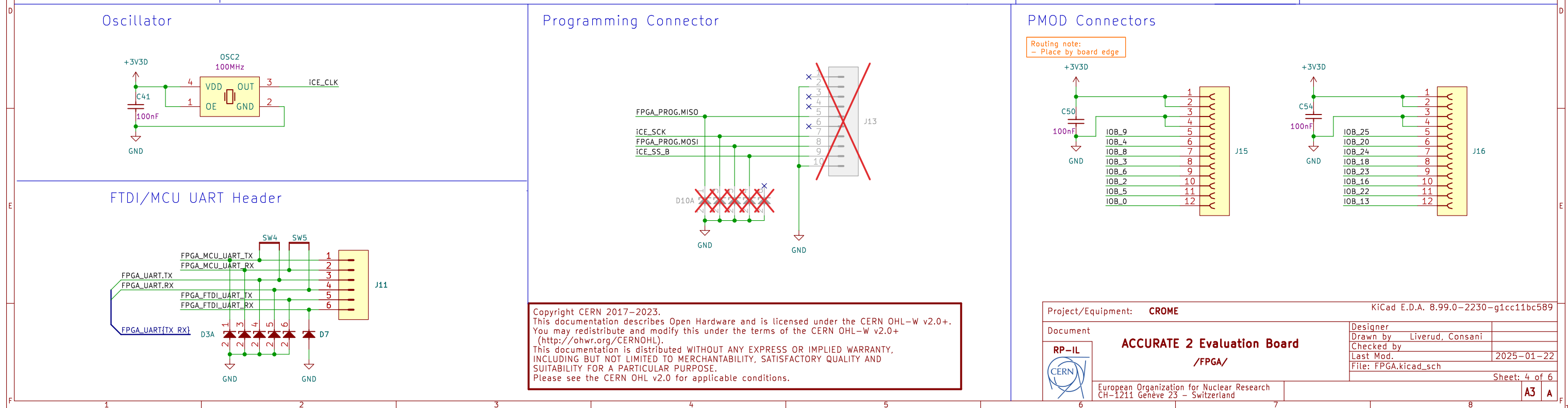
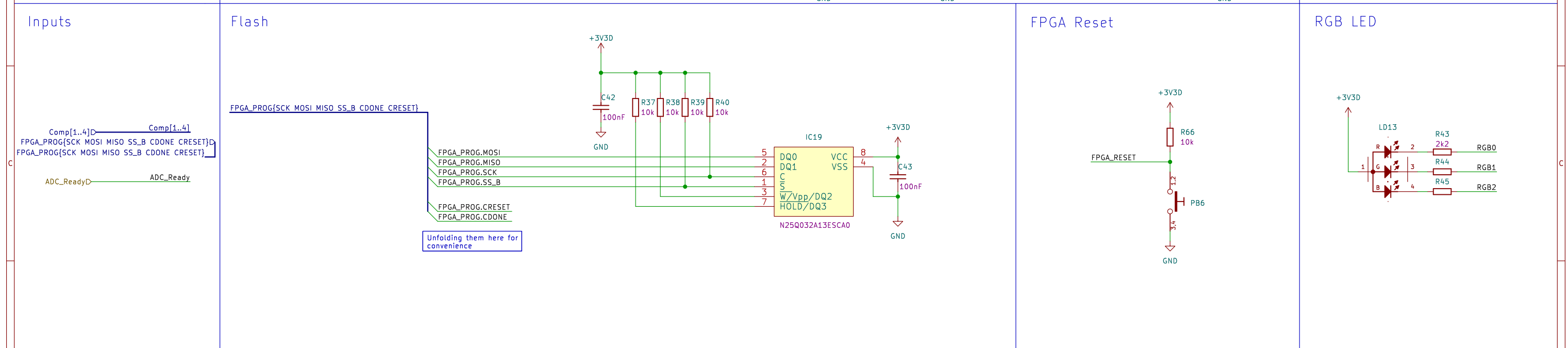
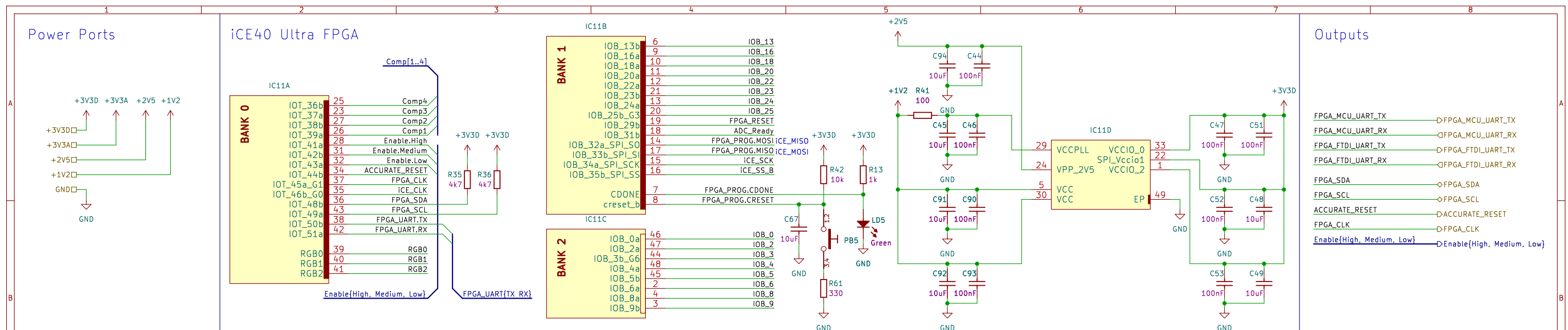
ACCURATE 2 Evaluation Board
 /MCU/

Designer
 Drawn by Liverud, Consani
 Checked by
 Last Mod. 2025–01–22
 File: MCU.kicad_sch

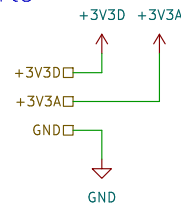


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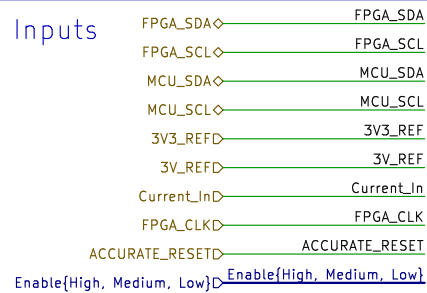
Sheet: 3 of 6
 A3 A



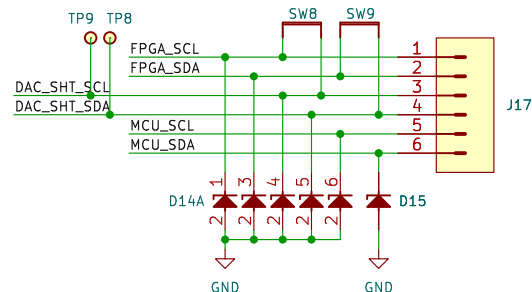
Power Ports



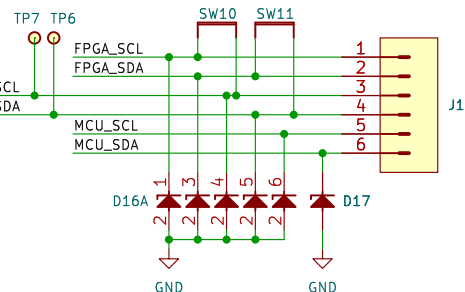
Inputs



FPGA/MCU I2C Headers

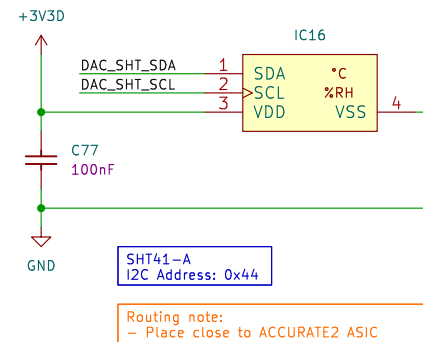


J17 (board oriented with ACCURATE up):
 || Use I2C from FPGA (Default)
 ..
 || Use I2C from MCU



J18 (board oriented with ACCURATE up):
 || Use I2C from FPGA (Default)
 ..
 || Use I2C from MCU

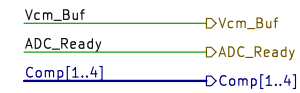
Humidity and Temperature sensor



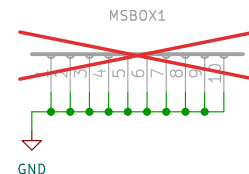
SHT41-A
 I2C Address: 0x44

Routing note:
 - Place close to ACCURATE2 ASIC

Outputs



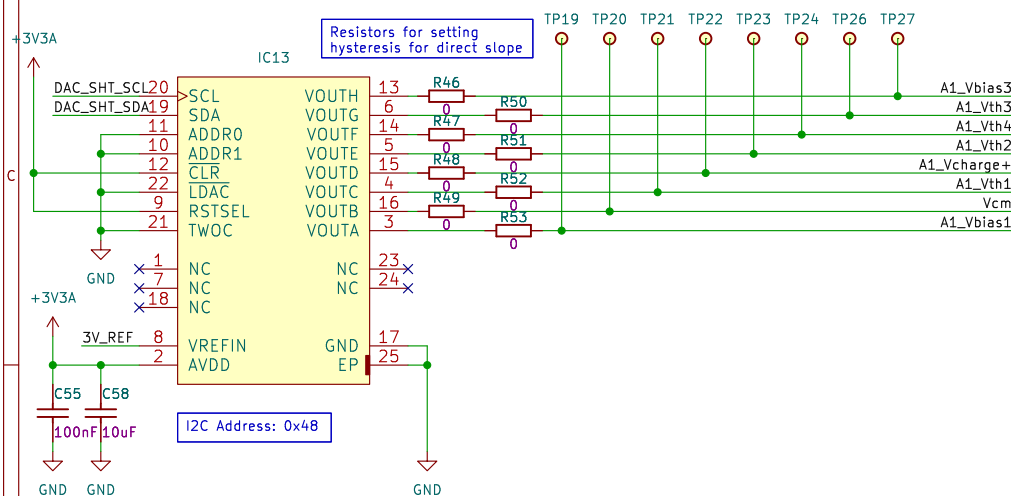
Shielding box



Routing note:
 - Add shielding guard similar to Lambda1 board (EDA-03726-V3-0)
 - Place J3 and J4 connectors inside shield box on bottom side of board
 - Every component on this sheet except for headers should be below the shield

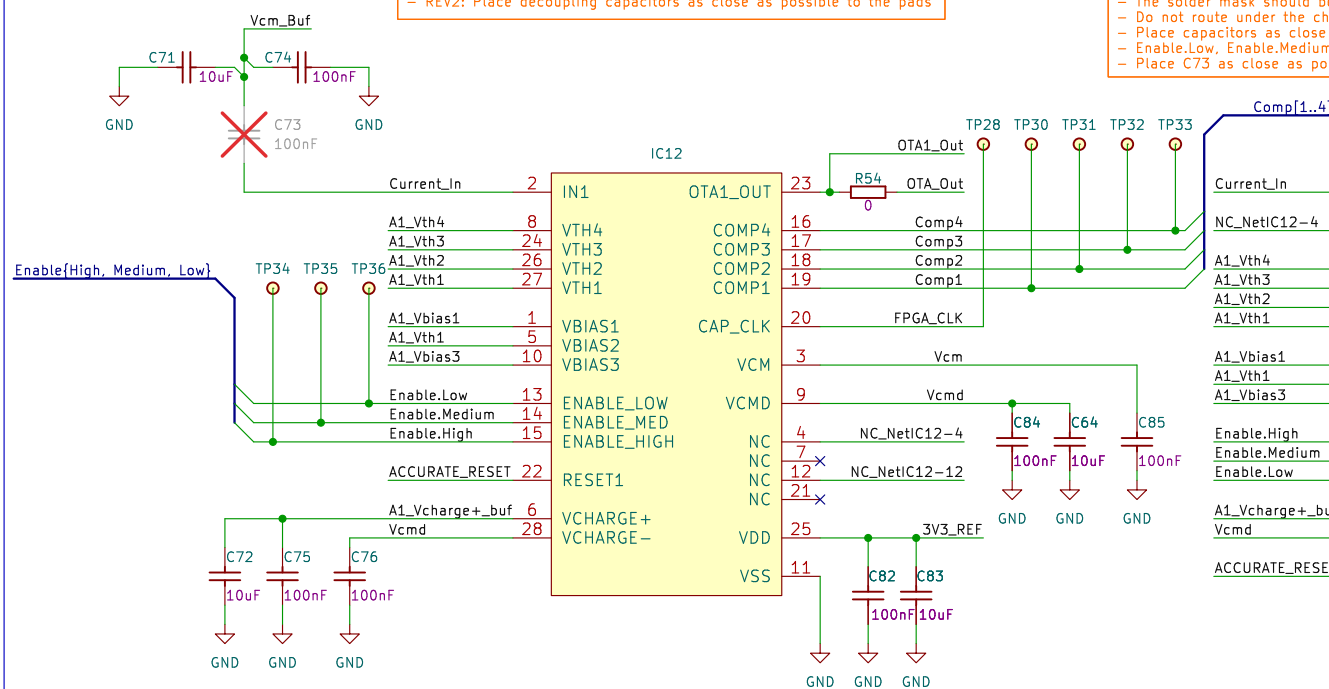
DACs

Routing note:
 - Place capacitors close to the destination
 - Possible to swap signals for easier routing



Accurate ASIC

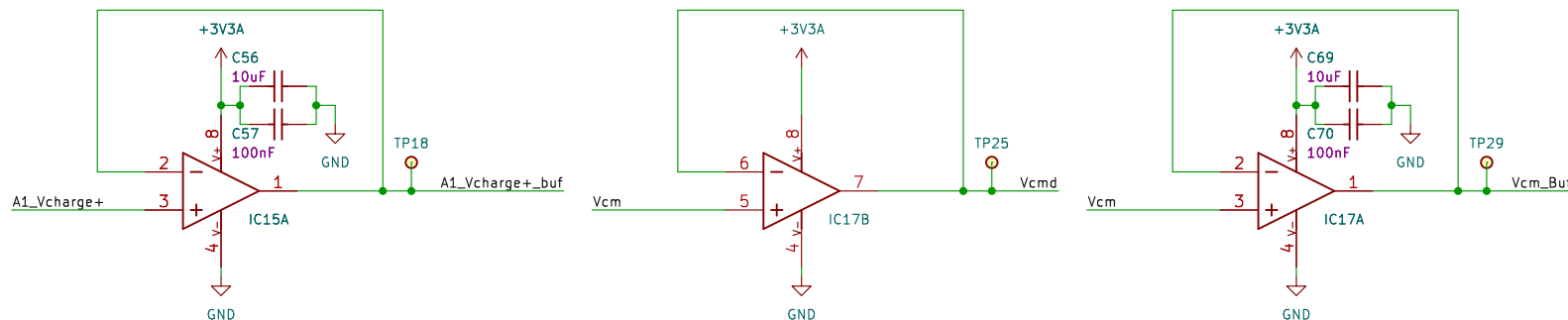
Routing note:
 - REV2: Put solder mask on input lines
 - REV2: Smaller capacitors must be placed closest to chip
 - REV2: Place decoupling capacitors as close as possible to the pads



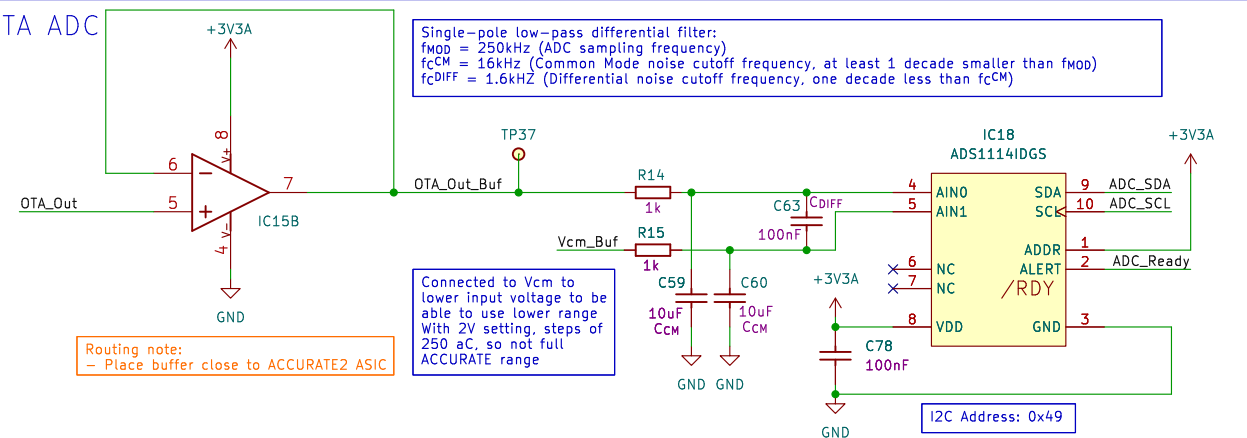
Routing note:
 - IC14 shall be placed in the middle of IC12. The PCB-pads of IC14 shall be deleted in the layout. This is to have both the option of the packaged and bonded version of the ASIC
 - The solder mask should be extended outside of IC12's pads
 - Do not route under the chip
 - Place capacitors as close as possible to the chip, with privilege to the smallest one
 - Enable.Low, Enable.Medium, Enable.High, and FPGA_CLK should be length matched, max 1 ns delay difference
 - Place C73 as close as possible to Current_In junction

Buffers

Buffers required due to dynamic loads which needs large bypass caps to drive.



OTA ADC



Single-pole low-pass differential filter:
 $f_{\text{MD}} = 250\text{kHz}$ (ADC sampling frequency)
 $f_{\text{CM}} = 16\text{kHz}$ (Common Mode noise cutoff frequency, at least 1 decade smaller than f_{MD})
 $f_{\text{DIFF}} = 1.6\text{kHz}$ (Differential noise cutoff frequency, one decade less than f_{CM})

Connected to Vcm to lower input voltage to be able to use lower range
 With 2V setting, steps of 250 aC, so not full ACCURATE range

Project/Equipment: CROME

KiCad E.D.A. 8.99.0-2230-g1cc11bc589

Document

ACCURATE 2 Evaluation Board
 /ACCURATE ASIC/

Designer
 Drawn by Liverud, Consani
 Checked by
 Last Mod. 2025-01-22
 File: ACCURATE ASIC.kicad_sch

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Sheet: 5 of 6

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