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MCUXpresso SDK API Reference Manual

NXP Semiconductors



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Chapter 1

Introduction

The MCUXpresso Software Development Kit (MCUXpresso SDK) is a collection of software enablement for NXP Microcontrollers that includes peripheral drivers, multicore support and integrated RTOS support for FreeRTOS™. In addition to the base enablement, the MCUXpresso SDK is augmented with demo applications, driver example projects, and API documentation to help users quickly leverage the support provided by MCUXpresso SDK. The [MCUXpresso SDK Web Builder](#) is available to provide access to all MCUXpresso SDK packages. See the *MCUXpresso Software Development Kit (SDK) Release Notes* (document MCUXSDKRN) in the Supported Devices section at [MCUXpresso-SDK: Software Development Kit for MCUXpresso](#) for details.

The MCUXpresso SDK is built with the following runtime software components:

- Arm® and DSP standard libraries, and CMSIS-compliant device header files which provide direct access to the peripheral registers.
- Peripheral drivers that provide stateless, high-performance, ease-of-use APIs. Communication drivers provide higher-level transactional APIs for a higher-performance option.
- RTOS wrapper driver built on top of MCUXpresso SDK peripheral drivers and leverage native RTOS services to better comply to the RTOS cases.
- Real time operation systems (RTOS) for FreeRTOS OS.
- Stacks and middleware in source or object formats including:
 - CMSIS-DSP, a suite of common signal processing functions.
 - The MCUXpresso SDK comes complete with software examples demonstrating the usage of the peripheral drivers, RTOS wrapper drivers, middleware, and RTOSes.

All demo applications and driver examples are provided with projects for the following toolchains:

- IAR Embedded Workbench
- GNU Arm Embedded Toolchain

The peripheral drivers and RTOS driver wrappers can be used across multiple devices within the product family without modification. The configuration items for each driver are encapsulated into C language data structures. Device-specific configuration information is provided as part of the MCUXpresso SDK and need not be modified by the user. If necessary, the user is able to modify the peripheral driver and RTOS wrapper driver configuration during runtime. The driver examples demonstrate how to configure the drivers by passing the proper configuration data to the APIs. The folder structure is organized to reduce the total number of includes required to compile a project.

The rest of this document describes the API references in detail for the peripheral drivers and RTOS wrapper drivers. For the latest version of this and other MCUXpresso SDK documents, see the mcuxpresso.nxp.com/apidoc/.

Deliverable	Location
Demo Applications	<install_dir>/boards/<board_name>/demo_apps
Driver Examples	<install_dir>/boards/<board_name>/driver_examples
Documentation	<install_dir>/docs
Middleware	<install_dir>/middleware
Drivers	<install_dir>/<device_name>/drivers/
CMSIS Standard Arm Cortex-M Headers, math and DSP Libraries	<install_dir>/CMSIS
Device Startup and Linker	<install_dir>/<device_name>/<toolchain>/
MCUXpresso SDK Utilities	<install_dir>/devices/<device_name>/utilities
RTOS Kernel Code	<install_dir>/rtos

MCUXpresso SDK Folder Structure

Chapter 2

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Chapter 3

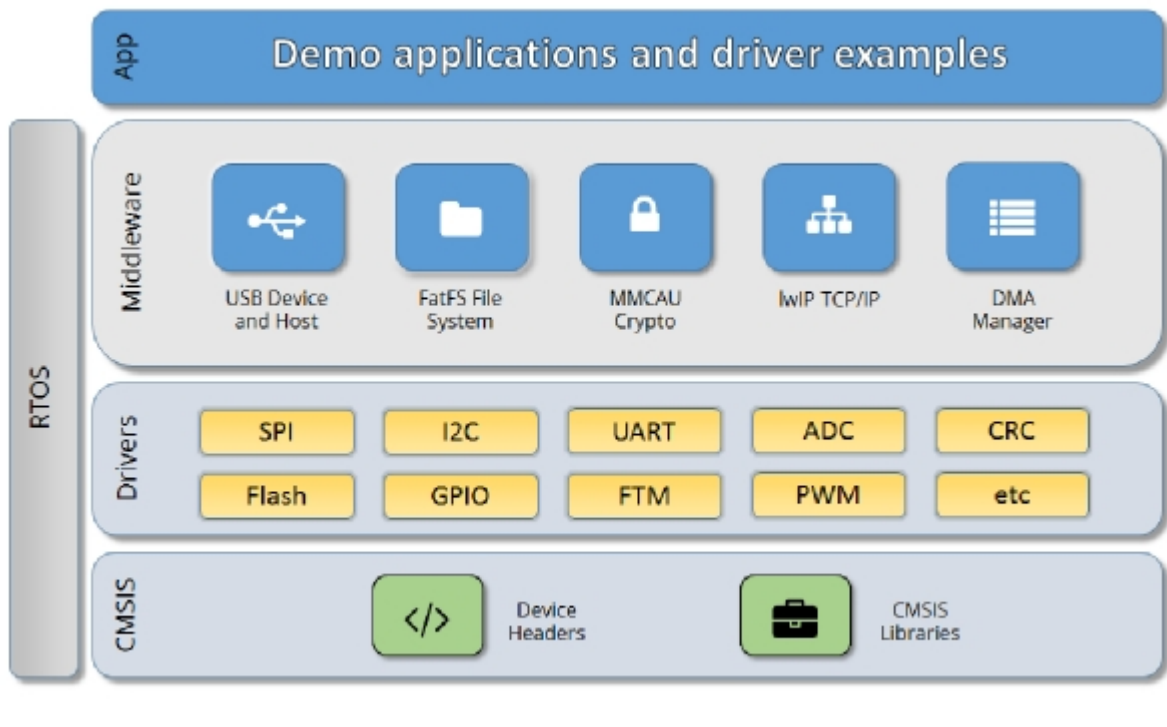
Architectural Overview

This chapter provides the architectural overview for the MCUXpresso Software Development Kit (MCUXpresso SDK). It describes each layer within the architecture and its associated components.

Overview

The MCUXpresso SDK architecture consists of five key components listed below.

1. The Arm Cortex Microcontroller Software Interface Standard (CMSIS) CORE compliance device-specific header files, SOC Header, and CMSIS math/DSP libraries.
2. Peripheral Drivers
3. Real-time Operating Systems (RTOS)
4. Stacks and Middleware that integrate with the MCUXpresso SDK
5. Demo Applications based on the MCUXpresso SDK



MCUXpresso SDK Block Diagram

MCU header files

Each supported MCU device in the MCUXpresso SDK has an overall System-on Chip (SoC) memory-

mapped header file. This header file contains the memory map and register base address for each peripheral and the IRQ vector table with associated vector numbers. The overall SoC header file provides access to the peripheral registers through pointers and predefined bit masks. In addition to the overall SoC memory-mapped header file, the MCUXpresso SDK includes a feature header file for each device. The feature header file allows NXP to deliver a single software driver for a given peripheral. The feature file ensures that the driver is properly compiled for the target SOC.

CMSIS Support

Along with the SoC header files and peripheral extension header files, the MCUXpresso SDK also includes common CMSIS header files for the Arm Cortex-M core and the math and DSP libraries from the latest CMSIS release. The CMSIS DSP library source code is also included for reference.

MCUXpresso SDK Peripheral Drivers

The MCUXpresso SDK peripheral drivers mainly consist of low-level functional APIs for the MCU product family on-chip peripherals and also of high-level transactional APIs for some bus drivers/DM-A driver/eDMA driver to quickly enable the peripherals and perform transfers.

All MCUXpresso SDK peripheral drivers only depend on the CMSIS headers, device feature files, `fsl_common.h`, and `fsl_clock.h` files so that users can easily pull selected drivers and their dependencies into projects. With the exception of the clock/power-relevant peripherals, each peripheral has its own driver. Peripheral drivers handle the peripheral clock gating/ungating inside the drivers during initialization and deinitialization respectively.

Low-level functional APIs provide common peripheral functionality, abstracting the hardware peripheral register accesses into a set of stateless basic functional operations. These APIs primarily focus on the control, configuration, and function of basic peripheral operations. The APIs hide the register access details and various MCU peripheral instantiation differences so that the application can be abstracted from the low-level hardware details. The API prototypes are intentionally similar to help ensure easy portability across supported MCUXpresso SDK devices.

Transactional APIs provide a quick method for customers to utilize higher-level functionality of the peripherals. The transactional APIs utilize interrupts and perform asynchronous operations without user intervention. Transactional APIs operate on high-level logic that requires data storage for internal operation context handling. However, the Peripheral Drivers do not allocate this memory space. Rather, the user passes in the memory to the driver for internal driver operation. Transactional APIs ensure the NVIC is enabled properly inside the drivers. The transactional APIs do not meet all customer needs, but provide a baseline for development of custom user APIs.

Note that the transactional drivers never disable an NVIC after use. This is due to the shared nature of interrupt vectors on devices. It is up to the user to ensure that NVIC interrupts are properly disabled after usage is complete.

Interrupt handling for transactional APIs

A double weak mechanism is introduced for drivers with transactional API. The double weak indicates two levels of weak vector entries. See the examples below:

```
PUBWEAK SPI0_IRQHandler
PUBWEAK SPI0_DriverIRQHandler
SPI0_IRQHandler
```

```
LDR    R0, =SPI0_DriverIRQHandler
BX     R0
```

The first level of the weak implementation are the functions defined in the vector table. In the devices/⟨DEVICE_NAME⟩/⟨TOOLCHAIN⟩/startup_⟨DEVICE_NAME⟩.s/.S file, the implementation of the first layer weak function calls the second layer of weak function. The implementation of the second layer weak function (ex. SPI0_DriverIRQHandler) jumps to itself (B). The MCUXpresso SDK drivers with transactional APIs provide the reimplement of the second layer function inside of the peripheral driver. If the MCUXpresso SDK drivers with transactional APIs are linked into the image, the SPI0_DriverIRQHandler is replaced with the function implemented in the MCUXpresso SDK SPI driver.

The reason for implementing the double weak functions is to provide a better user experience when using the transactional APIs. For drivers with a transactional function, call the transactional APIs and the drivers complete the interrupt-driven flow. Users are not required to redefine the vector entries out of the box. At the same time, if users are not satisfied by the second layer weak function implemented in the MCUXpresso SDK drivers, users can redefine the first layer weak function and implement their own interrupt handler functions to suit their implementation.


The limitation of the double weak mechanism is that it cannot be used for peripherals that share the same vector entry. For this use case, redefine the first layer weak function to enable the desired peripheral interrupt functionality. For example, if the MCU's UART0 and UART1 share the same vector entry, redefine the UART0_UART1_IRQHandler according to the use case requirements.

Feature Header Files

The peripheral drivers are designed to be reusable regardless of the peripheral functional differences from one MCU device to another. An overall Peripheral Feature Header File is provided for the MCUXpresso SDK-supported MCU device to define the features or configuration differences for each sub-family device.

Application

See the *Getting Started with MCUXpresso SDK* document (MCUXSDKGSUG).



Chapter 4

AUDIOMIX Driver

AUDIOMIX driver provides APIs to control AUDIOMIX clock.

Chapter 5

Clock Driver

5.1 Overview

The MCUXpresso SDK provides APIs for MCUXpresso SDK devices' clock operation.

The clock driver supports:

- Clock generator (PLL, FLL, and so on) configuration
- Clock mux and divider configuration
- Getting clock frequency

Data Structures

- struct [ccm_analog_frac_pll_config_t](#)
Fractional-N PLL configuration. [More...](#)
- struct [ccm_analog_integer_pll_config_t](#)
Integer PLL configuration. [More...](#)

Macros

- #define [OSC24M_CLK_FREQ](#) 24000000U
XTAL 24M clock frequency.
- #define [CLKPAD_FREQ](#) 0U
pad clock frequency.
- #define [ECSPI_CLOCKS](#)
Clock ip name array for ECSPI.
- #define [EDMA_CLOCKS](#)
Clock ip name array for EDMA.
- #define [ENET_CLOCKS](#)
Clock ip name array for ENET.
- #define [ENETQOS_CLOCKS](#)
Clock ip name array for ENET_QOS.
- #define [FLEXCAN_CLOCKS](#)
Clock ip name array for FLEXCAN.
- #define [GPIO_CLOCKS](#)
Clock ip name array for GPIO.
- #define [GPT_CLOCKS](#)
Clock ip name array for GPT.
- #define [I2C_CLOCKS](#)
Clock ip name array for I2C.
- #define [IOMUX_CLOCKS](#)
Clock ip name array for IOMUX.
- #define [IPMUX_CLOCKS](#)
Clock ip name array for IPMUX.
- #define [PWM_CLOCKS](#)
Clock ip name array for PWM.

- #define **RDC_CLOCKS**
Clock ip name array for RDC.
- #define **SAI_CLOCKS**
Clock ip name array for SAI.
- #define **RDC_SEMA42_CLOCKS**
Clock ip name array for RDC SEMA42.
- #define **UART_CLOCKS**
Clock ip name array for UART.
- #define **USDHC_CLOCKS**
Clock ip name array for USDHC.
- #define **WDOG_CLOCKS**
Clock ip name array for WDOG.
- #define **TMU_CLOCKS**
Clock ip name array for TEMPSENSOR.
- #define **SDMA_CLOCKS**
Clock ip name array for SDMA.
- #define **MU_CLOCKS**
Clock ip name array for MU.
- #define **QSPI_CLOCKS**
Clock ip name array for QSPI.
- #define **PDM_CLOCKS**
Clock ip name array for PDM.
- #define **ASRC_CLOCKS**
Clock ip name array for ASRC.
- #define **CCM_BIT_FIELD_EXTRACTION**(val, mask, shift) (((val) & (mask)) >> (shift))
CCM reg macros to extract corresponding registers bit field.
- #define **CCM_REG_OFF**(root, off) (*((volatile uint32_t *)((uintptr_t)(root) + (off))))
CCM reg macros to map corresponding registers.
- #define **AUDIO_PLL1_GEN_CTRL_OFFSET** 0x00
CCM Analog registers offset.
- #define **CCM_ANALOG_TUPLE**(reg, shift) (((reg)&0xFFFFU) << 16U | ((shift)))
CCM ANALOG tuple macros to map corresponding registers and bit fields.
- #define **CLOCK_GATE_IN_AUDIOMIX** (1U)
CCM CCGR and root tuple.
- #define **AUDIOMIX_TUPLE**(offset, gate, root) (((**CLOCK_GATE_IN_AUDIOMIX**) << 28U) | ((offset)&0xFU) << 24U | (((gate)&0xFFU) << 16U) | ((root)&0xFFFFU))
audio mix CCGR
- #define **kCLOCK_CoreSysClk** **kCLOCK_CoreM7Clk**
For compatible with other platforms without CCM.
- #define **CLOCK_GetCoreSysClkFreq** **CLOCK_GetCoreM7Freq**
For compatible with other platforms without CCM.

Enumerations

- enum **clock_name_t** {
kCLOCK_CoreM7Clk,
kCLOCK_AxiClk,
kCLOCK_AhbClk,
kCLOCK_IpgClk,
kCLOCK_PerClk }

- Clock name used to get clock frequency.*
- enum `clock_ip_name_t` { ,

```

kCLOCK_Debug = CCM_TUPLE(4U, 32U),
kCLOCK_Dram = CCM_TUPLE(5U, 64U),
kCLOCK_Ecspi1 = CCM_TUPLE(7U, 101U),
kCLOCK_Ecspi2 = CCM_TUPLE(8U, 102U),
kCLOCK_Ecspi3 = CCM_TUPLE(9U, 131U),
kCLOCK_Enet1 = CCM_TUPLE(10U, 17U),
kCLOCK_Gpio1 = CCM_TUPLE(11U, 33U),
kCLOCK_Gpio2 = CCM_TUPLE(12U, 33U),
kCLOCK_Gpio3 = CCM_TUPLE(13U, 33U),
kCLOCK_Gpio4 = CCM_TUPLE(14U, 33U),
kCLOCK_Gpio5 = CCM_TUPLE(15U, 33U),
kCLOCK_Gpt1 = CCM_TUPLE(16U, 107U),
kCLOCK_Gpt2 = CCM_TUPLE(17U, 108U),
kCLOCK_Gpt3 = CCM_TUPLE(18U, 109U),
kCLOCK_Gpt4 = CCM_TUPLE(19U, 110U),
kCLOCK_Gpt5 = CCM_TUPLE(20U, 111U),
kCLOCK_Gpt6 = CCM_TUPLE(21U, 112U),
kCLOCK_I2c1 = CCM_TUPLE(23U, 90U),
kCLOCK_I2c2 = CCM_TUPLE(24U, 91U),
kCLOCK_I2c3 = CCM_TUPLE(25U, 92U),
kCLOCK_I2c4 = CCM_TUPLE(26U, 93U),
kCLOCK_I2c5 = CCM_TUPLE(51U, 73U),
kCLOCK_I2c6 = CCM_TUPLE(52U, 74U),
kCLOCK_Can1 = CCM_TUPLE(53U, 68U),
kCLOCK_Can2 = CCM_TUPLE(54U, 69U),
kCLOCK_Enet_Qos = CCM_TUPLE(59U, 81U),
kCLOCK_Iomux = CCM_TUPLE(27U, 33U),
kCLOCK_Ipmux1 = CCM_TUPLE(28U, 33U),
kCLOCK_Ipmux2 = CCM_TUPLE(29U, 33U),
kCLOCK_Ipmux3 = CCM_TUPLE(30U, 33U),
kCLOCK_Mu = CCM_TUPLE(33U, 33U),
kCLOCK_Ocram = CCM_TUPLE(35U, 33U),
kCLOCK_OcramS = CCM_TUPLE(36U, 32U),
kCLOCK_Pwm1 = CCM_TUPLE(40U, 103U),
kCLOCK_Pwm2 = CCM_TUPLE(41U, 104U),
kCLOCK_Pwm3 = CCM_TUPLE(42U, 105U),
kCLOCK_Pwm4 = CCM_TUPLE(43U, 106U),
kCLOCK_Qspi = CCM_TUPLE(47U, 87U),
kCLOCK_Nand = CCM_TUPLE(48U, 86U),
kCLOCK_Rdc = CCM_TUPLE(49U, 33U),
kCLOCK_Sdma1 = CCM_TUPLE(58U, 33U),
kCLOCK_Sec_Debug = CCM_TUPLE(60U, 33U),
kCLOCK_Sema42_1 = CCM_TUPLE(61U, 33U),
kCLOCK_Sema42_2 = CCM_TUPLE(62U, 33U),
kCLOCK_Sim_enet = CCM_TUPLE(64U, 17U),
kCLOCK_Sim_m = CCM_TUPLE(65U, 32U),
kCLOCK_Sim_main = CCM_TUPLE(66U, 32U),
kCLOCK_Sim_s = CCM_TUPLE(67U, 32U),
kCLOCK_Sim_wakeup = CCM_TUPLE(68U, 32U),

```

```
kCLOCK_Ocram_A = AUDIOMIX_TUPLE(4U, 0U, 0xFFFF) }
```

CCM CCGR gate control.

- enum `clock_root_control_t` {


```

kCLOCK_RootM7 = (uintptr_t)(amp(ccm)->ROOT[1].TARGET_ROOT),
kCLOCK_RootHsioAxi = (uintptr_t)(amp(ccm)->ROOT[7].TARGET_ROOT),
kCLOCK_RootMainAxi = (uintptr_t)(amp(ccm)->ROOT[16].TARGET_ROOT),
kCLOCK_RootEnetAxi = (uintptr_t)(amp(ccm)->ROOT[17].TARGET_ROOT),
kCLOCK_RootNandUsdhcBus = (uintptr_t)(amp(ccm)->ROOT[18].TARGET_ROOT),
kCLOCK_RootVpuBus = (uintptr_t)(amp(ccm)->ROOT[19].TARGET_ROOT),
kCLOCK_RootMediaAxi = (uintptr_t)(amp(ccm)->ROOT[20].TARGET_ROOT),
kCLOCK_RootMediaApb = (uintptr_t)(amp(ccm)->ROOT[21].TARGET_ROOT),
kCLOCK_RootHdmiApb = (uintptr_t)(amp(ccm)->ROOT[22].TARGET_ROOT),
kCLOCK_RootNoc = (uintptr_t)(amp(ccm)->ROOT[26].TARGET_ROOT),
kCLOCK_RootAhb = (uintptr_t)(amp(ccm)->ROOT[32].TARGET_ROOT),
kCLOCK_RootIpg = (uintptr_t)(amp(ccm)->ROOT[33].TARGET_ROOT),
kCLOCK_RootAudioAhb = (uintptr_t)(amp(ccm)->ROOT[34].TARGET_ROOT),
kCLOCK_RootAudioIpg = (uintptr_t)(amp(ccm)->ROOT[35].TARGET_ROOT),
kCLOCK_RootDramAlt = (uintptr_t)(amp(ccm)->ROOT[64].TARGET_ROOT),
kCLOCK_RootFlexCan1 = (uintptr_t)(amp(ccm)->ROOT[68].TARGET_ROOT),
kCLOCK_RootFlexCan2 = (uintptr_t)(amp(ccm)->ROOT[69].TARGET_ROOT),
kCLOCK_RootSai1 = (uintptr_t)(amp(ccm)->ROOT[75].TARGET_ROOT),
kCLOCK_RootSai2 = (uintptr_t)(amp(ccm)->ROOT[76].TARGET_ROOT),
kCLOCK_RootSai3 = (uintptr_t)(amp(ccm)->ROOT[77].TARGET_ROOT),
kCLOCK_RootSai5 = (uintptr_t)(amp(ccm)->ROOT[79].TARGET_ROOT),
kCLOCK_RootSai6 = (uintptr_t)(amp(ccm)->ROOT[80].TARGET_ROOT),
kCLOCK_RootSai7 = (uintptr_t)(amp(ccm)->ROOT[134].TARGET_ROOT),
kCLOCK_RootEnetQos = (uintptr_t)(amp(ccm)->ROOT[81].TARGET_ROOT),
kCLOCK_RootEnetQosTimer = (uintptr_t)(amp(ccm)->ROOT[82].TARGET_ROOT),
kCLOCK_RootEnetRef = (uintptr_t)(amp(ccm)->ROOT[83].TARGET_ROOT),
kCLOCK_RootEnetTimer = (uintptr_t)(amp(ccm)->ROOT[84].TARGET_ROOT),
kCLOCK_RootEnetPhy = (uintptr_t)(amp(ccm)->ROOT[85].TARGET_ROOT),
kCLOCK_RootNand = (uintptr_t)(amp(ccm)->ROOT[86].TARGET_ROOT),
kCLOCK_RootQspi = (uintptr_t)(amp(ccm)->ROOT[87].TARGET_ROOT),
kCLOCK_RootUsdhc1 = (uintptr_t)(amp(ccm)->ROOT[88].TARGET_ROOT),
kCLOCK_RootUsdhc2 = (uintptr_t)(amp(ccm)->ROOT[89].TARGET_ROOT),
kCLOCK_RootUsdhc3 = (uintptr_t)(amp(ccm)->ROOT[121].TARGET_ROOT),
kCLOCK_RootI2c1 = (uintptr_t)(amp(ccm)->ROOT[90].TARGET_ROOT),
kCLOCK_RootI2c2 = (uintptr_t)(amp(ccm)->ROOT[91].TARGET_ROOT),
kCLOCK_RootI2c3 = (uintptr_t)(amp(ccm)->ROOT[92].TARGET_ROOT),
kCLOCK_RootI2c4 = (uintptr_t)(amp(ccm)->ROOT[93].TARGET_ROOT),
kCLOCK_RootI2c5 = (uintptr_t)(amp(ccm)->ROOT[73].TARGET_ROOT),
kCLOCK_RootI2c6 = (uintptr_t)(amp(ccm)->ROOT[74].TARGET_ROOT),
kCLOCK_RootUart1 = (uintptr_t)(amp(ccm)->ROOT[94].TARGET_ROOT),
kCLOCK_RootUart2 = (uintptr_t)(amp(ccm)->ROOT[95].TARGET_ROOT),
kCLOCK_RootUart3 = (uintptr_t)(amp(ccm)->ROOT[96].TARGET_ROOT),
kCLOCK_RootUart4 = (uintptr_t)(amp(ccm)->ROOT[97].TARGET_ROOT),
kCLOCK_RootGic = (uintptr_t)(amp(ccm)->ROOT[100].TARGET_ROOT),
kCLOCK_RootEcspi1 = (uintptr_t)(amp(ccm)->ROOT[101].TARGET_ROOT),
kCLOCK_RootEcspi2 = (uintptr_t)(amp(ccm)->ROOT[102].TARGET_ROOT),
kCLOCK_RootEcspi3 = (uintptr_t)(amp(ccm)->ROOT[123].TARGET_ROOT),
kCLOCK_RootPwm1 = (uintptr_t)(amp(ccm)->ROOT[103].TARGET_ROOT),
kCLOCK_RootPwm2 = (uintptr_t)(amp(ccm)->ROOT[104].TARGET_ROOT),

```

```
kCLOCK_RootPdm = (uintptr_t)(amp(CCM)->ROOT[132].TARGET_ROOT) }
```

ccm root name used to get clock frequency.

- enum clock_rootmux_m7_clk_sel_t {
 - kCLOCK_M7RootmuxOsc24M = 0U,
 - kCLOCK_M7RootmuxSysPll2Div5 = 1U,
 - kCLOCK_M7RootmuxSysPll2Div4 = 2U,
 - kCLOCK_M7RootmuxSysVpuPll = 3U,
 - kCLOCK_M7RootmuxSysPll1 = 4U,
 - kCLOCK_M7RootmuxAudioPll1 = 5U,
 - kCLOCK_M7RootmuxVideoPll1 = 6U,
 - kCLOCK_M7RootmuxSysPll3 = 7U }

Root clock select enumeration for ARM Cortex-M7 core.
- enum clock_rootmux_axi_clk_sel_t {
 - kCLOCK_AxiRootmuxOsc24M = 0U,
 - kCLOCK_AxiRootmuxSysPll2Div3 = 1U,
 - kCLOCK_AxiRootmuxSysPll1 = 2U,
 - kCLOCK_AxiRootmuxSysPll2Div4 = 3U,
 - kCLOCK_AxiRootmuxSysPll2 = 4U,
 - kCLOCK_AxiRootmuxAudioPll1 = 5U,
 - kCLOCK_AxiRootmuxVideoPll1 = 6U,
 - kCLOCK_AxiRootmuxSysPll1Div8 = 7U }

Root clock select enumeration for MAIN AXI bus.
- enum clock_rootmux_ahb_clk_sel_t {
 - kCLOCK_AhbRootmuxOsc24M = 0U,
 - kCLOCK_AhbRootmuxSysPll1Div6 = 1U,
 - kCLOCK_AhbRootmuxSysPll1 = 2U,
 - kCLOCK_AhbRootmuxSysPll1Div2 = 3U,
 - kCLOCK_AhbRootmuxSysPll2Div8 = 4U,
 - kCLOCK_AhbRootmuxSysPll3 = 5U,
 - kCLOCK_AhbRootmuxAudioPll1 = 6U,
 - kCLOCK_AhbRootmuxVideoPll1 = 7U }

Root clock select enumeration for AHB bus.
- enum clock_rootmux_audio_ahb_clk_sel_t {
 - kCLOCK_AudioAhbRootmuxOsc24M = 0U,
 - kCLOCK_AudioAhbRootmuxSysPll2Div2 = 1U,
 - kCLOCK_AudioAhbRootmuxSysPll1 = 2U,
 - kCLOCK_AudioAhbRootmuxSysPll2 = 3U,
 - kCLOCK_AudioAhbRootmuxSysPll2Div6 = 4U,
 - kCLOCK_AudioAhbRootmuxSysPll3 = 5U,
 - kCLOCK_AudioAhbRootmuxAudioPll1 = 6U,
 - kCLOCK_AudioAhbRootmuxVideoPll1 = 7U }

Root clock select enumeration for Audio AHB bus.
- enum clock_rootmux_qspi_clk_sel_t {

```

kCLOCK_QspiRootmuxOsc24M = 0U,
kCLOCK_QspiRootmuxSysPll1Div2 = 1U,
kCLOCK_QspiRootmuxSysPll2Div3 = 2U,
kCLOCK_QspiRootmuxSysPll2Div2 = 3U,
kCLOCK_QspiRootmuxAudioPll2 = 4U,
kCLOCK_QspiRootmuxSysPll1Div3 = 5U,
kCLOCK_QspiRootmuxSysPll3 = 6,
kCLOCK_QspiRootmuxSysPll1Div8 = 7U }

```

Root clock select enumeration for QSPI peripheral.

- enum `clock_rootmux_ecspi_clk_sel_t` {
`kCLOCK_EcspiRootmuxOsc24M = 0U,`
`kCLOCK_EcspiRootmuxSysPll2Div5 = 1U,`
`kCLOCK_EcspiRootmuxSysPll1Div20 = 2U,`
`kCLOCK_EcspiRootmuxSysPll1Div5 = 3U,`
`kCLOCK_EcspiRootmuxSysPll1 = 4U,`
`kCLOCK_EcspiRootmuxSysPll3 = 5U,`
`kCLOCK_EcspiRootmuxSysPll2Div4 = 6U,`
`kCLOCK_EcspiRootmuxAudioPll2 = 7U }`

Root clock select enumeration for ECSPi peripheral.

- enum `clock_rootmux_enet_axi_clk_sel_t` {
`kCLOCK_EnetAxiRootmuxOsc24M = 0U,`
`kCLOCK_EnetAxiRootmuxSysPll1Div3 = 1U,`
`kCLOCK_EnetAxiRootmuxSysPll1 = 2U,`
`kCLOCK_EnetAxiRootmuxSysPll2Div4 = 3U,`
`kCLOCK_EnetAxiRootmuxSysPll2Div5 = 4U,`
`kCLOCK_EnetAxiRootmuxAudioPll1 = 5U,`
`kCLOCK_EnetAxiRootmuxVideoPll1 = 6U,`
`kCLOCK_EnetAxiRootmuxSysPll3 = 7U }`

Root clock select enumeration for ENET AXI bus.

- enum `clock_rootmux_enet_qos_clk_sel_t` {
`kCLOCK_EnetQosRootmuxOsc24M = 0U,`
`kCLOCK_EnetQosRootmuxSysPll2Div8 = 1U,`
`kCLOCK_EnetQosRootmuxSysPll2Div20 = 2U,`
`kCLOCK_EnetQosRootmuxSysPll2Div10 = 3U,`
`kCLOCK_EnetQosRootmuxSysPll1Div5 = 4U,`
`kCLOCK_EnetQosRootmuxAudioPll1 = 5U,`
`kCLOCK_EnetQosRootmuxVideoPll1 = 6U,`
`kCLOCK_EnetQosRootmuxExtClk4 = 7U }`

Root clock select enumeration for ENET QOS Clcok.

- enum `clock_rootmux_enet_ref_clk_sel_t` {

```

kCLOCK_EnetRefRootmuxOsc24M = 0U,
kCLOCK_EnetRefRootmuxSysPll2Div8 = 1U,
kCLOCK_EnetRefRootmuxSysPll2Div20 = 2U,
kCLOCK_EnetRefRootmuxSysPll2Div10 = 3U,
kCLOCK_EnetRefRootmuxSysPll1Div5 = 4U,
kCLOCK_EnetRefRootmuxAudioPll1 = 5U,
kCLOCK_EnetRefRootmuxVideoPll1 = 6U,
kCLOCK_EnetRefRootmuxExtClk4 = 7U }

```

Root clock select enumeration for ENET REF Clcok.

- enum `clock_rootmux_enet_qos_timer_clk_sel_t` {
`kCLOCK_EnetQosTimerRootmuxOsc24M` = 0U,
`kCLOCK_EnetQosTimerRootmuxSysPll2Div10` = 1U,
`kCLOCK_EnetQosTimerRootmuxAudioPll1` = 2U,
`kCLOCK_EnetQosTimerRootmuxExtClk1` = 3U,
`kCLOCK_EnetQosTimerRootmuxExtClk2` = 4U,
`kCLOCK_EnetQosTimerRootmuxExtClk3` = 5U,
`kCLOCK_EnetQosTimerRootmuxExtClk4` = 6U,
`kCLOCK_EnetQosTimerRootmuxVideoPll1` = 7U }

Root clock select enumeration for ENET QOS TIMER Clcok.

- enum `clock_rootmux_enet_timer_clk_sel_t` {
`kCLOCK_EnetTimerRootmuxOsc24M` = 0U,
`kCLOCK_EnetTimerRootmuxSysPll2Div10` = 1U,
`kCLOCK_EnetTimerRootmuxAudioPll1` = 2U,
`kCLOCK_EnetTimerRootmuxExtClk1` = 3U,
`kCLOCK_EnetTimerRootmuxExtClk2` = 4U,
`kCLOCK_EnetTimerRootmuxExtClk3` = 5U,
`kCLOCK_EnetTimerRootmuxExtClk4` = 6U,
`kCLOCK_EnetTimerRootmuxVideoPll1` = 7U }

Root clock select enumeration for ENET TIMER Clcok.

- enum `clock_rootmux_enet_phy_clk_sel_t` {
`kCLOCK_EnetPhyRootmuxOsc24M` = 0U,
`kCLOCK_EnetPhyRootmuxSysPll2Div20` = 1U,
`kCLOCK_EnetPhyRootmuxSysPll2Div8` = 2U,
`kCLOCK_EnetPhyRootmuxSysPll2Div5` = 3U,
`kCLOCK_EnetPhyRootmuxSysPll2Div2` = 4U,
`kCLOCK_EnetPhyRootmuxAudioPll1` = 5U,
`kCLOCK_EnetPhyRootmuxVideoPll1` = 6U,
`kCLOCK_EnetPhyRootmuxAudioPll2` = 7U }

Root clock select enumeration for ENET PHY Clcok.

- enum `clock_rootmux_flexcan_clk_sel_t` {

```

kCLOCK_FlexCanRootmuxOsc24M = 0U,
kCLOCK_FlexCanRootmuxSysPll2Div5 = 1U,
kCLOCK_FlexCanRootmuxSysPll1Div20 = 2U,
kCLOCK_FlexCanRootmuxSysPll1Div5 = 3U,
kCLOCK_FlexCanRootmuxSysPll1 = 4U,
kCLOCK_FlexCanRootmuxSysPll3 = 5U,
kCLOCK_FlexCanRootmuxSysPll2Div4 = 6U,
kCLOCK_FlexCanRootmuxAudioPll2 = 7U }

```

Root clock select enumeration for FLEXCAN peripheral.

- enum clock_rootmux_i2c_clk_sel_t {


```

kCLOCK_I2cRootmuxOsc24M = 0U,
kCLOCK_I2cRootmuxSysPll1Div5 = 1U,
kCLOCK_I2cRootmuxSysPll2Div20 = 2U,
kCLOCK_I2cRootmuxSysPll3 = 3U,
kCLOCK_I2cRootmuxAudioPll1 = 4U,
kCLOCK_I2cRootmuxVideoPll1 = 5U,
kCLOCK_I2cRootmuxAudioPll2 = 6U,
kCLOCK_I2cRootmuxSysPll1Div6 = 7U }

```

Root clock select enumeration for I2C peripheral.

- enum clock_rootmux_uart_clk_sel_t {


```

kCLOCK_UartRootmuxOsc24M = 0U,
kCLOCK_UartRootmuxSysPll1Div10 = 1U,
kCLOCK_UartRootmuxSysPll2Div5 = 2U,
kCLOCK_UartRootmuxSysPll2Div10 = 3U,
kCLOCK_UartRootmuxSysPll3 = 4U,
kCLOCK_UartRootmuxExtClk2 = 5U,
kCLOCK_UartRootmuxExtClk34 = 6U,
kCLOCK_UartRootmuxAudioPll2 = 7U }

```

Root clock select enumeration for UART peripheral.

- enum clock_rootmux_gpt_t {


```

kCLOCK_GptRootmuxOsc24M = 0U,
kCLOCK_GptRootmuxSystemPll2Div10 = 1U,
kCLOCK_GptRootmuxSysPll1Div2 = 2U,
kCLOCK_GptRootmuxSysPll1Div20 = 3U,
kCLOCK_GptRootmuxVideoPll1 = 4U,
kCLOCK_GptRootmuxSystemPll1Div10 = 5U,
kCLOCK_GptRootmuxAudioPll1 = 6U,
kCLOCK_GptRootmuxExtClk123 = 7U }

```

Root clock select enumeration for GPT peripheral.

- enum clock_rootmux_wdog_clk_sel_t {

```

kCLOCK_WdogRootmuxOsc24M = 0U,
kCLOCK_WdogRootmuxSysPll1Div6 = 1U,
kCLOCK_WdogRootmuxSysPll1Div5 = 2U,
kCLOCK_WdogRootmuxVpuPll = 3U,
kCLOCK_WdogRootmuxSystemPll2Div8 = 4U,
kCLOCK_WdogRootmuxSystemPll3 = 5U,
kCLOCK_WdogRootmuxSystemPll1Div10 = 6U,
kCLOCK_WdogRootmuxSystemPll2Div6 = 7U }

```

Root clock select enumeration for WDOG peripheral.

- enum `clock_rootmux_Pwm_clk_sel_t` {
`kCLOCK_PwmRootmuxOsc24M` = 0U,
`kCLOCK_PwmRootmuxSysPll2Div10` = 1U,
`kCLOCK_PwmRootmuxSysPll1Div5` = 2U,
`kCLOCK_PwmRootmuxSysPll1Div20` = 3U,
`kCLOCK_PwmRootmuxSystemPll3` = 4U,
`kCLOCK_PwmRootmuxExtClk12` = 5U,
`kCLOCK_PwmRootmuxSystemPll1Div10` = 6U,
`kCLOCK_PwmRootmuxVideoPll1` = 7U }

Root clock select enumeration for PWM peripheral.

- enum `clock_rootmux_sai_clk_sel_t` {
`kCLOCK_SaiRootmuxOsc24M` = 0U,
`kCLOCK_SaiRootmuxAudioPll1` = 1U,
`kCLOCK_SaiRootmuxAudioPll2` = 2U,
`kCLOCK_SaiRootmuxVideoPll1` = 3U,
`kCLOCK_SaiRootmuxSysPll1Div6` = 4U,
`kCLOCK_SaiRootmuxOsc26m` = 5U,
`kCLOCK_SaiRootmuxExtClk1` = 6U,
`kCLOCK_SaiRootmuxExtClk2` = 7U }

Root clock select enumeration for SAI peripheral.

- enum `clock_rootmux_pdm_clk_sel_t` {
`kCLOCK_PdmRootmuxOsc24M` = 0U,
`kCLOCK_PdmRootmuxSysPll2Div10` = 1U,
`kCLOCK_PdmRootmuxAudioPll1` = 2U,
`kCLOCK_PdmRootmuxSysPll1` = 3U,
`kCLOCK_PdmRootmuxSysPll2` = 4U,
`kCLOCK_PdmRootmuxSysPll3` = 5U,
`kCLOCK_PdmRootmuxExtClk3` = 6U,
`kCLOCK_PdmRootmuxAudioPll2` = 7U }

Root clock select enumeration for PDM peripheral.

- enum `clock_rootmux_noc_clk_sel_t` {


```

kCLOCK_NocRootmuxOsc24M = 0U,
kCLOCK_NocRootmuxSysPll1 = 1U,
kCLOCK_NocRootmuxSysPll3 = 2U,
kCLOCK_NocRootmuxSysPll2 = 3U,
kCLOCK_NocRootmuxSysPll2Div2 = 4U,
kCLOCK_NocRootmuxAudioPll1 = 5U,
kCLOCK_NocRootmuxVideoPll1 = 6U,
kCLOCK_NocRootmuxAudioPll2 = 7U }

```

Root clock select enumeration for NOC CLK.

- enum `clock_pll_gate_t` {


```

kCLOCK_ArmPllGate = (uintptr_t)(amp(CCM)->PLL_CTRL[12].PLL_CTRL),
kCLOCK_GpuPllGate = (uintptr_t)(amp(CCM)->PLL_CTRL[13].PLL_CTRL),
kCLOCK_VpuPllGate = (uintptr_t)(amp(CCM)->PLL_CTRL[14].PLL_CTRL),
kCLOCK_DramPllGate = (uintptr_t)(amp(CCM)->PLL_CTRL[15].PLL_CTRL),
kCLOCK_SysPll1Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[16].PLL_CTRL),
kCLOCK_SysPll1Div2Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[17].PLL_CTRL),
kCLOCK_SysPll1Div3Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[18].PLL_CTRL),
kCLOCK_SysPll1Div4Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[19].PLL_CTRL),
kCLOCK_SysPll1Div5Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[20].PLL_CTRL),
kCLOCK_SysPll1Div6Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[21].PLL_CTRL),
kCLOCK_SysPll1Div8Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[22].PLL_CTRL),
kCLOCK_SysPll1Div10Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[23].PLL_CTRL),
kCLOCK_SysPll1Div20Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[24].PLL_CTRL),
kCLOCK_SysPll2Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[25].PLL_CTRL),
kCLOCK_SysPll2Div2Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[26].PLL_CTRL),
kCLOCK_SysPll2Div3Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[27].PLL_CTRL),
kCLOCK_SysPll2Div4Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[28].PLL_CTRL),
kCLOCK_SysPll2Div5Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[29].PLL_CTRL),
kCLOCK_SysPll2Div6Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[30].PLL_CTRL),
kCLOCK_SysPll2Div8Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[31].PLL_CTRL),
kCLOCK_SysPll2Div10Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[32].PLL_CTRL),
kCLOCK_SysPll2Div20Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[33].PLL_CTRL),
kCLOCK_SysPll3Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[34].PLL_CTRL),
kCLOCK_AudioPll1Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[35].PLL_CTRL),
kCLOCK_AudioPll2Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[36].PLL_CTRL),
kCLOCK_VideoPll1Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[37].PLL_CTRL),
kCLOCK_VideoPll2Gate = (uintptr_t)(amp(CCM)->PLL_CTRL[38].PLL_CTRL) }

```

CCM PLL gate control.

- enum `clock_gate_value_t` {


```

kCLOCK_ClockNotNeeded = 0x00U,
kCLOCK_ClockNeededRun = 0x1111U,
kCLOCK_ClockNeededRunWait = 0x2222U,
kCLOCK_ClockNeededAll = 0x3333U }

```

CCM gate control value.

- enum `clock_pll_bypass_ctrl_t` {

```

kCLOCK_AudioPll1BypassCtrl,
kCLOCK_AudioPll2BypassCtrl,
kCLOCK_VideoPll1BypassCtrl,
kCLOCK_DramPllInternalPll1BypassCtrl,
kCLOCK_ArmPllPwrBypassCtrl,
kCLOCK_SysPll1InternalPll1BypassCtrl,
kCLOCK_SysPll2InternalPll1BypassCtrl,
kCLOCK_SysPll3InternalPll1BypassCtrl }

```

PLL control names for PLL bypass.

- enum `clock_pll_clke_t` {


```

kCLOCK_AudioPll1Clke,
kCLOCK_AudioPll2Clke,
kCLOCK_VideoPll1Clke,
kCLOCK_DramPllClke,
kCLOCK_ArmPllClke,
kCLOCK_SystemPll1Clke,
kCLOCK_SystemPll1Div2Clke,
kCLOCK_SystemPll1Div3Clke,
kCLOCK_SystemPll1Div4Clke,
kCLOCK_SystemPll1Div5Clke,
kCLOCK_SystemPll1Div6Clke,
kCLOCK_SystemPll1Div8Clke,
kCLOCK_SystemPll1Div10Clke,
kCLOCK_SystemPll1Div20Clke,
kCLOCK_SystemPll2Clke,
kCLOCK_SystemPll2Div2Clke,
kCLOCK_SystemPll2Div3Clke,
kCLOCK_SystemPll2Div4Clke,
kCLOCK_SystemPll2Div5Clke,
kCLOCK_SystemPll2Div6Clke,
kCLOCK_SystemPll2Div8Clke,
kCLOCK_SystemPll2Div10Clke,
kCLOCK_SystemPll2Div20Clke,
kCLOCK_SystemPll3Clke }

```

PLL clock names for clock enable/disable settings.

- enum `clock_pll_ctrl_t`
- *ANALOG Power down override control.*
- enum {


```

kANALOG_PllRefOsc24M = 0U,
kANALOG_PllPadClk = 1U }

```

PLL reference clock select.

Driver version

- #define `FSL_CLOCK_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 1)`)
CLOCK driver version 2.0.1.

CCM Root Clock Setting

- static void [CLOCK_SetRootMux](#) ([clock_root_control_t](#) rootClk, [uint32_t](#) mux)
Set clock root mux.
- static [uint32_t](#) [CLOCK_GetRootMux](#) ([clock_root_control_t](#) rootClk)
Get clock root mux.
- static void [CLOCK_EnableRoot](#) ([clock_root_control_t](#) rootClk)
Enable clock root.
- static void [CLOCK_DisableRoot](#) ([clock_root_control_t](#) rootClk)
Disable clock root.
- static bool [CLOCK_IsRootEnabled](#) ([clock_root_control_t](#) rootClk)
Check whether clock root is enabled.
- void [CLOCK_UpdateRoot](#) ([clock_root_control_t](#) ccmRootClk, [uint32_t](#) mux, [uint32_t](#) pre, [uint32_t](#) post)
Update clock root in one step, for dynamical clock switching Note: The PRE and POST dividers in this function are the actually divider, software will map it to register value.
- void [CLOCK_SetRootDivider](#) ([clock_root_control_t](#) ccmRootClk, [uint32_t](#) pre, [uint32_t](#) post)
Set root clock divider Note: The PRE and POST dividers in this function are the actually divider, software will map it to register value.
- static [uint32_t](#) [CLOCK_GetRootPreDivider](#) ([clock_root_control_t](#) rootClk)
Get clock root PRE_PODF.
- static [uint32_t](#) [CLOCK_GetRootPostDivider](#) ([clock_root_control_t](#) rootClk)
Get clock root POST_PODF.

CCM Gate Control

- static void [CLOCK_ControlGate](#) ([uintptr_t](#) ccmGate, [clock_gate_value_t](#) control)
Set PLL or CCGR gate control.
- void [CLOCK_EnableClock](#) ([clock_ip_name_t](#) ccmGate)
Enable CCGR clock gate and root clock gate for each module User should set specific gate for each module according to the description of the table of system clocks, gating and override in CCM chapter of reference manual.
- void [CLOCK_DisableClock](#) ([clock_ip_name_t](#) ccmGate)
Disable CCGR clock gate for the each module User should set specific gate for each module according to the description of the table of system clocks, gating and override in CCM chapter of reference manual.

CCM Analog PLL Operatoin Functions

- static void [CLOCK_PowerUpPll](#) ([CCM_ANALOG_Type](#) *base, [clock_pll_ctrl_t](#) pllControl)
Power up PLL.
- static void [CLOCK_PowerDownPll](#) ([CCM_ANALOG_Type](#) *base, [clock_pll_ctrl_t](#) pllControl)
Power down PLL.
- static void [CLOCK_SetPllBypass](#) ([CCM_ANALOG_Type](#) *base, [clock_pll_bypass_ctrl_t](#) pllControl, bool bypass)
PLL bypass setting.
- static bool [CLOCK_IsPllBypassed](#) ([CCM_ANALOG_Type](#) *base, [clock_pll_bypass_ctrl_t](#) pllControl)
Check if PLL is bypassed.
- static bool [CLOCK_IsPllLocked](#) ([CCM_ANALOG_Type](#) *base, [clock_pll_ctrl_t](#) pllControl)
Check if PLL clock is locked.

- static void **CLOCK_EnableAnalogClock** (CCM_ANALOG_Type *base, clock_pll_clke_t pllClock)
Enable PLL clock.
- static void **CLOCK_DisableAnalogClock** (CCM_ANALOG_Type *base, clock_pll_clke_t pllClock)
Disable PLL clock.
- static void **CLOCK_OverridePllClke** (CCM_ANALOG_Type *base, clock_pll_clke_t ovClock, bool override)
Override PLL clock output enable.
- static void **CLOCK_OverridePllPd** (CCM_ANALOG_Type *base, clock_pll_ctrl_t pdClock, bool override)
Override PLL power down.
- void **CLOCK_InitArmPll** (const ccm_analog_integer_pll_config_t *config)
Initializes the ANALOG ARM PLL.
- void **CLOCK_DeinitArmPll** (void)
De-initialize the ARM PLL.
- void **CLOCK_InitSysPll1** (const ccm_analog_integer_pll_config_t *config)
Initializes the ANALOG SYS PLL1.
- void **CLOCK_DeinitSysPll1** (void)
De-initialize the System PLL1.
- void **CLOCK_InitSysPll2** (const ccm_analog_integer_pll_config_t *config)
Initializes the ANALOG SYS PLL2.
- void **CLOCK_DeinitSysPll2** (void)
De-initialize the System PLL2.
- void **CLOCK_InitSysPll3** (const ccm_analog_integer_pll_config_t *config)
Initializes the ANALOG SYS PLL3.
- void **CLOCK_DeinitSysPll3** (void)
De-initialize the System PLL3.
- void **CLOCK_InitAudioPll1** (const ccm_analog_frac_pll_config_t *config)
Initializes the ANALOG AUDIO PLL1.
- void **CLOCK_DeinitAudioPll1** (void)
De-initialize the Audio PLL1.
- void **CLOCK_InitAudioPll2** (const ccm_analog_frac_pll_config_t *config)
Initializes the ANALOG AUDIO PLL2.
- void **CLOCK_DeinitAudioPll2** (void)
De-initialize the Audio PLL2.
- void **CLOCK_InitVideoPll1** (const ccm_analog_frac_pll_config_t *config)
Initializes the ANALOG VIDEO PLL1.
- void **CLOCK_DeinitVideoPll1** (void)
De-initialize the Video PLL1.
- void **CLOCK_InitIntegerPll** (CCM_ANALOG_Type *base, const ccm_analog_integer_pll_config_t *config, clock_pll_ctrl_t type)
Initializes the ANALOG Integer PLL.
- uint32_t **CLOCK_GetIntegerPllFreq** (CCM_ANALOG_Type *base, clock_pll_ctrl_t type, uint32_t refClkFreq, bool pll1Bypass)
Get the ANALOG Integer PLL clock frequency.
- void **CLOCK_InitFracPll** (CCM_ANALOG_Type *base, const ccm_analog_frac_pll_config_t *config, clock_pll_ctrl_t type)
Initializes the ANALOG Fractional PLL.
- uint32_t **CLOCK_GetFracPllFreq** (CCM_ANALOG_Type *base, clock_pll_ctrl_t type, uint32_t

refClkFreq)

Gets the ANALOG Fractional PLL clock frequency.

- uint32_t [CLOCK_GetPllFreq](#) (clock_pll_ctrl_t pll)

Gets PLL clock frequency.

- uint32_t [CLOCK_GetPllRefClkFreq](#) (clock_pll_ctrl_t ctrl)

Gets PLL reference clock frequency.

CCM Get frequency

- uint32_t [CLOCK_GetFreq](#) (clock_name_t clockName)

Gets the clock frequency for a specific clock name.

- uint32_t [CLOCK_GetCoreM7Freq](#) (void)

Get the CCM Cortex M7 core frequency.

- uint32_t [CLOCK_GetAxiFreq](#) (void)

Get the CCM Axi bus frequency.

- uint32_t [CLOCK_GetAhbFreq](#) (void)

Get the CCM Ahb bus frequency.

5.2 Data Structure Documentation

5.2.1 struct ccm_analog_frac_pll_config_t

Note: all the dividers in this configuration structure are the actually divider, software will map it to register value

Data Fields

- uint8_t [refSel](#)
pll reference clock sel
- uint32_t [mainDiv](#)
Value of the 10-bit programmable main-divider, range must be 64~1023.
- uint32_t [dsm](#)
Value of 16-bit DSM.
- uint8_t [preDiv](#)
Value of the 6-bit programmable pre-divider, range must be 1~63.
- uint8_t [postDiv](#)
Value of the 3-bit programmable Scaler, range must be 0~6.

5.2.2 struct ccm_analog_integer_pll_config_t

Note: all the dividers in this configuration structure are the actually divider, software will map it to register value

Data Fields

- uint8_t [refSel](#)

- *pll reference clock sel*
uint32_t [mainDiv](#)
Value of the 10-bit programmable main-divider, range must be 64~1023.
- uint8_t [preDiv](#)
Value of the 6-bit programmable pre-divider, range must be 1~63.
- uint8_t [postDiv](#)
Value of the 3-bit programmable Scaler, range must be 0~6.

5.3 Macro Definition Documentation

5.3.1 #define FSL_CLOCK_DRIVER_VERSION (MAKE_VERSION(2, 0, 1))

5.3.2 #define ECSPI_CLOCKS

Value:

```
{
    kCLOCK_IpInvalid, kCLOCK_Ecspi1, kCLOCK_Ecspi2, \
    kCLOCK_Ecspi3, \
}
```

5.3.3 #define EDMA_CLOCKS

Value:

```
{
    \
    kCLOCK_Edma, \
}
```

5.3.4 #define ENET_CLOCKS

Value:

```
{
    \
    kCLOCK_Enet1, \
}
```

5.3.5 #define ENETQOS_CLOCKS

Value:

```
{
    \
    kCLOCK_Enet_Qos \
}
```

5.3.6 #define FLEXCAN_CLOCKS

Value:

```
{
    kCLOCK_IpInvalid, kCLOCK_Can1, kCLOCK_Can2, \
}
```

5.3.7 #define GPIO_CLOCKS

Value:

```
{
    kCLOCK_IpInvalid, kCLOCK_Gpio1, kCLOCK_Gpio2, \
    kCLOCK_Gpio3, kCLOCK_Gpio4, kCLOCK_Gpio5, \
}
```

5.3.8 #define GPT_CLOCKS

Value:

```
{
    kCLOCK_IpInvalid, kCLOCK_Gpt1, kCLOCK_Gpt2, \
    kCLOCK_Gpt3, kCLOCK_Gpt4, kCLOCK_Gpt5, \
    kCLOCK_Gpt6, \
}
```

5.3.9 #define I2C_CLOCKS

Value:

```
{
    kCLOCK_IpInvalid, kCLOCK_I2c1, kCLOCK_I2c2, \
    kCLOCK_I2c3, kCLOCK_I2c4, kCLOCK_I2c5, \
    kCLOCK_I2c6, \
}
```

5.3.10 #define IOMUX_CLOCKS

Value:

```
{
    kCLOCK_Iomux, \
}
```

5.3.11 #define IPMUX_CLOCKS

Value:

```
{
    kCLOCK_Ipmux1, kCLOCK_Ipmux2, \
    kCLOCK_Ipmux3, \
}
```

5.3.12 #define PWM_CLOCKS

Value:

```
{
    kCLOCK_IpInvalid, kCLOCK_Pwm1, kCLOCK_Pwm2, \
    kCLOCK_Pwm3, kCLOCK_Pwm4, \
}
```

5.3.13 #define RDC_CLOCKS

Value:

```
{
    \
    kCLOCK_Rdc, \
}
```

5.3.14 #define SAI_CLOCKS

Value:

```
{
    kCLOCK_IpInvalid, kCLOCK_Sai1, kCLOCK_Sai2, \
    kCLOCK_Sai3, kCLOCK_IpInvalid, kCLOCK_Sai5, kCLOCK_Sai6, \
    kCLOCK_Sai7 \
}
```

5.3.15 #define RDC_SEMA42_CLOCKS

Value:

```
{
    kCLOCK_IpInvalid, kCLOCK_Sema42_1, kCLOCK_Sema42_2 \
}
```

5.3.16 #define UART_CLOCKS

Value:

```

{
    kCLOCK_IpInvalid, kCLOCK_Uart1, kCLOCK_Uart2,
    kCLOCK_Uart3, kCLOCK_Uart4, \
}

```

5.3.17 #define USDHC_CLOCKS

Value:

```

{
    kCLOCK_IpInvalid, kCLOCK_Usdhc1, kCLOCK_Usdhc2,
    kCLOCK_Usdhc3 \
}

```

5.3.18 #define WDOG_CLOCKS

Value:

```

{
    kCLOCK_IpInvalid, kCLOCK_Wdog1, kCLOCK_Wdog2,
    kCLOCK_Wdog3 \
}

```

5.3.19 #define TMU_CLOCKS

Value:

```

{
    kCLOCK_TempSensor, \
}

```

5.3.20 #define SDMA_CLOCKS

Value:

```

{
    kCLOCK_Sdma1, kCLOCK_Sdma2, kCLOCK_Sdma3, \
}

```

5.3.21 #define MU_CLOCKS

Value:

```
{
    kCLOCK_Mu \
}
```

5.3.22 #define QSPI_CLOCKS

Value:

```
{
    kCLOCK_Qspi \
}
```

5.3.23 #define PDM_CLOCKS

Value:

```
{
    kCLOCK_Pdm \
}
```

5.3.24 #define ASRC_CLOCKS

Value:

```
{
    kCLOCK_Asrc \
}
```

5.3.25 #define kCLOCK_CoreSysClk kCLOCK_CoreM7Clk

5.3.26 #define CLOCK_GetCoreSysClkFreq CLOCK_GetCoreM7Freq

5.4 Enumeration Type Documentation

5.4.1 enum clock_name_t

Enumerator

kCLOCK_CoreM7Clk ARM M7 Core clock.

kCLOCK_AxiClk Main AXI bus clock.
kCLOCK_AhbClk AHB bus clock.
kCLOCK_IpgClk IPG bus clock.
kCLOCK_PerClk Peripheral Clock.

5.4.2 enum clock_ip_name_t

Enumerator

kCLOCK_Debug DEBUG Clock Gate.
kCLOCK_Dram DRAM Clock Gate.
kCLOCK_Ecspi1 ECSPI1 Clock Gate.
kCLOCK_Ecspi2 ECSPI2 Clock Gate.
kCLOCK_Ecspi3 ECSPI3 Clock Gate.
kCLOCK_Enet1 ENET1 Clock Gate.
kCLOCK_Gpio1 GPIO1 Clock Gate.
kCLOCK_Gpio2 GPIO2 Clock Gate.
kCLOCK_Gpio3 GPIO3 Clock Gate.
kCLOCK_Gpio4 GPIO4 Clock Gate.
kCLOCK_Gpio5 GPIO5 Clock Gate.
kCLOCK_Gpt1 GPT1 Clock Gate.
kCLOCK_Gpt2 GPT2 Clock Gate.
kCLOCK_Gpt3 GPT3 Clock Gate.
kCLOCK_Gpt4 GPT4 Clock Gate.
kCLOCK_Gpt5 GPT5 Clock Gate.
kCLOCK_Gpt6 GPT6 Clock Gate.
kCLOCK_I2c1 I2C1 Clock Gate.
kCLOCK_I2c2 I2C2 Clock Gate.
kCLOCK_I2c3 I2C3 Clock Gate.
kCLOCK_I2c4 I2C4 Clock Gate.
kCLOCK_I2c5 I2C5 Clock Gate.
kCLOCK_I2c6 I2C6 Clock Gate.
kCLOCK_Can1 FlexCAN1 Clock Gate.
kCLOCK_Can2 FlexCAN2 Clock Gate.
kCLOCK_Enet_Qos ENET QOS Clock Gate.
kCLOCK_Iomux IOMUX Clock Gate.
kCLOCK_Ipmux1 IPMUX1 Clock Gate.
kCLOCK_Ipmux2 IPMUX2 Clock Gate.
kCLOCK_Ipmux3 IPMUX3 Clock Gate.
kCLOCK_Mu MU Clock Gate.
kCLOCK_Ocram OCRAM Clock Gate.
kCLOCK_OcramS OCRAM S Clock Gate.
kCLOCK_Pwm1 PWM1 Clock Gate.
kCLOCK_Pwm2 PWM2 Clock Gate.

kCLOCK_Pwm3 PWM3 Clock Gate.
kCLOCK_Pwm4 PWM4 Clock Gate.
kCLOCK_Qspi QSPI Clock Gate.
kCLOCK_Nand NAND Clock Gate.
kCLOCK_Rdc RDC Clock Gate.
kCLOCK_Sdma1 SDMA1 Clock Gate.
kCLOCK_Sec_Debug SEC_DEBUG Clock Gate.
kCLOCK_Sema42_1 RDC SEMA42 Clock Gate.
kCLOCK_Sema42_2 RDC SEMA42 Clock Gate.
kCLOCK_Sim_enet SIM_ENET Clock Gate.
kCLOCK_Sim_m SIM_M Clock Gate.
kCLOCK_Sim_main SIM_MAIN Clock Gate.
kCLOCK_Sim_s SIM_S Clock Gate.
kCLOCK_Sim_wakeup SIM_WAKEUP Clock Gate.
kCLOCK_Gpu2D GPU2D Clock Gate.
kCLOCK_Gpu3D GPU3D Clock Gate.
kCLOCK_Uart1 UART1 Clock Gate.
kCLOCK_Uart2 UART2 Clock Gate.
kCLOCK_Uart3 UART3 Clock Gate.
kCLOCK_Uart4 UART4 Clock Gate.
kCLOCK_Usdhc1 USDHC1 Clock Gate.
kCLOCK_Usdhc2 USDHC2 Clock Gate.
kCLOCK_Wdog1 WDOG1 Clock Gate.
kCLOCK_Wdog2 WDOG2 Clock Gate.
kCLOCK_Wdog3 WDOG3 Clock Gate.
kCLOCK_Vpu_G1 VPU_G1 Clock Gate.
kCLOCK_Gpu GPU Clock Gate.
kCLOCK_Vpu_Vc8ke VPU_VC8KE Clock Gate.
kCLOCK_Vpu_G2 VPU_G2 Clock Gate.
kCLOCK_Npu NPU Clock Gate.
kCLOCK_Hsio HSIO Clock Gate.
kCLOCK_Media MEDIA Clock Gate.
kCLOCK_Usdhc3 USDHC3 Clock Gate.
kCLOCK_Hdmi HDMI Clock Gate.
kCLOCK_TempSensor TempSensor Clock Gate.
kCLOCK_Audio AUDIO Clock Gate.
kCLOCK_Earc EARC clock gate.
kCLOCK_AudioDspDebug AUDIO DSP DEBUG clock gate.
kCLOCK_AudioDsp audio dsp clock gate
kCLOCK_Spba2 SPBA2 clock gate.
kCLOCK_Sdma3 SDMA3 clock gate.
kCLOCK_Sdma2 SDMA2 clock gate.
kCLOCK_Pdm PDM clock gate.
kCLOCK_Asrc ASRC clock gate.
kCLOCK_Sai7_Mclk3 SAI7 MCLK3 clock gate.

kCLOCK_Sai7_Mclk2 SAI7 MCLK2 clock gate.
kCLOCK_Sai7_Mclk1 SAI7 MCLK1 clock gate.
kCLOCK_Sai7 SAI7 clock gate.
kCLOCK_Sai6_Mclk3 SAI6 MCLK3 clock gate.
kCLOCK_Sai6_Mclk2 SAI6 MCLK2 clock gate.
kCLOCK_Sai6_Mclk1 SAI6 MCLK1 clock gate.
kCLOCK_Sai6 SAI6 clock gate.
kCLOCK_Sai5_Mclk3 SAI5 MCLK3 clock gate.
kCLOCK_Sai5_Mclk2 sai5 MCLK2 clock gate
kCLOCK_Sai5_Mclk1 SAI5 MCLK1 clock gate.
kCLOCK_Sai5 SAI5 clock gate.
kCLOCK_Sai3_Mclk3 SAI3 MCLK3 clock gate.
kCLOCK_Sai3_Mclk2 SAI3 MCLK2 clock gate.
kCLOCK_Sai3_Mclk1 SAI3 MCLK1 clock gate.
kCLOCK_Sai3 SAI3 clock gate.
kCLOCK_Sai2_Mclk3 SAI2 MCLK3 clock gate.
kCLOCK_Sai2_Mclk2 SAI2 MCLK2 clock gate.
kCLOCK_Sai2_Mclk1 SAI2 MCLK1 clock gate.
kCLOCK_Sai2 SAI2 clock gate.
kCLOCK_Sai1_Mclk3 SAI1 MCLK3 clock gate.
kCLOCK_Sai1_Mclk2 SAI1 MCLK2 clock gate.
kCLOCK_Sai1_Mclk1 SAI1 MCLK1 clock gate.
kCLOCK_Sai1 SAI1 clock gate.
kCLOCK_EarcPhy EARC PHY clock gate.
kCLOCK_Mu3 MU3 clock gate.
kCLOCK_Mu2 MU2 clock gate.
kCLOCK_Pll PLL clock gate.
kCLOCK_Edma EDMA clock gate.
kCLOCK_Aud2htx AUD2HTX clock gate.
kCLOCK_Ocram_A OCRAM A clock gate.

5.4.3 enum clock_root_control_t

Enumerator

kCLOCK_RootM7 ARM Cortex-M7 Clock control name.
kCLOCK_RootHsioAxi HSIO AXI Clock control name.
kCLOCK_RootMainAxi MAIN AXI Clock control name.
kCLOCK_RootEnetAxi ENET AXI Clock control name.
kCLOCK_RootNandUsdhcBus NAND USDHC BUS Clock control name.
kCLOCK_RootVpuBus VPU BUS Clock control name.
kCLOCK_RootMediaAxi MEDIA AXI Clock control name.
kCLOCK_RootMediaApb MEDIA APB Clock control name.
kCLOCK_RootHdmiApb HDMI APB Clock control name.

kCLOCK_RootNoc NOC Clock control name.
kCLOCK_RootAhb AHB Clock control name.
kCLOCK_RootIpg IPG Clock control name.
kCLOCK_RootAudioAhb Audio AHB Clock control name.
kCLOCK_RootAudioIpg Audio IPG Clock control name.
kCLOCK_RootDramAlt DRAM ALT Clock control name.
kCLOCK_RootFlexCan1 FLEXCAN1 Clock control name.
kCLOCK_RootFlexCan2 FLEXCAN2 Clock control name.
kCLOCK_RootSai1 SAI1 Clock control name.
kCLOCK_RootSai2 SAI2 Clock control name.
kCLOCK_RootSai3 SAI3 Clock control name.
kCLOCK_RootSai5 SAI5 Clock control name.
kCLOCK_RootSai6 SAI6 Clock control name.
kCLOCK_RootSai7 SAI7 Clock control name.
kCLOCK_RootEnetQos ENET QOS Clock control name.
kCLOCK_RootEnetQosTimer ENET QOS TIMER Clock control name.
kCLOCK_RootEnetRef ENET Clock control name.
kCLOCK_RootEnetTimer ENET TIMER Clock control name.
kCLOCK_RootEnetPhy ENET PHY Clock control name.
kCLOCK_RootNand NAND Clock control name.
kCLOCK_RootQspi QSPI Clock control name.
kCLOCK_RootUsdhc1 USDHC1 Clock control name.
kCLOCK_RootUsdhc2 USDHC2 Clock control name.
kCLOCK_RootUsdhc3 USDHC3 Clock control name.
kCLOCK_RootI2c1 I2C1 Clock control name.
kCLOCK_RootI2c2 I2C2 Clock control name.
kCLOCK_RootI2c3 I2C3 Clock control name.
kCLOCK_RootI2c4 I2C4 Clock control name.
kCLOCK_RootI2c5 I2C5 Clock control name.
kCLOCK_RootI2c6 I2C6 Clock control name.
kCLOCK_RootUart1 UART1 Clock control name.
kCLOCK_RootUart2 UART2 Clock control name.
kCLOCK_RootUart3 UART3 Clock control name.
kCLOCK_RootUart4 UART4 Clock control name.
kCLOCK_RootGic GIC Clock control name.
kCLOCK_RootEcspi1 ECSPi1 Clock control name.
kCLOCK_RootEcspi2 ECSPi2 Clock control name.
kCLOCK_RootEcspi3 ECSPi3 Clock control name.
kCLOCK_RootPwm1 PWM1 Clock control name.
kCLOCK_RootPwm2 PWM2 Clock control name.
kCLOCK_RootPwm3 PWM3 Clock control name.
kCLOCK_RootPwm4 PWM4 Clock control name.
kCLOCK_RootGpt1 GPT1 Clock control name.
kCLOCK_RootGpt2 GPT2 Clock control name.
kCLOCK_RootGpt3 GPT3 Clock control name.

kCLOCK_RootGpt4 GPT4 Clock control name.
kCLOCK_RootGpt5 GPT5 Clock control name.
kCLOCK_RootGpt6 GPT6 Clock control name.
kCLOCK_RootWdog WDOG Clock control name.
kCLOCK_RootPdm PDM Clock control name.

5.4.4 enum clock_rootmux_m7_clk_sel_t

Enumerator

kCLOCK_M7RootmuxOsc24M ARM Cortex-M7 Clock from OSC 24M.
kCLOCK_M7RootmuxSysPll2Div5 ARM Cortex-M7 Clock from SYSTEM PLL2 divided by 5.
kCLOCK_M7RootmuxSysPll2Div4 ARM Cortex-M7 Clock from SYSTEM PLL2 divided by 4.
kCLOCK_M7RootmuxSysVpuPll ARM Cortex-M7 Clock from VPU PLL.
kCLOCK_M7RootmuxSysPll1 ARM Cortex-M7 Clock from SYSTEM PLL1.
kCLOCK_M7RootmuxAudioPll1 ARM Cortex-M7 Clock from AUDIO PLL1.
kCLOCK_M7RootmuxVideoPll1 ARM Cortex-M7 Clock from VIDEO PLL1.
kCLOCK_M7RootmuxSysPll3 ARM Cortex-M7 Clock from SYSTEM PLL3.

5.4.5 enum clock_rootmux_axi_clk_sel_t

Enumerator

kCLOCK_AxiRootmuxOsc24M ARM MAIN AXI Clock from OSC 24M.
kCLOCK_AxiRootmuxSysPll2Div3 ARM MAIN AXI Clock from SYSTEM PLL2 divided by 3.
kCLOCK_AxiRootmuxSysPll1 ARM MAIN AXI Clock from SYSTEM PLL1.
kCLOCK_AxiRootmuxSysPll2Div4 ARM MAIN AXI Clock from SYSTEM PLL2 divided by 4.
kCLOCK_AxiRootmuxSysPll2 ARM MAIN AXI Clock from SYSTEM PLL2.
kCLOCK_AxiRootmuxAudioPll1 ARM MAIN AXI Clock from AUDIO PLL1.
kCLOCK_AxiRootmuxVideoPll1 ARM MAIN AXI Clock from VIDEO PLL1.
kCLOCK_AxiRootmuxSysPll1Div8 ARM MAIN AXI Clock from SYSTEM PLL1 divided by 8.

5.4.6 enum clock_rootmux_ahb_clk_sel_t

Enumerator

kCLOCK_AhbRootmuxOsc24M ARM AHB Clock from OSC 24M.
kCLOCK_AhbRootmuxSysPll1Div6 ARM AHB Clock from SYSTEM PLL1 divided by 6.
kCLOCK_AhbRootmuxSysPll1 ARM AHB Clock from SYSTEM PLL1.
kCLOCK_AhbRootmuxSysPll1Div2 ARM AHB Clock from SYSTEM PLL1 divided by 2.
kCLOCK_AhbRootmuxSysPll2Div8 ARM AHB Clock from SYSTEM PLL2 divided by 8.

kCLOCK_AhbRootmuxSysPll3 ARM AHB Clock from SYSTEM PLL3.
kCLOCK_AhbRootmuxAudioPll1 ARM AHB Clock from AUDIO PLL1.
kCLOCK_AhbRootmuxVideoPll1 ARM AHB Clock from VIDEO PLL1.

5.4.7 enum clock_rootmux_audio_ahb_clk_sel_t

Enumerator

kCLOCK_AudioAhbRootmuxOsc24M ARM Audio AHB Clock from OSC 24M.
kCLOCK_AudioAhbRootmuxSysPll2Div2 ARM Audio AHB Clock from SYSTEM PLL2 divided by 2.
kCLOCK_AudioAhbRootmuxSysPll1 ARM Audio AHB Clock from SYSTEM PLL1.
kCLOCK_AudioAhbRootmuxSysPll2 ARM Audio AHB Clock from SYSTEM PLL2.
kCLOCK_AudioAhbRootmuxSysPll2Div6 ARM Audio AHB Clock from SYSTEM PLL2 divided by 6.
kCLOCK_AudioAhbRootmuxSysPll3 ARM Audio AHB Clock from SYSTEM PLL3.
kCLOCK_AudioAhbRootmuxAudioPll1 ARM Audio AHB Clock from AUDIO PLL1.
kCLOCK_AudioAhbRootmuxVideoPll1 ARM Audio AHB Clock from VIDEO PLL1.

5.4.8 enum clock_rootmux_qspi_clk_sel_t

Enumerator

kCLOCK_QspiRootmuxOsc24M ARM QSPI Clock from OSC 24M.
kCLOCK_QspiRootmuxSysPll1Div2 ARM QSPI Clock from SYSTEM PLL1 divided by 2.
kCLOCK_QspiRootmuxSysPll2Div3 ARM QSPI Clock from SYSTEM PLL2 divided by 3.
kCLOCK_QspiRootmuxSysPll2Div2 ARM QSPI Clock from SYSTEM PLL2 divided by 2.
kCLOCK_QspiRootmuxAudioPll2 ARM QSPI Clock from AUDIO PLL2.
kCLOCK_QspiRootmuxSysPll1Div3 ARM QSPI Clock from SYSTEM PLL1 divided by 3.
kCLOCK_QspiRootmuxSysPll3 ARM QSPI Clock from SYSTEM PLL3.
kCLOCK_QspiRootmuxSysPll1Div8 ARM QSPI Clock from SYSTEM PLL1 divided by 8.

5.4.9 enum clock_rootmux_ecspi_clk_sel_t

Enumerator

kCLOCK_EcspiRootmuxOsc24M ECSPi Clock from OSC 24M.
kCLOCK_EcspiRootmuxSysPll2Div5 ECSPi Clock from SYSTEM PLL2 divided by 5.
kCLOCK_EcspiRootmuxSysPll1Div20 ECSPi Clock from SYSTEM PLL1 divided by 20.
kCLOCK_EcspiRootmuxSysPll1Div5 ECSPi Clock from SYSTEM PLL1 divided by 5.
kCLOCK_EcspiRootmuxSysPll1 ECSPi Clock from SYSTEM PLL1.

kCLOCK_EcspiRootmuxSysPll3 ECSPi Clock from SYSTEM PLL3.

kCLOCK_EcspiRootmuxSysPll2Div4 ECSPi Clock from SYSTEM PLL2 divided by 4.

kCLOCK_EcspiRootmuxAudioPll2 ECSPi Clock from AUDIO PLL2.

5.4.10 enum clock_rootmux_enet_axi_clk_sel_t

Enumerator

kCLOCK_EnetAxiRootmuxOsc24M ENET AXI Clock from OSC 24M.

kCLOCK_EnetAxiRootmuxSysPll1Div3 ENET AXI Clock from SYSTEM PLL1 divided by 3.

kCLOCK_EnetAxiRootmuxSysPll1 ENET AXI Clock from SYSTEM PLL1.

kCLOCK_EnetAxiRootmuxSysPll2Div4 ENET AXI Clock from SYSTEM PLL2 divided by 4.

kCLOCK_EnetAxiRootmuxSysPll2Div5 ENET AXI Clock from SYSTEM PLL2 divided by 5.

kCLOCK_EnetAxiRootmuxAudioPll1 ENET AXI Clock from AUDIO PLL1.

kCLOCK_EnetAxiRootmuxVideoPll1 ENET AXI Clock from VIDEO PLL1.

kCLOCK_EnetAxiRootmuxSysPll3 ENET AXI Clock from SYSTEM PLL3.

5.4.11 enum clock_rootmux_enet_qos_clk_sel_t

Enumerator

kCLOCK_EnetQosRootmuxOsc24M ENET QOS Clock from OSC 24M.

kCLOCK_EnetQosRootmuxSysPll2Div8 ENET QOS Clock from SYSTEM PLL2 divided by 8.

kCLOCK_EnetQosRootmuxSysPll2Div20 ENET QOS Clock from SYSTEM PLL2 divided by 20.

kCLOCK_EnetQosRootmuxSysPll2Div10 ENET QOS Clock from SYSTEM PLL2 divided by 10.

kCLOCK_EnetQosRootmuxSysPll1Div5 ENET QOS Clock from SYSTEM PLL1 divided by 5.

kCLOCK_EnetQosRootmuxAudioPll1 ENET QOS Clock from AUDIO PLL1.

kCLOCK_EnetQosRootmuxVideoPll1 ENET QOS Clock from VIDEO PLL1.

kCLOCK_EnetQosRootmuxExtClk4 ENET QOS Clock from External Clock 4.

5.4.12 enum clock_rootmux_enet_ref_clk_sel_t

Enumerator

kCLOCK_EnetRefRootmuxOsc24M ENET REF Clock from OSC 24M.

kCLOCK_EnetRefRootmuxSysPll2Div8 ENET REF Clock from SYSTEM PLL2 divided by 8.

kCLOCK_EnetRefRootmuxSysPll2Div20 ENET REF Clock from SYSTEM PLL2 divided by 20.

kCLOCK_EnetRefRootmuxSysPll2Div10 ENET REF Clock from SYSTEM PLL2 divided by 10.

kCLOCK_EnetRefRootmuxSysPll1Div5 ENET REF Clock from SYSTEM PLL1 divided by 5.

kCLOCK_EnetRefRootmuxAudioPll1 ENET REF Clock from AUDIO PLL1.

kCLOCK_EnetRefRootmuxVideoPll1 ENET REF Clock from VIDEO PLL1.

kCLOCK_EnetRefRootmuxExtClk4 ENET REF Clock from External Clock 4.

5.4.13 enum clock_rootmux_enet_qos_timer_clk_sel_t

Enumerator

kCLOCK_EnetQosTimerRootmuxOsc24M ENET QOS TIMER Clock from OSC 24M.
kCLOCK_EnetQosTimerRootmuxSysPll2Div10 ENET QOS TIMER Clock from SYSTEM PLL2 divided by 10.
kCLOCK_EnetQosTimerRootmuxAudioPll1 ENET QOS TIMER Clock from AUDIO PLL1.
kCLOCK_EnetQosTimerRootmuxExtClk1 ENET QOS TIMER Clock from External Clock 1.
kCLOCK_EnetQosTimerRootmuxExtClk2 ENET QOS TIMER Clock External Clock 2.
kCLOCK_EnetQosTimerRootmuxExtClk3 ENET QOS TIMER Clock from External Clock 3.
kCLOCK_EnetQosTimerRootmuxExtClk4 ENET QOS TIMER Clock from External Clock 4.
kCLOCK_EnetQosTimerRootmuxVideoPll1 ENET QOS TIMER Clock from VIDEO PLL1.

5.4.14 enum clock_rootmux_enet_timer_clk_sel_t

Enumerator

kCLOCK_EnetTimerRootmuxOsc24M ENET TIMER Clock from OSC 24M.
kCLOCK_EnetTimerRootmuxSysPll2Div10 ENET TIMER Clock from SYSTEM PLL2 divided by 10.
kCLOCK_EnetTimerRootmuxAudioPll1 ENET TIMER Clock from AUDIO PLL1.
kCLOCK_EnetTimerRootmuxExtClk1 ENET TIMER Clock from External Clock 1.
kCLOCK_EnetTimerRootmuxExtClk2 ENET TIMER Clock External Clock 2.
kCLOCK_EnetTimerRootmuxExtClk3 ENET TIMER Clock from External Clock 3.
kCLOCK_EnetTimerRootmuxExtClk4 ENET TIMER Clock from External Clock 4.
kCLOCK_EnetTimerRootmuxVideoPll1 ENET TIMER Clock from VIDEO PLL1.

5.4.15 enum clock_rootmux_enet_phy_clk_sel_t

Enumerator

kCLOCK_EnetPhyRootmuxOsc24M ENET PHY Clock from OSC 24M.
kCLOCK_EnetPhyRootmuxSysPll2Div20 ENET PHY Clock from SYSTEM PLL2 divided by 20.
kCLOCK_EnetPhyRootmuxSysPll2Div8 ENET PHY Clock from SYSTEM PLL2 divided by 8.
kCLOCK_EnetPhyRootmuxSysPll2Div5 ENET PHY Clock from SYSTEM PLL2 divided by 5.
kCLOCK_EnetPhyRootmuxSysPll2Div2 ENET PHY Clock from SYSTEM PLL2 divided by 2.
kCLOCK_EnetPhyRootmuxAudioPll1 ENET PHY Clock from AUDIO PLL1.
kCLOCK_EnetPhyRootmuxVideoPll1 ENET PHY Clock from VIDEO PLL1.
kCLOCK_EnetPhyRootmuxAudioPll2 ENET PHY Clock from AUDIO PLL2.

5.4.16 enum clock_rootmux_flexcan_clk_sel_t

Enumerator

kCLOCK_FlexCanRootmuxOsc24M FLEXCAN Clock from OSC 24M.
kCLOCK_FlexCanRootmuxSysPll2Div5 FLEXCAN Clock from SYSTEM PLL2 divided by 5.
kCLOCK_FlexCanRootmuxSysPll1Div20 FLEXCAN Clock from SYSTEM PLL1 divided by 20.
kCLOCK_FlexCanRootmuxSysPll1Div5 FLEXCAN Clock from SYSTEM PLL1 divided by 5.
kCLOCK_FlexCanRootmuxSysPll1 FLEXCAN Clock from SYSTEM PLL1.
kCLOCK_FlexCanRootmuxSysPll3 FLEXCAN Clock from SYSTEM PLL3.
kCLOCK_FlexCanRootmuxSysPll2Div4 FLEXCAN Clock from SYSTEM PLL2 divided by 4.
kCLOCK_FlexCanRootmuxAudioPll2 FLEXCAN Clock from AUDIO PLL2.

5.4.17 enum clock_rootmux_i2c_clk_sel_t

Enumerator

kCLOCK_I2cRootmuxOsc24M I2C Clock from OSC 24M.
kCLOCK_I2cRootmuxSysPll1Div5 I2C Clock from SYSTEM PLL1 divided by 5.
kCLOCK_I2cRootmuxSysPll2Div20 I2C Clock from SYSTEM PLL2 divided by 20.
kCLOCK_I2cRootmuxSysPll3 I2C Clock from SYSTEM PLL3 .
kCLOCK_I2cRootmuxAudioPll1 I2C Clock from AUDIO PLL1.
kCLOCK_I2cRootmuxVideoPll1 I2C Clock from VIDEO PLL1.
kCLOCK_I2cRootmuxAudioPll2 I2C Clock from AUDIO PLL2.
kCLOCK_I2cRootmuxSysPll1Div6 I2C Clock from SYSTEM PLL1 divided by 6.

5.4.18 enum clock_rootmux_uart_clk_sel_t

Enumerator

kCLOCK_UartRootmuxOsc24M UART Clock from OSC 24M.
kCLOCK_UartRootmuxSysPll1Div10 UART Clock from SYSTEM PLL1 divided by 10.
kCLOCK_UartRootmuxSysPll2Div5 UART Clock from SYSTEM PLL2 divided by 5.
kCLOCK_UartRootmuxSysPll2Div10 UART Clock from SYSTEM PLL2 divided by 10.
kCLOCK_UartRootmuxSysPll3 UART Clock from SYSTEM PLL3.
kCLOCK_UartRootmuxExtClk2 UART Clock from External Clock 2.
kCLOCK_UartRootmuxExtClk34 UART Clock from External Clock 3, External Clock 4.
kCLOCK_UartRootmuxAudioPll2 UART Clock from Audio PLL2.

5.4.19 enum clock_rootmux_gpt_t

Enumerator

kCLOCK_GptRootmuxOsc24M GPT Clock from OSC 24M.
kCLOCK_GptRootmuxSystemPll2Div10 GPT Clock from SYSTEM PLL2 divided by 10.
kCLOCK_GptRootmuxSysPll1Div2 GPT Clock from SYSTEM PLL1 divided by 2.
kCLOCK_GptRootmuxSysPll1Div20 GPT Clock from SYSTEM PLL1 divided by 20.
kCLOCK_GptRootmuxVideoPll1 GPT Clock from VIDEO PLL1.
kCLOCK_GptRootmuxSystemPll1Div10 GPT Clock from SYSTEM PLL1 divided by 10.
kCLOCK_GptRootmuxAudioPll1 GPT Clock from AUDIO PLL1.
kCLOCK_GptRootmuxExtClk123 GPT Clock from External Clock1, External Clock2, External Clock3.

5.4.20 enum clock_rootmux_wdog_clk_sel_t

Enumerator

kCLOCK_WdogRootmuxOsc24M WDOG Clock from OSC 24M.
kCLOCK_WdogRootmuxSysPll1Div6 WDOG Clock from SYSTEM PLL1 divided by 6.
kCLOCK_WdogRootmuxSysPll1Div5 WDOG Clock from SYSTEM PLL1 divided by 5.
kCLOCK_WdogRootmuxVpuPll WDOG Clock from VPU DLL.
kCLOCK_WdogRootmuxSystemPll2Div8 WDOG Clock from SYSTEM PLL2 divided by 8.
kCLOCK_WdogRootmuxSystemPll3 WDOG Clock from SYSTEM PLL3.
kCLOCK_WdogRootmuxSystemPll1Div10 WDOG Clock from SYSTEM PLL1 divided by 10.
kCLOCK_WdogRootmuxSystemPll2Div6 WDOG Clock from SYSTEM PLL2 divided by 6.

5.4.21 enum clock_rootmux_Pwm_clk_sel_t

Enumerator

kCLOCK_PwmRootmuxOsc24M PWM Clock from OSC 24M.
kCLOCK_PwmRootmuxSysPll2Div10 PWM Clock from SYSTEM PLL2 divided by 10.
kCLOCK_PwmRootmuxSysPll1Div5 PWM Clock from SYSTEM PLL1 divided by 5.
kCLOCK_PwmRootmuxSysPll1Div20 PWM Clock from SYSTEM PLL1 divided by 20.
kCLOCK_PwmRootmuxSystemPll3 PWM Clock from SYSTEM PLL3.
kCLOCK_PwmRootmuxExtClk12 PWM Clock from External Clock1, External Clock2.
kCLOCK_PwmRootmuxSystemPll1Div10 PWM Clock from SYSTEM PLL1 divided by 10.
kCLOCK_PwmRootmuxVideoPll1 PWM Clock from VIDEO PLL1.

5.4.22 enum clock_rootmux_sai_clk_sel_t

Enumerator

kCLOCK_SaiRootmuxOsc24M SAI Clock from OSC 24M.
kCLOCK_SaiRootmuxAudioPll1 SAI Clock from AUDIO PLL1.
kCLOCK_SaiRootmuxAudioPll2 SAI Clock from AUDIO PLL2.
kCLOCK_SaiRootmuxVideoPll1 SAI Clock from VIDEO PLL1.
kCLOCK_SaiRootmuxSysPll1Div6 SAI Clock from SYSTEM PLL1 divided by 6.
kCLOCK_SaiRootmuxOsc26m SAI Clock from OSC HDMI 26M.
kCLOCK_SaiRootmuxExtClk1 SAI Clock from External Clock1, External Clock2, External Clock3.
kCLOCK_SaiRootmuxExtClk2 SAI Clock from External Clock2, External Clock3, External Clock4.

5.4.23 enum clock_rootmux_pdm_clk_sel_t

Enumerator

kCLOCK_PdmRootmuxOsc24M PDM Clock from OSC 24M.
kCLOCK_PdmRootmuxSysPll2Div10 PDM Clock from SYSTEM PLL2 divided by 10.
kCLOCK_PdmRootmuxAudioPll1 PDM Clock from AUDIO PLL1.
kCLOCK_PdmRootmuxSysPll1 PDM Clock from SYSTEM PLL1.
kCLOCK_PdmRootmuxSysPll2 PDM Clock from SYSTEM PLL2.
kCLOCK_PdmRootmuxSysPll3 PDM Clock from SYSTEM PLL3.
kCLOCK_PdmRootmuxExtClk3 PDM Clock from External Clock3.
kCLOCK_PdmRootmuxAudioPll2 PDM Clock from AUDIO PLL2.

5.4.24 enum clock_rootmux_noc_clk_sel_t

Enumerator

kCLOCK_NocRootmuxOsc24M NOC Clock from OSC 24M.
kCLOCK_NocRootmuxSysPll1 NOC Clock from SYSTEM PLL1.
kCLOCK_NocRootmuxSysPll3 NOC Clock from SYSTEM PLL3.
kCLOCK_NocRootmuxSysPll2 NOC Clock from SYSTEM PLL2.
kCLOCK_NocRootmuxSysPll2Div2 NOC Clock from SYSTEM PLL2 divided by 2.
kCLOCK_NocRootmuxAudioPll1 NOC Clock from AUDIO PLL1.
kCLOCK_NocRootmuxVideoPll1 NOC Clock from VIDEO PLL1.
kCLOCK_NocRootmuxAudioPll2 NOC Clock from AUDIO PLL2.

5.4.25 enum clock_pll_gate_t

Enumerator

kCLOCK_ArmPllGate ARM PLL Gate.
kCLOCK_GpuPllGate GPU PLL Gate.
kCLOCK_VpuPllGate VPU PLL Gate.
kCLOCK_DramPllGate DRAM PLL1 Gate.
kCLOCK_SysPll1Gate SYSTEM PLL1 Gate.
kCLOCK_SysPll1Div2Gate SYSTEM PLL1 Div2 Gate.
kCLOCK_SysPll1Div3Gate SYSTEM PLL1 Div3 Gate.
kCLOCK_SysPll1Div4Gate SYSTEM PLL1 Div4 Gate.
kCLOCK_SysPll1Div5Gate SYSTEM PLL1 Div5 Gate.
kCLOCK_SysPll1Div6Gate SYSTEM PLL1 Div6 Gate.
kCLOCK_SysPll1Div8Gate SYSTEM PLL1 Div8 Gate.
kCLOCK_SysPll1Div10Gate SYSTEM PLL1 Div10 Gate.
kCLOCK_SysPll1Div20Gate SYSTEM PLL1 Div20 Gate.
kCLOCK_SysPll2Gate SYSTEM PLL2 Gate.
kCLOCK_SysPll2Div2Gate SYSTEM PLL2 Div2 Gate.
kCLOCK_SysPll2Div3Gate SYSTEM PLL2 Div3 Gate.
kCLOCK_SysPll2Div4Gate SYSTEM PLL2 Div4 Gate.
kCLOCK_SysPll2Div5Gate SYSTEM PLL2 Div5 Gate.
kCLOCK_SysPll2Div6Gate SYSTEM PLL2 Div6 Gate.
kCLOCK_SysPll2Div8Gate SYSTEM PLL2 Div8 Gate.
kCLOCK_SysPll2Div10Gate SYSTEM PLL2 Div10 Gate.
kCLOCK_SysPll2Div20Gate SYSTEM PLL2 Div20 Gate.
kCLOCK_SysPll3Gate SYSTEM PLL3 Gate.
kCLOCK_AudioPll1Gate AUDIO PLL1 Gate.
kCLOCK_AudioPll2Gate AUDIO PLL2 Gate.
kCLOCK_VideoPll1Gate VIDEO PLL1 Gate.
kCLOCK_VideoPll2Gate VIDEO PLL2 Gate.

5.4.26 enum clock_gate_value_t

Enumerator

kCLOCK_ClockNotNeeded Clock always disabled.
kCLOCK_ClockNeededRun Clock enabled when CPU is running.
kCLOCK_ClockNeededRunWait Clock enabled when CPU is running or in WAIT mode.
kCLOCK_ClockNeededAll Clock always enabled.

5.4.27 enum clock_pll_bypass_ctrl_t

These constants define the PLL control names for PLL bypass.

- 0:15: REG offset to CCM_ANALOG_BASE in bytes.
- 16:20: bypass bit shift.

Enumerator

kCLOCK_AudioPll1BypassCtrl CCM Audio PLL1 bypass Control.
kCLOCK_AudioPll2BypassCtrl CCM Audio PLL2 bypass Control.
kCLOCK_VideoPll1BypassCtrl CCM Video Pll1 bypass Control.
kCLOCK_DramPllInternalPll1BypassCtrl CCM DRAM PLL bypass Control.
kCLOCK_ArmPllPwrBypassCtrl CCM Arm PLL bypass Control.
kCLOCK_SysPll1InternalPll1BypassCtrl CCM System PLL1 bypass Control.
kCLOCK_SysPll2InternalPll1BypassCtrl CCM System PLL2 bypass Control.
kCLOCK_SysPll3InternalPll1BypassCtrl CCM System PLL3 bypass Control.

5.4.28 enum clock_pll_clke_t

These constants define the PLL clock names for PLL clock enable/disable operations.

- 0:15: REG offset to CCM_ANALOG_BASE in bytes.
- 16:20: Clock enable bit shift.

Enumerator

kCLOCK_AudioPll1Clke Audio pll1 clke.
kCLOCK_AudioPll2Clke Audio pll2 clke.
kCLOCK_VideoPll1Clke Video pll1 clke.
kCLOCK_DramPllClke Dram pll clke.
kCLOCK_ArmPllClke Arm pll clke.
kCLOCK_SystemPll1Clke System pll1 clke.
kCLOCK_SystemPll1Div2Clke System pll1 Div2 clke.
kCLOCK_SystemPll1Div3Clke System pll1 Div3 clke.
kCLOCK_SystemPll1Div4Clke System pll1 Div4 clke.
kCLOCK_SystemPll1Div5Clke System pll1 Div5 clke.
kCLOCK_SystemPll1Div6Clke System pll1 Div6 clke.
kCLOCK_SystemPll1Div8Clke System pll1 Div8 clke.
kCLOCK_SystemPll1Div10Clke System pll1 Div10 clke.
kCLOCK_SystemPll1Div20Clke System pll1 Div20 clke.
kCLOCK_SystemPll2Clke System pll2 clke.
kCLOCK_SystemPll2Div2Clke System pll2 Div2 clke.
kCLOCK_SystemPll2Div3Clke System pll2 Div3 clke.
kCLOCK_SystemPll2Div4Clke System pll2 Div4 clke.

kCLOCK_SystemPll2Div5Clke System pll2 Div5 clke.
kCLOCK_SystemPll2Div6Clke System pll2 Div6 clke.
kCLOCK_SystemPll2Div8Clke System pll2 Div8 clke.
kCLOCK_SystemPll2Div10Clke System pll2 Div10 clke.
kCLOCK_SystemPll2Div20Clke System pll2 Div20 clke.
kCLOCK_SystemPll3Clke System pll3 clke.

5.4.29 anonymous enum

Enumerator

kANALOG_PllRefOsc24M reference OSC 24M
kANALOG_PllPadClk reference PAD CLK

5.5 Function Documentation

5.5.1 static void CLOCK_SetRootMux (clock_root_control_t rootClk, uint32_t mux) [inline], [static]

User maybe need to set more than one mux ROOT according to the clock tree description in the reference manual.

Parameters

<i>rootClk</i>	Root clock control (see clock_root_control_t enumeration).
<i>mux</i>	Root mux value (see _ccm_rootmux_xxx enumeration).

5.5.2 static uint32_t CLOCK_GetRootMux (clock_root_control_t rootClk) [inline], [static]

In order to get the clock source of root, user maybe need to get more than one ROOT's mux value to obtain the final clock source of root.

Parameters

<i>rootClk</i>	Root clock control (see clock_root_control_t enumeration).
----------------	--

Returns

Root mux value (see [_ccm_rootmux_xxx](#) enumeration).

5.5.3 static void CLOCK_EnableRoot (clock_root_control_t rootClk) [inline], [static]

Parameters

<i>rootClk</i>	Root clock control (see clock_root_control_t enumeration)
----------------	---

5.5.4 static void CLOCK_DisableRoot (clock_root_control_t *rootClk*) [inline], [static]

Parameters

<i>rootClk</i>	Root control (see clock_root_control_t enumeration)
----------------	---

5.5.5 static bool CLOCK_IsRootEnabled (clock_root_control_t *rootClk*) [inline], [static]

Parameters

<i>rootClk</i>	Root control (see clock_root_control_t enumeration)
----------------	---

Returns

CCM root enabled or not.

- true: Clock root is enabled.
- false: Clock root is disabled.

5.5.6 void CLOCK_UpdateRoot (clock_root_control_t *ccmRootClk*, uint32_t *mux*, uint32_t *pre*, uint32_t *post*)

Parameters

<i>ccmRootClk</i>	Root control (see clock_root_control_t enumeration)
<i>mux</i>	mux value (see _ccm_rootmux_xxx enumeration)
<i>pre</i>	Pre divider value (0-7, divider=n+1)

<i>post</i>	Post divider value (0-63, divider=n+1)
-------------	--

5.5.7 void CLOCK_SetRootDivider (clock_root_control_t *ccmRootClk*, uint32_t *pre*, uint32_t *post*)

Parameters

<i>ccmRootClk</i>	Root control (see clock_root_control_t enumeration)
<i>pre</i>	Pre divider value (1-8)
<i>post</i>	Post divider value (1-64)

5.5.8 static uint32_t CLOCK_GetRootPreDivider (clock_root_control_t *rootClk*) [inline], [static]

In order to get the clock source of root, user maybe need to get more than one ROOT's mux value to obtain the final clock source of root.

Parameters

<i>rootClk</i>	Root clock name (see clock_root_control_t enumeration).
----------------	---

Returns

Root Pre divider value.

5.5.9 static uint32_t CLOCK_GetRootPostDivider (clock_root_control_t *rootClk*) [inline], [static]

In order to get the clock source of root, user maybe need to get more than one ROOT's mux value to obtain the final clock source of root.

Parameters

<i>rootClk</i>	Root clock name (see clock_root_control_t enumeration).
----------------	---

Returns

Root Post divider value.

5.5.10 static void CLOCK_ControlGate (uintptr_t *ccmGate*, clock_gate_value_t *control*) [inline], [static]

Parameters

<i>ccmGate</i>	Gate control (see clock_pll_gate_t and clock_ip_name_t enumeration)
<i>control</i>	Gate control value (see clock_gate_value_t)

5.5.11 void CLOCK_EnableClock (clock_ip_name_t *ccmGate*)

Take care of that one module may need to set more than one clock gate.

Parameters

<i>ccmGate</i>	Gate control for each module (see clock_ip_name_t enumeration).
----------------	---

5.5.12 void CLOCK_DisableClock (clock_ip_name_t *ccmGate*)

Take care of that one module may need to set more than one clock gate.

Parameters

<i>ccmGate</i>	Gate control for each module (see clock_ip_name_t enumeration).
----------------	---

5.5.13 static void CLOCK_PowerUpPll (CCM_ANALOG_Type * *base*, clock_pll_ctrl_t *pllControl*) [inline], [static]

Parameters

<i>base</i>	CCM_ANALOG base pointer.
<i>pllControl</i>	PLL control name (see clock_pll_ctrl_t enumeration)

**5.5.14 static void CLOCK_PowerDownPll (CCM_ANALOG_Type * *base*,
clock_pll_ctrl_t *pllControl*) [inline], [static]**

Parameters

<i>base</i>	CCM_ANALOG base pointer.
<i>pllControl</i>	PLL control name (see clock_pll_ctrl_t enumeration)

**5.5.15 static void CLOCK_SetPllBypass (CCM_ANALOG_Type * *base*,
clock_pll_bypass_ctrl_t *pllControl*, bool *bypass*) [inline], [static]**

Parameters

<i>base</i>	CCM_ANALOG base pointer.
<i>pllControl</i>	PLL control name (see clock_pll_bypass_ctrl_t enumeration)
<i>bypass</i>	Bypass the PLL. <ul style="list-style-type: none"> • true: Bypass the PLL. • false: Do not bypass the PLL.

**5.5.16 static bool CLOCK_IsPllBypassed (CCM_ANALOG_Type * *base*,
clock_pll_bypass_ctrl_t *pllControl*) [inline], [static]**

Parameters

<i>base</i>	CCM_ANALOG base pointer.
<i>pllControl</i>	PLL control name (see clock_pll_bypass_ctrl_t enumeration)

Returns

- PLL bypass status.
- true: The PLL is bypassed.

- false: The PLL is not bypassed.

**5.5.17 static bool CLOCK_IsPllLocked (CCM_ANALOG_Type * *base*,
clock_pll_ctrl_t *pllControl*) [inline], [static]**

Parameters

<i>base</i>	CCM_ANALOG base pointer.
<i>pllControl</i>	PLL control name (see clock_pll_ctrl_t enumeration)

Returns

PLL lock status.

- true: The PLL clock is locked.
- false: The PLL clock is not locked.

**5.5.18 static void CLOCK_EnableAnalogClock (CCM_ANALOG_Type * *base*,
clock_pll_clke_t *pllClock*) [inline], [static]**

Parameters

<i>base</i>	CCM_ANALOG base pointer.
<i>pllClock</i>	PLL clock name (see clock_pll_clke_t enumeration)

**5.5.19 static void CLOCK_DisableAnalogClock (CCM_ANALOG_Type * *base*,
clock_pll_clke_t *pllClock*) [inline], [static]**

Parameters

<i>base</i>	CCM_ANALOG base pointer.
<i>pllClock</i>	PLL clock name (see clock_pll_clke_t enumeration)

**5.5.20 static void CLOCK_OverridePllClke (CCM_ANALOG_Type * *base*,
clock_pll_clke_t *ovClock*, bool *override*) [inline], [static]**

Parameters

<i>base</i>	CCM_ANALOG base pointer.
<i>ovClock</i>	PLL clock name (see clock_pll_clke_t enumeration)
<i>override</i>	Override the PLL. <ul style="list-style-type: none"> • true: Override the PLL clke, CCM will handle it. • false: Do not override the PLL clke.

5.5.21 static void CLOCK_OverridePIIPd (CCM_ANALOG_Type * *base*, clock_pll_ctrl_t *pdClock*, bool *override*) [inline], [static]

Parameters

<i>base</i>	CCM_ANALOG base pointer.
<i>pdClock</i>	PLL clock name (see clock_pll_ctrl_t enumeration)
<i>override</i>	Override the PLL. <ul style="list-style-type: none"> • true: Override the PLL clke, CCM will handle it. • false: Do not override the PLL clke.

5.5.22 void CLOCK_InitArmPll (const ccm_analog_integer_pll_config_t * *config*)

Parameters

<i>config</i>	Pointer to the configuration structure(see ccm_analog_integer_pll_config_t enumeration).
---------------	--

Note

This function can't detect whether the Arm PLL has been enabled and used by some IPs.

5.5.23 void CLOCK_InitSysPll1 (const ccm_analog_integer_pll_config_t * *config*)

Parameters

<i>config</i>	Pointer to the configuration structure(see ccm_analog_integer_pll_config_t enumeration).
---------------	--

Note

This function can't detect whether the SYS PLL has been enabled and used by some IPs.

5.5.24 void CLOCK_InitSysPII2 (const ccm_analog_integer_pll_config_t * *config*)

Parameters

<i>config</i>	Pointer to the configuration structure(see ccm_analog_integer_pll_config_t enumeration).
---------------	--

Note

This function can't detect whether the SYS PLL has been enabled and used by some IPs.

5.5.25 void CLOCK_InitSysPII3 (const ccm_analog_integer_pll_config_t * *config*)

Parameters

<i>config</i>	Pointer to the configuration structure(see ccm_analog_integer_pll_config_t enumeration).
---------------	--

Note

This function can't detect whether the SYS PLL has been enabled and used by some IPs.

5.5.26 void CLOCK_InitAudioPII1 (const ccm_analog_frac_pll_config_t * *config*)

Parameters

<i>config</i>	Pointer to the configuration structure(see ccm_analog_frac_pll_config_t enumeration).
---------------	---

Note

This function can't detect whether the AUDIO PLL has been enabled and used by some IPs.

5.5.27 void CLOCK_InitAudioPll2 (const ccm_analog_frac_pll_config_t * *config*)

Parameters

<i>config</i>	Pointer to the configuration structure(see ccm_analog_frac_pll_config_t enumeration).
---------------	---

Note

This function can't detect whether the AUDIO PLL has been enabled and used by some IPs.

5.5.28 void CLOCK_InitVideoPll1 (const ccm_analog_frac_pll_config_t * *config*)

Parameters

<i>config</i>	Pointer to the configuration structure(see ccm_analog_frac_pll_config_t enumeration).
---------------	---

5.5.29 void CLOCK_InitIntegerPll (CCM_ANALOG_Type * *base*, const ccm_analog_integer_pll_config_t * *config*, clock_pll_ctrl_t *type*)

Parameters

<i>base</i>	CCM ANALOG base address
-------------	-------------------------

<i>config</i>	Pointer to the configuration structure(see ccm_analog_integer_pll_config_t enumeration).
<i>type</i>	integer pll type

5.5.30 **uint32_t CLOCK_GetIntegerPllFreq (CCM_ANALOG_Type * *base*, clock_pll_ctrl_t *type*, uint32_t *refClkFreq*, bool *pll1Bypass*)**

Parameters

<i>base</i>	CCM ANALOG base address.
<i>type</i>	integer pll type
<i>refClkFreq</i>	Reference clock frequency.
<i>pll1Bypass</i>	pll1 bypass flag

Returns

Clock frequency

5.5.31 **void CLOCK_InitFracPll (CCM_ANALOG_Type * *base*, const ccm_analog_frac_pll_config_t * *config*, clock_pll_ctrl_t *type*)**

Parameters

<i>base</i>	CCM ANALOG base address.
<i>config</i>	Pointer to the configuration structure(see ccm_analog_frac_pll_config_t enumeration).
<i>type</i>	fractional pll type.

5.5.32 **uint32_t CLOCK_GetFracPllFreq (CCM_ANALOG_Type * *base*, clock_pll_ctrl_t *type*, uint32_t *refClkFreq*)**

Parameters

<i>base</i>	CCM_ANALOG base pointer.
<i>type</i>	fractional pll type.
<i>refClkFreq</i>	Reference clock frequency.

Returns

Clock frequency

5.5.33 uint32_t CLOCK_GetPIIFreq (clock_pll_ctrl_t *pll*)

Parameters

<i>pll</i>	fractional pll type.
------------	----------------------

Returns

Clock frequency

5.5.34 uint32_t CLOCK_GetPIIRefClkFreq (clock_pll_ctrl_t *ctrl*)

Parameters

<i>ctrl</i>	fractional pll type.
-------------	----------------------

Returns

Clock frequency

5.5.35 uint32_t CLOCK_GetFreq (clock_name_t *clockName*)

This function checks the current clock configurations and then calculates the clock frequency for a specific clock name defined in clock_name_t.

Parameters

<i>clockName</i>	Clock names defined in clock_name_t
------------------	-------------------------------------

Returns

Clock frequency value in hertz

5.5.36 uint32_t CLOCK_GetCoreM7Freq (void)

Returns

Clock frequency; If the clock is invalid, returns 0.

5.5.37 uint32_t CLOCK_GetAxiFreq (void)

Returns

Clock frequency; If the clock is invalid, returns 0.

5.5.38 uint32_t CLOCK_GetAhbFreq (void)

Returns

Clock frequency; If the clock is invalid, returns 0.

Chapter 6

IOMUXC: IOMUX Controller

6.1 Overview

IOMUXC driver provides APIs for pin configuration. It also supports the miscellaneous functions integrated in IOMUXC.

Files

- file [fsl_iomuxc.h](#)

Driver version

- #define [FSL_IOMUXC_DRIVER_VERSION](#) ([MAKE_VERSION](#)(2, 0, 4))
IOMUXC driver version 2.0.4.

Pin function ID

The pin function ID is a tuple of <muxRegister muxMode inputRegister inputDaisy configRegister>

- #define **IOMUXC_BOOT_MODE0_SRC_BOOT_MODE0** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330250
- #define **IOMUXC_BOOT_MODE1_SRC_BOOT_MODE1** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330254
- #define **IOMUXC_BOOT_MODE2_SRC_BOOT_MODE2** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330258
- #define **IOMUXC_BOOT_MODE3_SRC_BOOT_MODE3** 0x00000000, 0x0, 0x00000000, 0x0, 0x3033025C
- #define **IOMUXC_JTAG_MOD_JTAG_MODE** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330260
- #define **IOMUXC_JTAG_TDI_JTAG_TDI** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330264
- #define **IOMUXC_JTAG_TMS_JTAG_TMS** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330268
- #define **IOMUXC_JTAG_TCK_JTAG_TCK** 0x00000000, 0x0, 0x00000000, 0x0, 0x3033026C
- #define **IOMUXC_JTAG_TDO_JTAG_TDO** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330270
- #define **IOMUXC_RTC_XTALI_SNVS_RTC** 0x00000000, 0x0, 0x00000000, 0x0, 0x00000000
- #define **IOMUXC_PMIC_STBY_REQ_CCM_PMIC_STBY_REQ** 0x00000000, 0x0, 0x00000000, 0x0, 0x00000000
- #define **IOMUXC_PMIC_ON_REQ_SNVS_PMIC_ON_REQ** 0x00000000, 0x0, 0x00000000, 0x0, 0x00000000
- #define **IOMUXC_ONOFF_SNVS_ONOFF** 0x00000000, 0x0, 0x00000000, 0x0, 0x00000000
- #define **IOMUXC_POR_B_SNVS_POR_B** 0x00000000, 0x0, 0x00000000, 0x0, 0x00000000
- #define **IOMUXC_GPIO1_IO00_GPIO1_IO00** 0x30330014, 0x0, 0x00000000, 0x0, 0x30330274
- #define **IOMUXC_GPIO1_IO00_CCM_ENET_PHY_REF_CLK_ROOT** 0x30330014, 0x1, 0x00000000, 0x0, 0x30330274
- #define **IOMUXC_GPIO1_IO00_ISP_FL_TRIG_0** 0x30330014, 0x3, 0x303305D4, 0x0, 0x30330274
- #define **IOMUXC_GPIO1_IO00_ANAMIX_REF_CLK_32K** 0x30330014, 0x5, 0x00000000, 0x0, 0x30330274

- #define **IOMUXC_GPIO1_IO00_CCM_EXT_CLK1** 0x30330014, 0x6, 0x00000000, 0x0, 0x30330274
- #define **IOMUXC_GPIO1_IO01_GPIO1_IO01** 0x30330018, 0x0, 0x00000000, 0x0, 0x30330278
- #define **IOMUXC_GPIO1_IO01_PWM1_OUT** 0x30330018, 0x1, 0x00000000, 0x0, 0x30330278
- #define **IOMUXC_GPIO1_IO01_ISP_SHUTTER_TRIG_0** 0x30330018, 0x3, 0x303305DC, 0x0, 0x30330278
- #define **IOMUXC_GPIO1_IO01_ANAMIX_REF_CLK_24M** 0x30330018, 0x5, 0x00000000, 0x0, 0x30330278
- #define **IOMUXC_GPIO1_IO01_CCM_EXT_CLK2** 0x30330018, 0x6, 0x00000000, 0x0, 0x30330278
- #define **IOMUXC_GPIO1_IO02_GPIO1_IO02** 0x3033001C, 0x0, 0x00000000, 0x0, 0x3033027-C
- #define **IOMUXC_GPIO1_IO02_WDOG1_WDOG_B** 0x3033001C, 0x1, 0x00000000, 0x0, 0x3033027C
- #define **IOMUXC_GPIO1_IO02_ISP_FLASH_TRIG_0** 0x3033001C, 0x3, 0x00000000, 0x0, 0x3033027C
- #define **IOMUXC_GPIO1_IO02_WDOG1_WDOG_ANY** 0x3033001C, 0x5, 0x00000000, 0x0, 0x3033027C
- #define **IOMUXC_GPIO1_IO02_SJC_DE_B** 0x3033001C, 0x7, 0x00000000, 0x0, 0x3033027C
- #define **IOMUXC_GPIO1_IO03_GPIO1_IO03** 0x30330020, 0x0, 0x00000000, 0x0, 0x30330280
- #define **IOMUXC_GPIO1_IO03_USDHC1_VSELECT** 0x30330020, 0x1, 0x00000000, 0x0, 0x30330280
- #define **IOMUXC_GPIO1_IO03_ISP_PRELIGHT_TRIG_0** 0x30330020, 0x3, 0x00000000, 0x0, 0x30330280
- #define **IOMUXC_GPIO1_IO03_SDMA1_EXT_EVENT0** 0x30330020, 0x5, 0x00000000, 0x0, 0x30330280
- #define **IOMUXC_GPIO1_IO04_GPIO1_IO04** 0x30330024, 0x0, 0x00000000, 0x0, 0x30330284
- #define **IOMUXC_GPIO1_IO04_USDHC2_VSELECT** 0x30330024, 0x1, 0x00000000, 0x0, 0x30330284
- #define **IOMUXC_GPIO1_IO04_ISP_SHUTTER_OPEN_0** 0x30330024, 0x3, 0x00000000, 0x0, 0x30330284
- #define **IOMUXC_GPIO1_IO04_SDMA1_EXT_EVENT1** 0x30330024, 0x5, 0x00000000, 0x0, 0x30330284
- #define **IOMUXC_GPIO1_IO05_GPIO1_IO05** 0x30330028, 0x0, 0x00000000, 0x0, 0x30330288
- #define **IOMUXC_GPIO1_IO05_M7_NMI** 0x30330028, 0x1, 0x00000000, 0x0, 0x30330288
- #define **IOMUXC_GPIO1_IO05_ISP_FL_TRIG_1** 0x30330028, 0x3, 0x303305D8, 0x0, 0x30330288
- #define **IOMUXC_GPIO1_IO05_CCM_PMIC_READY** 0x30330028, 0x5, 0x30330554, 0x0, 0x30330288
- #define **IOMUXC_GPIO1_IO06_GPIO1_IO06** 0x3033002C, 0x0, 0x00000000, 0x0, 0x3033028-C
- #define **IOMUXC_GPIO1_IO06_ENET_QOS_MDC** 0x3033002C, 0x1, 0x00000000, 0x0, 0x3033028C
- #define **IOMUXC_GPIO1_IO06_ISP_SHUTTER_TRIG_1** 0x3033002C, 0x3, 0x303305E0, 0x0, 0x3033028C
- #define **IOMUXC_GPIO1_IO06_USDHC1_CD_B** 0x3033002C, 0x5, 0x00000000, 0x0, 0x3033028C
- #define **IOMUXC_GPIO1_IO06_CCM_EXT_CLK3** 0x3033002C, 0x6, 0x00000000, 0x0, 0x3033028C
- #define **IOMUXC_GPIO1_IO07_GPIO1_IO07** 0x30330030, 0x0, 0x00000000, 0x0, 0x30330290
- #define **IOMUXC_GPIO1_IO07_ENET_QOS_MDIO** 0x30330030, 0x1, 0x30330590, 0x0,

- 0x30330290
- #define **IOMUXC_GPIO1_IO07_ISP_FLASH_TRIG_1** 0x30330030, 0x3, 0x00000000, 0x0, 0x30330290
- #define **IOMUXC_GPIO1_IO07_USDHC1_WP** 0x30330030, 0x5, 0x00000000, 0x0, 0x30330290
- #define **IOMUXC_GPIO1_IO07_CCM_EXT_CLK4** 0x30330030, 0x6, 0x00000000, 0x0, 0x30330290
- #define **IOMUXC_GPIO1_IO08_GPIO1_IO08** 0x30330034, 0x0, 0x00000000, 0x0, 0x30330294
- #define **IOMUXC_GPIO1_IO08_ENET_QOS_1588_EVENT0_IN** 0x30330034, 0x1, 0x00000000, 0x0, 0x30330294
- #define **IOMUXC_GPIO1_IO08_PWM1_OUT** 0x30330034, 0x2, 0x00000000, 0x0, 0x30330294
- #define **IOMUXC_GPIO1_IO08_ISP_PRELIGHT_TRIG_1** 0x30330034, 0x3, 0x00000000, 0x0, 0x30330294
- #define **IOMUXC_GPIO1_IO08_ENET_QOS_1588_EVENT0_AUX_IN** 0x30330034, 0x4, 0x00000000, 0x0, 0x30330294
- #define **IOMUXC_GPIO1_IO08_USDHC2_RESET_B** 0x30330034, 0x5, 0x00000000, 0x0, 0x30330294
- #define **IOMUXC_GPIO1_IO09_GPIO1_IO09** 0x30330038, 0x0, 0x00000000, 0x0, 0x30330298
- #define **IOMUXC_GPIO1_IO09_ENET_QOS_1588_EVENT0_OUT** 0x30330038, 0x1, 0x00000000, 0x0, 0x30330298
- #define **IOMUXC_GPIO1_IO09_PWM2_OUT** 0x30330038, 0x2, 0x00000000, 0x0, 0x30330298
- #define **IOMUXC_GPIO1_IO09_ISP_SHUTTER_OPEN_1** 0x30330038, 0x3, 0x00000000, 0x0, 0x30330298
- #define **IOMUXC_GPIO1_IO09_USDHC3_RESET_B** 0x30330038, 0x4, 0x00000000, 0x0, 0x30330298
- #define **IOMUXC_GPIO1_IO09_SDMA2_EXT_EVENT0** 0x30330038, 0x5, 0x00000000, 0x0, 0x30330298
- #define **IOMUXC_GPIO1_IO10_GPIO1_IO10** 0x3033003C, 0x0, 0x00000000, 0x0, 0x3033029C
- #define **IOMUXC_GPIO1_IO10_USB1_ID** 0x3033003C, 0x1, 0x00000000, 0x0, 0x3033029C
- #define **IOMUXC_GPIO1_IO10_PWM3_OUT** 0x3033003C, 0x2, 0x00000000, 0x0, 0x3033029C
- #define **IOMUXC_GPIO1_IO11_GPIO1_IO11** 0x30330040, 0x0, 0x00000000, 0x0, 0x303302A0
- #define **IOMUXC_GPIO1_IO11_USB2_ID** 0x30330040, 0x1, 0x00000000, 0x0, 0x303302A0
- #define **IOMUXC_GPIO1_IO11_PWM2_OUT** 0x30330040, 0x2, 0x00000000, 0x0, 0x303302A0
- #define **IOMUXC_GPIO1_IO11_USDHC3_VSELECT** 0x30330040, 0x4, 0x00000000, 0x0, 0x303302A0
- #define **IOMUXC_GPIO1_IO11_CCM_PMIC_READY** 0x30330040, 0x5, 0x30330554, 0x1, 0x303302A0
- #define **IOMUXC_GPIO1_IO12_GPIO1_IO12** 0x30330044, 0x0, 0x00000000, 0x0, 0x303302A4
- #define **IOMUXC_GPIO1_IO12_USB1_PWR** 0x30330044, 0x1, 0x00000000, 0x0, 0x303302A4
- #define **IOMUXC_GPIO1_IO12_SDMA2_EXT_EVENT1** 0x30330044, 0x5, 0x00000000, 0x0, 0x303302A4
- #define **IOMUXC_GPIO1_IO13_GPIO1_IO13** 0x30330048, 0x0, 0x00000000, 0x0, 0x303302A8
- #define **IOMUXC_GPIO1_IO13_USB1_OC** 0x30330048, 0x1, 0x00000000, 0x0, 0x303302A8
- #define **IOMUXC_GPIO1_IO13_PWM2_OUT** 0x30330048, 0x5, 0x00000000, 0x0, 0x303302A8
- #define **IOMUXC_GPIO1_IO14_GPIO1_IO14** 0x3033004C, 0x0, 0x00000000, 0x0, 0x303302-

- AC
- #define **IOMUXC_GPIO1_IO14_USB2_PWR** 0x3033004C, 0x1, 0x00000000, 0x0, 0x303302-AC
- #define **IOMUXC_GPIO1_IO14_USDHC3_CD_B** 0x3033004C, 0x4, 0x30330608, 0x0, 0x303302AC
- #define **IOMUXC_GPIO1_IO14_PWM3_OUT** 0x3033004C, 0x5, 0x00000000, 0x0, 0x303302-AC
- #define **IOMUXC_GPIO1_IO14_CCM_CLKO1** 0x3033004C, 0x6, 0x00000000, 0x0, 0x303302AC
- #define **IOMUXC_GPIO1_IO15_GPIO1_IO15** 0x30330050, 0x0, 0x00000000, 0x0, 0x303302-B0
- #define **IOMUXC_GPIO1_IO15_USB2_OC** 0x30330050, 0x1, 0x00000000, 0x0, 0x303302B0
- #define **IOMUXC_GPIO1_IO15_USDHC3_WP** 0x30330050, 0x4, 0x30330634, 0x0, 0x303302-B0
- #define **IOMUXC_GPIO1_IO15_PWM4_OUT** 0x30330050, 0x5, 0x00000000, 0x0, 0x303302-B0
- #define **IOMUXC_GPIO1_IO15_CCM_CLKO2** 0x30330050, 0x6, 0x00000000, 0x0, 0x303302-B0
- #define **IOMUXC_ENET_MDC_ENET_QOS_MDC** 0x30330054, 0x0, 0x00000000, 0x0, 0x303302B4
- #define **IOMUXC_ENET_MDC_AUDIOMIX_SAI6_TX_DATA0** 0x30330054, 0x2, 0x00000000, 0x0, 0x303302B4
- #define **IOMUXC_ENET_MDC_GPIO1_IO16** 0x30330054, 0x5, 0x00000000, 0x0, 0x303302-B4
- #define **IOMUXC_ENET_MDC_USDHC3_STROBE** 0x30330054, 0x6, 0x30330630, 0x0, 0x303302B4
- #define **IOMUXC_ENET_MDIO_ENET_QOS_MDIO** 0x30330058, 0x0, 0x30330590, 0x1, 0x303302B8
- #define **IOMUXC_ENET_MDIO_AUDIOMIX_SAI6_TX_SYNC** 0x30330058, 0x2, 0x30330528, 0x0, 0x303302B8
- #define **IOMUXC_ENET_MDIO_AUDIOMIX_PDM_BIT_STREAM3** 0x30330058, 0x3, 0x303304CC, 0x0, 0x303302B8
- #define **IOMUXC_ENET_MDIO_GPIO1_IO17** 0x30330058, 0x5, 0x00000000, 0x0, 0x303302-B8
- #define **IOMUXC_ENET_MDIO_USDHC3_DATA5** 0x30330058, 0x6, 0x30330624, 0x0, 0x303302B8
- #define **IOMUXC_ENET_TD3_ENET_QOS_RGMII_TD3** 0x3033005C, 0x0, 0x00000000, 0x0, 0x303302BC
- #define **IOMUXC_ENET_TD3_AUDIOMIX_SAI6_TX_BCLK** 0x3033005C, 0x2, 0x30330524, 0x0, 0x303302BC
- #define **IOMUXC_ENET_TD3_AUDIOMIX_PDM_BIT_STREAM2** 0x3033005C, 0x3, 0x303304C8, 0x0, 0x303302BC
- #define **IOMUXC_ENET_TD3_GPIO1_IO18** 0x3033005C, 0x5, 0x00000000, 0x0, 0x303302B-C
- #define **IOMUXC_ENET_TD3_USDHC3_DATA6** 0x3033005C, 0x6, 0x30330628, 0x0, 0x303302BC
- #define **IOMUXC_ENET_TD2_ENET_QOS_RGMII_TD2** 0x30330060, 0x0, 0x00000000, 0x0, 0x303302C0
- #define **IOMUXC_ENET_TD2_CCM_ENET_QOS_CLOCK_GENERATE_REF_CLK** 0x30330060, 0x1, 0x00000000, 0x0, 0x303302C0

- #define **IOMUXC_ENET_TD2_AUDIOMIX_SAI6_RX_DATA0** 0x30330060, 0x2, 0x3033051-C, 0x0, 0x303302C0
- #define **IOMUXC_ENET_TD2_AUDIOMIX_PDM_BIT_STREAM1** 0x30330060, 0x3, 0x303304C4, 0x0, 0x303302C0
- #define **IOMUXC_ENET_TD2_GPIO1_IO19** 0x30330060, 0x5, 0x00000000, 0x0, 0x303302C0
- #define **IOMUXC_ENET_TD2_USDHC3_DATA7** 0x30330060, 0x6, 0x3033062C, 0x0, 0x303302C0
- #define **IOMUXC_ENET_TD1_ENET_QOS_RGMII_TD1** 0x30330064, 0x0, 0x00000000, 0x0, 0x303302C4
- #define **IOMUXC_ENET_TD1_AUDIOMIX_SAI6_RX_SYNC** 0x30330064, 0x2, 0x30330520, 0x0, 0x303302C4
- #define **IOMUXC_ENET_TD1_AUDIOMIX_PDM_BIT_STREAM0** 0x30330064, 0x3, 0x303304C0, 0x0, 0x303302C4
- #define **IOMUXC_ENET_TD1_GPIO1_IO20** 0x30330064, 0x5, 0x00000000, 0x0, 0x303302C4
- #define **IOMUXC_ENET_TD1_USDHC3_CD_B** 0x30330064, 0x6, 0x30330608, 0x1, 0x303302C4
- #define **IOMUXC_ENET_TD0_ENET_QOS_RGMII_TD0** 0x30330068, 0x0, 0x00000000, 0x0, 0x303302C8
- #define **IOMUXC_ENET_TD0_AUDIOMIX_SAI6_RX_BCLK** 0x30330068, 0x2, 0x30330518, 0x0, 0x303302C8
- #define **IOMUXC_ENET_TD0_AUDIOMIX_PDM_CLK** 0x30330068, 0x3, 0x00000000, 0x0, 0x303302C8
- #define **IOMUXC_ENET_TD0_GPIO1_IO21** 0x30330068, 0x5, 0x00000000, 0x0, 0x303302C8
- #define **IOMUXC_ENET_TD0_USDHC3_WP** 0x30330068, 0x6, 0x30330634, 0x1, 0x303302-C8
- #define **IOMUXC_ENET_TX_CTL_ENET_QOS_RGMII_TX_CTL** 0x3033006C, 0x0, 0x00000000, 0x0, 0x303302CC
- #define **IOMUXC_ENET_TX_CTL_AUDIOMIX_SAI6_MCLK** 0x3033006C, 0x2, 0x30330514, 0x0, 0x303302CC
- #define **IOMUXC_ENET_TX_CTL_AUDIOMIX_SPDIF1_OUT** 0x3033006C, 0x3, 0x00000000, 0x0, 0x303302CC
- #define **IOMUXC_ENET_TX_CTL_GPIO1_IO22** 0x3033006C, 0x5, 0x00000000, 0x0, 0x303302CC
- #define **IOMUXC_ENET_TX_CTL_USDHC3_DATA0** 0x3033006C, 0x6, 0x30330610, 0x0, 0x303302CC
- #define **IOMUXC_ENET_TXC_CCM_ENET_QOS_CLOCK_GENERATE_TX_CLK** 0x30330070, 0x0, 0x00000000, 0x0, 0x303302D0
- #define **IOMUXC_ENET_TXC_ENET_QOS_TX_ER** 0x30330070, 0x1, 0x00000000, 0x0, 0x303302D0
- #define **IOMUXC_ENET_TXC_AUDIOMIX_SAI7_TX_DATA0** 0x30330070, 0x2, 0x00000000, 0x0, 0x303302D0
- #define **IOMUXC_ENET_TXC_GPIO1_IO23** 0x30330070, 0x5, 0x00000000, 0x0, 0x303302D0
- #define **IOMUXC_ENET_TXC_USDHC3_DATA1** 0x30330070, 0x6, 0x30330614, 0x0, 0x303302D0
- #define **IOMUXC_ENET_RX_CTL_ENET_QOS_RGMII_RX_CTL** 0x30330074, 0x0, 0x00000000, 0x0, 0x303302D4
- #define **IOMUXC_ENET_RX_CTL_AUDIOMIX_SAI7_TX_SYNC** 0x30330074, 0x2, 0x30330540, 0x0, 0x303302D4
- #define **IOMUXC_ENET_RX_CTL_AUDIOMIX_PDM_BIT_STREAM3** 0x30330074, 0x3, 0x303304CC, 0x1, 0x303302D4

- **#define IOMUXC_ENET_RX_CTL_GPIO1_IO24** 0x30330074, 0x5, 0x00000000, 0x0, 0x303302D4
- **#define IOMUXC_ENET_RX_CTL_USDHC3_DATA2** 0x30330074, 0x6, 0x30330618, 0x0, 0x303302D4
- **#define IOMUXC_ENET_RXC_CCM_ENET_QOS_CLOCK_GENERATE_RX_CLK** 0x30330078, 0x0, 0x00000000, 0x0, 0x303302D8
- **#define IOMUXC_ENET_RXC_ENET_QOS_RX_ER** 0x30330078, 0x1, 0x00000000, 0x0, 0x303302D8
- **#define IOMUXC_ENET_RXC_AUDIOMIX_SAI7_TX_BCLK** 0x30330078, 0x2, 0x3033053C, 0x0, 0x303302D8
- **#define IOMUXC_ENET_RXC_AUDIOMIX_PDM_BIT_STREAM2** 0x30330078, 0x3, 0x303304C8, 0x1, 0x303302D8
- **#define IOMUXC_ENET_RXC_GPIO1_IO25** 0x30330078, 0x5, 0x00000000, 0x0, 0x303302D8
- **#define IOMUXC_ENET_RXC_USDHC3_DATA3** 0x30330078, 0x6, 0x3033061C, 0x0, 0x303302D8
- **#define IOMUXC_ENET_RD0_ENET_QOS_RGMII_RD0** 0x3033007C, 0x0, 0x00000000, 0x0, 0x303302DC
- **#define IOMUXC_ENET_RD0_AUDIOMIX_SAI7_RX_DATA0** 0x3033007C, 0x2, 0x30330534, 0x0, 0x303302DC
- **#define IOMUXC_ENET_RD0_AUDIOMIX_PDM_BIT_STREAM1** 0x3033007C, 0x3, 0x303304C4, 0x1, 0x303302DC
- **#define IOMUXC_ENET_RD0_GPIO1_IO26** 0x3033007C, 0x5, 0x00000000, 0x0, 0x303302DC
- **#define IOMUXC_ENET_RD0_USDHC3_DATA4** 0x3033007C, 0x6, 0x30330620, 0x0, 0x303302DC
- **#define IOMUXC_ENET_RD1_ENET_QOS_RGMII_RD1** 0x30330080, 0x0, 0x00000000, 0x0, 0x303302E0
- **#define IOMUXC_ENET_RD1_AUDIOMIX_SAI7_RX_SYNC** 0x30330080, 0x2, 0x30330538, 0x0, 0x303302E0
- **#define IOMUXC_ENET_RD1_AUDIOMIX_PDM_BIT_STREAM0** 0x30330080, 0x3, 0x303304C0, 0x1, 0x303302E0
- **#define IOMUXC_ENET_RD1_GPIO1_IO27** 0x30330080, 0x5, 0x00000000, 0x0, 0x303302E0
- **#define IOMUXC_ENET_RD1_USDHC3_RESET_B** 0x30330080, 0x6, 0x00000000, 0x0, 0x303302E0
- **#define IOMUXC_ENET_RD2_ENET_QOS_RGMII_RD2** 0x30330084, 0x0, 0x00000000, 0x0, 0x303302E4
- **#define IOMUXC_ENET_RD2_AUDIOMIX_SAI7_RX_BCLK** 0x30330084, 0x2, 0x30330530, 0x0, 0x303302E4
- **#define IOMUXC_ENET_RD2_AUDIOMIX_PDM_CLK** 0x30330084, 0x3, 0x00000000, 0x0, 0x303302E4
- **#define IOMUXC_ENET_RD2_GPIO1_IO28** 0x30330084, 0x5, 0x00000000, 0x0, 0x303302E4
- **#define IOMUXC_ENET_RD2_USDHC3_CLK** 0x30330084, 0x6, 0x30330604, 0x0, 0x303302E4
- **#define IOMUXC_ENET_RD3_ENET_QOS_RGMII_RD3** 0x30330088, 0x0, 0x00000000, 0x0, 0x303302E8
- **#define IOMUXC_ENET_RD3_AUDIOMIX_SAI7_MCLK** 0x30330088, 0x2, 0x3033052C, 0x0, 0x303302E8
- **#define IOMUXC_ENET_RD3_AUDIOMIX_SPDIF1_IN** 0x30330088, 0x3, 0x30330544, 0x0, 0x303302E8

- #define **IOMUXC_ENET_RD3_GPIO1_IO29** 0x30330088, 0x5, 0x00000000, 0x0, 0x303302E8
- #define **IOMUXC_ENET_RD3_USDHC3_CMD** 0x30330088, 0x6, 0x3033060C, 0x0, 0x303302E8
- #define **IOMUXC_SD1_CLK_USDHC1_CLK** 0x3033008C, 0x0, 0x00000000, 0x0, 0x303302EC
- #define **IOMUXC_SD1_CLK_ENET1_MDC** 0x3033008C, 0x1, 0x00000000, 0x0, 0x303302EC
- #define **IOMUXC_SD1_CLK_I2C5_SCL** 0x3033008C, 0x3, 0x303305C4, 0x0, 0x303302EC
- #define **IOMUXC_SD1_CLK_UART1_TX** 0x3033008C, 0x4, 0x00000000, 0x0, 0x303302EC
- #define **IOMUXC_SD1_CLK_UART1_RX** 0x3033008C, 0x4, 0x303305E8, 0x0, 0x303302EC
- #define **IOMUXC_SD1_CLK_GPIO2_IO00** 0x3033008C, 0x5, 0x00000000, 0x0, 0x303302EC
- #define **IOMUXC_SD1_CMD_USDHC1_CMD** 0x30330090, 0x0, 0x00000000, 0x0, 0x303302F0
- #define **IOMUXC_SD1_CMD_ENET1_MDIO** 0x30330090, 0x1, 0x3033057C, 0x0, 0x303302F0
- #define **IOMUXC_SD1_CMD_I2C5_SDA** 0x30330090, 0x3, 0x303305C8, 0x0, 0x303302F0
- #define **IOMUXC_SD1_CMD_UART1_RX** 0x30330090, 0x4, 0x303305E8, 0x1, 0x303302F0
- #define **IOMUXC_SD1_CMD_UART1_TX** 0x30330090, 0x4, 0x00000000, 0x0, 0x303302F0
- #define **IOMUXC_SD1_CMD_GPIO2_IO01** 0x30330090, 0x5, 0x00000000, 0x0, 0x303302F0
- #define **IOMUXC_SD1_DATA0_USDHC1_DATA0** 0x30330094, 0x0, 0x00000000, 0x0, 0x303302F4
- #define **IOMUXC_SD1_DATA0_ENET1_RGMII_TD1** 0x30330094, 0x1, 0x00000000, 0x0, 0x303302F4
- #define **IOMUXC_SD1_DATA0_I2C6_SCL** 0x30330094, 0x3, 0x303305CC, 0x0, 0x303302F4
- #define **IOMUXC_SD1_DATA0_UART1_RTS_B** 0x30330094, 0x4, 0x303305E4, 0x0, 0x303302F4
- #define **IOMUXC_SD1_DATA0_UART1_CTS_B** 0x30330094, 0x4, 0x00000000, 0x0, 0x303302F4
- #define **IOMUXC_SD1_DATA0_GPIO2_IO02** 0x30330094, 0x5, 0x00000000, 0x0, 0x303302F4
- #define **IOMUXC_SD1_DATA1_USDHC1_DATA1** 0x30330098, 0x0, 0x00000000, 0x0, 0x303302F8
- #define **IOMUXC_SD1_DATA1_ENET1_RGMII_TD0** 0x30330098, 0x1, 0x00000000, 0x0, 0x303302F8
- #define **IOMUXC_SD1_DATA1_I2C6_SDA** 0x30330098, 0x3, 0x303305D0, 0x0, 0x303302F8
- #define **IOMUXC_SD1_DATA1_UART1_CTS_B** 0x30330098, 0x4, 0x00000000, 0x0, 0x303302F8
- #define **IOMUXC_SD1_DATA1_UART1_RTS_B** 0x30330098, 0x4, 0x303305E4, 0x1, 0x303302F8
- #define **IOMUXC_SD1_DATA1_GPIO2_IO03** 0x30330098, 0x5, 0x00000000, 0x0, 0x303302F8
- #define **IOMUXC_SD1_DATA2_USDHC1_DATA2** 0x3033009C, 0x0, 0x00000000, 0x0, 0x303302FC
- #define **IOMUXC_SD1_DATA2_ENET1_RGMII_RD0** 0x3033009C, 0x1, 0x30330580, 0x0, 0x303302FC
- #define **IOMUXC_SD1_DATA2_I2C4_SCL** 0x3033009C, 0x3, 0x303305BC, 0x0, 0x303302FC
- #define **IOMUXC_SD1_DATA2_UART2_TX** 0x3033009C, 0x4, 0x00000000, 0x0, 0x303302FC
- #define **IOMUXC_SD1_DATA2_UART2_RX** 0x3033009C, 0x4, 0x303305F0, 0x0, 0x303302FC
- #define **IOMUXC_SD1_DATA2_GPIO2_IO04** 0x3033009C, 0x5, 0x00000000, 0x0, 0x303302FC
- #define **IOMUXC_SD1_DATA3_USDHC1_DATA3** 0x303300A0, 0x0, 0x00000000, 0x0, 0x303302FC


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0x30330300
• #define IOMUXC_SD1_DATA3_ENET1_RGMII_RD1 0x303300A0, 0x1, 0x30330584, 0x0,
  0x30330300
• #define IOMUXC_SD1_DATA3_I2C4_SDA 0x303300A0, 0x3, 0x303305C0, 0x0, 0x30330300
• #define IOMUXC_SD1_DATA3_UART2_RX 0x303300A0, 0x4, 0x303305F0, 0x1, 0x30330300
• #define IOMUXC_SD1_DATA3_UART2_TX 0x303300A0, 0x4, 0x00000000, 0x0, 0x30330300
• #define IOMUXC_SD1_DATA3_GPIO2_IO05 0x303300A0, 0x5, 0x00000000, 0x0, 0x30330300
• #define IOMUXC_SD1_DATA4_USDHC1_DATA4 0x303300A4, 0x0, 0x00000000, 0x0,
  0x30330304
• #define IOMUXC_SD1_DATA4_ENET1_RGMII_TX_CTL 0x303300A4, 0x1, 0x00000000,
  0x0, 0x30330304
• #define IOMUXC_SD1_DATA4_I2C1_SCL 0x303300A4, 0x3, 0x303305A4, 0x0, 0x30330304
• #define IOMUXC_SD1_DATA4_UART2_RTS_B 0x303300A4, 0x4, 0x303305EC, 0x0,
  0x30330304
• #define IOMUXC_SD1_DATA4_UART2_CTS_B 0x303300A4, 0x4, 0x00000000, 0x0,
  0x30330304
• #define IOMUXC_SD1_DATA4_GPIO2_IO06 0x303300A4, 0x5, 0x00000000, 0x0, 0x30330304
• #define IOMUXC_SD1_DATA5_USDHC1_DATA5 0x303300A8, 0x0, 0x00000000, 0x0,
  0x30330308
• #define IOMUXC_SD1_DATA5_ENET1_TX_ER 0x303300A8, 0x1, 0x00000000, 0x0,
  0x30330308
• #define IOMUXC_SD1_DATA5_I2C1_SDA 0x303300A8, 0x3, 0x303305A8, 0x0, 0x30330308
• #define IOMUXC_SD1_DATA5_UART2_CTS_B 0x303300A8, 0x4, 0x00000000, 0x0,
  0x30330308
• #define IOMUXC_SD1_DATA5_UART2_RTS_B 0x303300A8, 0x4, 0x303305EC, 0x1,
  0x30330308
• #define IOMUXC_SD1_DATA5_GPIO2_IO07 0x303300A8, 0x5, 0x00000000, 0x0, 0x30330308
• #define IOMUXC_SD1_DATA6_USDHC1_DATA6 0x303300AC, 0x0, 0x00000000, 0x0,
  0x3033030C
• #define IOMUXC_SD1_DATA6_ENET1_RGMII_RX_CTL 0x303300AC, 0x1, 0x30330588,
  0x0, 0x3033030C
• #define IOMUXC_SD1_DATA6_I2C2_SCL 0x303300AC, 0x3, 0x303305AC, 0x0, 0x3033030C
• #define IOMUXC_SD1_DATA6_UART3_TX 0x303300AC, 0x4, 0x00000000, 0x0, 0x3033030-
  C
• #define IOMUXC_SD1_DATA6_UART3_RX 0x303300AC, 0x4, 0x303305F8, 0x0, 0x3033030-
  C
• #define IOMUXC_SD1_DATA6_GPIO2_IO08 0x303300AC, 0x5, 0x00000000, 0x0, 0x3033030-
  C
• #define IOMUXC_SD1_DATA7_USDHC1_DATA7 0x303300B0, 0x0, 0x00000000, 0x0,
  0x30330310
• #define IOMUXC_SD1_DATA7_ENET1_RX_ER 0x303300B0, 0x1, 0x3033058C, 0x0,
  0x30330310
• #define IOMUXC_SD1_DATA7_I2C2_SDA 0x303300B0, 0x3, 0x303305B0, 0x0, 0x30330310
• #define IOMUXC_SD1_DATA7_UART3_RX 0x303300B0, 0x4, 0x303305F8, 0x1, 0x30330310
• #define IOMUXC_SD1_DATA7_UART3_TX 0x303300B0, 0x4, 0x00000000, 0x0, 0x30330310
• #define IOMUXC_SD1_DATA7_GPIO2_IO09 0x303300B0, 0x5, 0x00000000, 0x0, 0x30330310
• #define IOMUXC_SD1_RESET_B_USDHC1_RESET_B 0x303300B4, 0x0, 0x00000000, 0x0,
  0x30330314
• #define IOMUXC_SD1_RESET_B_ENET1_TX_CLK 0x303300B4, 0x1, 0x30330578, 0x0,
  0x30330314
• #define IOMUXC_SD1_RESET_B_I2C3_SCL 0x303300B4, 0x3, 0x303305B4, 0x0, 0x30330314

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- #define **IOMUXC_SD1_RESET_B_UART3_RTS_B** 0x303300B4, 0x4, 0x303305F4, 0x0, 0x30330314
- #define **IOMUXC_SD1_RESET_B_UART3_CTS_B** 0x303300B4, 0x4, 0x00000000, 0x0, 0x30330314
- #define **IOMUXC_SD1_RESET_B_GPIO2_IO10** 0x303300B4, 0x5, 0x00000000, 0x0, 0x30330314
- #define **IOMUXC_SD1_STROBE_USDHC1_STROBE** 0x303300B8, 0x0, 0x00000000, 0x0, 0x30330318
- #define **IOMUXC_SD1_STROBE_I2C3_SDA** 0x303300B8, 0x3, 0x303305B8, 0x0, 0x30330318
- #define **IOMUXC_SD1_STROBE_UART3_CTS_B** 0x303300B8, 0x4, 0x00000000, 0x0, 0x30330318
- #define **IOMUXC_SD1_STROBE_UART3_RTS_B** 0x303300B8, 0x4, 0x303305F4, 0x1, 0x30330318
- #define **IOMUXC_SD1_STROBE_GPIO2_IO11** 0x303300B8, 0x5, 0x00000000, 0x0, 0x30330318
- #define **IOMUXC_SD2_CD_B_USDHC2_CD_B** 0x303300BC, 0x0, 0x00000000, 0x0, 0x3033031C
- #define **IOMUXC_SD2_CD_B_GPIO2_IO12** 0x303300BC, 0x5, 0x00000000, 0x0, 0x3033031C
- #define **IOMUXC_SD2_CLK_USDHC2_CLK** 0x303300C0, 0x0, 0x00000000, 0x0, 0x30330320
- #define **IOMUXC_SD2_CLK_ECSP12_SCLK** 0x303300C0, 0x2, 0x30330568, 0x0, 0x30330320
- #define **IOMUXC_SD2_CLK_UART4_RX** 0x303300C0, 0x3, 0x30330600, 0x0, 0x30330320
- #define **IOMUXC_SD2_CLK_UART4_TX** 0x303300C0, 0x3, 0x00000000, 0x0, 0x30330320
- #define **IOMUXC_SD2_CLK_GPIO2_IO13** 0x303300C0, 0x5, 0x00000000, 0x0, 0x30330320
- #define **IOMUXC_SD2_CMD_USDHC2_CMD** 0x303300C4, 0x0, 0x00000000, 0x0, 0x30330324
- #define **IOMUXC_SD2_CMD_ECSP12_MOSI** 0x303300C4, 0x2, 0x30330570, 0x0, 0x30330324
- #define **IOMUXC_SD2_CMD_UART4_TX** 0x303300C4, 0x3, 0x00000000, 0x0, 0x30330324
- #define **IOMUXC_SD2_CMD_UART4_RX** 0x303300C4, 0x3, 0x30330600, 0x1, 0x30330324
- #define **IOMUXC_SD2_CMD_AUDIOMIX_PDM_CLK** 0x303300C4, 0x4, 0x00000000, 0x0, 0x30330324
- #define **IOMUXC_SD2_CMD_GPIO2_IO14** 0x303300C4, 0x5, 0x00000000, 0x0, 0x30330324
- #define **IOMUXC_SD2_DATA0_USDHC2_DATA0** 0x303300C8, 0x0, 0x00000000, 0x0, 0x30330328
- #define **IOMUXC_SD2_DATA0_I2C4_SDA** 0x303300C8, 0x2, 0x303305C0, 0x1, 0x30330328
- #define **IOMUXC_SD2_DATA0_UART2_RX** 0x303300C8, 0x3, 0x303305F0, 0x2, 0x30330328
- #define **IOMUXC_SD2_DATA0_UART2_TX** 0x303300C8, 0x3, 0x00000000, 0x0, 0x30330328
- #define **IOMUXC_SD2_DATA0_AUDIOMIX_PDM_BIT_STREAM0** 0x303300C8, 0x4, 0x303304C0, 0x2, 0x30330328
- #define **IOMUXC_SD2_DATA0_GPIO2_IO15** 0x303300C8, 0x5, 0x00000000, 0x0, 0x30330328
- #define **IOMUXC_SD2_DATA1_USDHC2_DATA1** 0x303300CC, 0x0, 0x00000000, 0x0, 0x3033032C
- #define **IOMUXC_SD2_DATA1_I2C4_SCL** 0x303300CC, 0x2, 0x303305BC, 0x1, 0x3033032C
- #define **IOMUXC_SD2_DATA1_UART2_TX** 0x303300CC, 0x3, 0x00000000, 0x0, 0x3033032C
- #define **IOMUXC_SD2_DATA1_UART2_RX** 0x303300CC, 0x3, 0x303305F0, 0x3, 0x3033032C
- #define **IOMUXC_SD2_DATA1_AUDIOMIX_PDM_BIT_STREAM1** 0x303300CC, 0x4, 0x303304C4, 0x2, 0x3033032C
- #define **IOMUXC_SD2_DATA1_GPIO2_IO16** 0x303300CC, 0x5, 0x00000000, 0x0, 0x3033032C
- #define **IOMUXC_SD2_DATA2_USDHC2_DATA2** 0x303300D0, 0x0, 0x00000000, 0x0, 0x30330330
- #define **IOMUXC_SD2_DATA2_ECSP12_SS0** 0x303300D0, 0x2, 0x30330574, 0x0, 0x30330330

- #define **IOMUXC_SD2_DATA2_AUDIOMIX_SPDIF1_OUT** 0x303300D0, 0x3, 0x00000000, 0x0, 0x30330330
- #define **IOMUXC_SD2_DATA2_AUDIOMIX_PDM_BIT_STREAM2** 0x303300D0, 0x4, 0x303304C8, 0x2, 0x30330330
- #define **IOMUXC_SD2_DATA2_GPIO2_IO17** 0x303300D0, 0x5, 0x00000000, 0x0, 0x30330330
- #define **IOMUXC_SD2_DATA3_USDHC2_DATA3** 0x303300D4, 0x0, 0x00000000, 0x0, 0x30330334
- #define **IOMUXC_SD2_DATA3_ECSP12_MISO** 0x303300D4, 0x2, 0x3033056C, 0x0, 0x30330334
- #define **IOMUXC_SD2_DATA3_AUDIOMIX_SPDIF1_IN** 0x303300D4, 0x3, 0x30330544, 0x1, 0x30330334
- #define **IOMUXC_SD2_DATA3_AUDIOMIX_PDM_BIT_STREAM3** 0x303300D4, 0x4, 0x303304CC, 0x2, 0x30330334
- #define **IOMUXC_SD2_DATA3_GPIO2_IO18** 0x303300D4, 0x5, 0x00000000, 0x0, 0x30330334
- #define **IOMUXC_SD2_RESET_B_USDHC2_RESET_B** 0x303300D8, 0x0, 0x00000000, 0x0, 0x30330338
- #define **IOMUXC_SD2_RESET_B_GPIO2_IO19** 0x303300D8, 0x5, 0x00000000, 0x0, 0x30330338
- #define **IOMUXC_SD2_WP_USDHC2_WP** 0x303300DC, 0x0, 0x00000000, 0x0, 0x3033033C
- #define **IOMUXC_SD2_WP_GPIO2_IO20** 0x303300DC, 0x5, 0x00000000, 0x0, 0x3033033C
- #define **IOMUXC_SD2_WP_CORESIGHT_EVENTI** 0x303300DC, 0x6, 0x00000000, 0x0, 0x3033033C
- #define **IOMUXC_NAND_ALE_NAND_ALE** 0x303300E0, 0x0, 0x00000000, 0x0, 0x30330340
- #define **IOMUXC_NAND_ALE_FLEXSPI_A_SCLK** 0x303300E0, 0x1, 0x00000000, 0x0, 0x30330340
- #define **IOMUXC_NAND_ALE_AUDIOMIX_SAI3_TX_BCLK** 0x303300E0, 0x2, 0x303304E8, 0x0, 0x30330340
- #define **IOMUXC_NAND_ALE_ISP_FL_TRIG_0** 0x303300E0, 0x3, 0x303305D4, 0x1, 0x30330340
- #define **IOMUXC_NAND_ALE_UART3_RX** 0x303300E0, 0x4, 0x303305F8, 0x2, 0x30330340
- #define **IOMUXC_NAND_ALE_UART3_TX** 0x303300E0, 0x4, 0x00000000, 0x0, 0x30330340
- #define **IOMUXC_NAND_ALE_GPIO3_IO00** 0x303300E0, 0x5, 0x00000000, 0x0, 0x30330340
- #define **IOMUXC_NAND_ALE_CORESIGHT_TRACE_CLK** 0x303300E0, 0x6, 0x00000000, 0x0, 0x30330340
- #define **IOMUXC_NAND_CE0_B_NAND_CE0_B** 0x303300E4, 0x0, 0x00000000, 0x0, 0x30330344
- #define **IOMUXC_NAND_CE0_B_FLEXSPI_A_SS0_B** 0x303300E4, 0x1, 0x00000000, 0x0, 0x30330344
- #define **IOMUXC_NAND_CE0_B_AUDIOMIX_SAI3_TX_DATA0** 0x303300E4, 0x2, 0x00000000, 0x0, 0x30330344
- #define **IOMUXC_NAND_CE0_B_ISP_SHUTTER_TRIG_0** 0x303300E4, 0x3, 0x303305DC, 0x1, 0x30330344
- #define **IOMUXC_NAND_CE0_B_UART3_TX** 0x303300E4, 0x4, 0x00000000, 0x0, 0x30330344
- #define **IOMUXC_NAND_CE0_B_UART3_RX** 0x303300E4, 0x4, 0x303305F8, 0x3, 0x30330344
- #define **IOMUXC_NAND_CE0_B_GPIO3_IO01** 0x303300E4, 0x5, 0x00000000, 0x0, 0x30330344
- #define **IOMUXC_NAND_CE0_B_CORESIGHT_TRACE_CTL** 0x303300E4, 0x6, 0x00000000, 0x0, 0x30330344
- #define **IOMUXC_NAND_CE1_B_NAND_CE1_B** 0x303300E8, 0x0, 0x00000000, 0x0, 0x30330348
- #define **IOMUXC_NAND_CE1_B_FLEXSPI_A_SS1_B** 0x303300E8, 0x1, 0x00000000, 0x0, 0x30330348

- 0x30330348
- #define **IOMUXC_NAND_CE1_B_USDHC3_STROBE** 0x303300E8, 0x2, 0x30330630, 0x1, 0x30330348
- #define **IOMUXC_NAND_CE1_B_I2C4_SCL** 0x303300E8, 0x4, 0x303305BC, 0x2, 0x30330348
- #define **IOMUXC_NAND_CE1_B_GPIO3_IO02** 0x303300E8, 0x5, 0x00000000, 0x0, 0x30330348
- #define **IOMUXC_NAND_CE1_B_CORESIGHT_TRACE00** 0x303300E8, 0x6, 0x00000000, 0x0, 0x30330348
- #define **IOMUXC_NAND_CE2_B_NAND_CE2_B** 0x303300EC, 0x0, 0x00000000, 0x0, 0x3033034C
- #define **IOMUXC_NAND_CE2_B_FLEXSPI_B_SS0_B** 0x303300EC, 0x1, 0x00000000, 0x0, 0x3033034C
- #define **IOMUXC_NAND_CE2_B_USDHC3_DATA5** 0x303300EC, 0x2, 0x30330624, 0x1, 0x3033034C
- #define **IOMUXC_NAND_CE2_B_I2C4_SDA** 0x303300EC, 0x4, 0x303305C0, 0x2, 0x3033034C
- #define **IOMUXC_NAND_CE2_B_GPIO3_IO03** 0x303300EC, 0x5, 0x00000000, 0x0, 0x3033034C
- #define **IOMUXC_NAND_CE2_B_CORESIGHT_TRACE01** 0x303300EC, 0x6, 0x00000000, 0x0, 0x3033034C
- #define **IOMUXC_NAND_CE3_B_NAND_CE3_B** 0x303300F0, 0x0, 0x00000000, 0x0, 0x30330350
- #define **IOMUXC_NAND_CE3_B_FLEXSPI_B_SS1_B** 0x303300F0, 0x1, 0x00000000, 0x0, 0x30330350
- #define **IOMUXC_NAND_CE3_B_USDHC3_DATA6** 0x303300F0, 0x2, 0x30330628, 0x1, 0x30330350
- #define **IOMUXC_NAND_CE3_B_I2C3_SDA** 0x303300F0, 0x4, 0x303305B8, 0x1, 0x30330350
- #define **IOMUXC_NAND_CE3_B_GPIO3_IO04** 0x303300F0, 0x5, 0x00000000, 0x0, 0x30330350
- #define **IOMUXC_NAND_CE3_B_CORESIGHT_TRACE02** 0x303300F0, 0x6, 0x00000000, 0x0, 0x30330350
- #define **IOMUXC_NAND_CLE_NAND_CLE** 0x303300F4, 0x0, 0x00000000, 0x0, 0x30330354
- #define **IOMUXC_NAND_CLE_FLEXSPI_B_SCLK** 0x303300F4, 0x1, 0x00000000, 0x0, 0x30330354
- #define **IOMUXC_NAND_CLE_USDHC3_DATA7** 0x303300F4, 0x2, 0x3033062C, 0x1, 0x30330354
- #define **IOMUXC_NAND_CLE_UART4_RX** 0x303300F4, 0x4, 0x30330600, 0x2, 0x30330354
- #define **IOMUXC_NAND_CLE_UART4_TX** 0x303300F4, 0x4, 0x00000000, 0x0, 0x30330354
- #define **IOMUXC_NAND_CLE_GPIO3_IO05** 0x303300F4, 0x5, 0x00000000, 0x0, 0x30330354
- #define **IOMUXC_NAND_CLE_CORESIGHT_TRACE03** 0x303300F4, 0x6, 0x00000000, 0x0, 0x30330354
- #define **IOMUXC_NAND_DATA00_NAND_DATA00** 0x303300F8, 0x0, 0x00000000, 0x0, 0x30330358
- #define **IOMUXC_NAND_DATA00_FLEXSPI_A_DATA0** 0x303300F8, 0x1, 0x00000000, 0x0, 0x30330358
- #define **IOMUXC_NAND_DATA00_AUDIOMIX_SAI3_RX_DATA0** 0x303300F8, 0x2, 0x303304E4, 0x0, 0x30330358
- #define **IOMUXC_NAND_DATA00_ISP_FLASH_TRIG_0** 0x303300F8, 0x3, 0x00000000, 0x0, 0x30330358
- #define **IOMUXC_NAND_DATA00_UART4_RX** 0x303300F8, 0x4, 0x30330600, 0x3,

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0x30330358
• #define IOMUXC_NAND_DATA00_UART4_TX 0x303300F8, 0x4, 0x00000000, 0x0,
  0x30330358
• #define IOMUXC_NAND_DATA00_GPIO3_IO06 0x303300F8, 0x5, 0x00000000, 0x0,
  0x30330358
• #define IOMUXC_NAND_DATA00_CORESIGHT_TRACE04 0x303300F8, 0x6, 0x00000000,
  0x0, 0x30330358
• #define IOMUXC_NAND_DATA01_NAND_DATA01 0x303300FC, 0x0, 0x00000000, 0x0,
  0x3033035C
• #define IOMUXC_NAND_DATA01_FLEXSPI_A_DATA1 0x303300FC, 0x1, 0x00000000,
  0x0, 0x3033035C
• #define IOMUXC_NAND_DATA01_AUDIOMIX_SAI3_TX_SYNC 0x303300FC, 0x2,
  0x303304EC, 0x0, 0x3033035C
• #define IOMUXC_NAND_DATA01_ISP_PRELIGHT_TRIG_0 0x303300FC, 0x3, 0x00000000,
  0x0, 0x3033035C
• #define IOMUXC_NAND_DATA01_UART4_TX 0x303300FC, 0x4, 0x00000000, 0x0,
  0x3033035C
• #define IOMUXC_NAND_DATA01_UART4_RX 0x303300FC, 0x4, 0x30330600, 0x4,
  0x3033035C
• #define IOMUXC_NAND_DATA01_GPIO3_IO07 0x303300FC, 0x5, 0x00000000, 0x0,
  0x3033035C
• #define IOMUXC_NAND_DATA01_CORESIGHT_TRACE05 0x303300FC, 0x6, 0x00000000,
  0x0, 0x3033035C
• #define IOMUXC_NAND_DATA02_NAND_DATA02 0x30330100, 0x0, 0x00000000, 0x0,
  0x30330360
• #define IOMUXC_NAND_DATA02_FLEXSPI_A_DATA2 0x30330100, 0x1, 0x00000000, 0x0,
  0x30330360
• #define IOMUXC_NAND_DATA02_USDHC3_CD_B 0x30330100, 0x2, 0x30330608, 0x2,
  0x30330360
• #define IOMUXC_NAND_DATA02_UART4_CTS_B 0x30330100, 0x3, 0x00000000, 0x0,
  0x30330360
• #define IOMUXC_NAND_DATA02_UART4_RTS_B 0x30330100, 0x3, 0x303305FC, 0x0,
  0x30330360
• #define IOMUXC_NAND_DATA02_I2C4_SDA 0x30330100, 0x4, 0x303305C0, 0x3, 0x30330360
• #define IOMUXC_NAND_DATA02_GPIO3_IO08 0x30330100, 0x5, 0x00000000, 0x0,
  0x30330360
• #define IOMUXC_NAND_DATA02_CORESIGHT_TRACE06 0x30330100, 0x6, 0x00000000,
  0x0, 0x30330360
• #define IOMUXC_NAND_DATA03_NAND_DATA03 0x30330104, 0x0, 0x00000000, 0x0,
  0x30330364
• #define IOMUXC_NAND_DATA03_FLEXSPI_A_DATA3 0x30330104, 0x1, 0x00000000, 0x0,
  0x30330364
• #define IOMUXC_NAND_DATA03_USDHC3_WP 0x30330104, 0x2, 0x30330634, 0x2,
  0x30330364
• #define IOMUXC_NAND_DATA03_UART4_RTS_B 0x30330104, 0x3, 0x303305FC, 0x1,
  0x30330364
• #define IOMUXC_NAND_DATA03_UART4_CTS_B 0x30330104, 0x3, 0x00000000, 0x0,
  0x30330364
• #define IOMUXC_NAND_DATA03_ISP_FL_TRIG_1 0x30330104, 0x4, 0x303305D8, 0x1,
  0x30330364

```

- `#define IOMUXC_NAND_DATA03_GPIO3_IO09 0x30330104, 0x5, 0x00000000, 0x0, 0x30330364`
- `#define IOMUXC_NAND_DATA03_CORESIGHT_TRACE07 0x30330104, 0x6, 0x00000000, 0x0, 0x30330364`
- `#define IOMUXC_NAND_DATA04_NAND_DATA04 0x30330108, 0x0, 0x00000000, 0x0, 0x30330368`
- `#define IOMUXC_NAND_DATA04_FLEXSPI_B_DATA0 0x30330108, 0x1, 0x00000000, 0x0, 0x30330368`
- `#define IOMUXC_NAND_DATA04_USDHC3_DATA0 0x30330108, 0x2, 0x30330610, 0x1, 0x30330368`
- `#define IOMUXC_NAND_DATA04_FLEXSPI_A_DATA4 0x30330108, 0x3, 0x00000000, 0x0, 0x30330368`
- `#define IOMUXC_NAND_DATA04_ISP_SHUTTER_TRIG_1 0x30330108, 0x4, 0x303305E0, 0x1, 0x30330368`
- `#define IOMUXC_NAND_DATA04_GPIO3_IO10 0x30330108, 0x5, 0x00000000, 0x0, 0x30330368`
- `#define IOMUXC_NAND_DATA04_CORESIGHT_TRACE08 0x30330108, 0x6, 0x00000000, 0x0, 0x30330368`
- `#define IOMUXC_NAND_DATA05_NAND_DATA05 0x3033010C, 0x0, 0x00000000, 0x0, 0x3033036C`
- `#define IOMUXC_NAND_DATA05_FLEXSPI_B_DATA1 0x3033010C, 0x1, 0x00000000, 0x0, 0x3033036C`
- `#define IOMUXC_NAND_DATA05_USDHC3_DATA1 0x3033010C, 0x2, 0x30330614, 0x1, 0x3033036C`
- `#define IOMUXC_NAND_DATA05_FLEXSPI_A_DATA5 0x3033010C, 0x3, 0x00000000, 0x0, 0x3033036C`
- `#define IOMUXC_NAND_DATA05_ISP_FLASH_TRIG_1 0x3033010C, 0x4, 0x00000000, 0x0, 0x3033036C`
- `#define IOMUXC_NAND_DATA05_GPIO3_IO11 0x3033010C, 0x5, 0x00000000, 0x0, 0x3033036C`
- `#define IOMUXC_NAND_DATA05_CORESIGHT_TRACE09 0x3033010C, 0x6, 0x00000000, 0x0, 0x3033036C`
- `#define IOMUXC_NAND_DATA06_NAND_DATA06 0x30330110, 0x0, 0x00000000, 0x0, 0x30330370`
- `#define IOMUXC_NAND_DATA06_FLEXSPI_B_DATA2 0x30330110, 0x1, 0x00000000, 0x0, 0x30330370`
- `#define IOMUXC_NAND_DATA06_USDHC3_DATA2 0x30330110, 0x2, 0x30330618, 0x1, 0x30330370`
- `#define IOMUXC_NAND_DATA06_FLEXSPI_A_DATA6 0x30330110, 0x3, 0x00000000, 0x0, 0x30330370`
- `#define IOMUXC_NAND_DATA06_ISP_PRELIGHT_TRIG_1 0x30330110, 0x4, 0x00000000, 0x0, 0x30330370`
- `#define IOMUXC_NAND_DATA06_GPIO3_IO12 0x30330110, 0x5, 0x00000000, 0x0, 0x30330370`
- `#define IOMUXC_NAND_DATA06_CORESIGHT_TRACE10 0x30330110, 0x6, 0x00000000, 0x0, 0x30330370`
- `#define IOMUXC_NAND_DATA07_NAND_DATA07 0x30330114, 0x0, 0x00000000, 0x0, 0x30330374`
- `#define IOMUXC_NAND_DATA07_FLEXSPI_B_DATA3 0x30330114, 0x1, 0x00000000, 0x0, 0x30330374`

- 0x30330374
- #define **IOMUXC_NAND_DATA07_USDHC3_DATA3** 0x30330114, 0x2, 0x3033061C, 0x1, 0x30330374
- #define **IOMUXC_NAND_DATA07_FLEXSPI_A_DATA7** 0x30330114, 0x3, 0x00000000, 0x0, 0x30330374
- #define **IOMUXC_NAND_DATA07_ISP_SHUTTER_OPEN_1** 0x30330114, 0x4, 0x00000000, 0x0, 0x30330374
- #define **IOMUXC_NAND_DATA07_GPIO3_IO13** 0x30330114, 0x5, 0x00000000, 0x0, 0x30330374
- #define **IOMUXC_NAND_DATA07_CORESIGHT_TRACE11** 0x30330114, 0x6, 0x00000000, 0x0, 0x30330374
- #define **IOMUXC_NAND_DQS_NAND_DQS** 0x30330118, 0x0, 0x00000000, 0x0, 0x30330378
- #define **IOMUXC_NAND_DQS_FLEXSPI_A_DQS** 0x30330118, 0x1, 0x00000000, 0x0, 0x30330378
- #define **IOMUXC_NAND_DQS_AUDIOMIX_SAI3_MCLK** 0x30330118, 0x2, 0x303304E0, 0x0, 0x30330378
- #define **IOMUXC_NAND_DQS_ISP_SHUTTER_OPEN_0** 0x30330118, 0x3, 0x00000000, 0x0, 0x30330378
- #define **IOMUXC_NAND_DQS_I2C3_SCL** 0x30330118, 0x4, 0x303305B4, 0x1, 0x30330378
- #define **IOMUXC_NAND_DQS_GPIO3_IO14** 0x30330118, 0x5, 0x00000000, 0x0, 0x30330378
- #define **IOMUXC_NAND_DQS_CORESIGHT_TRACE12** 0x30330118, 0x6, 0x00000000, 0x0, 0x30330378
- #define **IOMUXC_NAND_RE_B_NAND_RE_B** 0x3033011C, 0x0, 0x00000000, 0x0, 0x3033037-C
- #define **IOMUXC_NAND_RE_B_FLEXSPI_B_DQS** 0x3033011C, 0x1, 0x00000000, 0x0, 0x3033037C
- #define **IOMUXC_NAND_RE_B_USDHC3_DATA4** 0x3033011C, 0x2, 0x30330620, 0x1, 0x3033037C
- #define **IOMUXC_NAND_RE_B_UART4_TX** 0x3033011C, 0x4, 0x00000000, 0x0, 0x3033037-C
- #define **IOMUXC_NAND_RE_B_UART4_RX** 0x3033011C, 0x4, 0x30330600, 0x5, 0x3033037-C
- #define **IOMUXC_NAND_RE_B_GPIO3_IO15** 0x3033011C, 0x5, 0x00000000, 0x0, 0x3033037-C
- #define **IOMUXC_NAND_RE_B_CORESIGHT_TRACE13** 0x3033011C, 0x6, 0x00000000, 0x0, 0x3033037C
- #define **IOMUXC_NAND_READY_B_NAND_READY_B** 0x30330120, 0x0, 0x00000000, 0x0, 0x30330380
- #define **IOMUXC_NAND_READY_B_USDHC3_RESET_B** 0x30330120, 0x2, 0x00000000, 0x0, 0x30330380
- #define **IOMUXC_NAND_READY_B_I2C3_SCL** 0x30330120, 0x4, 0x303305B4, 0x2, 0x30330380
- #define **IOMUXC_NAND_READY_B_GPIO3_IO16** 0x30330120, 0x5, 0x00000000, 0x0, 0x30330380
- #define **IOMUXC_NAND_READY_B_CORESIGHT_TRACE14** 0x30330120, 0x6, 0x00000000, 0x0, 0x30330380
- #define **IOMUXC_NAND_WE_B_NAND_WE_B** 0x30330124, 0x0, 0x00000000, 0x0, 0x30330384
- #define **IOMUXC_NAND_WE_B_USDHC3_CLK** 0x30330124, 0x2, 0x30330604, 0x1, 0x30330384

- #define **IOMUXC_NAND_WE_B_I2C3_SDA** 0x30330124, 0x4, 0x303305B8, 0x2, 0x30330384
- #define **IOMUXC_NAND_WE_B_GPIO3_IO17** 0x30330124, 0x5, 0x00000000, 0x0, 0x30330384
- #define **IOMUXC_NAND_WE_B_CORESIGHT_TRACE15** 0x30330124, 0x6, 0x00000000, 0x0, 0x30330384
- #define **IOMUXC_NAND_WP_B_NAND_WP_B** 0x30330128, 0x0, 0x00000000, 0x0, 0x30330388
- #define **IOMUXC_NAND_WP_B_USDHC3_CMD** 0x30330128, 0x2, 0x3033060C, 0x1, 0x30330388
- #define **IOMUXC_NAND_WP_B_I2C4_SCL** 0x30330128, 0x4, 0x303305BC, 0x3, 0x30330388
- #define **IOMUXC_NAND_WP_B_GPIO3_IO18** 0x30330128, 0x5, 0x00000000, 0x0, 0x30330388
- #define **IOMUXC_NAND_WP_B_CORESIGHT_EVENT0** 0x30330128, 0x6, 0x00000000, 0x0, 0x30330388
- #define **IOMUXC_SAI5_RXFS_AUDIOMIX_SAI5_RX_SYNC** 0x3033012C, 0x0, 0x30330508, 0x0, 0x3033038C
- #define **IOMUXC_SAI5_RXFS_AUDIOMIX_SAI1_TX_DATA0** 0x3033012C, 0x1, 0x00000000, 0x0, 0x3033038C
- #define **IOMUXC_SAI5_RXFS_PWM4_OUT** 0x3033012C, 0x2, 0x00000000, 0x0, 0x3033038C
- #define **IOMUXC_SAI5_RXFS_I2C6_SCL** 0x3033012C, 0x3, 0x303305CC, 0x1, 0x3033038C
- #define **IOMUXC_SAI5_RXFS_GPIO3_IO19** 0x3033012C, 0x5, 0x00000000, 0x0, 0x3033038C
- #define **IOMUXC_SAI5_RXC_AUDIOMIX_SAI5_RX_BCLK** 0x30330130, 0x0, 0x303304F4, 0x0, 0x30330390
- #define **IOMUXC_SAI5_RXC_AUDIOMIX_SAI1_TX_DATA1** 0x30330130, 0x1, 0x00000000, 0x0, 0x30330390
- #define **IOMUXC_SAI5_RXC_PWM3_OUT** 0x30330130, 0x2, 0x00000000, 0x0, 0x30330390
- #define **IOMUXC_SAI5_RXC_I2C6_SDA** 0x30330130, 0x3, 0x303305D0, 0x1, 0x30330390
- #define **IOMUXC_SAI5_RXC_AUDIOMIX_PDM_CLK** 0x30330130, 0x4, 0x00000000, 0x0, 0x30330390
- #define **IOMUXC_SAI5_RXC_GPIO3_IO20** 0x30330130, 0x5, 0x00000000, 0x0, 0x30330390
- #define **IOMUXC_SAI5_RXD0_AUDIOMIX_SAI5_RX_DATA0** 0x30330134, 0x0, 0x303304F8, 0x0, 0x30330394
- #define **IOMUXC_SAI5_RXD0_AUDIOMIX_SAI1_TX_DATA2** 0x30330134, 0x1, 0x00000000, 0x0, 0x30330394
- #define **IOMUXC_SAI5_RXD0_PWM2_OUT** 0x30330134, 0x2, 0x00000000, 0x0, 0x30330394
- #define **IOMUXC_SAI5_RXD0_I2C5_SCL** 0x30330134, 0x3, 0x303305C4, 0x1, 0x30330394
- #define **IOMUXC_SAI5_RXD0_AUDIOMIX_PDM_BIT_STREAM0** 0x30330134, 0x4, 0x303304C0, 0x3, 0x30330394
- #define **IOMUXC_SAI5_RXD0_GPIO3_IO21** 0x30330134, 0x5, 0x00000000, 0x0, 0x30330394
- #define **IOMUXC_SAI5_RXD1_AUDIOMIX_SAI5_RX_DATA1** 0x30330138, 0x0, 0x303304FC, 0x0, 0x30330398
- #define **IOMUXC_SAI5_RXD1_AUDIOMIX_SAI1_TX_DATA3** 0x30330138, 0x1, 0x00000000, 0x0, 0x30330398
- #define **IOMUXC_SAI5_RXD1_AUDIOMIX_SAI1_TX_SYNC** 0x30330138, 0x2, 0x303304D8, 0x0, 0x30330398
- #define **IOMUXC_SAI5_RXD1_AUDIOMIX_SAI5_TX_SYNC** 0x30330138, 0x3, 0x30330510, 0x0, 0x30330398
- #define **IOMUXC_SAI5_RXD1_AUDIOMIX_PDM_BIT_STREAM1** 0x30330138, 0x4, 0x303304C4, 0x3, 0x30330398
- #define **IOMUXC_SAI5_RXD1_GPIO3_IO22** 0x30330138, 0x5, 0x00000000, 0x0, 0x30330398
- #define **IOMUXC_SAI5_RXD1_CAN1_TX** 0x30330138, 0x6, 0x00000000, 0x0, 0x30330398

- #define **IOMUXC_SAI5_RXD2_AUDIOMIX_SAI5_RX_DATA2** 0x3033013C, 0x0, 0x30330500, 0x0, 0x3033039C
- #define **IOMUXC_SAI5_RXD2_AUDIOMIX_SAI1_TX_DATA4** 0x3033013C, 0x1, 0x00000000, 0x0, 0x3033039C
- #define **IOMUXC_SAI5_RXD2_AUDIOMIX_SAI1_TX_SYNC** 0x3033013C, 0x2, 0x303304D8, 0x1, 0x3033039C
- #define **IOMUXC_SAI5_RXD2_AUDIOMIX_SAI5_TX_BCLK** 0x3033013C, 0x3, 0x3033050C, 0x0, 0x3033039C
- #define **IOMUXC_SAI5_RXD2_AUDIOMIX_PDM_BIT_STREAM2** 0x3033013C, 0x4, 0x303304C8, 0x3, 0x3033039C
- #define **IOMUXC_SAI5_RXD2_GPIO3_IO23** 0x3033013C, 0x5, 0x00000000, 0x0, 0x3033039C
- #define **IOMUXC_SAI5_RXD2_CAN1_RX** 0x3033013C, 0x6, 0x3033054C, 0x0, 0x3033039C
- #define **IOMUXC_SAI5_RXD3_AUDIOMIX_SAI5_RX_DATA3** 0x30330140, 0x0, 0x30330504, 0x0, 0x303303A0
- #define **IOMUXC_SAI5_RXD3_AUDIOMIX_SAI1_TX_DATA5** 0x30330140, 0x1, 0x00000000, 0x0, 0x303303A0
- #define **IOMUXC_SAI5_RXD3_AUDIOMIX_SAI1_TX_SYNC** 0x30330140, 0x2, 0x303304D8, 0x2, 0x303303A0
- #define **IOMUXC_SAI5_RXD3_AUDIOMIX_SAI5_TX_DATA0** 0x30330140, 0x3, 0x00000000, 0x0, 0x303303A0
- #define **IOMUXC_SAI5_RXD3_AUDIOMIX_PDM_BIT_STREAM3** 0x30330140, 0x4, 0x303304CC, 0x3, 0x303303A0
- #define **IOMUXC_SAI5_RXD3_GPIO3_IO24** 0x30330140, 0x5, 0x00000000, 0x0, 0x303303A0
- #define **IOMUXC_SAI5_RXD3_CAN2_TX** 0x30330140, 0x6, 0x00000000, 0x0, 0x303303A0
- #define **IOMUXC_SAI5_MCLK_AUDIOMIX_SAI5_MCLK** 0x30330144, 0x0, 0x303304F0, 0x0, 0x303303A4
- #define **IOMUXC_SAI5_MCLK_AUDIOMIX_SAI1_TX_BCLK** 0x30330144, 0x1, 0x303304D4, 0x0, 0x303303A4
- #define **IOMUXC_SAI5_MCLK_PWM1_OUT** 0x30330144, 0x2, 0x00000000, 0x0, 0x303303A4
- #define **IOMUXC_SAI5_MCLK_I2C5_SDA** 0x30330144, 0x3, 0x303305C8, 0x1, 0x303303A4
- #define **IOMUXC_SAI5_MCLK_GPIO3_IO25** 0x30330144, 0x5, 0x00000000, 0x0, 0x303303A4
- #define **IOMUXC_SAI5_MCLK_CAN2_RX** 0x30330144, 0x6, 0x30330550, 0x0, 0x303303A4
- #define **IOMUXC_SAI1_RXFS_AUDIOMIX_SAI1_RX_SYNC** 0x30330148, 0x0, 0x303304D0, 0x0, 0x303303A8
- #define **IOMUXC_SAI1_RXFS_ENET1_1588_EVENT0_IN** 0x30330148, 0x4, 0x00000000, 0x0, 0x303303A8
- #define **IOMUXC_SAI1_RXFS_GPIO4_IO00** 0x30330148, 0x5, 0x00000000, 0x0, 0x303303A8
- #define **IOMUXC_SAI1_RXC_AUDIOMIX_SAI1_RX_BCLK** 0x3033014C, 0x0, 0x00000000, 0x0, 0x303303AC
- #define **IOMUXC_SAI1_RXC_AUDIOMIX_PDM_CLK** 0x3033014C, 0x3, 0x00000000, 0x0, 0x303303AC
- #define **IOMUXC_SAI1_RXC_ENET1_1588_EVENT0_OUT** 0x3033014C, 0x4, 0x00000000, 0x0, 0x303303AC
- #define **IOMUXC_SAI1_RXC_GPIO4_IO01** 0x3033014C, 0x5, 0x00000000, 0x0, 0x303303AC
- #define **IOMUXC_SAI1_RXD0_AUDIOMIX_SAI1_RX_DATA0** 0x30330150, 0x0, 0x00000000, 0x0, 0x303303B0
- #define **IOMUXC_SAI1_RXD0_AUDIOMIX_SAI1_TX_DATA1** 0x30330150, 0x2, 0x00000000, 0x0, 0x303303B0

- 0x0, 0x303303B0
- #define **IOMUXC_SAI1_RXD0_AUDIOMIX_PDM_BIT_STREAM0** 0x30330150, 0x3, 0x303304C0, 0x4, 0x303303B0
- #define **IOMUXC_SAI1_RXD0_ENET1_1588_EVENT1_IN** 0x30330150, 0x4, 0x00000000, 0x0, 0x303303B0
- #define **IOMUXC_SAI1_RXD0_GPIO4_IO02** 0x30330150, 0x5, 0x00000000, 0x0, 0x303303B0
- #define **IOMUXC_SAI1_RXD1_AUDIOMIX_SAI1_RX_DATA1** 0x30330154, 0x0, 0x00000000, 0x0, 0x303303B4
- #define **IOMUXC_SAI1_RXD1_AUDIOMIX_PDM_BIT_STREAM1** 0x30330154, 0x3, 0x303304C4, 0x4, 0x303303B4
- #define **IOMUXC_SAI1_RXD1_ENET1_1588_EVENT1_OUT** 0x30330154, 0x4, 0x00000000, 0x0, 0x303303B4
- #define **IOMUXC_SAI1_RXD1_GPIO4_IO03** 0x30330154, 0x5, 0x00000000, 0x0, 0x303303B4
- #define **IOMUXC_SAI1_RXD2_AUDIOMIX_SAI1_RX_DATA2** 0x30330158, 0x0, 0x00000000, 0x0, 0x303303B8
- #define **IOMUXC_SAI1_RXD2_AUDIOMIX_PDM_BIT_STREAM2** 0x30330158, 0x3, 0x303304C8, 0x4, 0x303303B8
- #define **IOMUXC_SAI1_RXD2_ENET1_MDC** 0x30330158, 0x4, 0x00000000, 0x0, 0x303303B8
- #define **IOMUXC_SAI1_RXD2_GPIO4_IO04** 0x30330158, 0x5, 0x00000000, 0x0, 0x303303B8
- #define **IOMUXC_SAI1_RXD3_AUDIOMIX_SAI1_RX_DATA3** 0x3033015C, 0x0, 0x00000000, 0x0, 0x303303BC
- #define **IOMUXC_SAI1_RXD3_AUDIOMIX_PDM_BIT_STREAM3** 0x3033015C, 0x3, 0x303304CC, 0x4, 0x303303BC
- #define **IOMUXC_SAI1_RXD3_ENET1_MDIO** 0x3033015C, 0x4, 0x3033057C, 0x1, 0x303303BC
- #define **IOMUXC_SAI1_RXD3_GPIO4_IO05** 0x3033015C, 0x5, 0x00000000, 0x0, 0x303303BC
- #define **IOMUXC_SAI1_RXD4_AUDIOMIX_SAI1_RX_DATA4** 0x30330160, 0x0, 0x00000000, 0x0, 0x303303C0
- #define **IOMUXC_SAI1_RXD4_AUDIOMIX_SAI6_TX_BCLK** 0x30330160, 0x1, 0x30330524, 0x1, 0x303303C0
- #define **IOMUXC_SAI1_RXD4_AUDIOMIX_SAI6_RX_BCLK** 0x30330160, 0x2, 0x30330518, 0x1, 0x303303C0
- #define **IOMUXC_SAI1_RXD4_ENET1_RGMII_RD0** 0x30330160, 0x4, 0x30330580, 0x1, 0x303303C0
- #define **IOMUXC_SAI1_RXD4_GPIO4_IO06** 0x30330160, 0x5, 0x00000000, 0x0, 0x303303C0
- #define **IOMUXC_SAI1_RXD5_AUDIOMIX_SAI1_RX_DATA5** 0x30330164, 0x0, 0x00000000, 0x0, 0x303303C4
- #define **IOMUXC_SAI1_RXD5_AUDIOMIX_SAI6_TX_DATA0** 0x30330164, 0x1, 0x00000000, 0x0, 0x303303C4
- #define **IOMUXC_SAI1_RXD5_AUDIOMIX_SAI6_RX_DATA0** 0x30330164, 0x2, 0x3033051C, 0x1, 0x303303C4
- #define **IOMUXC_SAI1_RXD5_AUDIOMIX_SAI1_RX_SYNC** 0x30330164, 0x3, 0x303304D0, 0x1, 0x303303C4
- #define **IOMUXC_SAI1_RXD5_ENET1_RGMII_RD1** 0x30330164, 0x4, 0x30330584, 0x1, 0x303303C4
- #define **IOMUXC_SAI1_RXD5_GPIO4_IO07** 0x30330164, 0x5, 0x00000000, 0x0, 0x303303C4
- #define **IOMUXC_SAI1_RXD6_AUDIOMIX_SAI1_RX_DATA6** 0x30330168, 0x0, 0x00000000, 0x0, 0x303303C8

- #define **IOMUXC_SAI1_RXD6_AUDIOMIX_SAI6_TX_SYNC** 0x30330168, 0x1, 0x30330528, 0x1, 0x303303C8
- #define **IOMUXC_SAI1_RXD6_AUDIOMIX_SAI6_RX_SYNC** 0x30330168, 0x2, 0x30330520, 0x1, 0x303303C8
- #define **IOMUXC_SAI1_RXD6_ENET1_RGMII_RD2** 0x30330168, 0x4, 0x00000000, 0x0, 0x303303C8
- #define **IOMUXC_SAI1_RXD6_GPIO4_IO08** 0x30330168, 0x5, 0x00000000, 0x0, 0x303303C8
- #define **IOMUXC_SAI1_RXD7_AUDIOMIX_SAI1_RX_DATA7** 0x3033016C, 0x0, 0x00000000, 0x0, 0x303303CC
- #define **IOMUXC_SAI1_RXD7_AUDIOMIX_SAI6_MCLK** 0x3033016C, 0x1, 0x30330514, 0x1, 0x303303CC
- #define **IOMUXC_SAI1_RXD7_AUDIOMIX_SAI1_TX_SYNC** 0x3033016C, 0x2, 0x303304D8, 0x3, 0x303303CC
- #define **IOMUXC_SAI1_RXD7_AUDIOMIX_SAI1_TX_DATA4** 0x3033016C, 0x3, 0x00000000, 0x0, 0x303303CC
- #define **IOMUXC_SAI1_RXD7_ENET1_RGMII_RD3** 0x3033016C, 0x4, 0x00000000, 0x0, 0x303303CC
- #define **IOMUXC_SAI1_RXD7_GPIO4_IO09** 0x3033016C, 0x5, 0x00000000, 0x0, 0x303303CC
- #define **IOMUXC_SAI1_TXFS_AUDIOMIX_SAI1_TX_SYNC** 0x30330170, 0x0, 0x303304D8, 0x4, 0x303303D0
- #define **IOMUXC_SAI1_TXFS_ENET1_RGMII_RX_CTL** 0x30330170, 0x4, 0x30330588, 0x1, 0x303303D0
- #define **IOMUXC_SAI1_TXFS_GPIO4_IO10** 0x30330170, 0x5, 0x00000000, 0x0, 0x303303D0
- #define **IOMUXC_SAI1_TXC_AUDIOMIX_SAI1_TX_BCLK** 0x30330174, 0x0, 0x303304D4, 0x1, 0x303303D4
- #define **IOMUXC_SAI1_TXC_ENET1_RGMII_RXC** 0x30330174, 0x4, 0x00000000, 0x0, 0x303303D4
- #define **IOMUXC_SAI1_TXC_GPIO4_IO11** 0x30330174, 0x5, 0x00000000, 0x0, 0x303303D4
- #define **IOMUXC_SAI1_TXD0_AUDIOMIX_SAI1_TX_DATA0** 0x30330178, 0x0, 0x00000000, 0x0, 0x303303D8
- #define **IOMUXC_SAI1_TXD0_ENET1_RGMII_TD0** 0x30330178, 0x4, 0x00000000, 0x0, 0x303303D8
- #define **IOMUXC_SAI1_TXD0_GPIO4_IO12** 0x30330178, 0x5, 0x00000000, 0x0, 0x303303D8
- #define **IOMUXC_SAI1_TXD1_AUDIOMIX_SAI1_TX_DATA1** 0x3033017C, 0x0, 0x00000000, 0x0, 0x303303DC
- #define **IOMUXC_SAI1_TXD1_ENET1_RGMII_TD1** 0x3033017C, 0x4, 0x00000000, 0x0, 0x303303DC
- #define **IOMUXC_SAI1_TXD1_GPIO4_IO13** 0x3033017C, 0x5, 0x00000000, 0x0, 0x303303DC
- #define **IOMUXC_SAI1_TXD2_AUDIOMIX_SAI1_TX_DATA2** 0x30330180, 0x0, 0x00000000, 0x0, 0x303303E0
- #define **IOMUXC_SAI1_TXD2_ENET1_RGMII_TD2** 0x30330180, 0x4, 0x00000000, 0x0, 0x303303E0
- #define **IOMUXC_SAI1_TXD2_GPIO4_IO14** 0x30330180, 0x5, 0x00000000, 0x0, 0x303303E0
- #define **IOMUXC_SAI1_TXD3_AUDIOMIX_SAI1_TX_DATA3** 0x30330184, 0x0, 0x00000000, 0x0, 0x303303E4
- #define **IOMUXC_SAI1_TXD3_ENET1_RGMII_TD3** 0x30330184, 0x4, 0x00000000, 0x0, 0x303303E4
- #define **IOMUXC_SAI1_TXD3_GPIO4_IO15** 0x30330184, 0x5, 0x00000000, 0x0, 0x303303E4

- #define **IOMUXC_SAI1_TXD4_AUDIOMIX_SAI1_TX_DATA4** 0x30330188, 0x0, 0x00000000, 0x0, 0x303303E8
- #define **IOMUXC_SAI1_TXD4_AUDIOMIX_SAI6_RX_BCLK** 0x30330188, 0x1, 0x30330518, 0x2, 0x303303E8
- #define **IOMUXC_SAI1_TXD4_AUDIOMIX_SAI6_TX_BCLK** 0x30330188, 0x2, 0x30330524, 0x2, 0x303303E8
- #define **IOMUXC_SAI1_TXD4_ENET1_RGMII_TX_CTL** 0x30330188, 0x4, 0x00000000, 0x0, 0x303303E8
- #define **IOMUXC_SAI1_TXD4_GPIO4_IO16** 0x30330188, 0x5, 0x00000000, 0x0, 0x303303E8
- #define **IOMUXC_SAI1_TXD5_AUDIOMIX_SAI1_TX_DATA5** 0x3033018C, 0x0, 0x00000000, 0x0, 0x303303EC
- #define **IOMUXC_SAI1_TXD5_AUDIOMIX_SAI6_RX_DATA0** 0x3033018C, 0x1, 0x3033051C, 0x2, 0x303303EC
- #define **IOMUXC_SAI1_TXD5_AUDIOMIX_SAI6_TX_DATA0** 0x3033018C, 0x2, 0x00000000, 0x0, 0x303303EC
- #define **IOMUXC_SAI1_TXD5_ENET1_RGMII_TXC** 0x3033018C, 0x4, 0x00000000, 0x0, 0x303303EC
- #define **IOMUXC_SAI1_TXD5_GPIO4_IO17** 0x3033018C, 0x5, 0x00000000, 0x0, 0x303303EC
- #define **IOMUXC_SAI1_TXD6_AUDIOMIX_SAI1_TX_DATA6** 0x30330190, 0x0, 0x00000000, 0x0, 0x303303F0
- #define **IOMUXC_SAI1_TXD6_AUDIOMIX_SAI6_RX_SYNC** 0x30330190, 0x1, 0x30330520, 0x2, 0x303303F0
- #define **IOMUXC_SAI1_TXD6_AUDIOMIX_SAI6_TX_SYNC** 0x30330190, 0x2, 0x30330528, 0x2, 0x303303F0
- #define **IOMUXC_SAI1_TXD6_ENET1_RX_ER** 0x30330190, 0x4, 0x3033058C, 0x1, 0x303303F0
- #define **IOMUXC_SAI1_TXD6_GPIO4_IO18** 0x30330190, 0x5, 0x00000000, 0x0, 0x303303F0
- #define **IOMUXC_SAI1_TXD7_AUDIOMIX_SAI1_TX_DATA7** 0x30330194, 0x0, 0x00000000, 0x0, 0x303303F4
- #define **IOMUXC_SAI1_TXD7_AUDIOMIX_SAI6_MCLK** 0x30330194, 0x1, 0x30330514, 0x2, 0x303303F4
- #define **IOMUXC_SAI1_TXD7_AUDIOMIX_PDM_CLK** 0x30330194, 0x3, 0x00000000, 0x0, 0x303303F4
- #define **IOMUXC_SAI1_TXD7_ENET1_TX_ER** 0x30330194, 0x4, 0x00000000, 0x0, 0x303303F4
- #define **IOMUXC_SAI1_TXD7_GPIO4_IO19** 0x30330194, 0x5, 0x00000000, 0x0, 0x303303F4
- #define **IOMUXC_SAI1_MCLK_AUDIOMIX_SAI1_MCLK** 0x30330198, 0x0, 0x00000000, 0x0, 0x303303F8
- #define **IOMUXC_SAI1_MCLK_AUDIOMIX_SAI1_TX_BCLK** 0x30330198, 0x2, 0x303304D4, 0x2, 0x303303F8
- #define **IOMUXC_SAI1_MCLK_ENET1_TX_CLK** 0x30330198, 0x4, 0x30330578, 0x1, 0x303303F8
- #define **IOMUXC_SAI1_MCLK_GPIO4_IO20** 0x30330198, 0x5, 0x00000000, 0x0, 0x303303F8
- #define **IOMUXC_SAI2_RXFS_AUDIOMIX_SAI2_RX_SYNC** 0x3033019C, 0x0, 0x00000000, 0x0, 0x303303FC
- #define **IOMUXC_SAI2_RXFS_AUDIOMIX_SAI5_TX_SYNC** 0x3033019C, 0x1, 0x30330510, 0x2, 0x303303FC
- #define **IOMUXC_SAI2_RXFS_AUDIOMIX_SAI5_TX_DATA1** 0x3033019C, 0x2, 0x00000000,

- 0x0, 0x303303FC
- #define **IOMUXC_SAI2_RXFS_AUDIOMIX_SAI2_RX_DATA1** 0x3033019C, 0x3, 0x303304DC, 0x0, 0x303303FC
- #define **IOMUXC_SAI2_RXFS_UART1_TX** 0x3033019C, 0x4, 0x00000000, 0x0, 0x303303FC
- #define **IOMUXC_SAI2_RXFS_UART1_RX** 0x3033019C, 0x4, 0x303305E8, 0x2, 0x303303FC
- #define **IOMUXC_SAI2_RXFS_GPIO4_IO21** 0x3033019C, 0x5, 0x00000000, 0x0, 0x303303FC
- #define **IOMUXC_SAI2_RXFS_AUDIOMIX_PDM_BIT_STREAM2** 0x3033019C, 0x6, 0x303304C8, 0x5, 0x303303FC
- #define **IOMUXC_SAI2_RXC_AUDIOMIX_SAI2_RX_BCLK** 0x303301A0, 0x0, 0x00000000, 0x0, 0x30330400
- #define **IOMUXC_SAI2_RXC_AUDIOMIX_SAI5_TX_BCLK** 0x303301A0, 0x1, 0x3033050C, 0x2, 0x30330400
- #define **IOMUXC_SAI2_RXC_CAN1_TX** 0x303301A0, 0x3, 0x00000000, 0x0, 0x30330400
- #define **IOMUXC_SAI2_RXC_UART1_RX** 0x303301A0, 0x4, 0x303305E8, 0x3, 0x30330400
- #define **IOMUXC_SAI2_RXC_UART1_TX** 0x303301A0, 0x4, 0x00000000, 0x0, 0x30330400
- #define **IOMUXC_SAI2_RXC_GPIO4_IO22** 0x303301A0, 0x5, 0x00000000, 0x0, 0x30330400
- #define **IOMUXC_SAI2_RXC_AUDIOMIX_PDM_BIT_STREAM1** 0x303301A0, 0x6, 0x303304C4, 0x5, 0x30330400
- #define **IOMUXC_SAI2_RXD0_AUDIOMIX_SAI2_RX_DATA0** 0x303301A4, 0x0, 0x00000000, 0x0, 0x30330404
- #define **IOMUXC_SAI2_RXD0_AUDIOMIX_SAI5_TX_DATA0** 0x303301A4, 0x1, 0x00000000, 0x0, 0x30330404
- #define **IOMUXC_SAI2_RXD0_ENET_QOS_1588_EVENT2_OUT** 0x303301A4, 0x2, 0x00000000, 0x0, 0x30330404
- #define **IOMUXC_SAI2_RXD0_AUDIOMIX_SAI2_TX_DATA1** 0x303301A4, 0x3, 0x00000000, 0x0, 0x30330404
- #define **IOMUXC_SAI2_RXD0_UART1_RTS_B** 0x303301A4, 0x4, 0x303305E4, 0x2, 0x30330404
- #define **IOMUXC_SAI2_RXD0_UART1_CTS_B** 0x303301A4, 0x4, 0x00000000, 0x0, 0x30330404
- #define **IOMUXC_SAI2_RXD0_GPIO4_IO23** 0x303301A4, 0x5, 0x00000000, 0x0, 0x30330404
- #define **IOMUXC_SAI2_RXD0_AUDIOMIX_PDM_BIT_STREAM3** 0x303301A4, 0x6, 0x303304CC, 0x5, 0x30330404
- #define **IOMUXC_SAI2_TXFS_AUDIOMIX_SAI2_TX_SYNC** 0x303301A8, 0x0, 0x00000000, 0x0, 0x30330408
- #define **IOMUXC_SAI2_TXFS_AUDIOMIX_SAI5_TX_DATA1** 0x303301A8, 0x1, 0x00000000, 0x0, 0x30330408
- #define **IOMUXC_SAI2_TXFS_ENET_QOS_1588_EVENT3_OUT** 0x303301A8, 0x2, 0x00000000, 0x0, 0x30330408
- #define **IOMUXC_SAI2_TXFS_AUDIOMIX_SAI2_TX_DATA1** 0x303301A8, 0x3, 0x00000000, 0x0, 0x30330408
- #define **IOMUXC_SAI2_TXFS_UART1_CTS_B** 0x303301A8, 0x4, 0x00000000, 0x0, 0x30330408
- #define **IOMUXC_SAI2_TXFS_UART1_RTS_B** 0x303301A8, 0x4, 0x303305E4, 0x3, 0x30330408
- #define **IOMUXC_SAI2_TXFS_GPIO4_IO24** 0x303301A8, 0x5, 0x00000000, 0x0, 0x30330408
- #define **IOMUXC_SAI2_TXFS_AUDIOMIX_PDM_BIT_STREAM2** 0x303301A8, 0x6, 0x303304C8, 0x6, 0x30330408
- #define **IOMUXC_SAI2_TXC_AUDIOMIX_SAI2_TX_BCLK** 0x303301AC, 0x0, 0x00000000, 0x0, 0x3033040C

- #define **IOMUXC_SAI2_TXC_AUDIOMIX_SAI5_TX_DATA2** 0x303301AC, 0x1, 0x00000000, 0x0, 0x3033040C
- #define **IOMUXC_SAI2_TXC_CAN1_RX** 0x303301AC, 0x3, 0x3033054C, 0x1, 0x3033040C
- #define **IOMUXC_SAI2_TXC_GPIO4_IO25** 0x303301AC, 0x5, 0x00000000, 0x0, 0x3033040C
- #define **IOMUXC_SAI2_TXC_AUDIOMIX_PDM_BIT_STREAM1** 0x303301AC, 0x6, 0x303304C4, 0x6, 0x3033040C
- #define **IOMUXC_SAI2_TXD0_AUDIOMIX_SAI2_TX_DATA0** 0x303301B0, 0x0, 0x00000000, 0x0, 0x30330410
- #define **IOMUXC_SAI2_TXD0_AUDIOMIX_SAI5_TX_DATA3** 0x303301B0, 0x1, 0x00000000, 0x0, 0x30330410
- #define **IOMUXC_SAI2_TXD0_ENET_QOS_1588_EVENT2_IN** 0x303301B0, 0x2, 0x00000000, 0x0, 0x30330410
- #define **IOMUXC_SAI2_TXD0_CAN2_TX** 0x303301B0, 0x3, 0x00000000, 0x0, 0x30330410
- #define **IOMUXC_SAI2_TXD0_ENET_QOS_1588_EVENT2_AUX_IN** 0x303301B0, 0x4, 0x00000000, 0x0, 0x30330410
- #define **IOMUXC_SAI2_TXD0_GPIO4_IO26** 0x303301B0, 0x5, 0x00000000, 0x0, 0x30330410
- #define **IOMUXC_SAI2_MCLK_AUDIOMIX_SAI2_MCLK** 0x303301B4, 0x0, 0x00000000, 0x0, 0x30330414
- #define **IOMUXC_SAI2_MCLK_AUDIOMIX_SAI5_MCLK** 0x303301B4, 0x1, 0x303304F0, 0x2, 0x30330414
- #define **IOMUXC_SAI2_MCLK_ENET_QOS_1588_EVENT3_IN** 0x303301B4, 0x2, 0x00000000, 0x0, 0x30330414
- #define **IOMUXC_SAI2_MCLK_CAN2_RX** 0x303301B4, 0x3, 0x30330550, 0x1, 0x30330414
- #define **IOMUXC_SAI2_MCLK_ENET_QOS_1588_EVENT3_AUX_IN** 0x303301B4, 0x4, 0x00000000, 0x0, 0x30330414
- #define **IOMUXC_SAI2_MCLK_GPIO4_IO27** 0x303301B4, 0x5, 0x00000000, 0x0, 0x30330414
- #define **IOMUXC_SAI2_MCLK_AUDIOMIX_SAI3_MCLK** 0x303301B4, 0x6, 0x303304E0, 0x1, 0x30330414
- #define **IOMUXC_SAI3_RXFS_AUDIOMIX_SAI3_RX_SYNC** 0x303301B8, 0x0, 0x00000000, 0x0, 0x30330418
- #define **IOMUXC_SAI3_RXFS_AUDIOMIX_SAI2_RX_DATA1** 0x303301B8, 0x1, 0x303304DC, 0x1, 0x30330418
- #define **IOMUXC_SAI3_RXFS_AUDIOMIX_SAI5_RX_SYNC** 0x303301B8, 0x2, 0x30330508, 0x2, 0x30330418
- #define **IOMUXC_SAI3_RXFS_AUDIOMIX_SAI3_RX_DATA1** 0x303301B8, 0x3, 0x00000000, 0x0, 0x30330418
- #define **IOMUXC_SAI3_RXFS_AUDIOMIX_SPDIF1_IN** 0x303301B8, 0x4, 0x30330544, 0x2, 0x30330418
- #define **IOMUXC_SAI3_RXFS_GPIO4_IO28** 0x303301B8, 0x5, 0x00000000, 0x0, 0x30330418
- #define **IOMUXC_SAI3_RXFS_AUDIOMIX_PDM_BIT_STREAM0** 0x303301B8, 0x6, 0x303304C0, 0x5, 0x30330418
- #define **IOMUXC_SAI3_RXC_AUDIOMIX_SAI3_RX_BCLK** 0x303301BC, 0x0, 0x00000000, 0x0, 0x3033041C
- #define **IOMUXC_SAI3_RXC_AUDIOMIX_SAI2_RX_DATA2** 0x303301BC, 0x1, 0x00000000, 0x0, 0x3033041C
- #define **IOMUXC_SAI3_RXC_AUDIOMIX_SAI5_RX_BCLK** 0x303301BC, 0x2, 0x303304F4, 0x2, 0x3033041C
- #define **IOMUXC_SAI3_RXC_GPT1_CLK** 0x303301BC, 0x3, 0x3033059C, 0x0, 0x3033041C
- #define **IOMUXC_SAI3_RXC_UART2_CTS_B** 0x303301BC, 0x4, 0x00000000, 0x0, 0x3033041C
- #define **IOMUXC_SAI3_RXC_UART2_RTS_B** 0x303301BC, 0x4, 0x303305EC, 0x2,

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0x3033041C
• #define IOMUXC_SAI3_RXC_GPIO4_IO29 0x303301BC, 0x5, 0x00000000, 0x0, 0x3033041C
• #define IOMUXC_SAI3_RXC_AUDIOMIX_PDM_CLK 0x303301BC, 0x6, 0x00000000, 0x0,
  0x3033041C
• #define IOMUXC_SAI3_RXD_AUDIOMIX_SAI3_RX_DATA0 0x303301C0, 0x0, 0x303304-
  E4, 0x1, 0x30330420
• #define IOMUXC_SAI3_RXD_AUDIOMIX_SAI2_RX_DATA3 0x303301C0, 0x1, 0x00000000,
  0x0, 0x30330420
• #define IOMUXC_SAI3_RXD_AUDIOMIX_SAI5_RX_DATA0 0x303301C0, 0x2, 0x303304-
  F8, 0x2, 0x30330420
• #define IOMUXC_SAI3_RXD_UART2_RTS_B 0x303301C0, 0x4, 0x303305EC, 0x3,
  0x30330420
• #define IOMUXC_SAI3_RXD_UART2_CTS_B 0x303301C0, 0x4, 0x00000000, 0x0, 0x30330420
• #define IOMUXC_SAI3_RXD_GPIO4_IO30 0x303301C0, 0x5, 0x00000000, 0x0, 0x30330420
• #define IOMUXC_SAI3_RXD_AUDIOMIX_PDM_BIT_STREAM1 0x303301C0, 0x6,
  0x303304C4, 0x7, 0x30330420
• #define IOMUXC_SAI3_TXFS_AUDIOMIX_SAI3_TX_SYNC 0x303301C4, 0x0, 0x303304E-
  C, 0x1, 0x30330424
• #define IOMUXC_SAI3_TXFS_AUDIOMIX_SAI2_TX_DATA1 0x303301C4, 0x1, 0x00000000,
  0x0, 0x30330424
• #define IOMUXC_SAI3_TXFS_AUDIOMIX_SAI5_RX_DATA1 0x303301C4, 0x2, 0x303304-
  FC, 0x2, 0x30330424
• #define IOMUXC_SAI3_TXFS_AUDIOMIX_SAI3_TX_DATA1 0x303301C4, 0x3, 0x00000000,
  0x0, 0x30330424
• #define IOMUXC_SAI3_TXFS_UART2_RX 0x303301C4, 0x4, 0x303305F0, 0x4, 0x30330424
• #define IOMUXC_SAI3_TXFS_UART2_TX 0x303301C4, 0x4, 0x00000000, 0x0, 0x30330424
• #define IOMUXC_SAI3_TXFS_GPIO4_IO31 0x303301C4, 0x5, 0x00000000, 0x0, 0x30330424
• #define IOMUXC_SAI3_TXFS_AUDIOMIX_PDM_BIT_STREAM3 0x303301C4, 0x6,
  0x303304CC, 0x6, 0x30330424
• #define IOMUXC_SAI3_TXC_AUDIOMIX_SAI3_TX_BCLK 0x303301C8, 0x0, 0x303304E8,
  0x1, 0x30330428
• #define IOMUXC_SAI3_TXC_AUDIOMIX_SAI2_TX_DATA2 0x303301C8, 0x1, 0x00000000,
  0x0, 0x30330428
• #define IOMUXC_SAI3_TXC_AUDIOMIX_SAI5_RX_DATA2 0x303301C8, 0x2, 0x30330500,
  0x2, 0x30330428
• #define IOMUXC_SAI3_TXC_GPT1_CAPTURE1 0x303301C8, 0x3, 0x30330594, 0x0,
  0x30330428
• #define IOMUXC_SAI3_TXC_UART2_TX 0x303301C8, 0x4, 0x00000000, 0x0, 0x30330428
• #define IOMUXC_SAI3_TXC_UART2_RX 0x303301C8, 0x4, 0x303305F0, 0x5, 0x30330428
• #define IOMUXC_SAI3_TXC_GPIO5_IO00 0x303301C8, 0x5, 0x00000000, 0x0, 0x30330428
• #define IOMUXC_SAI3_TXC_AUDIOMIX_PDM_BIT_STREAM2 0x303301C8, 0x6,
  0x303304C8, 0x7, 0x30330428
• #define IOMUXC_SAI3_TXD_AUDIOMIX_SAI3_TX_DATA0 0x303301CC, 0x0, 0x00000000,
  0x0, 0x3033042C
• #define IOMUXC_SAI3_TXD_AUDIOMIX_SAI2_TX_DATA3 0x303301CC, 0x1, 0x00000000,
  0x0, 0x3033042C
• #define IOMUXC_SAI3_TXD_AUDIOMIX_SAI5_RX_DATA3 0x303301CC, 0x2, 0x30330504,
  0x2, 0x3033042C
• #define IOMUXC_SAI3_TXD_GPT1_CAPTURE2 0x303301CC, 0x3, 0x30330598, 0x0,
  0x3033042C
• #define IOMUXC_SAI3_TXD_AUDIOMIX_SPDIF1_EXT_CLK 0x303301CC, 0x4, 0x30330548,

```

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0x0, 0x3033042C
• #define IOMUXC_SAI3_TXD_GPIO5_IO01 0x303301CC, 0x5, 0x00000000, 0x0, 0x3033042C
• #define IOMUXC_SAI3_MCLK_AUDIOMIX_SAI3_MCLK 0x303301D0, 0x0, 0x303304E0,
0x2, 0x30330430
• #define IOMUXC_SAI3_MCLK_PWM4_OUT 0x303301D0, 0x1, 0x00000000, 0x0, 0x30330430
• #define IOMUXC_SAI3_MCLK_AUDIOMIX_SAI5_MCLK 0x303301D0, 0x2, 0x303304F0,
0x3, 0x30330430
• #define IOMUXC_SAI3_MCLK_AUDIOMIX_SPDIF1_OUT 0x303301D0, 0x4, 0x00000000,
0x0, 0x30330430
• #define IOMUXC_SAI3_MCLK_GPIO5_IO02 0x303301D0, 0x5, 0x00000000, 0x0, 0x30330430
• #define IOMUXC_SAI3_MCLK_AUDIOMIX_SPDIF1_IN 0x303301D0, 0x6, 0x30330544,
0x3, 0x30330430
• #define IOMUXC_SPDIF_TX_AUDIOMIX_SPDIF1_OUT 0x303301D4, 0x0, 0x00000000,
0x0, 0x30330434
• #define IOMUXC_SPDIF_TX_PWM3_OUT 0x303301D4, 0x1, 0x00000000, 0x0, 0x30330434
• #define IOMUXC_SPDIF_TX_I2C5_SCL 0x303301D4, 0x2, 0x303305C4, 0x2, 0x30330434
• #define IOMUXC_SPDIF_TX_GPT1_COMPARE1 0x303301D4, 0x3, 0x00000000, 0x0,
0x30330434
• #define IOMUXC_SPDIF_TX_CAN1_TX 0x303301D4, 0x4, 0x00000000, 0x0, 0x30330434
• #define IOMUXC_SPDIF_TX_GPIO5_IO03 0x303301D4, 0x5, 0x00000000, 0x0, 0x30330434
• #define IOMUXC_SPDIF_RX_AUDIOMIX_SPDIF1_IN 0x303301D8, 0x0, 0x30330544, 0x4,
0x30330438
• #define IOMUXC_SPDIF_RX_PWM2_OUT 0x303301D8, 0x1, 0x00000000, 0x0, 0x30330438
• #define IOMUXC_SPDIF_RX_I2C5_SDA 0x303301D8, 0x2, 0x303305C8, 0x2, 0x30330438
• #define IOMUXC_SPDIF_RX_GPT1_COMPARE2 0x303301D8, 0x3, 0x00000000, 0x0,
0x30330438
• #define IOMUXC_SPDIF_RX_CAN1_RX 0x303301D8, 0x4, 0x3033054C, 0x2, 0x30330438
• #define IOMUXC_SPDIF_RX_GPIO5_IO04 0x303301D8, 0x5, 0x00000000, 0x0, 0x30330438
• #define IOMUXC_SPDIF_EXT_CLK_AUDIOMIX_SPDIF1_EXT_CLK 0x303301DC, 0x0,
0x30330548, 0x1, 0x3033043C
• #define IOMUXC_SPDIF_EXT_CLK_PWM1_OUT 0x303301DC, 0x1, 0x00000000, 0x0,
0x3033043C
• #define IOMUXC_SPDIF_EXT_CLK_GPT1_COMPARE3 0x303301DC, 0x3, 0x00000000,
0x0, 0x3033043C
• #define IOMUXC_SPDIF_EXT_CLK_GPIO5_IO05 0x303301DC, 0x5, 0x00000000, 0x0,
0x3033043C
• #define IOMUXC_ECSP11_SCLK_ECSP11_SCLK 0x303301E0, 0x0, 0x30330558, 0x0,
0x30330440
• #define IOMUXC_ECSP11_SCLK_UART3_RX 0x303301E0, 0x1, 0x303305F8, 0x4,
0x30330440
• #define IOMUXC_ECSP11_SCLK_UART3_TX 0x303301E0, 0x1, 0x00000000, 0x0, 0x30330440
• #define IOMUXC_ECSP11_SCLK_I2C1_SCL 0x303301E0, 0x2, 0x303305A4, 0x1, 0x30330440
• #define IOMUXC_ECSP11_SCLK_AUDIOMIX_SAI7_RX_SYNC 0x303301E0, 0x3, 0x30330538,
0x1, 0x30330440
• #define IOMUXC_ECSP11_SCLK_GPIO5_IO06 0x303301E0, 0x5, 0x00000000, 0x0,
0x30330440
• #define IOMUXC_ECSP11_MOSI_ECSP11_MOSI 0x303301E4, 0x0, 0x30330560, 0x0,
0x30330444
• #define IOMUXC_ECSP11_MOSI_UART3_TX 0x303301E4, 0x1, 0x00000000, 0x0, 0x30330444
• #define IOMUXC_ECSP11_MOSI_UART3_RX 0x303301E4, 0x1, 0x303305F8, 0x5, 0x30330444
• #define IOMUXC_ECSP11_MOSI_I2C1_SDA 0x303301E4, 0x2, 0x303305A8, 0x1, 0x30330444
• #define IOMUXC_ECSP11_MOSI_AUDIOMIX_SAI7_RX_BCLK 0x303301E4, 0x3, 0x30330530,

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0x1, 0x30330444
• #define IOMUXC_ECSP11_MOSI_GPIO5_IO07 0x303301E4, 0x5, 0x00000000, 0x0,
0x30330444
• #define IOMUXC_ECSP11_MISO_ECSP11_MISO 0x303301E8, 0x0, 0x3033055C, 0x0,
0x30330448
• #define IOMUXC_ECSP11_MISO_UART3_CTS_B 0x303301E8, 0x1, 0x00000000, 0x0,
0x30330448
• #define IOMUXC_ECSP11_MISO_UART3_RTS_B 0x303301E8, 0x1, 0x303305F4, 0x2,
0x30330448
• #define IOMUXC_ECSP11_MISO_I2C2_SCL 0x303301E8, 0x2, 0x303305AC, 0x1, 0x30330448
• #define IOMUXC_ECSP11_MISO_AUDIOMIX_SAI7_RX_DATA0 0x303301E8, 0x3,
0x30330534, 0x1, 0x30330448
• #define IOMUXC_ECSP11_MISO_GPIO5_IO08 0x303301E8, 0x5, 0x00000000, 0x0,
0x30330448
• #define IOMUXC_ECSP11_SS0_ECSP11_SS0 0x303301EC, 0x0, 0x30330564, 0x0, 0x3033044-
C
• #define IOMUXC_ECSP11_SS0_UART3_RTS_B 0x303301EC, 0x1, 0x303305F4, 0x3,
0x3033044C
• #define IOMUXC_ECSP11_SS0_UART3_CTS_B 0x303301EC, 0x1, 0x00000000, 0x0,
0x3033044C
• #define IOMUXC_ECSP11_SS0_I2C2_SDA 0x303301EC, 0x2, 0x303305B0, 0x1, 0x3033044C
• #define IOMUXC_ECSP11_SS0_AUDIOMIX_SAI7_TX_SYNC 0x303301EC, 0x3, 0x30330540,
0x1, 0x3033044C
• #define IOMUXC_ECSP11_SS0_GPIO5_IO09 0x303301EC, 0x5, 0x00000000, 0x0, 0x3033044-
C
• #define IOMUXC_ECSP12_SCLK_ECSP12_SCLK 0x303301F0, 0x0, 0x30330568, 0x1,
0x30330450
• #define IOMUXC_ECSP12_SCLK_UART4_RX 0x303301F0, 0x1, 0x30330600, 0x6, 0x30330450
• #define IOMUXC_ECSP12_SCLK_UART4_TX 0x303301F0, 0x1, 0x00000000, 0x0, 0x30330450
• #define IOMUXC_ECSP12_SCLK_I2C3_SCL 0x303301F0, 0x2, 0x303305B4, 0x3, 0x30330450
• #define IOMUXC_ECSP12_SCLK_AUDIOMIX_SAI7_TX_BCLK 0x303301F0, 0x3, 0x3033053-
C, 0x1, 0x30330450
• #define IOMUXC_ECSP12_SCLK_GPIO5_IO10 0x303301F0, 0x5, 0x00000000, 0x0,
0x30330450
• #define IOMUXC_ECSP12_MOSI_ECSP12_MOSI 0x303301F4, 0x0, 0x30330570, 0x1,
0x30330454
• #define IOMUXC_ECSP12_MOSI_UART4_TX 0x303301F4, 0x1, 0x00000000, 0x0, 0x30330454
• #define IOMUXC_ECSP12_MOSI_UART4_RX 0x303301F4, 0x1, 0x30330600, 0x7, 0x30330454
• #define IOMUXC_ECSP12_MOSI_I2C3_SDA 0x303301F4, 0x2, 0x303305B8, 0x3, 0x30330454
• #define IOMUXC_ECSP12_MOSI_AUDIOMIX_SAI7_TX_DATA0 0x303301F4, 0x3,
0x00000000, 0x0, 0x30330454
• #define IOMUXC_ECSP12_MOSI_GPIO5_IO11 0x303301F4, 0x5, 0x00000000, 0x0,
0x30330454
• #define IOMUXC_ECSP12_MISO_ECSP12_MISO 0x303301F8, 0x0, 0x3033056C, 0x1,
0x30330458
• #define IOMUXC_ECSP12_MISO_UART4_CTS_B 0x303301F8, 0x1, 0x00000000, 0x0,
0x30330458
• #define IOMUXC_ECSP12_MISO_UART4_RTS_B 0x303301F8, 0x1, 0x303305FC, 0x2,
0x30330458
• #define IOMUXC_ECSP12_MISO_I2C4_SCL 0x303301F8, 0x2, 0x303305BC, 0x4, 0x30330458
• #define IOMUXC_ECSP12_MISO_AUDIOMIX_SAI7_MCLK 0x303301F8, 0x3, 0x3033052-

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- C, 0x1, 0x30330458
- #define **IOMUXC_ECSPi2_MISO_CCM_CLKO1** 0x303301F8, 0x4, 0x00000000, 0x0, 0x30330458
- #define **IOMUXC_ECSPi2_MISO_GPIO5_IO12** 0x303301F8, 0x5, 0x00000000, 0x0, 0x30330458
- #define **IOMUXC_ECSPi2_SS0_ECSPi2_SS0** 0x303301FC, 0x0, 0x30330574, 0x1, 0x3033045-C
- #define **IOMUXC_ECSPi2_SS0_UART4_RTS_B** 0x303301FC, 0x1, 0x303305FC, 0x3, 0x3033045C
- #define **IOMUXC_ECSPi2_SS0_UART4_CTS_B** 0x303301FC, 0x1, 0x00000000, 0x0, 0x3033045C
- #define **IOMUXC_ECSPi2_SS0_I2C4_SDA** 0x303301FC, 0x2, 0x303305C0, 0x4, 0x3033045C
- #define **IOMUXC_ECSPi2_SS0_CCM_CLKO2** 0x303301FC, 0x4, 0x00000000, 0x0, 0x3033045-C
- #define **IOMUXC_ECSPi2_SS0_GPIO5_IO13** 0x303301FC, 0x5, 0x00000000, 0x0, 0x3033045-C
- #define **IOMUXC_I2C1_SCL_I2C1_SCL** 0x30330200, 0x0, 0x303305A4, 0x2, 0x30330460
- #define **IOMUXC_I2C1_SCL_ENET_QOS_MDC** 0x30330200, 0x1, 0x00000000, 0x0, 0x30330460
- #define **IOMUXC_I2C1_SCL_ECSPi1_SCLK** 0x30330200, 0x3, 0x30330558, 0x1, 0x30330460
- #define **IOMUXC_I2C1_SCL_GPIO5_IO14** 0x30330200, 0x5, 0x00000000, 0x0, 0x30330460
- #define **IOMUXC_I2C1_SDA_I2C1_SDA** 0x30330204, 0x0, 0x303305A8, 0x2, 0x30330464
- #define **IOMUXC_I2C1_SDA_ENET_QOS_MDIO** 0x30330204, 0x1, 0x30330590, 0x2, 0x30330464
- #define **IOMUXC_I2C1_SDA_ECSPi1_MOSI** 0x30330204, 0x3, 0x30330560, 0x1, 0x30330464
- #define **IOMUXC_I2C1_SDA_GPIO5_IO15** 0x30330204, 0x5, 0x00000000, 0x0, 0x30330464
- #define **IOMUXC_I2C2_SCL_I2C2_SCL** 0x30330208, 0x0, 0x303305AC, 0x2, 0x30330468
- #define **IOMUXC_I2C2_SCL_ENET_QOS_1588_EVENT1_IN** 0x30330208, 0x1, 0x00000000, 0x0, 0x30330468
- #define **IOMUXC_I2C2_SCL_USDHC3_CD_B** 0x30330208, 0x2, 0x30330608, 0x3, 0x30330468
- #define **IOMUXC_I2C2_SCL_ECSPi1_MISO** 0x30330208, 0x3, 0x3033055C, 0x1, 0x30330468
- #define **IOMUXC_I2C2_SCL_ENET_QOS_1588_EVENT1_AUX_IN** 0x30330208, 0x4, 0x00000000, 0x0, 0x30330468
- #define **IOMUXC_I2C2_SCL_GPIO5_IO16** 0x30330208, 0x5, 0x00000000, 0x0, 0x30330468
- #define **IOMUXC_I2C2_SDA_I2C2_SDA** 0x3033020C, 0x0, 0x303305B0, 0x2, 0x3033046C
- #define **IOMUXC_I2C2_SDA_ENET_QOS_1588_EVENT1_OUT** 0x3033020C, 0x1, 0x00000000, 0x0, 0x3033046C
- #define **IOMUXC_I2C2_SDA_USDHC3_WP** 0x3033020C, 0x2, 0x30330634, 0x3, 0x3033046C
- #define **IOMUXC_I2C2_SDA_ECSPi1_SS0** 0x3033020C, 0x3, 0x30330564, 0x1, 0x3033046C
- #define **IOMUXC_I2C2_SDA_GPIO5_IO17** 0x3033020C, 0x5, 0x00000000, 0x0, 0x3033046C
- #define **IOMUXC_I2C3_SCL_I2C3_SCL** 0x30330210, 0x0, 0x303305B4, 0x4, 0x30330470
- #define **IOMUXC_I2C3_SCL_PWM4_OUT** 0x30330210, 0x1, 0x00000000, 0x0, 0x30330470
- #define **IOMUXC_I2C3_SCL_GPT2_CLK** 0x30330210, 0x2, 0x00000000, 0x0, 0x30330470
- #define **IOMUXC_I2C3_SCL_ECSPi2_SCLK** 0x30330210, 0x3, 0x30330568, 0x2, 0x30330470
- #define **IOMUXC_I2C3_SCL_GPIO5_IO18** 0x30330210, 0x5, 0x00000000, 0x0, 0x30330470
- #define **IOMUXC_I2C3_SDA_I2C3_SDA** 0x30330214, 0x0, 0x303305B8, 0x4, 0x30330474
- #define **IOMUXC_I2C3_SDA_PWM3_OUT** 0x30330214, 0x1, 0x00000000, 0x0, 0x30330474
- #define **IOMUXC_I2C3_SDA_GPT3_CLK** 0x30330214, 0x2, 0x00000000, 0x0, 0x30330474
- #define **IOMUXC_I2C3_SDA_ECSPi2_MOSI** 0x30330214, 0x3, 0x30330570, 0x2, 0x30330474
- #define **IOMUXC_I2C3_SDA_GPIO5_IO19** 0x30330214, 0x5, 0x00000000, 0x0, 0x30330474
- #define **IOMUXC_I2C4_SCL_I2C4_SCL** 0x30330218, 0x0, 0x303305BC, 0x5, 0x30330478
- #define **IOMUXC_I2C4_SCL_PWM2_OUT** 0x30330218, 0x1, 0x00000000, 0x0, 0x30330478
- #define **IOMUXC_I2C4_SCL_PCIE_CLKREQ_B** 0x30330218, 0x2, 0x303305A0, 0x0,

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0x30330478
• #define IOMUXC_I2C4_SCL_ECSPi2_MISO 0x30330218, 0x3, 0x3033056C, 0x2, 0x30330478
• #define IOMUXC_I2C4_SCL_GPIO5_IO20 0x30330218, 0x5, 0x00000000, 0x0, 0x30330478
• #define IOMUXC_I2C4_SDA_I2C4_SDA 0x3033021C, 0x0, 0x303305C0, 0x5, 0x3033047C
• #define IOMUXC_I2C4_SDA_PWM1_OUT 0x3033021C, 0x1, 0x00000000, 0x0, 0x3033047C
• #define IOMUXC_I2C4_SDA_ECSPi2_SS0 0x3033021C, 0x3, 0x30330574, 0x2, 0x3033047C
• #define IOMUXC_I2C4_SDA_GPIO5_IO21 0x3033021C, 0x5, 0x00000000, 0x0, 0x3033047C
• #define IOMUXC_UART1_RXD_UART1_RX 0x30330220, 0x0, 0x303305E8, 0x4, 0x30330480
• #define IOMUXC_UART1_RXD_UART1_TX 0x30330220, 0x0, 0x00000000, 0x0, 0x30330480
• #define IOMUXC_UART1_RXD_ECSPi3_SCLK 0x30330220, 0x1, 0x00000000, 0x0,
0x30330480
• #define IOMUXC_UART1_RXD_GPIO5_IO22 0x30330220, 0x5, 0x00000000, 0x0, 0x30330480
• #define IOMUXC_UART1_TXD_UART1_TX 0x30330224, 0x0, 0x00000000, 0x0, 0x30330484
• #define IOMUXC_UART1_TXD_UART1_RX 0x30330224, 0x0, 0x303305E8, 0x5, 0x30330484
• #define IOMUXC_UART1_TXD_ECSPi3_MOSI 0x30330224, 0x1, 0x00000000, 0x0,
0x30330484
• #define IOMUXC_UART1_TXD_GPIO5_IO23 0x30330224, 0x5, 0x00000000, 0x0, 0x30330484
• #define IOMUXC_UART2_RXD_UART2_RX 0x30330228, 0x0, 0x303305F0, 0x6, 0x30330488
• #define IOMUXC_UART2_RXD_UART2_TX 0x30330228, 0x0, 0x00000000, 0x0, 0x30330488
• #define IOMUXC_UART2_RXD_ECSPi3_MISO 0x30330228, 0x1, 0x00000000, 0x0,
0x30330488
• #define IOMUXC_UART2_RXD_GPT1_COMPARE3 0x30330228, 0x3, 0x00000000, 0x0,
0x30330488
• #define IOMUXC_UART2_RXD_GPIO5_IO24 0x30330228, 0x5, 0x00000000, 0x0, 0x30330488
• #define IOMUXC_UART2_TXD_UART2_TX 0x3033022C, 0x0, 0x00000000, 0x0, 0x3033048-
C
• #define IOMUXC_UART2_TXD_UART2_RX 0x3033022C, 0x0, 0x303305F0, 0x7, 0x3033048-
C
• #define IOMUXC_UART2_TXD_ECSPi3_SS0 0x3033022C, 0x1, 0x00000000, 0x0, 0x3033048-
C
• #define IOMUXC_UART2_TXD_GPT1_COMPARE2 0x3033022C, 0x3, 0x00000000, 0x0,
0x3033048C
• #define IOMUXC_UART2_TXD_GPIO5_IO25 0x3033022C, 0x5, 0x00000000, 0x0, 0x3033048-
C
• #define IOMUXC_UART3_RXD_UART3_RX 0x30330230, 0x0, 0x303305F8, 0x6, 0x30330490
• #define IOMUXC_UART3_RXD_UART3_TX 0x30330230, 0x0, 0x00000000, 0x0, 0x30330490
• #define IOMUXC_UART3_RXD_UART1_CTS_B 0x30330230, 0x1, 0x00000000, 0x0,
0x30330490
• #define IOMUXC_UART3_RXD_UART1_RTS_B 0x30330230, 0x1, 0x303305E4, 0x4,
0x30330490
• #define IOMUXC_UART3_RXD_USDHC3_RESET_B 0x30330230, 0x2, 0x00000000, 0x0,
0x30330490
• #define IOMUXC_UART3_RXD_GPT1_CAPTURE2 0x30330230, 0x3, 0x30330598, 0x1,
0x30330490
• #define IOMUXC_UART3_RXD_CAN2_TX 0x30330230, 0x4, 0x00000000, 0x0, 0x30330490
• #define IOMUXC_UART3_RXD_GPIO5_IO26 0x30330230, 0x5, 0x00000000, 0x0, 0x30330490
• #define IOMUXC_UART3_TXD_UART3_TX 0x30330234, 0x0, 0x00000000, 0x0, 0x30330494
• #define IOMUXC_UART3_TXD_UART3_RX 0x30330234, 0x0, 0x303305F8, 0x7, 0x30330494
• #define IOMUXC_UART3_TXD_UART1_RTS_B 0x30330234, 0x1, 0x303305E4, 0x5,
0x30330494
• #define IOMUXC_UART3_TXD_UART1_CTS_B 0x30330234, 0x1, 0x00000000, 0x0,
0x30330494

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- #define **IOMUXC_UART3_TXD_USDHC3_VSELECT** 0x30330234, 0x2, 0x00000000, 0x0, 0x30330494
- #define **IOMUXC_UART3_TXD_GPT1_CLK** 0x30330234, 0x3, 0x3033059C, 0x1, 0x30330494
- #define **IOMUXC_UART3_TXD_CAN2_RX** 0x30330234, 0x4, 0x30330550, 0x2, 0x30330494
- #define **IOMUXC_UART3_TXD_GPIO5_IO27** 0x30330234, 0x5, 0x00000000, 0x0, 0x30330494
- #define **IOMUXC_UART4_RXD_UART4_RX** 0x30330238, 0x0, 0x30330600, 0x8, 0x30330498
- #define **IOMUXC_UART4_RXD_UART4_TX** 0x30330238, 0x0, 0x00000000, 0x0, 0x30330498
- #define **IOMUXC_UART4_RXD_UART2_CTS_B** 0x30330238, 0x1, 0x00000000, 0x0, 0x30330498
- #define **IOMUXC_UART4_RXD_UART2_RTS_B** 0x30330238, 0x1, 0x303305EC, 0x4, 0x30330498
- #define **IOMUXC_UART4_RXD_PCIE_CLKREQ_B** 0x30330238, 0x2, 0x303305A0, 0x1, 0x30330498
- #define **IOMUXC_UART4_RXD_GPT1_COMPARE1** 0x30330238, 0x3, 0x00000000, 0x0, 0x30330498
- #define **IOMUXC_UART4_RXD_I2C6_SCL** 0x30330238, 0x4, 0x303305CC, 0x2, 0x30330498
- #define **IOMUXC_UART4_RXD_GPIO5_IO28** 0x30330238, 0x5, 0x00000000, 0x0, 0x30330498
- #define **IOMUXC_UART4_TXD_UART4_TX** 0x3033023C, 0x0, 0x00000000, 0x0, 0x3033049-C
- #define **IOMUXC_UART4_TXD_UART4_RX** 0x3033023C, 0x0, 0x30330600, 0x9, 0x3033049-C
- #define **IOMUXC_UART4_TXD_UART2_RTS_B** 0x3033023C, 0x1, 0x303305EC, 0x5, 0x3033049C
- #define **IOMUXC_UART4_TXD_UART2_CTS_B** 0x3033023C, 0x1, 0x00000000, 0x0, 0x3033049C
- #define **IOMUXC_UART4_TXD_GPT1_CAPTURE1** 0x3033023C, 0x3, 0x30330594, 0x1, 0x3033049C
- #define **IOMUXC_UART4_TXD_I2C6_SDA** 0x3033023C, 0x4, 0x303305D0, 0x2, 0x3033049C
- #define **IOMUXC_UART4_TXD_GPIO5_IO29** 0x3033023C, 0x5, 0x00000000, 0x0, 0x3033049-C
- #define **IOMUXC_HDMI_DDC_SCL_HDMIMIX_HDMI_SCL** 0x30330240, 0x0, 0x00000000, 0x0, 0x303304A0
- #define **IOMUXC_HDMI_DDC_SCL_I2C5_SCL** 0x30330240, 0x3, 0x303305C4, 0x3, 0x303304A0
- #define **IOMUXC_HDMI_DDC_SCL_CAN1_TX** 0x30330240, 0x4, 0x00000000, 0x0, 0x303304A0
- #define **IOMUXC_HDMI_DDC_SCL_GPIO3_IO26** 0x30330240, 0x5, 0x00000000, 0x0, 0x303304A0
- #define **IOMUXC_HDMI_DDC_SCL_EARC_TEST_OUT0** 0x30330240, 0x6, 0x00000000, 0x0, 0x303304A0
- #define **IOMUXC_HDMI_DDC_SDA_HDMIMIX_HDMI_SDA** 0x30330244, 0x0, 0x00000000, 0x0, 0x303304A4
- #define **IOMUXC_HDMI_DDC_SDA_I2C5_SDA** 0x30330244, 0x3, 0x303305C8, 0x3, 0x303304A4
- #define **IOMUXC_HDMI_DDC_SDA_CAN1_RX** 0x30330244, 0x4, 0x3033054C, 0x3, 0x303304A4
- #define **IOMUXC_HDMI_DDC_SDA_GPIO3_IO27** 0x30330244, 0x5, 0x00000000, 0x0, 0x303304A4
- #define **IOMUXC_HDMI_DDC_SDA_EARC_TEST_OUT1** 0x30330244, 0x6, 0x00000000, 0x0, 0x303304A4
- #define **IOMUXC_HDMI_CEC_HDMIMIX_HDMI_CEC** 0x30330248, 0x0, 0x00000000, 0x0,

- 0x303304A8
- #define **IOMUXC_HDMI_CEC_I2C6_SCL** 0x30330248, 0x3, 0x303305CC, 0x3, 0x303304A8
- #define **IOMUXC_HDMI_CEC_CAN2_TX** 0x30330248, 0x4, 0x00000000, 0x0, 0x303304A8
- #define **IOMUXC_HDMI_CEC_GPIO3_IO28** 0x30330248, 0x5, 0x00000000, 0x0, 0x303304A8
- #define **IOMUXC_HDMI_HPD_HDMIMIX_HDMI_HPD** 0x3033024C, 0x0, 0x00000000, 0x0, 0x303304AC
- #define **IOMUXC_HDMI_HPD_AUDIOMIX_HDMI_HPD_O** 0x3033024C, 0x1, 0x00000000, 0x0, 0x303304AC
- #define **IOMUXC_HDMI_HPD_I2C6_SDA** 0x3033024C, 0x3, 0x303305D0, 0x3, 0x303304AC
- #define **IOMUXC_HDMI_HPD_CAN2_RX** 0x3033024C, 0x4, 0x30330550, 0x3, 0x303304AC
- #define **IOMUXC_HDMI_HPD_GPIO3_IO29** 0x3033024C, 0x5, 0x00000000, 0x0, 0x303304AC

Configuration

- static void [IOMUXC_SetPinMux](#) (uint32_t muxRegister, uint32_t muxMode, uint32_t inputRegister, uint32_t inputDaisy, uint32_t configRegister, uint32_t inputOnfield)
Sets the IOMUXC pin mux mode.
- static void [IOMUXC_SetPinConfig](#) (uint32_t muxRegister, uint32_t muxMode, uint32_t inputRegister, uint32_t inputDaisy, uint32_t configRegister, uint32_t configValue)
Sets the IOMUXC pin configuration.

6.2 Macro Definition Documentation

6.2.1 #define FSL_IOMUXC_DRIVER_VERSION (MAKE_VERSION(2, 0, 4))

6.3 Function Documentation

6.3.1 static void IOMUXC_SetPinMux (uint32_t muxRegister, uint32_t muxMode, uint32_t inputRegister, uint32_t inputDaisy, uint32_t configRegister, uint32_t inputOnfield) [inline], [static]

Note

The first five parameters can be filled with the pin function ID macros.

This is an example to set the I2C4_SDA as the pwm1_OUT:

```
* IOMUXC_SetPinMux(IOMUXC_I2C4_SDA_PWM1_OUT, 0);
*
```

Parameters

<i>muxRegister</i>	The pin mux register_
<i>muxMode</i>	The pin mux mode_
<i>inputRegister</i>	The select input register_
<i>inputDaisy</i>	The input daisy_
<i>configRegister</i>	The config register_
<i>inputOnfield</i>	The pad->module input inversion_

6.3.2 static void IOMUXC_SetPinConfig (uint32_t *muxRegister*, uint32_t *muxMode*, uint32_t *inputRegister*, uint32_t *inputDaisy*, uint32_t *configRegister*, uint32_t *configValue*) [inline], [static]

Note

The previous five parameters can be filled with the pin function ID macros.

This is an example to set pin configuration for IOMUXC_I2C4_SDA_PWM1_OUT:

```
* IOMUXC_SetPinConfig(IOMUXC_I2C4_SDA_PWM1_OUT, IOMUXC_SW_PAD_CTL_PAD_ODE_MASK |
  IOMUXC0_SW_PAD_CTL_PAD_DSE(2U) )
*
```

Parameters

<i>muxRegister</i>	The pin mux register_
<i>muxMode</i>	The pin mux mode_
<i>inputRegister</i>	The select input register_
<i>inputDaisy</i>	The input daisy_
<i>configRegister</i>	The config register_
<i>configValue</i>	The pin config value_

Chapter 7

Common Driver

7.1 Overview

The MCUXpresso SDK provides a driver for the common module of MCUXpresso SDK devices.

Macros

- #define `FSL_DRIVER_TRANSFER_DOUBLE_WEAK_IRQ` 1
Macro to use the default weak IRQ handler in drivers.
- #define `MAKE_STATUS`(group, code) (((group)*100L) + (code)))
Construct a status code value from a group and code number.
- #define `MAKE_VERSION`(major, minor, bugfix) (((major) * 65536L) + ((minor) * 256L) + (bugfix))
Construct the version number for drivers.
- #define `DEBUG_CONSOLE_DEVICE_TYPE_NONE` 0U
No debug console.
- #define `DEBUG_CONSOLE_DEVICE_TYPE_UART` 1U
Debug console based on UART.
- #define `DEBUG_CONSOLE_DEVICE_TYPE_LPUART` 2U
Debug console based on LPUART.
- #define `DEBUG_CONSOLE_DEVICE_TYPE_LPSCI` 3U
Debug console based on LPSCI.
- #define `DEBUG_CONSOLE_DEVICE_TYPE_USBCDC` 4U
Debug console based on USBCDC.
- #define `DEBUG_CONSOLE_DEVICE_TYPE_FLEXCOMM` 5U
Debug console based on FLEXCOMM.
- #define `DEBUG_CONSOLE_DEVICE_TYPE_IUART` 6U
Debug console based on i.MX UART.
- #define `DEBUG_CONSOLE_DEVICE_TYPE_VUSART` 7U
Debug console based on LPC_VUSART.
- #define `DEBUG_CONSOLE_DEVICE_TYPE_MINI_USART` 8U
Debug console based on LPC_USART.
- #define `DEBUG_CONSOLE_DEVICE_TYPE_SWO` 9U
Debug console based on SWO.
- #define `DEBUG_CONSOLE_DEVICE_TYPE_QSCI` 10U
Debug console based on QSCI.
- #define `ARRAY_SIZE`(x) (sizeof(x) / sizeof((x)[0]))
Computes the number of elements in an array.

Typedefs

- typedef int32_t `status_t`
Type used for all status and error return values.

Enumerations

- enum `_status_groups` {
 - `kStatusGroup_Generic` = 0,
 - `kStatusGroup_FLASH` = 1,
 - `kStatusGroup_LPSPI` = 4,
 - `kStatusGroup_FLEXIO_SPI` = 5,
 - `kStatusGroup_DSPI` = 6,
 - `kStatusGroup_FLEXIO_UART` = 7,
 - `kStatusGroup_FLEXIO_I2C` = 8,
 - `kStatusGroup_LPI2C` = 9,
 - `kStatusGroup_UART` = 10,
 - `kStatusGroup_I2C` = 11,
 - `kStatusGroup_LPSCI` = 12,
 - `kStatusGroup_LPUART` = 13,
 - `kStatusGroup_SPI` = 14,
 - `kStatusGroup_XRDC` = 15,
 - `kStatusGroup_SEMA42` = 16,
 - `kStatusGroup_SDHC` = 17,
 - `kStatusGroup_SDMMC` = 18,
 - `kStatusGroup_SAI` = 19,
 - `kStatusGroup_MCG` = 20,
 - `kStatusGroup_SCG` = 21,
 - `kStatusGroup_SDSPI` = 22,
 - `kStatusGroup_FLEXIO_I2S` = 23,
 - `kStatusGroup_FLEXIO_MCULCD` = 24,
 - `kStatusGroup_FLASHIAP` = 25,
 - `kStatusGroup_FLEXCOMM_I2C` = 26,
 - `kStatusGroup_I2S` = 27,
 - `kStatusGroup_IUART` = 28,
 - `kStatusGroup_CSI` = 29,
 - `kStatusGroup_MIPI_DSI` = 30,
 - `kStatusGroup_SDRAMC` = 35,
 - `kStatusGroup_POWER` = 39,
 - `kStatusGroup_ENET` = 40,
 - `kStatusGroup_PHY` = 41,
 - `kStatusGroup_TRGMUX` = 42,
 - `kStatusGroup_SMARTCARD` = 43,
 - `kStatusGroup_LMEM` = 44,
 - `kStatusGroup_QSPI` = 45,
 - `kStatusGroup_DMA` = 50,
 - `kStatusGroup_EDMA` = 51,
 - `kStatusGroup_DMAMGR` = 52,
 - `kStatusGroup_FLEXCAN` = 53,
 - `kStatusGroup_LTC` = 54,
 - `kStatusGroup_FLEXIO_CAMERA` = 55,
 - `kStatusGroup_LPC_SPI` = 56,
 - `kStatusGroup_LPC_USMART` = 57,
 - `kStatusGroup_DMIC` = 58,
 - `kStatusGroup_SDIF` = 59,


```
kStatusGroup_POWER_MANAGER = 159 }
```

Status group numbers.

- enum {


```
kStatus_Success = MAKE_STATUS(kStatusGroup_Generic, 0),
kStatus_Fail = MAKE_STATUS(kStatusGroup_Generic, 1),
kStatus_ReadOnly = MAKE_STATUS(kStatusGroup_Generic, 2),
kStatus_OutOfRange = MAKE_STATUS(kStatusGroup_Generic, 3),
kStatus_InvalidArgument = MAKE_STATUS(kStatusGroup_Generic, 4),
kStatus_Timeout = MAKE_STATUS(kStatusGroup_Generic, 5),
kStatus_NoTransferInProgress,
kStatus_Busy = MAKE_STATUS(kStatusGroup_Generic, 7),
kStatus_NoData }
```

Generic status return codes.

Functions

- void * [SDK_Malloc](#) (size_t size, size_t alignbytes)
Allocate memory with given alignment and aligned size.
- void [SDK_Free](#) (void *ptr)
Free memory.
- void [SDK_DelayAtLeastUs](#) (uint32_t delayTime_us, uint32_t coreClock_Hz)
Delay at least for some time.

Driver version

- #define [FSL_COMMON_DRIVER_VERSION](#) ([MAKE_VERSION](#)(2, 3, 1))
common driver version.

Min/max macros

- #define [MIN](#)(a, b) (((a) < (b)) ? (a) : (b))
- #define [MAX](#)(a, b) (((a) > (b)) ? (a) : (b))

UINT16_MAX/UINT32_MAX value

- #define [UINT16_MAX](#) ((uint16_t)-1)
- #define [UINT32_MAX](#) ((uint32_t)-1)

Suppress fallthrough warning macro

- #define [SUPPRESS_FALL_THROUGH_WARNING](#)()

7.2 Macro Definition Documentation

7.2.1 #define FSL_DRIVER_TRANSFER_DOUBLE_WEAK_IRQ 1

7.2.2 #define MAKE_STATUS(group, code) (((group)*100L) + (code)))

7.2.3 **#define MAKE_VERSION(*major*, *minor*, *bugfix*) (((major) * 65536L) + ((minor) * 256L) + (bugfix))**

The driver version is a 32-bit number, for both 32-bit platforms(such as Cortex M) and 16-bit platforms(such as DSC).

Unused		Major Version		Minor Version		Bug Fix	
31	25	24	17	16	9	8	0

7.2.4 **#define FSL_COMMON_DRIVER_VERSION (MAKE_VERSION(2, 3, 1))**

7.2.5 **#define DEBUG_CONSOLE_DEVICE_TYPE_NONE 0U**

7.2.6 **#define DEBUG_CONSOLE_DEVICE_TYPE_UART 1U**

7.2.7 **#define DEBUG_CONSOLE_DEVICE_TYPE_LPUART 2U**

7.2.8 **#define DEBUG_CONSOLE_DEVICE_TYPE_LPSCI 3U**

7.2.9 **#define DEBUG_CONSOLE_DEVICE_TYPE_USBCDC 4U**

7.2.10 **#define DEBUG_CONSOLE_DEVICE_TYPE_FLEXCOMM 5U**

7.2.11 **#define DEBUG_CONSOLE_DEVICE_TYPE_IUART 6U**

7.2.12 **#define DEBUG_CONSOLE_DEVICE_TYPE_VUSART 7U**

7.2.13 **#define DEBUG_CONSOLE_DEVICE_TYPE_MINI_USART 8U**

7.2.14 **#define DEBUG_CONSOLE_DEVICE_TYPE_SWO 9U**

7.2.15 **#define DEBUG_CONSOLE_DEVICE_TYPE_QSCI 10U**

7.2.16 **#define ARRAY_SIZE(x) (sizeof(x) / sizeof((x)[0]))**

7.3 Typedef Documentation

7.3.1 **typedef int32_t status_t**

7.4 Enumeration Type Documentation

7.4.1 enum _status_groups

Enumerator

kStatusGroup_Generic Group number for generic status codes.
kStatusGroup_FLASH Group number for FLASH status codes.
kStatusGroup_LPSPI Group number for LPSPI status codes.
kStatusGroup_FLEXIO_SPI Group number for FLEXIO SPI status codes.
kStatusGroup_DSPI Group number for DSPI status codes.
kStatusGroup_FLEXIO_UART Group number for FLEXIO UART status codes.
kStatusGroup_FLEXIO_I2C Group number for FLEXIO I2C status codes.
kStatusGroup_LPI2C Group number for LPI2C status codes.
kStatusGroup_UART Group number for UART status codes.
kStatusGroup_I2C Group number for I2C status codes.
kStatusGroup_LPSCI Group number for LPSCI status codes.
kStatusGroup_LPUART Group number for LPUART status codes.
kStatusGroup_SPI Group number for SPI status code.
kStatusGroup_XRDC Group number for XRDC status code.
kStatusGroup_SEMA42 Group number for SEMA42 status code.
kStatusGroup_SDHC Group number for SDHC status code.
kStatusGroup_SDMMC Group number for SDMMC status code.
kStatusGroup_SAI Group number for SAI status code.
kStatusGroup_MCG Group number for MCG status codes.
kStatusGroup_SCG Group number for SCG status codes.
kStatusGroup_SDSPI Group number for SDSPI status codes.
kStatusGroup_FLEXIO_I2S Group number for FLEXIO I2S status codes.
kStatusGroup_FLEXIO_MCULCD Group number for FLEXIO LCD status codes.
kStatusGroup_FLASHIAP Group number for FLASHIAP status codes.
kStatusGroup_FLEXCOMM_I2C Group number for FLEXCOMM I2C status codes.
kStatusGroup_I2S Group number for I2S status codes.
kStatusGroup_IUART Group number for IUART status codes.
kStatusGroup_CSI Group number for CSI status codes.
kStatusGroup_MIPI_DSI Group number for MIPI DSI status codes.
kStatusGroup_SDRAMC Group number for SDRAMC status codes.
kStatusGroup_POWER Group number for POWER status codes.
kStatusGroup_ENET Group number for ENET status codes.
kStatusGroup_PHY Group number for PHY status codes.
kStatusGroup_TRGMUX Group number for TRGMUX status codes.
kStatusGroup_SMARTCARD Group number for SMARTCARD status codes.
kStatusGroup_LMEM Group number for LMEM status codes.
kStatusGroup_QSPI Group number for QSPI status codes.
kStatusGroup_DMA Group number for DMA status codes.
kStatusGroup_EDMA Group number for EDMA status codes.
kStatusGroup_DMAMGR Group number for DMAMGR status codes.

kStatusGroup_FLEXCAN Group number for FlexCAN status codes.

kStatusGroup_LTC Group number for LTC status codes.

kStatusGroup_FLEXIO_CAMERA Group number for FLEXIO CAMERA status codes.

kStatusGroup_LPC_SPI Group number for LPC_SPI status codes.

kStatusGroup_LPC_USART Group number for LPC_USART status codes.

kStatusGroup_DMIC Group number for DMIC status codes.

kStatusGroup_SDIF Group number for SDIF status codes.

kStatusGroup_SPIFI Group number for SPIFI status codes.

kStatusGroup_OTP Group number for OTP status codes.

kStatusGroup_MCAN Group number for MCAN status codes.

kStatusGroup_CAAM Group number for CAAM status codes.

kStatusGroup_ECSPI Group number for ECSPI status codes.

kStatusGroup_USDHC Group number for USDHC status codes.

kStatusGroup_LPC_I2C Group number for LPC_I2C status codes.

kStatusGroup_DCP Group number for DCP status codes.

kStatusGroup_MSCAN Group number for MSCAN status codes.

kStatusGroup_ESAI Group number for ESAI status codes.

kStatusGroup_FLEXSPI Group number for FLEXSPI status codes.

kStatusGroup_MMDC Group number for MMDC status codes.

kStatusGroup_PDM Group number for MIC status codes.

kStatusGroup_SDMA Group number for SDMA status codes.

kStatusGroup_ICS Group number for ICS status codes.

kStatusGroup_SPDIF Group number for SPDIF status codes.

kStatusGroup_LPC_MINISPI Group number for LPC_MINISPI status codes.

kStatusGroup_HASHCRYPT Group number for Hashcrypt status codes.

kStatusGroup_LPC_SPI_SSP Group number for LPC_SPI_SSP status codes.

kStatusGroup_I3C Group number for I3C status codes.

kStatusGroup_LPC_I2C_1 Group number for LPC_I2C_1 status codes.

kStatusGroup_NOTIFIER Group number for NOTIFIER status codes.

kStatusGroup_DebugConsole Group number for debug console status codes.

kStatusGroup_SEMC Group number for SEMC status codes.

kStatusGroup_ApplicationRangeStart Starting number for application groups.

kStatusGroup_IAP Group number for IAP status codes.

kStatusGroup_SFA Group number for SFA status codes.

kStatusGroup_SPC Group number for SPC status codes.

kStatusGroup_PUF Group number for PUF status codes.

kStatusGroup_TOUCH_PANEL Group number for touch panel status codes.

kStatusGroup_HAL_GPIO Group number for HAL GPIO status codes.

kStatusGroup_HAL_UART Group number for HAL UART status codes.

kStatusGroup_HAL_TIMER Group number for HAL TIMER status codes.

kStatusGroup_HAL_SPI Group number for HAL SPI status codes.

kStatusGroup_HAL_I2C Group number for HAL I2C status codes.

kStatusGroup_HAL_FLASH Group number for HAL FLASH status codes.

kStatusGroup_HAL_PWM Group number for HAL PWM status codes.

kStatusGroup_HAL_RNG Group number for HAL RNG status codes.

kStatusGroup_HAL_I2S Group number for HAL I2S status codes.

kStatusGroup_TIMERMANAGER Group number for TiMER MANAGER status codes.

kStatusGroup_SERIALMANAGER Group number for SERIAL MANAGER status codes.

kStatusGroup_LED Group number for LED status codes.

kStatusGroup_BUTTON Group number for BUTTON status codes.

kStatusGroup_EXTERN_EEPROM Group number for EXTERN EEPROM status codes.

kStatusGroup_SHELL Group number for SHELL status codes.

kStatusGroup_MEM_MANAGER Group number for MEM MANAGER status codes.

kStatusGroup_LIST Group number for List status codes.

kStatusGroup_OSA Group number for OSA status codes.

kStatusGroup_COMMON_TASK Group number for Common task status codes.

kStatusGroup_MSG Group number for messaging status codes.

kStatusGroup_SDK_OCOTP Group number for OCOTP status codes.

kStatusGroup_SDK_FLEXSPINOR Group number for FLEXSPINOR status codes.

kStatusGroup_CODEC Group number for codec status codes.

kStatusGroup_ASRC Group number for codec status ASRC.

kStatusGroup_OTFAD Group number for codec status codes.

kStatusGroup_SDIOSLV Group number for SDIOSLV status codes.

kStatusGroup_MECC Group number for MECC status codes.

kStatusGroup_ENET_QOS Group number for ENET_QOS status codes.

kStatusGroup_LOG Group number for LOG status codes.

kStatusGroup_I3CBUS Group number for I3CBUS status codes.

kStatusGroup_QSCI Group number for QSCI status codes.

kStatusGroup_SNT Group number for SNT status codes.

kStatusGroup_QUEUEDSPI Group number for QSPI status codes.

kStatusGroup_POWER_MANAGER Group number for POWER_MANAGER status codes.

7.4.2 anonymous enum

Enumerator

kStatus_Success Generic status for Success.

kStatus_Fail Generic status for Fail.

kStatus_ReadOnly Generic status for read only failure.

kStatus_OutOfRange Generic status for out of range access.

kStatus_InvalidArgument Generic status for invalid argument check.

kStatus_Timeout Generic status for timeout.

kStatus_NoTransferInProgress Generic status for no transfer in progress.

kStatus_Busy Generic status for module is busy.

kStatus_NoData Generic status for no data is found for the operation.

7.5 Function Documentation

7.5.1 void* SDK_Malloc (size_t *size*, size_t *alignbytes*)

This is provided to support the dynamically allocated memory used in cache-able region.

Parameters

<i>size</i>	The length required to malloc.
<i>alignbytes</i>	The alignment size.

Return values

<i>The</i>	allocated memory.
------------	-------------------

7.5.2 void SDK_Free (void * *ptr*)

Parameters

<i>ptr</i>	The memory to be release.
------------	---------------------------

7.5.3 void SDK_DelayAtLeastUs (uint32_t *delayTime_us*, uint32_t *coreClock_Hz*)

Please note that, this API uses while loop for delay, different run-time environments make the time not precise, if precise delay count was needed, please implement a new delay function with hardware timer.

Parameters

<i>delayTime_us</i>	Delay time in unit of microsecond.
<i>coreClock_Hz</i>	Core clock frequency with Hz.

Chapter 8

ASRC: Asynchronous sample rate converter

8.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Asynchronous sample rate converter module of MCUXpresso SDK devices.

The Asynchronous sample rate converter support convert between sample rate: kASRC_SampleRate_8000 = 8000, /*!< 8K sample rate

Modules

- [ASRC Driver](#)
- [ASRC SDMA Driver](#)

8.2 ASRC Driver

8.2.1 Overview

Data Structures

- struct [asrc_data_format_t](#)
asrc context data format [More...](#)
- struct [asrc_access_ctrl_t](#)
asrc context access control The ASRC provides interleaving support in hardware to ensure that a variety of sample source can be internally combined to conform with this format. [More...](#)
- struct [asrc_context_input_config_t](#)
asrc context input configuration [More...](#)
- struct [asrc_context_output_config_t](#)
asrc context output configuration [More...](#)
- struct [asrc_context_prefilter_config_t](#)
asrc context prefilter configuration [More...](#)
- struct [asrc_context_resampler_config_t](#)
asrc context resampler configuration [More...](#)
- struct [asrc_context_config_t](#)
asrc context configuration [More...](#)
- struct [asrc_transfer_t](#)
ASRC transfer. [More...](#)

Macros

- #define [FSL_ASRC_INPUT_FIFO_DEPTH](#) (128U)
ASRC fifo depth.
- #define [ASRC_SUPPORT_MAXIMUM_CONTEXT_PROCESSOR_NUMBER](#) 4U
ASRC support maximum channel number of context.

Enumerations

- enum {
[kStatus_ASRCIdle](#) = MAKE_STATUS(kStatusGroup_ASRC, 0),
[kStatus_ASRCBusy](#) = MAKE_STATUS(kStatusGroup_ASRC, 1),
[kStatus_ASRCInvalidArgument](#) = MAKE_STATUS(kStatusGroup_ASRC, 2),
[kStatus_ASRCConfigureFailed](#) = MAKE_STATUS(kStatusGroup_ASRC, 3),
[kStatus_ASRCConvertError](#) = MAKE_STATUS(kStatusGroup_ASRC, 4),
[kStatus_ASRCNotSupport](#) = MAKE_STATUS(kStatusGroup_ASRC, 5),
[kStatus_ASRCQueueFull](#) = MAKE_STATUS(kStatusGroup_ASRC, 6),
[kStatus_ASRCQueueIdle](#) = MAKE_STATUS(kStatusGroup_ASRC, 7),
[kStatus_ASRCLoadFirmwareFailed](#) = MAKE_STATUS(kStatusGroup_ASRC, 8),
[kStatus_ASRCResamplerConfigureFailed](#) = MAKE_STATUS(kStatusGroup_ASRC, 9),
[kStatus_ASRCPrefilterConfigureFailed](#) = MAKE_STATUS(kStatusGroup_ASRC, 10) }
ASRC return status, _asrc_status.

- enum `asrc_context_t` {
`kASRC_Context0` = 0,
`kASRC_Context1` = 1,
`kASRC_Context2` = 2,
`kASRC_Context3` = 3 }
asrc context id
- enum {
`kASRC_Context0InputFifoOverflow` = 1U,
`kASRC_Context1InputFifoOverflow` = 1U << 1U,
`kASRC_Context2InputFifoOverflow` = 1U << 2U,
`kASRC_Context3InputFifoOverflow` = 1U << 3U,
`kASRC_Context0OutFifoReadEmpty` = 1U << 4U,
`kASRC_Context1OutFifoReadEmpty` = 1U << 5U,
`kASRC_Context2OutFifoReadEmpty` = 1U << 6U,
`kASRC_Context3OutFifoReadEmpty` = 1U << 7U,
`kASRC_Context0RunStopDone` = 1U << 8U,
`kASRC_Context1RunStopDone` = 1U << 9U,
`kASRC_Context2RunStopDone` = 1U << 10U,
`kASRC_Context3RunStopDone` = 1U << 11U,
`kASRC_ContextAllInterruptStatus` = 0xFFFFU }
The ASRC interrupt enable flag, _asrc_interrupt_mask.
- enum {
`kASRC_FifoStatusInputFifoWatermarkFlag`,
`kASRC_FifoStatusOutputFifoWatermarkFlag` }
ASRC fifo status, _asrc_fifo_status.
- enum `asrc_data_endianness_t` {
`kASRC_DataEndianLittle` = 0U,
`kASRC_DataEndianBig` = 1U }
asrc data endianness
- enum `asrc_data_width_t` {
`kASRC_DataWidth32Bit` = 3U,
`kASRC_DataWidth24Bit` = 2U,
`kASRC_DataWidth20Bit` = 1U,
`kASRC_DataWidth16Bit` = 0U }
data width
- enum `asrc_data_type_t` {
`kASRC_DataTypeInteger` = 0U,
`kASRC_DataTypeFloat` = 1U }
data type
- enum `asrc_data_sign_t` {
`kASRC_DataSigned` = 0U,
`kASRC_DataUnsigned` = 1U }
sign extension
- enum `asrc_sampleBuffer_init_mode_t` {
`kASRC_SampleBufferNoPreFillOnInit` = 0U,
`kASRC_SampleBufferFillFirstSampleOnInit`,

- `kASRC_SampleBufferFillZeroOnInit = 2U }`
asrc prefilter and resampler sample buffer init mode
- `enum asrc_sampleBuffer_stop_mode_t {`
`kASRC_SampleBufferFillLastSampleOnStop,`
`kASRC_SampleBufferFillZeroOnStop = 1U }`
asrc prefilter and resampler sample buffer stop mode
- `enum asrc_prefilter_stage1_result_t {`
`kASRC_PrefilterStage1ResultInt = 0U,`
`kASRC_PrefilterStage1ResultFloat = 1U }`
ASRC prefilter stage1 result format.
- `enum asrc_resampler_taps_t {`
`kASRC_ResamplerTaps_32 = 32U,`
`kASRC_ResamplerTaps_64 = 64U,`
`kASRC_ResamplerTaps_128 = 128U }`
ASRC resampler taps.
- `enum {`
`kASRC_SampleRate_8000 = 8000,`
`kASRC_SampleRate_11025 = 11025,`
`kASRC_SampleRate_12000 = 12000,`
`kASRC_SampleRate_16000 = 16000,`
`kASRC_SampleRate_22050 = 22050,`
`kASRC_SampleRate_24000 = 24000,`
`kASRC_SampleRate_32000 = 32000,`
`kASRC_SampleRate_44100 = 44100,`
`kASRC_SampleRate_48000 = 48000,`
`kASRC_SampleRate_64000 = 64000,`
`kASRC_SampleRate_88200 = 88200,`
`kASRC_SampleRate_96000 = 96000,`
`kASRC_SampleRate_128000 = 128000,`
`kASRC_SampleRate_176400 = 176400,`
`kASRC_SampleRate_192000 = 192000,`
`kASRC_SampleRate_256000 = 256000,`
`kASRC_SampleRate_352800 = 352800,`
`kASRC_SampleRate_384000 = 384000,`
`kASRC_SampleRate_768000 = 768000 }`
ASRC support sample rate, _asrc_sample_rate.

Driver version

- `#define FSL_ASRC_DRIVER_VERSION (MAKE_VERSION(2, 0, 6))`
Version 2.0.6.

Initialization and deinitialization

- `uint32_t ASRC_GetInstance (ASRC_Type *base)`

- *Get instance number of the ASRC peripheral.*
- void [ASRC_Init](#) (ASRC_Type *base)
brief Initializes the asrc peripheral.
- void [ASRC_Deinit](#) (ASRC_Type *base)
De-initializes the ASRC peripheral.
- void [ASRC_GetContextDefaultConfig](#) (asrc_context_config_t *config, uint32_t channels, uint32_t inSampleRate, uint32_t outSampleRate)
ASRC get context default configuration.
- status_t [ASRC_SetContextConfig](#) (ASRC_Type *base, asrc_context_t context, asrc_context_config_t *config)
ASRC configure context.
- status_t [ASRC_SetContextOutputConfig](#) (ASRC_Type *base, asrc_context_t context, asrc_context_output_config_t *config)
ASRC configure context output.
- status_t [ASRC_SetContextInputConfig](#) (ASRC_Type *base, asrc_context_t context, asrc_context_input_config_t *config)
ASRC configure context input.
- static void [ASRC_EnableContextRun](#) (ASRC_Type *base, asrc_context_t context, bool enable)
ASRC context enable run.
- static void [ASRC_EnableContextRunStop](#) (ASRC_Type *base, asrc_context_t context, bool enable)
ASRC context enable run stop.
- static void [ASRC_EnableContextInDMA](#) (ASRC_Type *base, asrc_context_t context, bool enable)
ASRC context input DMA request enable.
- static void [ASRC_EnableContextOutDMA](#) (ASRC_Type *base, asrc_context_t context, bool enable)
ASRC context output DMA request enable.
- static void [ASRC_EnablePreFilterBypass](#) (ASRC_Type *base, asrc_context_t context, bool bypass)
ASRC prefilter bypass mode This function enable or disable the ASRC prefilter bypass mode.
- static void [ASRC_EnableResamplerBypass](#) (ASRC_Type *base, asrc_context_t context, bool bypass)
ASRC resampler bypass mode This function enable or disable the ASRC resampler bypass mode.
- static void [ASRC_SetContextChannelNumber](#) (ASRC_Type *base, asrc_context_t context, uint32_t channels)
ASRC set context channel number.
- uint32_t [ASRC_GetContextOutSampleSize](#) (uint32_t inSampleRate, uint32_t inSamplesSize, uint32_t inWidth, uint32_t outSampleRate, uint32_t outWidth)
ASRC get output sample count.

Interrupts

- static void [ASRC_EnableInterrupt](#) (ASRC_Type *base, uint32_t mask)
ASRC interrupt enable This function enable the ASRC interrupt with the provided mask.
- static void [ASRC_DisableInterrupt](#) (ASRC_Type *base, uint32_t mask)
ASRC interrupt disable This function disable the ASRC interrupt with the provided mask.

Status

- static uint32_t [ASRC_GetInterruptStatus](#) (ASRC_Type *base)
Gets the ASRC interrupt status flag state.
- static void [ASRC_ClearInterruptStatus](#) (ASRC_Type *base, uint32_t status)
clear the ASRC interrupt status flag state.
- static uint32_t [ASRC_GetFifoStatus](#) (ASRC_Type *base, [asrc_context_t](#) context)
Gets the ASRC fifo status flag.

fifo Operations

- static void [ASRC_WriteContextFifo](#) (ASRC_Type *base, [asrc_context_t](#) context, uint32_t data)
write the ASRC context fifo.
- static uint32_t [ASRC_ReadContextFifo](#) (ASRC_Type *base, [asrc_context_t](#) context)
read the ASRC context fifo.
- static uint32_t [ASRC_GetWriteContextFifoAddr](#) (ASRC_Type *base, [asrc_context_t](#) context)
Get ASRC write fifo address.
- static uint32_t [ASRC_GetReadContextFifoAddr](#) (ASRC_Type *base, [asrc_context_t](#) context)
Get the ASRC read context fifo address.
- uint32_t [ASRC_ReadFIFORemainedSample](#) (ASRC_Type *base, [asrc_context_t](#) context, uint32_t *outAddr, uint32_t outWidth, uint32_t sampleCount)
Get the ASRC read fifo remained samples.

Transactional

- [status_t ASRC_TransferBlocking](#) (ASRC_Type *base, [asrc_context_t](#) context, [asrc_transfer_t](#) *xfer)
ASRC blocking convert audio sample rate.

8.2.2 Data Structure Documentation

8.2.2.1 struct asrc_data_format_t

Data Fields

- uint8_t [dataPosition](#)
context input data sample position
- [asrc_data_endianness_t dataEndianness](#)
context input data endianness
- [asrc_data_width_t dataWidth](#)
context input data width
- [asrc_data_type_t dataType](#)
context input data type
- [asrc_data_sign_t dataSign](#)
context input data signed or unsigned

8.2.2.2 struct asrc_access_ctrl_t

The interleave pattern is controlled using 3 register fields: GROUP_LENGTH, ACCESS_LENGTH, ITERATIONIS. This is intended to support hardware configurations which distribute a single context across samples from multiple audio sources. Take an example as below: accessGroupLen = 6, the sample group length is 6 samples accessIterations = 2, the 2 sequential ACCESS_LENGTH read from single source accessLen = 2, the 2 samples fetch from one source.

Data Fields

- uint8_t [accessIterations](#)
number of sequential fetches per source
- uint8_t [accessGroupLen](#)
number of channels in a context
- uint8_t [accessLen](#)
number of channels per source

8.2.2.3 struct asrc_context_input_config_t

Data Fields

- uint32_t [sampleRate](#)
input audio data sample rate
- uint8_t [watermark](#)
input water mark per samples
- [asrc_access_ctrl_t](#) [accessCtrl](#)
input access control
- [asrc_data_format_t](#) [dataFormat](#)
input data format

8.2.2.4 struct asrc_context_output_config_t

Data Fields

- uint32_t [sampleRate](#)
output audio data sample rate
- uint8_t [watermark](#)
output water mark per samples
- [asrc_access_ctrl_t](#) [accessCtrl](#)
output access control
- [asrc_data_format_t](#) [dataFormat](#)
output data format
- bool [enableDither](#)
output path contains a TPDF dither function.
- bool [enableIEC60958](#)
output IEC60958 bit field insertion enable

Field Documentation

(1) `bool asrc_context_output_config_t::enableDither`

The dither function support all fixed output modes(16, 20, 24, 32bits) dither is not supported in 32bit floating point output mode

8.2.2.5 `struct asrc_context_prefilter_config_t`

Data Fields

- `asrc_sampleBuffer_init_mode_t` `initMode`
prefilter initial mode
- `asrc_sampleBuffer_stop_mode_t` `stopMode`
prefilter stop mode
- `asrc_prefilter_stage1_result_t` `stage1Result`
stage1 data store format
- `uint32_t` `filterSt1Taps`
prefilter stage1 taps
- `uint32_t` `filterSt2Taps`
prefilter stage2 taps
- `uint32_t` `filterSt1Exp`
prefilter stage1 expansion factor
- `const uint32_t *` `filterCoeffAddress`
prefilter coeff address

8.2.2.6 `struct asrc_context_resampler_config_t`

Data Fields

- `asrc_sampleBuffer_init_mode_t` `initMode`
initial mode
- `asrc_sampleBuffer_stop_mode_t` `stopMode`
resampler stop mode
- `asrc_resampler_taps_t` `tap`
resampleer taps
- `uint32_t` `filterPhases`
interpolation phases
- `uint64_t` `filterCenterTap`
interpolation center tap
- `const uint32_t *` `filterCoeffAddress`
interpolation coeff address

8.2.2.7 `struct asrc_context_config_t`

Data Fields

- `uint8_t` `contextChannelNums`

- *context channel numbers*
- [asrc_context_input_config_t](#) contextInput
context input configuration
- [asrc_context_output_config_t](#) contextOutput
context output configuration
- [asrc_context_prefilter_config_t](#) contextPrefilter
context pre filter configuration
- [asrc_context_resampler_config_t](#) contextResampler
context resampler configuration

8.2.2.8 struct asrc_transfer_t

Data Fields

- uint32_t * [inDataAddr](#)
address of audio data to be converted
- uint32_t [inDataSize](#)
size of the audio data
- uint32_t * [outDataAddr](#)
address of audio data that is been converted
- uint32_t [outDataSize](#)
size of the audio data

8.2.3 Enumeration Type Documentation

8.2.3.1 anonymous enum

Enumerator

kStatus_ASRCIdle ASRC is idle.
kStatus_ASRCBusy ASRC is busy.
kStatus_ASRCInvalidArgument ASRC invalid argument.
kStatus_ASRCConfigureFailed ASRC configure failed.
kStatus_ASRCConvertError ASRC convert error failed.
kStatus_ASRCNotSupport ASRC not support.
kStatus_ASRCQueueFull ASRC queue full.
kStatus_ASRCQueueIdle ASRC queue idle.
kStatus_ASRCLoadFirmwareFailed ASRC load firmware failed.
kStatus_ASRCResamplerConfigureFailed ASRC resampler configured failed.
kStatus_ASRCPrefilterConfigureFailed ASRC prefilter configured failed.

8.2.3.2 enum asrc_context_t

Enumerator

kASRC_Context0 Context 0 value.

kASRC_Context1 Context 1 value.
kASRC_Context2 Context 2 value.
kASRC_Context3 Context 3 value.

8.2.3.3 anonymous enum

Enumerator

kASRC_Context0InputFifoOverflow context 0 input fifo overflow
kASRC_Context1InputFifoOverflow context 1 input fifo overflow
kASRC_Context2InputFifoOverflow context 2 input fifo overflow
kASRC_Context3InputFifoOverflow context 3 input fifo overflow
kASRC_Context0OutFifoReadEmpty context 0 out fifo read empty
kASRC_Context1OutFifoReadEmpty context 1 out fifo read empty
kASRC_Context2OutFifoReadEmpty context 2 out fifo read empty
kASRC_Context3OutFifoReadEmpty context 3 out fifo read empty
kASRC_Context0RunStopDone context 0 run stop done interrupt
kASRC_Context1RunStopDone context 1 run stop done interrupt
kASRC_Context2RunStopDone context 2 run stop done interrupt
kASRC_Context3RunStopDone context 3 run stop done interrupt
kASRC_ContextAllInterruptStatus all the context interrupt status

8.2.3.4 anonymous enum

Enumerator

kASRC_FifoStatusInputFifoWatermarkFlag input water mark flag raised
kASRC_FifoStatusOutputFifoWatermarkFlag output water mark flag raised

8.2.3.5 enum asrc_data_endianness_t

Enumerator

kASRC_DataEndianLittle context data little endian
kASRC_DataEndianBig context data big endian

8.2.3.6 enum asrc_data_width_t

Enumerator

kASRC_DataWidth32Bit data width 32bit
kASRC_DataWidth24Bit data width 24bit
kASRC_DataWidth20Bit data width 20bit
kASRC_DataWidth16Bit data width 16bit

8.2.3.7 enum asrc_data_type_t

Enumerator

kASRC_DataTypeInteger data type int

kASRC_DataTypeFloat data type float, single precision floating point format

8.2.3.8 enum asrc_data_sign_t

Enumerator

kASRC_DataSigned input data is signed

kASRC_DataUnsigned input data is unsigned

8.2.3.9 enum asrc_sampleBuffer_init_mode_t

Enumerator

kASRC_SampleBufferNoPreFillOnInit do not pre-fill

kASRC_SampleBufferFillFirstSampleOnInit replicate the first sample to fill the right half of the sample buffer

kASRC_SampleBufferFillZeroOnInit zero fill the right half of the sample buffer

8.2.3.10 enum asrc_sampleBuffer_stop_mode_t

Enumerator

kASRC_SampleBufferFillLastSampleOnStop replicate the last sample to fill the left half of the sample buffer

kASRC_SampleBufferFillZeroOnStop zero fill the left half of the sample buffer

8.2.3.11 enum asrc_prefilter_stage1_result_t

Enumerator

kASRC_PrefilterStage1ResultInt prefilter stage1 results are stored in 32 bit int format

kASRC_PrefilterStage1ResultFloat prefilter stage1 results are stored in 32 bit float format

8.2.3.12 enum asrc_resampler_taps_t

Enumerator

kASRC_ResamplerTaps_32 resampler taps 32
kASRC_ResamplerTaps_64 resampler taps 64
kASRC_ResamplerTaps_128 resampler taps 128

8.2.3.13 anonymous enum

Enumerator

kASRC_SampleRate_8000 8K sample rate
kASRC_SampleRate_11025 11025 sample rate
kASRC_SampleRate_12000 12K sample rate
kASRC_SampleRate_16000 16K sample rate
kASRC_SampleRate_22050 22.05K sample rate
kASRC_SampleRate_24000 24K sample rate
kASRC_SampleRate_32000 32K sample rate
kASRC_SampleRate_44100 44.1K sample rate
kASRC_SampleRate_48000 48K sample rate
kASRC_SampleRate_64000 64K sample rate
kASRC_SampleRate_88200 88.2K sample rate
kASRC_SampleRate_96000 96K sample rate
kASRC_SampleRate_128000 128K sample rate
kASRC_SampleRate_176400 176K sample rate
kASRC_SampleRate_192000 256K sample rate
kASRC_SampleRate_256000 256K sample rate
kASRC_SampleRate_352800 352.8K sample rate
kASRC_SampleRate_384000 384K sample rate
kASRC_SampleRate_768000 768K sample rate

8.2.4 Function Documentation

8.2.4.1 uint32_t ASRC_GetInstance (ASRC_Type * *base*)

Parameters

<i>base</i>	ASRC base pointer.
-------------	--------------------

8.2.4.2 void ASRC_Init (ASRC_Type * *base*)

This API gates the asrc clock. The asrc module can't operate unless ASRC_Init is called to enable the clock.

param base asrc base pointer.

8.2.4.3 void ASRC_Deinit (ASRC_Type * *base*)

This API gates the ASRC clock and disable ASRC module. The ASRC module can't operate unless ASRC_Init

Parameters

<i>base</i>	ASRC base pointer.
-------------	--------------------

8.2.4.4 void ASRC_GetContextDefaultConfig (asrc_context_config_t * *config*, uint32_t *channels*, uint32_t *inSampleRate*, uint32_t *outSampleRate*)

Parameters

<i>config</i>	ASRC context configuration pointer.
<i>channels</i>	input audio data channel numbers.
<i>inSampleRate</i>	input sample rate.
<i>outSampleRate</i>	output sample rate.

8.2.4.5 status_t ASRC_SetContextConfig (ASRC_Type * *base*, asrc_context_t *context*, asrc_context_config_t * *config*)

Parameters

<i>base</i>	ASRC base pointer.
<i>context</i>	index of asrc context, reference asrc_context_t.
<i>config</i>	ASRC context configuration pointer.

Return values

<i>kStatus_InvalidArgument</i>	invalid parameters. kStatus_ASRCConfigureFailed context configure failed. kStatus_Success context configure success.
--------------------------------	--

8.2.4.6 status_t ASRC_SetContextOutputConfig (ASRC_Type * *base*, asrc_context_t *context*, asrc_context_output_config_t * *config*)

Parameters

<i>base</i>	ASRC base pointer.
<i>context</i>	index of asrc context, reference asrc_context_t.
<i>config</i>	ASRC context output configuration pointer.

8.2.4.7 status_t ASRC_SetContextInputConfig (ASRC_Type * *base*, asrc_context_t *context*, asrc_context_input_config_t * *config*)

Parameters

<i>base</i>	ASRC base pointer.
<i>context</i>	index of asrc context, reference asrc_context_t.
<i>config</i>	ASRC context input configuration pointer.

8.2.4.8 static void ASRC_EnableContextRun (ASRC_Type * *base*, asrc_context_t *context*, bool *enable*) [inline], [static]

All control files associated with a context must be stable prior to setting context run enable.

Parameters

<i>base</i>	ASRC base pointer.
<i>context</i>	ASRC context index.
<i>enable</i>	true is enable, inform the datapath begin processing sample data for the context. false is disable, data processing will halt immediately.

8.2.4.9 static void ASRC_EnableContextRunStop (ASRC_Type * *base*, asrc_context_t *context*, bool *enable*) [inline], [static]

This function used to flush the ASRC pipeline and completely end processing for a context.

Parameters

<i>base</i>	ASRC base pointer.
<i>context</i>	ASRC context index.
<i>enable</i>	true is enable, false is disable.

8.2.4.10 static void ASRC_EnableContextInDMA (ASRC_Type * *base*, asrc_context_t *context*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	ASRC base pointer.
<i>context</i>	ASRC context index.
<i>enable</i>	true is enable, false is disable.

8.2.4.11 static void ASRC_EnableContextOutDMA (ASRC_Type * *base*, asrc_context_t *context*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	ASRC base pointer.
<i>context</i>	ASRC context index.
<i>enable</i>	true is enable, false is disable.

8.2.4.12 static void ASRC_EnablePreFilterBypass (ASRC_Type * *base*, asrc_context_t *context*, bool *bypass*) [inline], [static]

Parameters

<i>base</i>	ASRC peripheral base address.
<i>context</i>	context processor number.
<i>bypass</i>	true is bypass, false is normal mode.

8.2.4.13 static void ASRC_EnableResamplerBypass (ASRC_Type * *base*, asrc_context_t *context*, bool *bypass*) [inline], [static]

Parameters

<i>base</i>	ASRC peripheral base address.
<i>context</i>	context processor number.
<i>bypass</i>	true is bypass, false is normal mode.

8.2.4.14 static void ASRC_SetContextChannelNumber (ASRC_Type * *base*, asrc_context_t *context*, uint32_t *channels*) [inline], [static]

Note: The maximum channel number in one context can not exceed 32.

Parameters

<i>base</i>	ASRC peripheral base address.
<i>context</i>	context number.
<i>channels</i>	channel number, should <= 32.

8.2.4.15 uint32_t ASRC_GetContextOutSampleSize (uint32_t *inSampleRate*, uint32_t *inSamplesSize*, uint32_t *inWidth*, uint32_t *outSampleRate*, uint32_t *outWidth*)

Parameters

<i>inSampleRate</i>	output sample rate.
<i>inSamplesSize</i>	input sample rate.
<i>inWidth</i>	input samples buffer size, the size of buffer should be converted to align with 4 byte .
<i>outSampleRate</i>	input sample width.
<i>outWidth</i>	Output width.

Return values

<i>output</i>	samples size.
---------------	---------------

8.2.4.16 static void ASRC_EnableInterrupt (ASRC_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	ASRC peripheral base address.
<i>mask</i>	The interrupts to enable. Logical OR of _asrc_interrupt_mask.

8.2.4.17 static void ASRC_DisableInterrupt (ASRC_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	ASRC peripheral base address.
<i>mask</i>	The interrupts to disable. Logical OR of _asrc_interrupt_mask.

8.2.4.18 static uint32_t ASRC_GetInterruptStatus (ASRC_Type * *base*) [inline], [static]

Parameters

<i>base</i>	ASRC base pointer
-------------	-------------------

Returns

ASRC Tx status flag value. Use the Status Mask to get the status value needed.

8.2.4.19 static void ASRC_ClearInterruptStatus (ASRC_Type * *base*, uint32_t *status*) [inline], [static]

Parameters

<i>base</i>	ASRC base pointer
<i>status</i>	status flag to be cleared.

8.2.4.20 static uint32_t ASRC_GetFifoStatus (ASRC_Type * *base*, asrc_context_t *context*) [inline], [static]

Parameters

<i>base</i>	ASRC base pointer
<i>context</i>	context id

8.2.4.21 `static void ASRC_WriteContextFifo (ASRC_Type * base, asrc_context_t context, uint32_t data) [inline], [static]`

Parameters

<i>base</i>	ASRC base pointer.
<i>context</i>	context id.
<i>data</i>	data to write.

8.2.4.22 `static uint32_t ASRC_ReadContextFifo (ASRC_Type * base, asrc_context_t context) [inline], [static]`

Parameters

<i>base</i>	ASRC base pointer.
<i>context</i>	context id.

Return values

<i>read</i>	data.
-------------	-------

8.2.4.23 `static uint32_t ASRC_GetWriteContextFifoAddr (ASRC_Type * base, asrc_context_t context) [inline], [static]`

Parameters

<i>base</i>	ASRC base pointer.
<i>context</i>	context id.

Return values

<i>write</i>	fifo address.
--------------	---------------

8.2.4.24 `static uint32_t ASRC_GetReadContextFifoAddr (ASRC_Type * base,
asrc_context_t context) [inline], [static]`

Parameters

<i>base</i>	ASRC base pointer.
<i>context</i>	context id.

Return values

<i>read</i>	fifo address.
-------------	---------------

8.2.4.25 `uint32_t ASRC_ReadFIFORemainedSample (ASRC_Type * base, asrc_context_t
context, uint32_t * outAddr, uint32_t outWidth, uint32_t sampleCount)`

Since the DMA request will be triggered only when the sample group in read fifo is bigger then the watermark, so when the data size cannot be divisibile by the (watermark + 1), then part of sample will left in read fifo, application should call this api to get the left samples.

Parameters

<i>base</i>	ASRC base pointer.
<i>context</i>	context id.
<i>outAddr</i>	address to receive remained sample in read fifo.
<i>outWidth</i>	output data width.
<i>sampleCount</i>	specify the read sample count.

Return values

<i>sample</i>	counts actual read from output fifo.
---------------	--------------------------------------

8.2.4.26 `status_t ASRC_TransferBlocking (ASRC_Type * base, asrc_context_t context,
asrc_transfer_t * xfer)`

This function depends on the configuration of input and output, so it should be called after the ASRC-
_SetContextConfig. The data format it supports: 1.16bit 16bit per sample in input buffer, input buffer

size should be calculate as: samples 2U output buffer size can be calculated by call function ASRC_GetContextOutSampleSize, the parameter outWidth should be 2. 2.20bit 24bit per sample in input buffer, input buffer size should be calculate as: samples 3U output buffer size can be calculated by call function ASRC_GetContextOutSampleSize, the outWidth should be 3. 3.24bit 24bit per sample in input buffer, input buffer size should be calculate as: samples * 3U output buffer size can be calculated by call function ASRC_GetContextOutSampleSize, the outWidth should be 3. 4.32bit 32bit per sample in input buffer, input buffer size should be calculate as: samples * 4U output buffer size can be calculated by call function ASRC_GetContextOutSampleSize, the outWidth should be 4.

Parameters

<i>base</i>	ASRC base pointer.
<i>context</i>	context id.
<i>xfer</i>	.xfer configuration.

Return values

<i>kStatus_Success.</i>	
-------------------------	--

8.3 ASRC SDMA Driver

8.3.1 Overview

Data Structures

- struct [asrc_p2p_sdma_config_t](#)
destination peripheral configuration [More...](#)
- struct [asrc_sdma_in_handle_t](#)
ASRC sdma in handle. [More...](#)
- struct [asrc_sdma_out_handle_t](#)
ASRC sdma out handle. [More...](#)
- struct [asrc_sdma_handle_t](#)
ASRC DMA transfer handle, users should not touch the content of the handle. [More...](#)

Macros

- #define [ASRC_XFER_IN_QUEUE_SIZE](#) 4U
ASRC xfer queue size.

Typedefs

- typedef void(* [asrc_sdma_callback_t](#))(ASRC_Type *base, asrc_sdma_handle_t *handle, [status_t](#) status, void *userData)
ASRC SDMA transfer callback function for finish and error.
- typedef void(* [asrc_start_peripheral_t](#))(bool start)
ASRC trigger peripheral function pointer.

Driver version

- #define [FSL_ASRC_SDMA_DRIVER_VERSION](#) (MAKE_VERSION(2, 0, 3))
Version 2.0.3.

ASRC SDMA Transactional

- void [ASRC_TransferInCreateHandleSDMA](#) (ASRC_Type *base, asrc_sdma_handle_t *handle, [asrc_sdma_callback_t](#) callback, [sdma_handle_t](#) *dmaHandle, uint32_t eventSource, [asrc_context_t](#) context, const [asrc_p2p_sdma_config_t](#) *periphConfig, void *userData)
Initializes the ASRC input SDMA handle.
- void [ASRC_TransferOutCreateHandleSDMA](#) (ASRC_Type *base, asrc_sdma_handle_t *handle, [asrc_sdma_callback_t](#) callback, [sdma_handle_t](#) *dmaHandle, uint32_t eventSource, [asrc_context_t](#) context, const [asrc_p2p_sdma_config_t](#) *periphConfig, void *userData)
Initializes the ASRC output SDMA handle.

- `status_t ASRC_TransferSetContextConfigSDMA` (ASRC_Type *base, asrc_sdma_handle_t *handle, asrc_context_config_t *asrcConfig)
Configures the ASRC context.
- `status_t ASRC_TransferSDMA` (ASRC_Type *base, asrc_sdma_handle_t *handle, asrc_transfer_t *xfer)
Performs a non-blocking ASRC transfer using DMA.
- `void ASRC_TransferAbortInSDMA` (ASRC_Type *base, asrc_sdma_handle_t *handle)
Aborts a ASRC in transfer using SDMA.
- `void ASRC_TransferAbortOutSDMA` (ASRC_Type *base, asrc_sdma_handle_t *handle)
brief Aborts a ASRC out transfer using SDMA.

8.3.2 Data Structure Documentation

8.3.2.1 struct asrc_p2p_sdma_config_t

Data Fields

- `uint32_t eventSource`
peripheral event source
- `uint8_t watermark`
peripheral watermark
- `uint8_t channel`
peripheral channel number
- `uint8_t fifoWidth`
peripheral fifo width
- `bool enableContinuous`
true is the amount of samples to be transferred is unknown and script will keep on transferring as long as both events are detected and script must be stopped by application, false is The amount of samples to be transferred is equal to the count field of mode word
- `asrc_start_peripheral_t startPeripheral`
trigger peripheral start

8.3.2.2 struct asrc_sdma_in_handle_t

Data Fields

- `sdma_handle_t * sdmaHandle`
DMA handler for ASRC.
- `uint32_t eventSource`
ASRC event source number.
- `asrc_sdma_callback_t callback`
Callback for users while transfer finish or error occurs.
- `void * userData`
User callback parameter.
- `sdma_buffer_descriptor_t bdPool [ASRC_XFER_IN_QUEUE_SIZE]`
BD pool for SDMA transfer.
- `uint8_t asrcInWatermark`
The transfer data count in a DMA request.

- `uint8_t bytesPerSample`
Bytes in a sample.
- `uint32_t * asrcQueue [ASRC_XFER_IN_QUEUE_SIZE]`
Transfer queue storing queued transfer.
- `size_t sdmaTransferSize [ASRC_XFER_IN_QUEUE_SIZE]`
Data bytes need to transfer.
- `volatile uint8_t queueUser`
Index for user to queue transfer.
- `volatile uint8_t queueDriver`
Index for driver to get the transfer data and size.
- `const asrc_p2p_sdma_config_t * peripheralConfig`
peripheral configuration
- `uint32_t state`
Internal state for ASRC SDMA transfer.

Field Documentation

- (1) `sdma_buffer_descriptor_t asrc_sdma_in_handle_t::bdPool[ASRC_XFER_IN_QUEUE_SIZE]`
- (2) `uint32_t* asrc_sdma_in_handle_t::asrcQueue[ASRC_XFER_IN_QUEUE_SIZE]`
- (3) `volatile uint8_t asrc_sdma_in_handle_t::queueUser`

8.3.2.3 struct asrc_sdma_out_handle_t

Data Fields

- `sdma_handle_t * sdmaHandle`
DMA handler for ASRC.
- `void * userData`
User callback parameter.
- `uint32_t state`
Internal state for ASRC SDMA transfer.
- `uint8_t bytesPerSample`
Bytes in a sample.
- `uint32_t eventSource`
ASRC event source number.
- `asrc_sdma_callback_t callback`
Callback for users while transfer finish or error occurs.
- `uint8_t asrcOutWatermark`
The transfer data count in a DMA request.
- `sdma_buffer_descriptor_t bdPool [ASRC_XFER_OUT_QUEUE_SIZE]`
BD pool for SDMA transfer.
- `uint32_t * asrcQueue [ASRC_XFER_OUT_QUEUE_SIZE]`
Transfer queue storing queued transfer.
- `size_t sdmaTransferSize [ASRC_XFER_OUT_QUEUE_SIZE]`
Data bytes need to transfer.
- `volatile uint8_t queueUser`
Index for user to queue transfer.
- `volatile uint8_t queueDriver`
Index for driver to get the transfer data and size.

- const [asrc_p2p_sdma_config_t](#) * *peripheralConfig*
peripheral configuration
- uint32_t [nonAlignSize](#)
non align size
- void * [nonAlignAddr](#)
non align address

Field Documentation

- (1) [sdma_buffer_descriptor_t](#) [asrc_sdma_out_handle_t::bdPool](#)[ASRC_XFER_OUT_QUEUE_SIZE]
- (2) uint32_t* [asrc_sdma_out_handle_t::asrcQueue](#)[ASRC_XFER_OUT_QUEUE_SIZE]
- (3) volatile uint8_t [asrc_sdma_out_handle_t::queueUser](#)

8.3.2.4 struct _asrc_sdma_handle

ASRC sdma handle prototype.

Data Fields

- [asrc_sdma_in_handle_t](#) *inDMAHandle*
input dma handle
- [asrc_sdma_out_handle_t](#) *outDMAHandle*
output dma handle
- [asrc_context_t](#) *context*
ASRC context number.
- uint8_t [dataChannels](#)
ASRC process data channel number.

8.3.3 Function Documentation

**8.3.3.1 void ASRC_TransferInCreateHandleSDMA (ASRC_Type * *base*,
[asrc_sdma_handle_t](#) * *handle*, [asrc_sdma_callback_t](#) *callback*, [sdma_handle_t](#)
* *dmaHandle*, uint32_t *eventSource*, [asrc_context_t](#) *context*, const
[asrc_p2p_sdma_config_t](#) * *periphConfig*, void * *userData*)**

This function initializes the ASRC input DMA handle, which can be used for other ASRC transactional APIs. Usually, for a specified ASRC context, call this API once to get the initialized handle.

Parameters

<i>base</i>	ASRC base pointer.
<i>handle</i>	ASRC SDMA handle pointer.
<i>base</i>	ASRC peripheral base address.
<i>callback</i>	Pointer to user callback function.
<i>dmaHandle</i>	SDMA handle pointer, this handle shall be static allocated by users.
<i>eventSource</i>	ASRC input sdma event source.
<i>context</i>	ASRC context number.
<i>periphConfig</i>	peripheral configurations, used for case.
<i>userData</i>	User parameter passed to the callback function.

8.3.3.2 void ASRC_TransferOutCreateHandleSDMA (ASRC_Type * *base*, asrc_sdma_handle_t * *handle*, asrc_sdma_callback_t *callback*, sdma_handle_t * *dmaHandle*, uint32_t *eventSource*, asrc_context_t *context*, const asrc_p2p_sdma_config_t * *periphConfig*, void * *userData*)

This function initializes the ASRC out DMA handle, which can be used for other ASRC transactional APIs. Usually, for a specified ASRC context, call this API once to get the initialized handle.

Parameters

<i>base</i>	ASRC base pointer.
<i>handle</i>	ASRC SDMA handle pointer.
<i>callback</i>	ASRC outcallback.
<i>dmaHandle</i>	SDMA handle pointer, this handle shall be static allocated by users.
<i>eventSource</i>	ASRC output event source.
<i>context</i>	ASRC context number.
<i>periphConfig</i>	peripheral configurations, used for case.
<i>userData</i>	User parameter passed to the callback function.

8.3.3.3 status_t ASRC_TransferSetContextConfigSDMA (ASRC_Type * *base*, asrc_sdma_handle_t * *handle*, asrc_context_config_t * *asrcConfig*)

Parameters

<i>base</i>	ASRC base pointer.
<i>handle</i>	ASRC SDMA handle pointer.
<i>asrcConfig</i>	asrc context configurations.

8.3.3.4 **status_t ASRC_TransferSDMA (ASRC_Type * *base*, asrc_sdma_handle_t * *handle*, asrc_transfer_t * *xfer*)**

Parameters

<i>base</i>	ASRC base pointer.
<i>handle</i>	ASRC SDMA handle pointer.
<i>xfer</i>	ASRC xfer configurations pointer.

Return values

<i>kStatus_Success</i>	Start a ASRC SDMA send successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.
<i>kStatus_TxBusy</i>	ASRC is busy sending data.

8.3.3.5 **void ASRC_TransferAbortInSDMA (ASRC_Type * *base*, asrc_sdma_handle_t * *handle*)**

Parameters

<i>base</i>	ASRC base pointer.
<i>handle</i>	ASRC SDMA handle pointer.

8.3.3.6 **void ASRC_TransferAbortOutSDMA (ASRC_Type * *base*, asrc_sdma_handle_t * *handle*)**

param base ASRC base pointer. param handle ASRC SDMA handle pointer.



Chapter 9

ECSPI: Enhanced Configurable Serial Peripheral Interface Driver

9.1 Overview

Modules

- [ECSPI CMSIS Driver](#)
- [ECSPI Driver](#)
- [ECSPI FreeRTOS Driver](#)
- [ECSPI SDMA Driver](#)

9.2 ECSPI Driver

9.2.1 Overview

ECSPI driver includes functional APIs and transactional APIs.

Functional APIs are feature/property target low level APIs. Functional APIs can be used for ECSPI initialization/configuration/operation for optimization/customization purpose. Using the functional API requires the knowledge of the SPI peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. ECSPI functional operation groups provide the functional API set.

Transactional APIs are transaction target high level APIs. Transactional APIs can be used to enable the peripheral and in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are a critical requirement, see the transactional API implementation and write a custom code. All transactional APIs use the `spi_handle_t` as the first parameter. Initialize the handle by calling the `SPI_MasterTransferCreateHandle()` or `SPI_SlaveTransferCreateHandle()` API.

Transactional APIs support asynchronous transfer. This means that the functions `SPI_MasterTransferNonBlocking()` and `SPI_SlaveTransferNonBlocking()` set up the interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the `kStatus_SPI_Idle` status.

9.2.2 Typical use case

9.2.2.1 SPI master transfer using polling method

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/ecspi`

9.2.2.2 SPI master transfer using an interrupt method

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/ecspi`

Data Structures

- struct `ecspi_channel_config_t`
ECSPI user channel configure structure. [More...](#)
- struct `ecspi_master_config_t`
ECSPI master configure structure. [More...](#)
- struct `ecspi_slave_config_t`
ECSPI slave configure structure. [More...](#)
- struct `ecspi_transfer_t`
ECSPI transfer structure. [More...](#)
- struct `ecspi_master_handle_t`
ECSPI master handle structure. [More...](#)

Macros

- #define `ECSPI_DUMMYDATA` (0xFFFFFFFFFU)
ECSPI dummy transfer data, the data is sent while txBuff is NULL.
- #define `SPI_RETRY_TIMES` 0U /* Define to zero means keep waiting until the flag is assert/deassert. */
Retry times for waiting flag.

Typedefs

- typedef `ecspi_master_handle_t` `ecspi_slave_handle_t`
Slave handle is the same with master handle.
- typedef void(* `ecspi_master_callback_t`)(ECSPI_Type *base, `ecspi_master_handle_t` *handle, `status_t` status, void *userData)
ECSPI master callback for finished transmit.
- typedef void(* `ecspi_slave_callback_t`)(ECSPI_Type *base, `ecspi_slave_handle_t` *handle, `status_t` status, void *userData)
ECSPI slave callback for finished transmit.

Enumerations

- enum {
 `kStatus_ECSPI_Busy` = MAKE_STATUS(kStatusGroup_ECSPI, 0),
 `kStatus_ECSPI_Idle` = MAKE_STATUS(kStatusGroup_ECSPI, 1),
 `kStatus_ECSPI_Error` = MAKE_STATUS(kStatusGroup_ECSPI, 2),
 `kStatus_ECSPI_HardwareOverflow` = MAKE_STATUS(kStatusGroup_ECSPI, 3),
 `kStatus_ECSPI_Timeout` = MAKE_STATUS(kStatusGroup_ECSPI, 4) }
Return status for the ECSPI driver.
- enum `ecspi_clock_polarity_t` {
 `kECSPI_PolarityActiveHigh` = 0x0U,
 `kECSPI_PolarityActiveLow` }
ECSPI clock polarity configuration.
- enum `ecspi_clock_phase_t` {
 `kECSPI_ClockPhaseFirstEdge`,
 `kECSPI_ClockPhaseSecondEdge` }
ECSPI clock phase configuration.
- enum {
 `kECSPI_TxfifoEmptyInterruptEnable` = ECSPI_INTREG_TEEN_MASK,
 `kECSPI_TxFifoDataRequestInterruptEnable` = ECSPI_INTREG_TDREN_MASK,
 `kECSPI_TxFifoFullInterruptEnable` = ECSPI_INTREG_TFEN_MASK,
 `kECSPI_RxFifoReadyInterruptEnable` = ECSPI_INTREG_RREN_MASK,
 `kECSPI_RxFifoDataRequestInterruptEnable` = ECSPI_INTREG_RDREN_MASK,
 `kECSPI_RxFifoFullInterruptEnable` = ECSPI_INTREG_RFEN_MASK,
 `kECSPI_RxFifoOverflowInterruptEnable` = ECSPI_INTREG_ROEN_MASK,
 `kECSPI_TransferCompleteInterruptEnable` = ECSPI_INTREG_TCEN_MASK,

`kECSPI_AllInterruptEnable` }

ECSPI interrupt sources.

- enum {
`kECSPI_TxFifoEmptyFlag` = `ECSPI_STATREG_TE_MASK`,
`kECSPI_TxFifoDataRequestFlag` = `ECSPI_STATREG_TDR_MASK`,
`kECSPI_TxFifoFullFlag` = `ECSPI_STATREG_TF_MASK`,
`kECSPI_RxFifoReadyFlag` = `ECSPI_STATREG_RR_MASK`,
`kECSPI_RxFifoDataRequestFlag` = `ECSPI_STATREG_RDR_MASK`,
`kECSPI_RxFifoFullFlag` = `ECSPI_STATREG_RF_MASK`,
`kECSPI_RxFifoOverflowFlag` = `ECSPI_STATREG_RO_MASK`,
`kECSPI_TransferCompleteFlag` = `ECSPI_STATREG_TC_MASK` }

ECSPI status flags.

- enum {
`kECSPI_TxDmaEnable` = `ECSPI_DMAREG_TEDEN_MASK`,
`kECSPI_RxDmaEnable` = `ECSPI_DMAREG_RXDEN_MASK`,
`kECSPI_DmaAllEnable` = (`ECSPI_DMAREG_TEDEN_MASK` | `ECSPI_DMAREG_RXDEN_MASK`) }

ECSPI DMA enable.

- enum `ecspi_Data_ready_t` {
`kECSPI_DataReadyIgnore` = `0x0U`,
`kECSPI_DataReadyFallingEdge`,
`kECSPI_DataReadyLowLevel` }

ECSPI SPI_RDY signal configuration.

- enum `ecspi_channel_source_t` {
`kECSPI_Channel0` = `0x0U`,
`kECSPI_Channel1`,
`kECSPI_Channel2`,
`kECSPI_Channel3` }

ECSPI channel select source.

- enum `ecspi_master_slave_mode_t` {
`kECSPI_Slave` = `0U`,
`kECSPI_Master` }

ECSPI master or slave mode configuration.

- enum `ecspi_data_line_inactive_state_t` {
`kECSPI_DataLineInactiveStateHigh` = `0x0U`,
`kECSPI_DataLineInactiveStateLow` }

ECSPI data line inactive state configuration.

- enum `ecspi_clock_inactive_state_t` {
`kECSPI_ClockInactiveStateLow` = `0x0U`,
`kECSPI_ClockInactiveStateHigh` }

ECSPI clock inactive state configuration.

- enum `ecspi_chip_select_active_state_t` {
`kECSPI_ChipSelectActiveStateLow` = `0x0U`,
`kECSPI_ChipSelectActiveStateHigh` }

ECSPI active state configuration.

- enum `ecspi_sample_period_clock_source_t` {
`kECSPI_spiClock` = `0x0U`,

`kECSPI_lowFreqClock` }
ECSPI sample period clock configuration.

Functions

- `uint32_t ECSPI_GetInstance` (ECSPI_Type *base)
Get the instance for ECSPI module.

Driver version

- `#define FSL_ECSPI_DRIVER_VERSION` (MAKE_VERSION(2, 2, 0))
ECSPI driver version.

Initialization and deinitialization

- `void ECSPI_MasterGetDefaultConfig` (ecspi_master_config_t *config)
Sets the ECSPI configuration structure to default values.
- `void ECSPI_MasterInit` (ECSPI_Type *base, const ecspi_master_config_t *config, uint32_t src-Clock_Hz)
Initializes the ECSPI with configuration.
- `void ECSPI_SlaveGetDefaultConfig` (ecspi_slave_config_t *config)
Sets the ECSPI configuration structure to default values.
- `void ECSPI_SlaveInit` (ECSPI_Type *base, const ecspi_slave_config_t *config)
Initializes the ECSPI with configuration.
- `void ECSPI_Deinit` (ECSPI_Type *base)
De-initializes the ECSPI.
- `static void ECSPI_Enable` (ECSPI_Type *base, bool enable)
Enables or disables the ECSPI.

Status

- `static uint32_t ECSPI_GetStatusFlags` (ECSPI_Type *base)
Gets the status flag.
- `static void ECSPI_ClearStatusFlags` (ECSPI_Type *base, uint32_t mask)
Clear the status flag.

Interrupts

- `static void ECSPI_EnableInterrupts` (ECSPI_Type *base, uint32_t mask)
Enables the interrupt for the ECSPI.
- `static void ECSPI_DisableInterrupts` (ECSPI_Type *base, uint32_t mask)
Disables the interrupt for the ECSPI.

Software Reset

- static void [ECSPI_SoftwareReset](#) (ECSPI_Type *base)
Software reset.

Channel mode check

- static bool [ECSPI_IsMaster](#) (ECSPI_Type *base, [ecspi_channel_source_t](#) channel)
Mode check.

DMA Control

- static void [ECSPI_EnableDMA](#) (ECSPI_Type *base, uint32_t mask, bool enable)
Enables the DMA source for ECSPI.

FIFO Operation

- static uint8_t [ECSPI_GetTxFifoCount](#) (ECSPI_Type *base)
Get the Tx FIFO data count.
- static uint8_t [ECSPI_GetRxFifoCount](#) (ECSPI_Type *base)
Get the Rx FIFO data count.

Bus Operations

- static void [ECSPI_SetChannelSelect](#) (ECSPI_Type *base, [ecspi_channel_source_t](#) channel)
Set channel select for transfer.
- void [ECSPI_SetChannelConfig](#) (ECSPI_Type *base, [ecspi_channel_source_t](#) channel, const [ecspi_channel_config_t](#) *config)
Set channel select configuration for transfer.
- void [ECSPI_SetBaudRate](#) (ECSPI_Type *base, uint32_t baudRate_Bps, uint32_t srcClock_Hz)
Sets the baud rate for ECSPI transfer.
- [status_t](#) [ECSPI_WriteBlocking](#) (ECSPI_Type *base, uint32_t *buffer, size_t size)
Sends a buffer of data bytes using a blocking method.
- static void [ECSPI_WriteData](#) (ECSPI_Type *base, uint32_t data)
Writes a data into the ECSPI data register.
- static uint32_t [ECSPI_ReadData](#) (ECSPI_Type *base)
Gets a data from the ECSPI data register.

Transactional

- void [ECSPI_MasterTransferCreateHandle](#) (ECSPI_Type *base, [ecspi_master_handle_t](#) *handle, [ecspi_master_callback_t](#) callback, void *userData)
Initializes the ECSPI master handle.
- [status_t](#) [ECSPI_MasterTransferBlocking](#) (ECSPI_Type *base, [ecspi_transfer_t](#) *xfer)

- Transfers a block of data using a polling method.
- [status_t ECSPI_MasterTransferNonBlocking](#) (ECSPI_Type *base, [ecspi_master_handle_t](#) *handle, [ecspi_transfer_t](#) *xfer)
- Performs a non-blocking ECSPI interrupt transfer.
- [status_t ECSPI_MasterTransferGetCount](#) (ECSPI_Type *base, [ecspi_master_handle_t](#) *handle, [size_t](#) *count)
- Gets the bytes of the ECSPI interrupt transferred.
- void [ECSPI_MasterTransferAbort](#) (ECSPI_Type *base, [ecspi_master_handle_t](#) *handle)
- Aborts an ECSPI transfer using interrupt.
- void [ECSPI_MasterTransferHandleIRQ](#) (ECSPI_Type *base, [ecspi_master_handle_t](#) *handle)
- Interrupts the handler for the ECSPI.
- void [ECSPI_SlaveTransferCreateHandle](#) (ECSPI_Type *base, [ecspi_slave_handle_t](#) *handle, [ecspi_slave_callback_t](#) callback, void *userData)
- Initializes the ECSPI slave handle.
- static [status_t ECSPI_SlaveTransferNonBlocking](#) (ECSPI_Type *base, [ecspi_slave_handle_t](#) *handle, [ecspi_transfer_t](#) *xfer)
- Performs a non-blocking ECSPI slave interrupt transfer.
- static [status_t ECSPI_SlaveTransferGetCount](#) (ECSPI_Type *base, [ecspi_slave_handle_t](#) *handle, [size_t](#) *count)
- Gets the bytes of the ECSPI interrupt transferred.
- static void [ECSPI_SlaveTransferAbort](#) (ECSPI_Type *base, [ecspi_slave_handle_t](#) *handle)
- Aborts an ECSPI slave transfer using interrupt.
- void [ECSPI_SlaveTransferHandleIRQ](#) (ECSPI_Type *base, [ecspi_slave_handle_t](#) *handle)
- Interrupts a handler for the ECSPI slave.

9.2.3 Data Structure Documentation

9.2.3.1 struct [ecspi_channel_config_t](#)

Data Fields

- [ecspi_master_slave_mode_t](#) channelMode
Channel mode.
- [ecspi_clock_inactive_state_t](#) clockInactiveState
Clock line (SCLK) inactive state.
- [ecspi_data_line_inactive_state_t](#) dataLineInactiveState
Data line (MOSI&MISO) inactive state.
- [ecspi_chip_select_active_state_t](#) chipSlectActiveState
Chip select(SS) line active state.
- [ecspi_clock_polarity_t](#) polarity
Clock polarity.
- [ecspi_clock_phase_t](#) phase
Clock phase.

9.2.3.2 struct ecspi_master_config_t

Data Fields

- [ecspi_channel_source_t channel](#)
Channel number.
- [ecspi_channel_config_t channelConfig](#)
Channel configuration.
- [ecspi_sample_period_clock_source_t samplePeriodClock](#)
Sample period clock source.
- [uint8_t burstLength](#)
Burst length.
- [uint8_t chipSelectDelay](#)
SS delay time.
- [uint16_t samplePeriod](#)
Sample period.
- [uint8_t txFifoThreshold](#)
TX Threshold.
- [uint8_t rxFifoThreshold](#)
RX Threshold.
- [uint32_t baudRate_Bps](#)
ECSPI baud rate for master mode.
- [bool enableLoopback](#)
Enable the ECSPI loopback test.

Field Documentation

(1) [bool ecspi_master_config_t::enableLoopback](#)

9.2.3.3 struct ecspi_slave_config_t

Data Fields

- [uint8_t burstLength](#)
Burst length.
- [uint8_t txFifoThreshold](#)
TX Threshold.
- [uint8_t rxFifoThreshold](#)
RX Threshold.
- [ecspi_channel_config_t channelConfig](#)
Channel configuration.

9.2.3.4 struct ecspi_transfer_t

Data Fields

- [uint32_t * txData](#)
Send buffer.
- [uint32_t * rxData](#)
Receive buffer.

- `size_t dataSize`
Transfer bytes.
- `ecspi_channel_source_t channel`
ECSPI channel select.

9.2.3.5 struct _ecspi_master_handle

Data Fields

- `ecspi_channel_source_t channel`
Channel number.
- `uint32_t *volatile txData`
Transfer buffer.
- `uint32_t *volatile rxData`
Receive buffer.
- `volatile size_t txRemainingBytes`
Send data remaining in bytes.
- `volatile size_t rxRemainingBytes`
Receive data remaining in bytes.
- `volatile uint32_t state`
ECSPI internal state.
- `size_t transferSize`
Bytes to be transferred.
- `ecspi_master_callback_t callback`
ECSPI callback.
- `void * userData`
Callback parameter.

9.2.4 Macro Definition Documentation

9.2.4.1 **#define FSL_ECSPi_DRIVER_VERSION (MAKE_VERSION(2, 2, 0))**

9.2.4.2 **#define ECSPi_DUMMYDATA (0xFFFFFFFFFU)**

9.2.4.3 **#define SPI_RETRY_TIMES 0U /* Define to zero means keep waiting until the flag is assert/deassert. */**

9.2.5 Enumeration Type Documentation

9.2.5.1 anonymous enum

Enumerator

kStatus_ECSPi_Busy ECSPI bus is busy.
kStatus_ECSPi_Idle ECSPI is idle.
kStatus_ECSPi_Error ECSPI error.

kStatus_ECSPI_HardwareOverflow ECSPI hardware overflow.

kStatus_ECSPI_Timeout ECSPI timeout polling status flags.

9.2.5.2 enum ecspi_clock_polarity_t

Enumerator

kECSPI_PolarityActiveHigh Active-high ECSPI polarity high (idles low).

kECSPI_PolarityActiveLow Active-low ECSPI polarity low (idles high).

9.2.5.3 enum ecspi_clock_phase_t

Enumerator

kECSPI_ClockPhaseFirstEdge First edge on SPCK occurs at the middle of the first cycle of a data transfer.

kECSPI_ClockPhaseSecondEdge First edge on SPCK occurs at the start of the first cycle of a data transfer.

9.2.5.4 anonymous enum

Enumerator

kECSPI_TxfifoEmptyInterruptEnable Transmit FIFO buffer empty interrupt.

kECSPI_TxFifoDataRequestInterruptEnable Transmit FIFO data request interrupt.

kECSPI_TxFifoFullInterruptEnable Transmit FIFO full interrupt.

kECSPI_RxFifoReadyInterruptEnable Receiver FIFO ready interrupt.

kECSPI_RxFifoDataRequestInterruptEnable Receiver FIFO data request interrupt.

kECSPI_RxFifoFullInterruptEnable Receiver FIFO full interrupt.

kECSPI_RxFifoOverflowInterruptEnable Receiver FIFO buffer overflow interrupt.

kECSPI_TransferCompleteInterruptEnable Transfer complete interrupt.

kECSPI_AllInterruptEnable All interrupt.

9.2.5.5 anonymous enum

Enumerator

kECSPI_TxfifoEmptyFlag Transmit FIFO buffer empty flag.

kECSPI_TxFifoDataRequestFlag Transmit FIFO data request flag.

kECSPI_TxFifoFullFlag Transmit FIFO full flag.

kECSPI_RxFifoReadyFlag Receiver FIFO ready flag.

kECSPI_RxFifoDataRequestFlag Receiver FIFO data request flag.

kECSPI_RxFifoFullFlag Receiver FIFO full flag.

kECSPI_RxFifoOverflowFlag Receiver FIFO buffer overflow flag.

kECSPI_TransferCompleteFlag Transfer complete flag.

9.2.5.6 anonymous enum

Enumerator

kECSPI_TxDmaEnable Tx DMA request source.
kECSPI_RxDmaEnable Rx DMA request source.
kECSPI_DmaAllEnable All DMA request source.

9.2.5.7 enum ecspi_Data_ready_t

Enumerator

kECSPI_DataReadyIgnore SPI_RDY signal is ignored.
kECSPI_DataReadyFallingEdge SPI_RDY signal will be triggered by the falling edge.
kECSPI_DataReadyLowLevel SPI_RDY signal will be triggered by a low level.

9.2.5.8 enum ecspi_channel_source_t

Enumerator

kECSPI_Channel0 Channel 0 is selected.
kECSPI_Channel1 Channel 1 is selected.
kECSPI_Channel2 Channel 2 is selected.
kECSPI_Channel3 Channel 3 is selected.

9.2.5.9 enum ecspi_master_slave_mode_t

Enumerator

kECSPI_Slave ECSPI peripheral operates in slave mode.
kECSPI_Master ECSPI peripheral operates in master mode.

9.2.5.10 enum ecspi_data_line_inactive_state_t

Enumerator

kECSPI_DataLineInactiveStateHigh The data line inactive state stays high.
kECSPI_DataLineInactiveStateLow The data line inactive state stays low.

9.2.5.11 enum ecspi_clock_inactive_state_t

Enumerator

kECSPI_ClockInactiveStateLow The SCLK inactive state stays low.

kECSPI_ClockInactiveStateHigh The SCLK inactive state stays high.

9.2.5.12 enum ecspi_chip_select_active_state_t

Enumerator

kECSPI_ChipSelectActiveStateLow The SS signal line active stays low.

kECSPI_ChipSelectActiveStateHigh The SS signal line active stays high.

9.2.5.13 enum ecspi_sample_period_clock_source_t

Enumerator

kECSPI_spiClock The sample period clock source is SCLK.

kECSPI_lowFreqClock The sample period clock source is low_frequency reference clock(32.768 kHz).

9.2.6 Function Documentation

9.2.6.1 uint32_t ECSPI_GetInstance (ECSPI_Type * *base*)

Parameters

<i>base</i>	ECSPI base address
-------------	--------------------

9.2.6.2 void ECSPI_MasterGetDefaultConfig (ecspi_master_config_t * *config*)

The purpose of this API is to get the configuration structure initialized for use in [ECSPI_MasterInit\(\)](#). User may use the initialized structure unchanged in ECSPI_MasterInit, or modify some fields of the structure before calling ECSPI_MasterInit. After calling this API, the master is ready to transfer. Example:

```
ecspi_master_config_t config;
ECSPI_MasterGetDefaultConfig(&config);
```

Parameters

<i>config</i>	pointer to config structure
---------------	-----------------------------

9.2.6.3 void ECSPI_MasterInit (ECSPI_Type * *base*, const *ecspi_master_config_t* * *config*, *uint32_t srcClock_Hz*)

The configuration structure can be filled by user from scratch, or be set with default values by [ECSPI_MasterGetDefaultConfig\(\)](#). After calling this API, the slave is ready to transfer. Example

```
ecspi_master_config_t config = {
    .baudRate_Bps = 400000,
    ...
};
ECSPI_MasterInit(ECSPI0, &config);
```

Parameters

<i>base</i>	ECSPI base pointer
<i>config</i>	pointer to master configuration structure
<i>srcClock_Hz</i>	Source clock frequency.

9.2.6.4 void ECSPI_SlaveGetDefaultConfig (*ecspi_slave_config_t* * *config*)

The purpose of this API is to get the configuration structure initialized for use in [ECSPI_SlaveInit\(\)](#). User may use the initialized structure unchanged in [ECSPI_SlaveInit\(\)](#), or modify some fields of the structure before calling [ECSPI_SlaveInit\(\)](#). After calling this API, the master is ready to transfer. Example:

```
ecspi_slaveconfig_t config;
ECSPI_SlaveGetDefaultConfig(&config);
```

Parameters

<i>config</i>	pointer to config structure
---------------	-----------------------------

9.2.6.5 void ECSPI_SlaveInit (ECSPI_Type * *base*, const *ecspi_slave_config_t* * *config*)

The configuration structure can be filled by user from scratch, or be set with default values by [ECSPI_SlaveGetDefaultConfig\(\)](#). After calling this API, the slave is ready to transfer. Example

```
ecspi_slaveconfig_t config = {
    .baudRate_Bps = 400000,
    ...
};
ECSPI_SlaveInit(ECSPI1, &config);
```

Parameters

<i>base</i>	ECSPI base pointer
<i>config</i>	pointer to master configuration structure

9.2.6.6 void ECSPI_Deinit (ECSPI_Type * *base*)

Calling this API resets the ECSPI module, gates the ECSPI clock. The ECSPI module can't work unless calling the ECSPI_MasterInit/ECSPI_SlaveInit to initialize module.

Parameters

<i>base</i>	ECSPI base pointer
-------------	--------------------

9.2.6.7 static void ECSPI_Enable (ECSPI_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	ECSPI base pointer
<i>enable</i>	pass true to enable module, false to disable module

9.2.6.8 static uint32_t ECSPI_GetStatusFlags (ECSPI_Type * *base*) [inline], [static]

Parameters

<i>base</i>	ECSPI base pointer
-------------	--------------------

Returns

ECSPI Status, use status flag to AND _ecspi_flags could get the related status.

9.2.6.9 static void ECSPI_ClearStatusFlags (ECSPI_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	ECSPI base pointer
<i>mask</i>	ECSPI Status, use status flag to AND _ecspi_flags could get the related status.

9.2.6.10 static void ECSPI_EnableInterrupts (ECSPI_Type * *base*, uint32_t *mask*)
[inline], [static]

Parameters

<i>base</i>	ECSPI base pointer
<i>mask</i>	ECSPI interrupt source. The parameter can be any combination of the following values: <ul style="list-style-type: none"> • kECSPI_TxfifoEmptyInterruptEnable • kECSPI_TxFifoDataRequestInterruptEnable • kECSPI_TxFifoFullInterruptEnable • kECSPI_RxFifoReadyInterruptEnable • kECSPI_RxFifoDataRequestInterruptEnable • kECSPI_RxFifoFullInterruptEnable • kECSPI_RxFifoOverflowInterruptEnable • kECSPI_TransferCompleteInterruptEnable • kECSPI_AllInterruptEnable

9.2.6.11 static void ECSPI_DisableInterrupts (ECSPI_Type * *base*, uint32_t *mask*)
[inline], [static]

Parameters

<i>base</i>	ECSPI base pointer
<i>mask</i>	ECSPI interrupt source. The parameter can be any combination of the following values: <ul style="list-style-type: none"> • kECSPI_TxfifoEmptyInterruptEnable • kECSPI_TxFifoDataRequestInterruptEnable • kECSPI_TxFifoFullInterruptEnable • kECSPI_RxFifoReadyInterruptEnable • kECSPI_RxFifoDataRequestInterruptEnable • kECSPI_RxFifoFullInterruptEnable • kECSPI_RxFifoOverflowInterruptEnable • kECSPI_TransferCompleteInterruptEnable • kECSPI_AllInterruptEnable

9.2.6.12 static void ECSPI_SoftwareReset (ECSPI_Type * *base*) [inline],
[static]

Parameters

<i>base</i>	ECSPI base pointer
-------------	--------------------

9.2.6.13 static bool ECSPI_IsMaster (ECSPI_Type * *base*, ecspi_channel_source_t
***channel*) [inline], [static]**

Parameters

<i>base</i>	ECSPI base pointer
<i>channel</i>	ECSPI channel source

Returns

mode of channel

9.2.6.14 static void ECSPI_EnableDMA (ECSPI_Type * *base*, uint32_t *mask*, bool *enable*
) [inline], [static]

Parameters

<i>base</i>	ECSPI base pointer
<i>mask</i>	ECSPI DMA source. The parameter can be any of the following values: <ul style="list-style-type: none"> • kECSPI_TxDmaEnable • kECSPI_RxDmaEnable • kECSPI_DmaAllEnable
<i>enable</i>	True means enable DMA, false means disable DMA

9.2.6.15 static uint8_t ECSPI_GetTxFifoCount (ECSPI_Type * *base*) [inline], [static]

Parameters

<i>base</i>	ECSPI base pointer.
-------------	---------------------

Returns

the number of words in Tx FIFO buffer.

9.2.6.16 static uint8_t ECSPI_GetRxFifoCount (ECSPI_Type * *base*) [inline], [static]

Parameters

<i>base</i>	ECSPI base pointer.
-------------	---------------------

Returns

the number of words in Rx FIFO buffer.

9.2.6.17 static void ECSPI_SetChannelSelect (ECSPI_Type * *base*, ecspi_channel_source_t *channel*) [inline], [static]

Parameters

<i>base</i>	ECSPI base pointer
<i>channel</i>	Channel source.

9.2.6.18 void ECSPI_SetChannelConfig (ECSPI_Type * *base*, *ecspi_channel_source_t* *channel*, const *ecspi_channel_config_t* * *config*)

The purpose of this API is to set the channel will be use to transfer. User may use this API after instance has been initialized or before transfer start. The configuration structure *ecspi_channel_config* can be filled by user from scratch. After calling this API, user can select this channel as transfer channel.

Parameters

<i>base</i>	ECSPI base pointer
<i>channel</i>	Channel source.
<i>config</i>	Configuration struct of channel

9.2.6.19 void ECSPI_SetBaudRate (ECSPI_Type * *base*, *uint32_t* *baudRate_Bps*, *uint32_t* *srcClock_Hz*)

This is only used in master.

Parameters

<i>base</i>	ECSPI base pointer
<i>baudRate_Bps</i>	baud rate needed in Hz.
<i>srcClock_Hz</i>	ECSPI source clock frequency in Hz.

9.2.6.20 *status_t* ECSPI_WriteBlocking (ECSPI_Type * *base*, *uint32_t* * *buffer*, *size_t* *size*)

Note

This function blocks via polling until all bytes have been sent.

Parameters

<i>base</i>	ECSPI base pointer
<i>buffer</i>	The data bytes to send
<i>size</i>	The number of data bytes to send

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_ECSPI_Timeout</i>	The transfer timed out and was aborted.

9.2.6.21 static void ECSPI_WriteData (ECSPI_Type * *base*, uint32_t *data*) [inline], [static]

Parameters

<i>base</i>	ECSPI base pointer
<i>data</i>	Data needs to be write.

9.2.6.22 static uint32_t ECSPI_ReadData (ECSPI_Type * *base*) [inline], [static]

Parameters

<i>base</i>	ECSPI base pointer
-------------	--------------------

Returns

Data in the register.

**9.2.6.23 void ECSPI_MasterTransferCreateHandle (ECSPI_Type * *base*,
ecspi_master_handle_t * *handle*, ecspi_master_callback_t *callback*, void *
userData)**

This function initializes the ECSPI master handle which can be used for other ECSPI master transactional APIs. Usually, for a specified ECSPI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	ECSPI handle pointer.
<i>callback</i>	Callback function.
<i>userData</i>	User data.

9.2.6.24 **status_t** **ECSPI_MasterTransferBlocking** (**ECSPI_Type** * *base*, **ecspi_transfer_t** * *xfer*)

Parameters

<i>base</i>	SPI base pointer
<i>xfer</i>	pointer to spi_xfer_config_t structure

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_ECSPi_Timeout</i>	The transfer timed out and was aborted.

9.2.6.25 **status_t** **ECSPI_MasterTransferNonBlocking** (**ECSPI_Type** * *base*, **ecspi_master_handle_t** * *handle*, **ecspi_transfer_t** * *xfer*)

Note

The API immediately returns after transfer initialization is finished.
If ECSPI transfer data frame size is 16 bits, the transfer size cannot be an odd number.

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	pointer to ecspi_master_handle_t structure which stores the transfer state
<i>xfer</i>	pointer to ecspi_transfer_t structure

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_ECSPi_Busy</i>	ECSPI is not idle, is running another transfer.

9.2.6.26 **status_t ECSPI_MasterTransferGetCount (ECSPI_Type * *base*, ecspi_master_handle_t * *handle*, size_t * *count*)**

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	Pointer to ECSPI transfer handle, this should be a static variable.
<i>count</i>	Transferred bytes of ECSPI master.

Return values

<i>kStatus_ECSPi_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferInProgress</i>	There is not a non-blocking transaction currently in progress.

9.2.6.27 **void ECSPI_MasterTransferAbort (ECSPI_Type * *base*, ecspi_master_handle_t * *handle*)**

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	Pointer to ECSPI transfer handle, this should be a static variable.

9.2.6.28 **void ECSPI_MasterTransferHandleIRQ (ECSPI_Type * *base*, ecspi_master_handle_t * *handle*)**

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	pointer to <code>ecspi_master_handle_t</code> structure which stores the transfer state.

**9.2.6.29 void ECSPISlaveTransferCreateHandle (ECSPISlaveType * *base*,
ecspi_slave_handle_t * *handle*, ecspi_slave_callback_t *callback*, void * *userData*
)**

This function initializes the ECSPI slave handle which can be used for other ECSPI slave transactional APIs. Usually, for a specified ECSPI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	ECSPI handle pointer.
<i>callback</i>	Callback function.
<i>userData</i>	User data.

**9.2.6.30 static status_t ECSPISlaveTransferNonBlocking (ECSPISlaveType * *base*,
ecspi_slave_handle_t * *handle*, ecspi_transfer_t * *xfer*) [inline], [static]**

Note

The API returns immediately after the transfer initialization is finished.

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	pointer to <code>ecspi_master_handle_t</code> structure which stores the transfer state
<i>xfer</i>	pointer to ecspi_transfer_t structure

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_ECSPISlave_Busy</i>	ECSPI is not idle, is running another transfer.

**9.2.6.31 static status_t ECSPISlaveTransferGetCount (ECSPISlaveType * *base*,
ecspi_slave_handle_t * *handle*, size_t * *count*) [inline], [static]**

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	Pointer to ECSPI transfer handle, this should be a static variable.
<i>count</i>	Transferred bytes of ECSPI slave.

Return values

<i>kStatus_ECSPI_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferInProgress</i>	There is not a non-blocking transaction currently in progress.

**9.2.6.32 static void ECSPI_SlaveTransferAbort (ECSPI_Type * *base*,
ecspi_slave_handle_t * *handle*) [inline], [static]**

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	Pointer to ECSPI transfer handle, this should be a static variable.

9.2.6.33 void ECSPI_SlaveTransferHandleIRQ (ECSPI_Type * *base*, ecspi_slave_handle_t * *handle*)

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	pointer to ecspi_slave_handle_t structure which stores the transfer state

9.3 ECSPI FreeRTOS Driver

9.3.1 Overview

Driver version

- #define `FSL_ECSPI_FREERTOS_DRIVER_VERSION` (`MAKE_VERSION(2, 2, 0)`)
ECSPI FreeRTOS driver version.

ECSPI RTOS Operation

- `status_t ECSPI_RTOS_Init` (`ecspi_rtos_handle_t *handle`, `ECSPI_Type *base`, `const ecspi_master_config_t *masterConfig`, `uint32_t srcClock_Hz`)
Initializes ECSPI.
- `status_t ECSPI_RTOS_Deinit` (`ecspi_rtos_handle_t *handle`)
Deinitializes the ECSPI.
- `status_t ECSPI_RTOS_Transfer` (`ecspi_rtos_handle_t *handle`, `ecspi_transfer_t *transfer`)
Performs ECSPI transfer.

9.3.2 Macro Definition Documentation

9.3.2.1 #define FSL_ECSPI_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 2, 0))

9.3.3 Function Documentation

9.3.3.1 `status_t ECSPI_RTOS_Init (ecspi_rtos_handle_t * handle, ECSPI_Type * base, const ecspi_master_config_t * masterConfig, uint32_t srcClock_Hz)`

This function initializes the ECSPI module and related RTOS context.

Parameters

<i>handle</i>	The RTOS ECSPI handle, the pointer to an allocated space for RTOS context.
<i>base</i>	The pointer base address of the ECSPI instance to initialize.
<i>masterConfig</i>	Configuration structure to set-up ECSPI in master mode.
<i>srcClock_Hz</i>	Frequency of input clock of the ECSPI module.

Returns

status of the operation.

9.3.3.2 `status_t ECSPI_RTOS_Deinit (ecspi_rtos_handle_t * handle)`

This function deinitializes the ECSPI module and related RTOS context.

Parameters

<i>handle</i>	The RTOS ECSPI handle.
---------------	------------------------

9.3.3.3 `status_t ECSPI_RTOS_Transfer (ecspi_rtos_handle_t * handle, ecspi_transfer_t * transfer)`

This function performs an ECSPI transfer according to data given in the transfer structure.

Parameters

<i>handle</i>	The RTOS ECSPI handle.
<i>transfer</i>	Structure specifying the transfer parameters.

Returns

status of the operation.

9.4 ECSPI SDMA Driver

9.4.1 Overview

Data Structures

- struct [ecspi_sdma_handle_t](#)
ECSPI SDMA transfer handle, users should not touch the content of the handle. [More...](#)

Typedefs

- typedef void(* [ecspi_sdma_callback_t](#))(ECSPI_Type *base, ecspi_sdma_handle_t *handle, [status_t](#) status, void *userData)
ECSPI SDMA callback called at the end of transfer.

Driver version

- #define [FSL_ECSPI_FREERTOS_DRIVER_VERSION](#) (MAKE_VERSION(2, 2, 0))
ECSPI FreeRTOS driver version.

DMA Transactional

- void [ECSPI_MasterTransferCreateHandleSDMA](#) (ECSPI_Type *base, ecspi_sdma_handle_t *handle, [ecspi_sdma_callback_t](#) callback, void *userData, [sdma_handle_t](#) *txHandle, [sdma_handle_t](#) *rxHandle, uint32_t eventSourceTx, uint32_t eventSourceRx, uint32_t TxChannel, uint32_t RxChannel)
Initialize the ECSPI master SDMA handle.
- void [ECSPI_SlaveTransferCreateHandleSDMA](#) (ECSPI_Type *base, ecspi_sdma_handle_t *handle, [ecspi_sdma_callback_t](#) callback, void *userData, [sdma_handle_t](#) *txHandle, [sdma_handle_t](#) *rxHandle, uint32_t eventSourceTx, uint32_t eventSourceRx, uint32_t TxChannel, uint32_t RxChannel)
Initialize the ECSPI slave SDMA handle.
- [status_t](#) [ECSPI_MasterTransferSDMA](#) (ECSPI_Type *base, ecspi_sdma_handle_t *handle, [ecspi_transfer_t](#) *xfer)
Perform a non-blocking ECSPI master transfer using SDMA.
- [status_t](#) [ECSPI_SlaveTransferSDMA](#) (ECSPI_Type *base, ecspi_sdma_handle_t *handle, [ecspi_transfer_t](#) *xfer)
Perform a non-blocking ECSPI slave transfer using SDMA.
- void [ECSPI_MasterTransferAbortSDMA](#) (ECSPI_Type *base, ecspi_sdma_handle_t *handle)
Abort a ECSPI master transfer using SDMA.
- void [ECSPI_SlaveTransferAbortSDMA](#) (ECSPI_Type *base, ecspi_sdma_handle_t *handle)
Abort a ECSPI slave transfer using SDMA.

9.4.2 Data Structure Documentation

9.4.2.1 struct _ecspi_sdma_handle

Data Fields

- bool [txInProgress](#)
Send transfer finished.
- bool [rxInProgress](#)
Receive transfer finished.
- [sdma_handle_t](#) * [txSdmaHandle](#)
DMA handler for ECSPI send.
- [sdma_handle_t](#) * [rxSdmaHandle](#)
DMA handler for ECSPI receive.
- [ecspi_sdma_callback_t](#) [callback](#)
Callback for ECSPI SDMA transfer.
- void * [userData](#)
User Data for ECSPI SDMA callback.
- uint32_t [state](#)
Internal state of ECSPI SDMA transfer.
- uint32_t [ChannelTx](#)
Channel for send handle.
- uint32_t [ChannelRx](#)
Channel for receive handler.

9.4.3 Macro Definition Documentation

9.4.3.1 #define FSL_ECSPi_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 2, 0))

9.4.4 Typedef Documentation

9.4.4.1 typedef void(* ecspi_sdma_callback_t)(ECSPi_Type *base, ecspi_sdma_handle_t *handle, status_t status, void *userData)

9.4.5 Function Documentation

9.4.5.1 void ECSPi_MasterTransferCreateHandleSDMA (ECSPi_Type * base, ecspi_sdma_handle_t * handle, ecspi_sdma_callback_t callback, void * userData, sdma_handle_t * txHandle, sdma_handle_t * rxHandle, uint32_t eventSourceTx, uint32_t eventSourceRx, uint32_t TxChannel, uint32_t RxChannel)

This function initializes the ECSPI master SDMA handle which can be used for other SPI master transactional APIs. Usually, for a specified ECSPI instance, user need only call this API once to get the initialized handle.

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	ECSPI handle pointer.
<i>callback</i>	User callback function called at the end of a transfer.
<i>userData</i>	User data for callback.
<i>txHandle</i>	SDMA handle pointer for ECSPI Tx, the handle shall be static allocated by users.
<i>rxHandle</i>	SDMA handle pointer for ECSPI Rx, the handle shall be static allocated by users.
<i>eventSourceTx</i>	event source for ECSPI send, which can be found in SDMA mapping.
<i>eventSourceRx</i>	event source for ECSPI receive, which can be found in SDMA mapping.
<i>TxChannel</i>	SDMA channel for ECSPI send.
<i>RxChannel</i>	SDMA channel for ECSPI receive.

**9.4.5.2 void ECSPI_SlaveTransferCreateHandleSDMA (ECSPI_Type * *base*,
 ecspi_sdma_handle_t * *handle*, ecspi_sdma_callback_t *callback*, void * *userData*,
 sdma_handle_t * *txHandle*, sdma_handle_t * *rxHandle*, uint32_t *eventSourceTx*,
 uint32_t *eventSourceRx*, uint32_t *TxChannel*, uint32_t *RxChannel*)**

This function initializes the ECSPI Slave SDMA handle which can be used for other SPI Slave transactional APIs. Usually, for a specified ECSPI instance, user need only call this API once to get the initialized handle.

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	ECSPI handle pointer.
<i>callback</i>	User callback function called at the end of a transfer.
<i>userData</i>	User data for callback.
<i>txHandle</i>	SDMA handle pointer for ECSPI Tx, the handle shall be static allocated by users.
<i>rxHandle</i>	SDMA handle pointer for ECSPI Rx, the handle shall be static allocated by users.
<i>eventSourceTx</i>	event source for ECSPI send, which can be found in SDMA mapping.
<i>eventSourceRx</i>	event source for ECSPI receive, which can be found in SDMA mapping.

<i>TxChannel</i>	SDMA channel for ECSPI send.
<i>RxChannel</i>	SDMA channel for ECSPI receive.

9.4.5.3 **status_t ECSPI_MasterTransferSDMA (ECSPI_Type * *base*, ecspi_sdma_handle_t * *handle*, ecspi_transfer_t * *xfer*)**

Note

This interface returned immediately after transfer initiates.

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	ECSPI SDMA handle pointer.
<i>xfer</i>	Pointer to sdma transfer structure.

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_ECSPI_Busy</i>	EECSPI is not idle, is running another transfer.

9.4.5.4 **status_t ECSPI_SlaveTransferSDMA (ECSPI_Type * *base*, ecspi_sdma_handle_t * *handle*, ecspi_transfer_t * *xfer*)**

Note

This interface returned immediately after transfer initiates.

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	ECSPI SDMA handle pointer.
<i>xfer</i>	Pointer to sdma transfer structure.

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_ECSPI_Busy</i>	EECSPI is not idle, is running another transfer.

9.4.5.5 void ECSPI_MasterTransferAbortSDMA (ECSPI_Type * *base*, ecsapi_sdma_handle_t * *handle*)

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	ECSPI SDMA handle pointer.

9.4.5.6 void ECSPI_SlaveTransferAbortSDMA (ECSPI_Type * *base*, ecsapi_sdma_handle_t * *handle*)

Parameters

<i>base</i>	ECSPI peripheral base address.
<i>handle</i>	ECSPI SDMA handle pointer.

9.5 ECSPI CMSIS Driver

This section describes the programming interface of the ecsapi Cortex Microcontroller Software Interface Standard (CMSIS) driver. And this driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method please refer to <http://www.keil.com/pack/doc/cmsis/Driver/html/index.html>.

9.5.1 Function groups

9.5.1.1 ECSPI CMSIS GetVersion Operation

This function group will return the ECSPI CMSIS Driver version to user.

9.5.1.2 ECSPI CMSIS GetCapabilities Operation

This function group will return the capabilities of this driver.

9.5.1.3 ECSPI CMSIS Initialize and Uninitialize Operation

This function will initialize and uninitialize the instance in master mode or slave mode. And this API must be called before you configure an instance or after you Deinit an instance. The right steps to start an instance is that you must initialize the instance which been selected firstly, then you can power on the instance. After these all have been done, you can configure the instance by using control operation. If you want to Uninitialize the instance, you must power off the instance first.

9.5.1.4 ECSPI CMSIS Transfer Operation

This function group controls the transfer, master send/receive data, and slave send/receive data.

9.5.1.5 ECSPI CMSIS Status Operation

This function group gets the ecsapi transfer status.

9.5.1.6 ECSPI CMSIS Control Operation

This function can select instance as master mode or slave mode, set baudrate for master mode transfer, get current baudrate of master mode transfer, set transfer data bits and set other control command.

9.5.2 Typical use case

9.5.2.1 Master Operation

```

/* Variables */
uint8_t masterRxData[TRANSFER_SIZE] = {0U};
uint8_t masterTxData[TRANSFER_SIZE] = {0U};

/*ECSPI master init*/
Driver_SPI0.Initialize(ECSPI_MasterSignalEvent_t);
Driver_SPI0.PowerControl(ARM_POWER_FULL);
Driver_SPI0.Control(ARM_SPI_MODE_MASTER, TRANSFER_BAUDRATE);

/* Start master transfer */
Driver_SPI0.Transfer(masterTxData, masterRxData, TRANSFER_SIZE);

/* Master power off */
Driver_SPI0.PowerControl(ARM_POWER_OFF);

/* Master uninitialized */
Driver_SPI0.Uninitialize();

```

9.5.2.2 Slave Operation

```

/* Variables */
uint8_t slaveRxData[TRANSFER_SIZE] = {0U};
uint8_t slaveTxData[TRANSFER_SIZE] = {0U};

/*DSPI slave init*/
Driver_SPI2.Initialize(ECSPI_SlaveSignalEvent_t);
Driver_SPI2.PowerControl(ARM_POWER_FULL);
Driver_SPI2.Control(ARM_SPI_MODE_SLAVE, false);

/* Start slave transfer */
Driver_SPI2.Transfer(slaveTxData, slaveRxData, TRANSFER_SIZE);

/* slave power off */
Driver_SPI2.PowerControl(ARM_POWER_OFF);

/* slave uninitialized */
Driver_SPI2.Uninitialize();

```

Chapter 10

GPC: General Power Controller Driver

10.1 Overview

The MCUXpresso SDK provides a peripheral driver for the General Power Controller (GPC) module of MCUXpresso SDK devices.

API functions are provided to configure the system about working in dedicated power mode. There are mainly about enabling the power for memory, enabling the wakeup sources for STOP modes, and power up/down operations for various peripherals.

Macros

- #define `GPC_PCG_TIME_SLOT_TOTAL_NUMBER` `GPC_SLT_CFG_PU_COUNT`
Total number of the timeslot.

Enumerations

- enum `_gpc_lpm_mode` {
 `kGPC_RunMode` = 0U,
 `kGPC_WaitMode` = 1U,
 `kGPC_StopMode` = 2U }
 GPC LPM mode definition.
- enum `_gpc_pgc_ack_sel` {
 `kGPC_DummyPGCPowerUpAck` = `GPC_PGC_ACK_SEL_DUMMY_PGC_PUP_ACK_MASK`,
 `kGPC_VirtualPGCPowerUpAck` = `GPC_PGC_ACK_SEL_VIRTUAL_PGC_PUP_ACK_MASK`,
 `kGPC_DummyPGCPowerDownAck` = `GPC_PGC_ACK_SEL_DUMMY_PGC_PDN_ACK_MASK`,
 `kGPC_VirtualPGCPowerDownAck` = `GPC_PGC_ACK_SEL_VIRTUAL_PGC_PDN_ACK_MASK`,
 `kGPC_NocPGCPowerUpAck` = `GPC_PGC_ACK_SEL_NOC_PGC_PUP_ACK`,
 `kGPC_NocPGCPowerDownAck` = `GPC_PGC_ACK_SEL_NOC_PGC_PDN_ACK` }
 PGC ack signal selection.
- enum `_gpc_standby_count` {
 `kGPC_StandbyCounter4CkilClk` = 0U,
 `kGPC_StandbyCounter8CkilClk` = 1U,
 `kGPC_StandbyCounter16CkilClk` = 2U,
 `kGPC_StandbyCounter32CkilClk` = 3U,
 `kGPC_StandbyCounter64CkilClk` = 4U,
 `kGPC_StandbyCounter128CkilClk` = 5U,
 `kGPC_StandbyCounter256CkilClk` = 6U,
 `kGPC_StandbyCounter512CkilClk` = 7U }

Standby counter which GPC will wait between PMIC_STBY_REQ negation and assertion of PMIC_READY.

Functions

- static void [GPC_AllowIRQs](#) (GPC_Type *base)
Allow all the IRQ/Events within the charge of GPC.
- static void [GPC_DisallowIRQs](#) (GPC_Type *base)
Disallow all the IRQ/Events within the charge of GPC.
- static uint32_t [GPC_GetLpmMode](#) (GPC_Type *base)
Get current LPM mode.
- void [GPC_EnableIRQ](#) (GPC_Type *base, uint32_t irqId)
Enable the IRQ.
- void [GPC_DisableIRQ](#) (GPC_Type *base, uint32_t irqId)
Disable the IRQ.
- bool [GPC_GetIRQStatusFlag](#) (GPC_Type *base, uint32_t irqId)
Get the IRQ/Event flag.
- static void [GPC_DsmTriggerMask](#) (GPC_Type *base, bool enable)
Mask the DSM trigger.
- static void [GPC_WFIMask](#) (GPC_Type *base, bool enable)
Mask the WFI.
- static void [GPC_SelectPGCAckSignal](#) (GPC_Type *base, uint32_t mask)
Select the PGC ACK signal.
- static void [GPC_PowerDownRequestMask](#) (GPC_Type *base, bool enable)
Power down request to virtual PGC mask or not.
- static void [GPC_PGCMapping](#) (GPC_Type *base, uint32_t mask)
PGC CPU Mapping.
- static void [GPC_TimeSlotConfigureForPUS](#) (GPC_Type *base, uint8_t slotIndex, uint32_t value)
Time slot configure.
- void [GPC_EnterWaitMode](#) (GPC_Type *base, gpc_lpm_config_t *config)
Enter WAIT mode.
- void [GPC_EnterStopMode](#) (GPC_Type *base, gpc_lpm_config_t *config)
Enter STOP mode.
- void [GPC_Init](#) (GPC_Type *base, uint32_t powerUpSlot, uint32_t powerDownSlot)
GPC init function.

Driver version

- #define [FSL_GPC_DRIVER_VERSION](#) ([MAKE_VERSION](#)(2, 2, 0))
GPC driver version 2.2.0.

10.2 Macro Definition Documentation

10.2.1 #define FSL_GPC_DRIVER_VERSION (MAKE_VERSION(2, 2, 0))

10.3 Enumeration Type Documentation

10.3.1 enum _gpc_lpm_mode

Enumerator

kGPC_RunMode run mode
kGPC_WaitMode wait mode
kGPC_StopMode stop mode

10.3.2 enum _gpc_pgc_ack_sel

Enumerator

kGPC_DummyPGCPowerUpAck dummy power up ack signal
kGPC_VirtualPGCPowerUpAck virtual pgc power up ack signal
kGPC_DummyPGCPowerDownAck dummy power down ack signal
kGPC_VirtualPGCPowerDownAck virtual pgc power down ack signal
kGPC_NocPGCPowerUpAck NOC power up ack signal.
kGPC_NocPGCPowerDownAck NOC power.

10.3.3 enum _gpc_standby_count

Enumerator

kGPC_StandbyCounter4CkilClk 4 ckil clocks
kGPC_StandbyCounter8CkilClk 8 ckil clocks
kGPC_StandbyCounter16CkilClk 16 ckil clocks
kGPC_StandbyCounter32CkilClk 32 ckil clocks
kGPC_StandbyCounter64CkilClk 64 ckil clocks
kGPC_StandbyCounter128CkilClk 128 ckil clocks
kGPC_StandbyCounter256CkilClk 256 ckil clocks
kGPC_StandbyCounter512CkilClk 512 ckil clocks

10.4 Function Documentation

10.4.1 static void GPC_AllowIRQs (GPC_Type * *base*) [inline], [static]

Parameters

<i>base</i>	GPC peripheral base address.
-------------	------------------------------

10.4.2 static void GPC_DisallowIRQs (GPC_Type * *base*) [inline], [static]

Parameters

<i>base</i>	GPC peripheral base address.
-------------	------------------------------

10.4.3 static uint32_t GPC_GetLpmMode (GPC_Type * *base*) [inline], [static]

Parameters

<i>base</i>	GPC peripheral base address.
-------------	------------------------------

Return values

<i>lpm</i>	mode, reference _gpc_lpm_mode
------------	-------------------------------

10.4.4 void GPC_EnableIRQ (GPC_Type * *base*, uint32_t *irqId*)

Parameters

<i>base</i>	GPC peripheral base address.
<i>irqId</i>	ID number of IRQ to be enabled, available range is 0-127,reference SOC headerfile IRQn_Type.

10.4.5 void GPC_DisableIRQ (GPC_Type * *base*, uint32_t *irqId*)

Parameters

<i>base</i>	GPC peripheral base address.
<i>irqId</i>	ID number of IRQ to be disabled, available range is 0-127,reference SOC headerfile IRQn_Type.

10.4.6 bool GPC_GetIRQStatusFlag (GPC_Type * *base*, uint32_t *irqId*)

Parameters

<i>base</i>	GPC peripheral base address.
<i>irqId</i>	ID number of IRQ to be enabled, available range is 0-127,reference SOC headerfile IRQn_Type.

Returns

Indicated IRQ/Event is asserted or not.

10.4.7 static void GPC_DsmTriggerMask (GPC_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	GPC peripheral base address.
<i>enable</i>	true to enable mask, false to disable mask.

10.4.8 static void GPC_WFIMask (GPC_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	GPC peripheral base address.
<i>enable</i>	true to enable mask, false to disable mask.

10.4.9 static void GPC_SelectPGCAckSignal (GPC_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	GPC peripheral base address.
<i>mask</i>	reference _gpc_pgc_ack_sel.

10.4.10 static void GPC_PowerDownRequestMask (GPC_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	GPC peripheral base address.
<i>enable</i>	true to mask, false to not mask.

10.4.11 static void GPC_PGCMapping (GPC_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	GPC peripheral base address.
<i>mask</i>	mask value reference PGC CPU mapping definition.

10.4.12 static void GPC_TimeSlotConfigureForPUS (GPC_Type * *base*, uint8_t *slotIndex*, uint32_t *value*) [inline], [static]

Parameters

<i>base</i>	GPC peripheral base address.
<i>slotIndex</i>	time slot index.
<i>value</i>	value to be configured

10.4.13 void GPC_EnterWaitMode (GPC_Type * *base*, gpc_lpm_config_t * *config*)

Parameters

<i>base</i>	GPC peripheral base address.
<i>config</i>	lpm mode configurations.

10.4.14 void GPC_EnterStopMode (GPC_Type * *base*, gpc_lpm_config_t * *config*)

Parameters

<i>base</i>	GPC peripheral base address.
<i>config</i>	lpm mode configurations.

10.4.15 void GPC_Init (GPC_Type * *base*, uint32_t *powerUpSlot*, uint32_t *powerDownSlot*)

Parameters

<i>base</i>	GPC peripheral base address.
<i>powerUpSlot</i>	power up slot number.
<i>powerDownSlot</i>	power down slot number.

Chapter 11

GPT: General Purpose Timer

11.1 Overview

The MCUXpresso SDK provides a driver for the General Purpose Timer (GPT) of MCUXpresso SDK devices.

11.2 Function groups

The gpt driver supports the generation of PWM signals, input capture, and setting up the timer match conditions.

11.2.1 Initialization and deinitialization

The function [GPT_Init\(\)](#) initializes the gpt with specified configurations. The function [GPT_GetDefaultConfig\(\)](#) gets the default configurations. The initialization function configures the restart/free-run mode and input selection when running.

The function [GPT_Deinit\(\)](#) stops the timer and turns off the module clock.

11.3 Typical use case

11.3.1 GPT interrupt example

Set up a channel to trigger a periodic interrupt after every 1 second. Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/gpt`

Data Structures

- struct [gpt_config_t](#)
Structure to configure the running mode. [More...](#)

Enumerations

- enum [gpt_clock_source_t](#) {
 [kGPT_ClockSource_Off](#) = 0U,
 [kGPT_ClockSource_Periph](#) = 1U,
 [kGPT_ClockSource_HighFreq](#) = 2U,
 [kGPT_ClockSource_Ext](#) = 3U,
 [kGPT_ClockSource_LowFreq](#) = 4U,
 [kGPT_ClockSource_Osc](#) = 5U }
List of clock sources.

- enum `gpt_input_capture_channel_t` {
`kGPT_InputCapture_Channel1` = 0U,
`kGPT_InputCapture_Channel2` = 1U }
List of input capture channel number.
- enum `gpt_input_operation_mode_t` {
`kGPT_InputOperation_Disabled` = 0U,
`kGPT_InputOperation_RiseEdge` = 1U,
`kGPT_InputOperation_FallEdge` = 2U,
`kGPT_InputOperation_BothEdge` = 3U }
List of input capture operation mode.
- enum `gpt_output_compare_channel_t` {
`kGPT_OutputCompare_Channel1` = 0U,
`kGPT_OutputCompare_Channel2` = 1U,
`kGPT_OutputCompare_Channel3` = 2U }
List of output compare channel number.
- enum `gpt_output_operation_mode_t` {
`kGPT_OutputOperation_Disconnected` = 0U,
`kGPT_OutputOperation_Toggle` = 1U,
`kGPT_OutputOperation_Clear` = 2U,
`kGPT_OutputOperation_Set` = 3U,
`kGPT_OutputOperation_Activelow` = 4U }
List of output compare operation mode.
- enum `gpt_interrupt_enable_t` {
`kGPT_OutputCompare1InterruptEnable` = GPT_IR_OF1IE_MASK,
`kGPT_OutputCompare2InterruptEnable` = GPT_IR_OF2IE_MASK,
`kGPT_OutputCompare3InterruptEnable` = GPT_IR_OF3IE_MASK,
`kGPT_InputCapture1InterruptEnable` = GPT_IR_IF1IE_MASK,
`kGPT_InputCapture2InterruptEnable` = GPT_IR_IF2IE_MASK,
`kGPT_RollOverFlagInterruptEnable` = GPT_IR_ROVIE_MASK }
List of GPT interrupts.
- enum `gpt_status_flag_t` {
`kGPT_OutputCompare1Flag` = GPT_SR_OF1_MASK,
`kGPT_OutputCompare2Flag` = GPT_SR_OF2_MASK,
`kGPT_OutputCompare3Flag` = GPT_SR_OF3_MASK,
`kGPT_InputCapture1Flag` = GPT_SR_IF1_MASK,
`kGPT_InputCapture2Flag` = GPT_SR_IF2_MASK,
`kGPT_RollOverFlag` = GPT_SR_ROV_MASK }
Status flag.

Driver version

- #define `FSL_GPT_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 3)`)

Initialization and deinitialization

- void `GPT_Init` (`GPT_Type *base`, const `gpt_config_t *initConfig`)
Initialize GPT to reset state and initialize running mode.

- void [GPT_Deinit](#) (GPT_Type *base)
Disables the module and gates the GPT clock.
- void [GPT_GetDefaultConfig](#) (gpt_config_t *config)
Fills in the GPT configuration structure with default settings.

Software Reset

- static void [GPT_SoftwareReset](#) (GPT_Type *base)
Software reset of GPT module.

Clock source and frequency control

- static void [GPT_SetClockSource](#) (GPT_Type *base, gpt_clock_source_t gptClkSource)
Set clock source of GPT.
- static gpt_clock_source_t [GPT_GetClockSource](#) (GPT_Type *base)
Get clock source of GPT.
- static void [GPT_SetClockDivider](#) (GPT_Type *base, uint32_t divider)
Set pre scaler of GPT.
- static uint32_t [GPT_GetClockDivider](#) (GPT_Type *base)
Get clock divider in GPT module.
- static void [GPT_SetOscClockDivider](#) (GPT_Type *base, uint32_t divider)
OSC 24M pre-scaler before selected by clock source.
- static uint32_t [GPT_GetOscClockDivider](#) (GPT_Type *base)
Get OSC 24M clock divider in GPT module.

Timer Start and Stop

- static void [GPT_StartTimer](#) (GPT_Type *base)
Start GPT timer.
- static void [GPT_StopTimer](#) (GPT_Type *base)
Stop GPT timer.

Read the timer period

- static uint32_t [GPT_GetCurrentTimerCount](#) (GPT_Type *base)
Reads the current GPT counting value.

GPT Input/Output Signal Control

- static void [GPT_SetInputOperationMode](#) (GPT_Type *base, gpt_input_capture_channel_t channel, gpt_input_operation_mode_t mode)
Set GPT operation mode of input capture channel.
- static gpt_input_operation_mode_t [GPT_GetInputOperationMode](#) (GPT_Type *base, gpt_input_capture_channel_t channel)
Get GPT operation mode of input capture channel.
- static uint32_t [GPT_GetInputCaptureValue](#) (GPT_Type *base, gpt_input_capture_channel_t channel)
Get GPT input capture value of certain channel.
- static void [GPT_SetOutputOperationMode](#) (GPT_Type *base, gpt_output_compare_channel_t channel, gpt_output_operation_mode_t mode)

- *Set GPT operation mode of output compare channel.*
static [gpt_output_operation_mode_t](#) [GPT_GetOutputOperationMode](#) (GPT_Type *base, [gpt_output_compare_channel_t](#) channel)
- *Get GPT operation mode of output compare channel.*
static void [GPT_SetOutputCompareValue](#) (GPT_Type *base, [gpt_output_compare_channel_t](#) channel, uint32_t value)
- *Set GPT output compare value of output compare channel.*
static uint32_t [GPT_GetOutputCompareValue](#) (GPT_Type *base, [gpt_output_compare_channel_t](#) channel)
- *Get GPT output compare value of output compare channel.*
static void [GPT_ForceOutput](#) (GPT_Type *base, [gpt_output_compare_channel_t](#) channel)
Force GPT output action on output compare channel, ignoring comparator.

GPT Interrupt and Status Interface

- static void [GPT_EnableInterrupts](#) (GPT_Type *base, uint32_t mask)
Enables the selected GPT interrupts.
- static void [GPT_DisableInterrupts](#) (GPT_Type *base, uint32_t mask)
Disables the selected GPT interrupts.
- static uint32_t [GPT_GetEnabledInterrupts](#) (GPT_Type *base)
Gets the enabled GPT interrupts.

Status Interface

- static uint32_t [GPT_GetStatusFlags](#) (GPT_Type *base, [gpt_status_flag_t](#) flags)
Get GPT status flags.
- static void [GPT_ClearStatusFlags](#) (GPT_Type *base, [gpt_status_flag_t](#) flags)
Clears the GPT status flags.

11.4 Data Structure Documentation

11.4.1 struct gpt_config_t

Data Fields

- [gpt_clock_source_t](#) clockSource
clock source for GPT module.
- uint32_t divider
clock divider (prescaler+1) from clock source to counter.
- bool enableFreeRun
true: FreeRun mode, false: Restart mode.
- bool enableRunInWait
GPT enabled in wait mode.
- bool enableRunInStop
GPT enabled in stop mode.
- bool enableRunInDoze
GPT enabled in doze mode.
- bool enableRunInDbg
GPT enabled in debug mode.

- bool `enableMode`
 true: counter reset to 0 when enabled;
 false: counter retain its value when enabled.

Field Documentation

- (1) `gpt_clock_source_t gpt_config_t::clockSource`
- (2) `uint32_t gpt_config_t::divider`
- (3) `bool gpt_config_t::enableFreeRun`
- (4) `bool gpt_config_t::enableRunInWait`
- (5) `bool gpt_config_t::enableRunInStop`
- (6) `bool gpt_config_t::enableRunInDoze`
- (7) `bool gpt_config_t::enableRunInDbg`
- (8) `bool gpt_config_t::enableMode`

11.5 Enumeration Type Documentation

11.5.1 enum `gpt_clock_source_t`

Note

Actual number of clock sources is SoC dependent

Enumerator

kGPT_ClockSource_Off GPT Clock Source Off.
kGPT_ClockSource_Periph GPT Clock Source from Peripheral Clock.
kGPT_ClockSource_HighFreq GPT Clock Source from High Frequency Reference Clock.
kGPT_ClockSource_Ext GPT Clock Source from external pin.
kGPT_ClockSource_LowFreq GPT Clock Source from Low Frequency Reference Clock.
kGPT_ClockSource_Osc GPT Clock Source from Crystal oscillator.

11.5.2 enum `gpt_input_capture_channel_t`

Enumerator

kGPT_InputCapture_Channel1 GPT Input Capture Channel1.
kGPT_InputCapture_Channel2 GPT Input Capture Channel2.

11.5.3 enum gpt_input_operation_mode_t

Enumerator

kGPT_InputOperation_Disabled Don't capture.
kGPT_InputOperation_RiseEdge Capture on rising edge of input pin.
kGPT_InputOperation_FallEdge Capture on falling edge of input pin.
kGPT_InputOperation_BothEdge Capture on both edges of input pin.

11.5.4 enum gpt_output_compare_channel_t

Enumerator

kGPT_OutputCompare_Channel1 Output Compare Channel1.
kGPT_OutputCompare_Channel2 Output Compare Channel2.
kGPT_OutputCompare_Channel3 Output Compare Channel3.

11.5.5 enum gpt_output_operation_mode_t

Enumerator

kGPT_OutputOperation_Disconnected Don't change output pin.
kGPT_OutputOperation_Toggle Toggle output pin.
kGPT_OutputOperation_Clear Set output pin low.
kGPT_OutputOperation_Set Set output pin high.
kGPT_OutputOperation_Activelow Generate a active low pulse on output pin.

11.5.6 enum gpt_interrupt_enable_t

Enumerator

kGPT_OutputCompare1InterruptEnable Output Compare Channel1 interrupt enable.
kGPT_OutputCompare2InterruptEnable Output Compare Channel2 interrupt enable.
kGPT_OutputCompare3InterruptEnable Output Compare Channel3 interrupt enable.
kGPT_InputCapture1InterruptEnable Input Capture Channel1 interrupt enable.
kGPT_InputCapture2InterruptEnable Input Capture Channel1 interrupt enable.
kGPT_RollOverFlagInterruptEnable Counter rolled over interrupt enable.

11.5.7 enum gpt_status_flag_t

Enumerator

kGPT_OutputCompare1Flag Output compare channel 1 event.
kGPT_OutputCompare2Flag Output compare channel 2 event.
kGPT_OutputCompare3Flag Output compare channel 3 event.
kGPT_InputCapture1Flag Input Capture channel 1 event.
kGPT_InputCapture2Flag Input Capture channel 2 event.
kGPT_RollOverFlag Counter reaches maximum value and rolled over to 0 event.

11.6 Function Documentation

11.6.1 void GPT_Init (GPT_Type * *base*, const gpt_config_t * *initConfig*)

Parameters

<i>base</i>	GPT peripheral base address.
<i>initConfig</i>	GPT mode setting configuration.

11.6.2 void GPT_Deinit (GPT_Type * *base*)

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

11.6.3 void GPT_GetDefaultConfig (gpt_config_t * *config*)

The default values are:

```

*   config->clockSource = kGPT_ClockSource_Periph;
*   config->divider = 1U;
*   config->enableRunInStop = true;
*   config->enableRunInWait = true;
*   config->enableRunInDoze = false;
*   config->enableRunInDbg = false;
*   config->enableFreeRun = false;
*   config->enableMode = true;
*

```


Parameters

<i>config</i>	Pointer to the user configuration structure.
---------------	--

11.6.4 static void GPT_SoftwareReset (GPT_Type * *base*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

11.6.5 static void GPT_SetClockSource (GPT_Type * *base*, gpt_clock_source_t *gptClkSource*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>gptClkSource</i>	Clock source (see gpt_clock_source_t typedef enumeration).

11.6.6 static gpt_clock_source_t GPT_GetClockSource (GPT_Type * *base*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

Returns

clock source (see [gpt_clock_source_t](#) typedef enumeration).

11.6.7 static void GPT_SetClockDivider (GPT_Type * *base*, uint32_t *divider*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>divider</i>	Divider of GPT (1-4096).

11.6.8 static uint32_t GPT_GetClockDivider (GPT_Type * *base*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

Returns

clock divider in GPT module (1-4096).

11.6.9 static void GPT_SetOscClockDivider (GPT_Type * *base*, uint32_t *divider*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>divider</i>	OSC Divider(1-16).

11.6.10 static uint32_t GPT_GetOscClockDivider (GPT_Type * *base*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

Returns

OSC clock divider in GPT module (1-16).

11.6.11 static void GPT_StartTimer (GPT_Type * *base*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

11.6.12 static void GPT_StopTimer (GPT_Type * *base*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

11.6.13 static uint32_t GPT_GetCurrentTimerCount (GPT_Type * *base*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

Returns

Current GPT counter value.

11.6.14 static void GPT_SetInputOperationMode (GPT_Type * *base*, gpt_input_capture_channel_t *channel*, gpt_input_operation_mode_t *mode*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT capture channel (see gpt_input_capture_channel_t typedef enumeration).
<i>mode</i>	GPT input capture operation mode (see gpt_input_operation_mode_t typedef enumeration).

11.6.15 static gpt_input_operation_mode_t GPT_GetInputOperationMode (GPT_Type * *base*, gpt_input_capture_channel_t *channel*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT capture channel (see gpt_input_capture_channel_t typedef enumeration).

Returns

GPT input capture operation mode (see [gpt_input_operation_mode_t](#) typedef enumeration).

11.6.16 `static uint32_t GPT_GetInputCaptureValue (GPT_Type * base,
gpt_input_capture_channel_t channel) [inline], [static]`

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT capture channel (see gpt_input_capture_channel_t typedef enumeration).

Returns

GPT input capture value.

11.6.17 `static void GPT_SetOutputOperationMode (GPT_Type * base,
gpt_output_compare_channel_t channel, gpt_output_operation_mode_t
mode) [inline], [static]`

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT output compare channel (see gpt_output_compare_channel_t typedef enumeration).
<i>mode</i>	GPT output operation mode (see gpt_output_operation_mode_t typedef enumeration).

11.6.18 `static gpt_output_operation_mode_t GPT_GetOutputOperationMode (
GPT_Type * base, gpt_output_compare_channel_t channel) [inline],
[static]`

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT output compare channel (see gpt_output_compare_channel_t typedef enumeration).

Returns

GPT output operation mode (see [gpt_output_operation_mode_t](#) typedef enumeration).

**11.6.19 static void GPT_SetOutputCompareValue (GPT_Type * *base*,
gpt_output_compare_channel_t *channel*, uint32_t *value*) [inline],
[static]**

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT output compare channel (see gpt_output_compare_channel_t typedef enumeration).
<i>value</i>	GPT output compare value.

**11.6.20 static uint32_t GPT_GetOutputCompareValue (GPT_Type * *base*,
gpt_output_compare_channel_t *channel*) [inline], [static]**

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT output compare channel (see gpt_output_compare_channel_t typedef enumeration).

Returns

GPT output compare value.

**11.6.21 static void GPT_ForceOutput (GPT_Type * *base*, gpt_output_compare_ -
channel_t *channel*) [inline], [static]**

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT output compare channel (see gpt_output_compare_channel_t typedef enumeration).

11.6.22 static void GPT_EnableInterrupts (GPT_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>mask</i>	The interrupts to enable. This is a logical OR of members of the enumeration gpt_interrupt_enable_t

11.6.23 static void GPT_DisableInterrupts (GPT_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address
<i>mask</i>	The interrupts to disable. This is a logical OR of members of the enumeration gpt_interrupt_enable_t

11.6.24 static uint32_t GPT_GetEnabledInterrupts (GPT_Type * *base*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address
-------------	-----------------------------

Returns

The enabled interrupts. This is the logical OR of members of the enumeration [gpt_interrupt_enable_t](#)

11.6.25 static uint32_t GPT_GetStatusFlags (GPT_Type * *base*, gpt_status_flag_t *flags*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>flags</i>	GPT status flag mask (see gpt_status_flag_t for bit definition).

Returns

GPT status, each bit represents one status flag.

11.6.26 static void GPT_ClearStatusFlags (GPT_Type * *base*, gpt_status_flag_t *flags*) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>flags</i>	GPT status flag mask (see gpt_status_flag_t for bit definition).

Chapter 12

GPIO: General-Purpose Input/Output Driver

12.1 Overview

The MCUXpresso SDK provides a peripheral driver for the General-Purpose Input/Output (GPIO) module of MCUXpresso SDK devices.

12.2 Typical use case

12.2.1 Input Operation

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/gpio`

Data Structures

- struct `gpio_pin_config_t`
GPIO Init structure definition. [More...](#)

Enumerations

- enum `gpio_pin_direction_t` {
 `kGPIO_DigitalInput` = 0U,
 `kGPIO_DigitalOutput` = 1U }
GPIO direction definition.
- enum `gpio_interrupt_mode_t` {
 `kGPIO_NoIntmode` = 0U,
 `kGPIO_IntLowLevel` = 1U,
 `kGPIO_IntHighLevel` = 2U,
 `kGPIO_IntRisingEdge` = 3U,
 `kGPIO_IntFallingEdge` = 4U,
 `kGPIO_IntRisingOrFallingEdge` = 5U }
GPIO interrupt mode definition.

Driver version

- #define `FSL_GPIO_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 5)`)
GPIO driver version.

GPIO Initialization and Configuration functions

- void `GPIO_PinInit` (`GPIO_Type *base`, `uint32_t pin`, const `gpio_pin_config_t *Config`)
Initializes the GPIO peripheral according to the specified parameters in the initConfig.

GPIO Reads and Write Functions

- void [GPIO_PinWrite](#) (GPIO_Type *base, uint32_t pin, uint8_t output)
Sets the output level of the individual GPIO pin to logic 1 or 0.
- static void [GPIO_WritePinOutput](#) (GPIO_Type *base, uint32_t pin, uint8_t output)
Sets the output level of the individual GPIO pin to logic 1 or 0.
- static void [GPIO_PortSet](#) (GPIO_Type *base, uint32_t mask)
Sets the output level of the multiple GPIO pins to the logic 1.
- static void [GPIO_SetPinsOutput](#) (GPIO_Type *base, uint32_t mask)
Sets the output level of the multiple GPIO pins to the logic 1.
- static void [GPIO_PortClear](#) (GPIO_Type *base, uint32_t mask)
Sets the output level of the multiple GPIO pins to the logic 0.
- static void [GPIO_ClearPinsOutput](#) (GPIO_Type *base, uint32_t mask)
Sets the output level of the multiple GPIO pins to the logic 0.
- static void [GPIO_PortToggle](#) (GPIO_Type *base, uint32_t mask)
Reverses the current output logic of the multiple GPIO pins.
- static uint32_t [GPIO_PinRead](#) (GPIO_Type *base, uint32_t pin)
Reads the current input value of the GPIO port.
- static uint32_t [GPIO_ReadPinInput](#) (GPIO_Type *base, uint32_t pin)
Reads the current input value of the GPIO port.

GPIO Reads Pad Status Functions

- static uint8_t [GPIO_PinReadPadStatus](#) (GPIO_Type *base, uint32_t pin)
Reads the current GPIO pin pad status.
- static uint8_t [GPIO_ReadPadStatus](#) (GPIO_Type *base, uint32_t pin)
Reads the current GPIO pin pad status.

Interrupts and flags management functions

- void [GPIO_PinSetInterruptConfig](#) (GPIO_Type *base, uint32_t pin, [gpio_interrupt_mode_t](#) pinInterruptMode)
Sets the current pin interrupt mode.
- static void [GPIO_SetPinInterruptConfig](#) (GPIO_Type *base, uint32_t pin, [gpio_interrupt_mode_t](#) pinInterruptMode)
Sets the current pin interrupt mode.
- static void [GPIO_PortEnableInterrupts](#) (GPIO_Type *base, uint32_t mask)
Enables the specific pin interrupt.
- static void [GPIO_EnableInterrupts](#) (GPIO_Type *base, uint32_t mask)
Enables the specific pin interrupt.
- static void [GPIO_PortDisableInterrupts](#) (GPIO_Type *base, uint32_t mask)
Disables the specific pin interrupt.
- static void [GPIO_DisableInterrupts](#) (GPIO_Type *base, uint32_t mask)
Disables the specific pin interrupt.
- static uint32_t [GPIO_PortGetInterruptFlags](#) (GPIO_Type *base)
Reads individual pin interrupt status.
- static uint32_t [GPIO_GetPinsInterruptFlags](#) (GPIO_Type *base)
Reads individual pin interrupt status.
- static void [GPIO_PortClearInterruptFlags](#) (GPIO_Type *base, uint32_t mask)
Clears pin interrupt flag.
- static void [GPIO_ClearPinsInterruptFlags](#) (GPIO_Type *base, uint32_t mask)

Clears pin interrupt flag.

12.3 Data Structure Documentation

12.3.1 struct gpio_pin_config_t

Data Fields

- [gpio_pin_direction_t direction](#)
Specifies the pin direction.
- uint8_t [outputLogic](#)
Set a default output logic, which has no use in input.
- [gpio_interrupt_mode_t interruptMode](#)
Specifies the pin interrupt mode, a value of [gpio_interrupt_mode_t](#).

Field Documentation

(1) [gpio_pin_direction_t gpio_pin_config_t::direction](#)

(2) [gpio_interrupt_mode_t gpio_pin_config_t::interruptMode](#)

12.4 Macro Definition Documentation

12.4.1 #define FSL_GPIO_DRIVER_VERSION (MAKE_VERSION(2, 0, 5))

12.5 Enumeration Type Documentation

12.5.1 enum gpio_pin_direction_t

Enumerator

kGPIO_DigitalInput Set current pin as digital input.
kGPIO_DigitalOutput Set current pin as digital output.

12.5.2 enum gpio_interrupt_mode_t

Enumerator

kGPIO_NoIntmode Set current pin general IO functionality.
kGPIO_IntLowLevel Set current pin interrupt is low-level sensitive.
kGPIO_IntHighLevel Set current pin interrupt is high-level sensitive.
kGPIO_IntRisingEdge Set current pin interrupt is rising-edge sensitive.
kGPIO_IntFallingEdge Set current pin interrupt is falling-edge sensitive.
kGPIO_IntRisingOrFallingEdge Enable the edge select bit to override the ICR register's configuration.

12.6 Function Documentation

12.6.1 void GPIO_PinInit (GPIO_Type * *base*, uint32_t *pin*, const gpio_pin_config_t * *Config*)

Parameters

<i>base</i>	GPIO base pointer.
<i>pin</i>	Specifies the pin number
<i>Config</i>	pointer to a gpio_pin_config_t structure that contains the configuration information.

12.6.2 void GPIO_PinWrite (GPIO_Type * *base*, uint32_t *pin*, uint8_t *output*)

Parameters

<i>base</i>	GPIO base pointer.
<i>pin</i>	GPIO port pin number.
<i>output</i>	GPIO pin output logic level. <ul style="list-style-type: none"> • 0: corresponding pin output low-logic level. • 1: corresponding pin output high-logic level.

12.6.3 static void GPIO_WritePinOutput (GPIO_Type * *base*, uint32_t *pin*, uint8_t *output*) [inline], [static]

Deprecated Do not use this function. It has been superseded by [GPIO_PinWrite](#).

12.6.4 static void GPIO_PortSet (GPIO_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIO1, GPIO2, GPIO3, and so on.)
<i>mask</i>	GPIO pin number macro

12.6.5 static void GPIO_SetPinsOutput (GPIO_Type * *base*, uint32_t *mask*) [inline], [static]

Deprecated Do not use this function. It has been superseded by [GPIO_PortSet](#).

12.6.6 `static void GPIO_PortClear (GPIO_Type * base, uint32_t mask)`
`[inline], [static]`

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIO1, GPIO2, GPIO3, and so on.)
<i>mask</i>	GPIO pin number macro

12.6.7 static void GPIO_ClearPinsOutput (GPIO_Type * *base*, uint32_t *mask*) [inline], [static]

Deprecated Do not use this function. It has been superceded by [GPIO_PortClear](#).

12.6.8 static void GPIO_PortToggle (GPIO_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIO1, GPIO2, GPIO3, and so on.)
<i>mask</i>	GPIO pin number macro

12.6.9 static uint32_t GPIO_PinRead (GPIO_Type * *base*, uint32_t *pin*) [inline], [static]

Parameters

<i>base</i>	GPIO base pointer.
<i>pin</i>	GPIO port pin number.

Return values

<i>GPIO</i>	port input value.
-------------	-------------------

12.6.10 static uint32_t GPIO_ReadPinInput (GPIO_Type * *base*, uint32_t *pin*) [inline], [static]

Deprecated Do not use this function. It has been superceded by [GPIO_PinRead](#).

12.6.11 `static uint8_t GPIO_PinReadPadStatus (GPIO_Type * base, uint32_t pin)`
 `[inline], [static]`

Parameters

<i>base</i>	GPIO base pointer.
<i>pin</i>	GPIO port pin number.

Return values

<i>GPIO</i>	pin pad status value.
-------------	-----------------------

12.6.12 `static uint8_t GPIO_ReadPadStatus (GPIO_Type * base, uint32_t pin)`
[inline], [static]

Deprecated Do not use this function. It has been superseded by [GPIO_PinReadPadStatus](#).

12.6.13 `void GPIO_PinSetInterruptConfig (GPIO_Type * base, uint32_t pin,
 gpio_interrupt_mode_t pinInterruptMode)`

Parameters

<i>base</i>	GPIO base pointer.
<i>pin</i>	GPIO port pin number.
<i>pinInterrupt- Mode</i>	pointer to a gpio_interrupt_mode_t structure that contains the interrupt mode information.

12.6.14 `static void GPIO_SetPinInterruptConfig (GPIO_Type * base, uint32_t pin,
 gpio_interrupt_mode_t pinInterruptMode)` **[inline], [static]**

Deprecated Do not use this function. It has been superseded by [GPIO_PinSetInterruptConfig](#).

12.6.15 `static void GPIO_PortEnableInterrupts (GPIO_Type * base, uint32_t mask
)` **[inline], [static]**

Parameters

<i>base</i>	GPIO base pointer.
<i>mask</i>	GPIO pin number macro.

12.6.16 static void GPIO_EnableInterrupts (GPIO_Type * *base*, uint32_t *mask*)
[inline], [static]

Parameters

<i>base</i>	GPIO base pointer.
<i>mask</i>	GPIO pin number macro.

12.6.17 static void GPIO_PortDisableInterrupts (GPIO_Type * *base*, uint32_t *mask*)
[inline], [static]

Parameters

<i>base</i>	GPIO base pointer.
<i>mask</i>	GPIO pin number macro.

12.6.18 static void GPIO_DisableInterrupts (GPIO_Type * *base*, uint32_t *mask*)
[inline], [static]

Deprecated Do not use this function. It has been superseded by [GPIO_PortDisableInterrupts](#).

12.6.19 static uint32_t GPIO_PortGetInterruptFlags (GPIO_Type * *base*)
[inline], [static]

Parameters

<i>base</i>	GPIO base pointer.
-------------	--------------------

Return values

<i>current</i>	pin interrupt status flag.
----------------	----------------------------

12.6.20 `static uint32_t GPIO_GetPinsInterruptFlags (GPIO_Type * base)`
[inline], [static]

Parameters

<i>base</i>	GPIO base pointer.
-------------	--------------------

Return values

<i>current</i>	pin interrupt status flag.
----------------	----------------------------

12.6.21 `static void GPIO_PortClearInterruptFlags (GPIO_Type * base, uint32_t`
***mask*) [inline], [static]**

Status flags are cleared by writing a 1 to the corresponding bit position.

Parameters

<i>base</i>	GPIO base pointer.
<i>mask</i>	GPIO pin number macro.

12.6.22 `static void GPIO_ClearPinsInterruptFlags (GPIO_Type * base, uint32_t`
***mask*) [inline], [static]**

Status flags are cleared by writing a 1 to the corresponding bit position.

Parameters

<i>base</i>	GPIO base pointer.
<i>mask</i>	GPIO pin number macro.



Chapter 13

I2C: Inter-Integrated Circuit Driver

13.1 Overview

Modules

- [I2C CMSIS Driver](#)
- [I2C Driver](#)
- [I2C FreeRTOS Driver](#)

13.2 I2C Driver

13.2.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Inter-Integrated Circuit (I2C) module of MCUXpresso SDK devices.

The I2C driver includes functional APIs and transactional APIs.

Functional APIs target the low-level APIs. Functional APIs can be used for the I2C master/slave initialization/configuration/operation for optimization/customization purpose. Using the functional APIs requires knowing the I2C master peripheral and how to organize functional APIs to meet the application requirements. The I2C functional operation groups provide the functional APIs set.

Transactional APIs target the high-level APIs. The transactional APIs can be used to enable the peripheral quickly and also in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code using the functional APIs or accessing the hardware registers.

Transactional APIs support asynchronous transfer. This means that the functions [I2C_MasterTransferNonBlocking\(\)](#) set up the interrupt non-blocking transfer. When the transfer completes, the upper layer is notified through a callback function with the status.

13.2.2 Typical use case

13.2.2.1 Master Operation in functional method

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/i2c`

13.2.2.2 Master Operation in interrupt transactional method

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/i2c`

13.2.2.3 Slave Operation in functional method

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/i2c`

13.2.2.4 Slave Operation in interrupt transactional method

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/i2c`

Data Structures

- struct [i2c_master_config_t](#)

- *I2C master user configuration. [More...](#)*
- struct [i2c_master_transfer_t](#)
I2C master transfer structure. [More...](#)
- struct [i2c_master_handle_t](#)
I2C master handle structure. [More...](#)
- struct [i2c_slave_config_t](#)
I2C slave user configuration. [More...](#)
- struct [i2c_slave_transfer_t](#)
I2C slave transfer structure. [More...](#)
- struct [i2c_slave_handle_t](#)
I2C slave handle structure. [More...](#)

Macros

- #define [I2C_RETRY_TIMES](#) 0U /* Define to zero means keep waiting until the flag is assert/deassert. */
Retry times for waiting flag.

Typedefs

- typedef void(* [i2c_master_transfer_callback_t](#))(I2C_Type *base, [i2c_master_handle_t](#) *handle, [status_t](#) status, void *userData)
I2C master transfer callback typedef.
- typedef void(* [i2c_slave_transfer_callback_t](#))(I2C_Type *base, [i2c_slave_transfer_t](#) *xfer, void *userData)
I2C slave transfer callback typedef.

Enumerations

- enum {
[kStatus_I2C_Busy](#) = MAKE_STATUS(kStatusGroup_I2C, 0),
[kStatus_I2C_Idle](#) = MAKE_STATUS(kStatusGroup_I2C, 1),
[kStatus_I2C_Nak](#) = MAKE_STATUS(kStatusGroup_I2C, 2),
[kStatus_I2C_ArbitrationLost](#) = MAKE_STATUS(kStatusGroup_I2C, 3),
[kStatus_I2C_Timeout](#) = MAKE_STATUS(kStatusGroup_I2C, 4),
[kStatus_I2C_Addr_Nak](#) = MAKE_STATUS(kStatusGroup_I2C, 5) }
I2C status return codes.
- enum [_i2c_flags](#) {
[kI2C_ReceiveNakFlag](#) = I2C_I2SR_RXAK_MASK,
[kI2C_IntPendingFlag](#) = I2C_I2SR_IIF_MASK,
[kI2C_TransferDirectionFlag](#) = I2C_I2SR_SRW_MASK,
[kI2C_ArbitrationLostFlag](#) = I2C_I2SR_IAL_MASK,
[kI2C_BusBusyFlag](#) = I2C_I2SR_IBB_MASK,
[kI2C_AddressMatchFlag](#) = I2C_I2SR_IAAS_MASK,
[kI2C_TransferCompleteFlag](#) = I2C_I2SR_ICF_MASK }

- *I2C peripheral flags.*
- enum `_i2c_interrupt_enable` { `kI2C_GlobalInterruptEnable` = `I2C_I2CR_IEN_MASK` }
- *I2C feature interrupt source.*
- enum `i2c_direction_t` {
`kI2C_Write` = `0x0U`,
`kI2C_Read` = `0x1U` }
- *The direction of master and slave transfers.*
- enum `_i2c_master_transfer_flags` {
`kI2C_TransferDefaultFlag` = `0x0U`,
`kI2C_TransferNoStartFlag` = `0x1U`,
`kI2C_TransferRepeatedStartFlag` = `0x2U`,
`kI2C_TransferNoStopFlag` = `0x4U` }
- *I2C transfer control flag.*
- enum `i2c_slave_transfer_event_t` {
`kI2C_SlaveAddressMatchEvent` = `0x01U`,
`kI2C_SlaveTransmitEvent` = `0x02U`,
`kI2C_SlaveReceiveEvent` = `0x04U`,
`kI2C_SlaveTransmitAckEvent` = `0x08U`,
`kI2C_SlaveCompletionEvent` = `0x20U`,
`kI2C_SlaveAllEvents` }
- *Set of events sent to the callback for nonblocking slave transfers.*

Driver version

- #define `FSL_I2C_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 7)`)
I2C driver version.

Initialization and deinitialization

- void `I2C_MasterInit` (`I2C_Type *base`, const `i2c_master_config_t *masterConfig`, `uint32_t src-Clock_Hz`)
Initializes the I2C peripheral.
- void `I2C_MasterDeinit` (`I2C_Type *base`)
De-initializes the I2C master peripheral.
- void `I2C_MasterGetDefaultConfig` (`i2c_master_config_t *masterConfig`)
Sets the I2C master configuration structure to default values.
- void `I2C_SlaveInit` (`I2C_Type *base`, const `i2c_slave_config_t *slaveConfig`)
Initializes the I2C peripheral.
- void `I2C_SlaveDeinit` (`I2C_Type *base`)
De-initializes the I2C slave peripheral.
- void `I2C_SlaveGetDefaultConfig` (`i2c_slave_config_t *slaveConfig`)
Sets the I2C slave configuration structure to default values.
- static void `I2C_Enable` (`I2C_Type *base`, bool enable)
Enables or disables the I2C peripheral operation.

Status

- static uint32_t [I2C_MasterGetStatusFlags](#) (I2C_Type *base)
Gets the I2C status flags.
- static void [I2C_MasterClearStatusFlags](#) (I2C_Type *base, uint32_t statusMask)
Clears the I2C status flag state.
- static uint32_t [I2C_SlaveGetStatusFlags](#) (I2C_Type *base)
Gets the I2C status flags.
- static void [I2C_SlaveClearStatusFlags](#) (I2C_Type *base, uint32_t statusMask)
Clears the I2C status flag state.

Interrupts

- void [I2C_EnableInterrupts](#) (I2C_Type *base, uint32_t mask)
Enables I2C interrupt requests.
- void [I2C_DisableInterrupts](#) (I2C_Type *base, uint32_t mask)
Disables I2C interrupt requests.

Bus Operations

- void [I2C_MasterSetBaudRate](#) (I2C_Type *base, uint32_t baudRate_Bps, uint32_t srcClock_Hz)
Sets the I2C master transfer baud rate.
- [status_t I2C_MasterStart](#) (I2C_Type *base, uint8_t address, [i2c_direction_t](#) direction)
Sends a START on the I2C bus.
- [status_t I2C_MasterStop](#) (I2C_Type *base)
Sends a STOP signal on the I2C bus.
- [status_t I2C_MasterRepeatedStart](#) (I2C_Type *base, uint8_t address, [i2c_direction_t](#) direction)
Sends a REPEATED START on the I2C bus.
- [status_t I2C_MasterWriteBlocking](#) (I2C_Type *base, const uint8_t *txBuff, size_t txSize, uint32_t flags)
Performs a polling send transaction on the I2C bus.
- [status_t I2C_MasterReadBlocking](#) (I2C_Type *base, uint8_t *rxBuff, size_t rxSize, uint32_t flags)
Performs a polling receive transaction on the I2C bus.
- [status_t I2C_SlaveWriteBlocking](#) (I2C_Type *base, const uint8_t *txBuff, size_t txSize)
Performs a polling send transaction on the I2C bus.
- [status_t I2C_SlaveReadBlocking](#) (I2C_Type *base, uint8_t *rxBuff, size_t rxSize)
Performs a polling receive transaction on the I2C bus.
- [status_t I2C_MasterTransferBlocking](#) (I2C_Type *base, [i2c_master_transfer_t](#) *xfer)
Performs a master polling transfer on the I2C bus.

Transactional

- void [I2C_MasterTransferCreateHandle](#) (I2C_Type *base, [i2c_master_handle_t](#) *handle, [i2c_master_transfer_callback_t](#) callback, void *userData)
Initializes the I2C handle which is used in transactional functions.
- [status_t I2C_MasterTransferNonBlocking](#) (I2C_Type *base, [i2c_master_handle_t](#) *handle, [i2c_master_transfer_t](#) *xfer)

- *Performs a master interrupt non-blocking transfer on the I2C bus.*
 • [status_t I2C_MasterTransferGetCount](#) (I2C_Type *base, i2c_master_handle_t *handle, size_t *count)
Gets the master transfer status during a interrupt non-blocking transfer.
- [status_t I2C_MasterTransferAbort](#) (I2C_Type *base, i2c_master_handle_t *handle)
Aborts an interrupt non-blocking transfer early.
- void [I2C_MasterTransferHandleIRQ](#) (I2C_Type *base, void *i2cHandle)
Master interrupt handler.
- void [I2C_SlaveTransferCreateHandle](#) (I2C_Type *base, i2c_slave_handle_t *handle, [i2c_slave_transfer_callback_t](#) callback, void *userData)
Initializes the I2C handle which is used in transactional functions.
- [status_t I2C_SlaveTransferNonBlocking](#) (I2C_Type *base, i2c_slave_handle_t *handle, uint32_t eventMask)
Starts accepting slave transfers.
- void [I2C_SlaveTransferAbort](#) (I2C_Type *base, i2c_slave_handle_t *handle)
Aborts the slave transfer.
- [status_t I2C_SlaveTransferGetCount](#) (I2C_Type *base, i2c_slave_handle_t *handle, size_t *count)
Gets the slave transfer remaining bytes during a interrupt non-blocking transfer.
- void [I2C_SlaveTransferHandleIRQ](#) (I2C_Type *base, void *i2cHandle)
Slave interrupt handler.

13.2.3 Data Structure Documentation

13.2.3.1 struct i2c_master_config_t

Data Fields

- bool [enableMaster](#)
Enables the I2C peripheral at initialization time.
- uint32_t [baudRate_Bps](#)
Baud rate configuration of I2C peripheral.

Field Documentation

(1) bool i2c_master_config_t::enableMaster

(2) uint32_t i2c_master_config_t::baudRate_Bps

13.2.3.2 struct i2c_master_transfer_t

Data Fields

- uint32_t [flags](#)
A transfer flag which controls the transfer.
- uint8_t [slaveAddress](#)
7-bit slave address.
- [i2c_direction_t](#) direction
A transfer direction, read or write.
- uint32_t [subaddress](#)

- *A sub address.*
- uint8_t [subaddressSize](#)
A size of the command buffer.
- uint8_t *volatile [data](#)
A transfer buffer.
- volatile size_t [dataSize](#)
A transfer size.

Field Documentation

- (1) uint32_t i2c_master_transfer_t::flags
- (2) uint8_t i2c_master_transfer_t::slaveAddress
- (3) i2c_direction_t i2c_master_transfer_t::direction
- (4) uint32_t i2c_master_transfer_t::subaddress

Transferred MSB first.

- (5) uint8_t i2c_master_transfer_t::subaddressSize
- (6) uint8_t* volatile i2c_master_transfer_t::data
- (7) volatile size_t i2c_master_transfer_t::dataSize

13.2.3.3 struct _i2c_master_handle

I2C master handle typedef.

Data Fields

- [i2c_master_transfer_t](#) transfer
I2C master transfer copy.
- size_t [transferSize](#)
Total bytes to be transferred.
- uint8_t [state](#)
A transfer state maintained during transfer.
- [i2c_master_transfer_callback_t](#) completionCallback
A callback function called when the transfer is finished.
- void * [userData](#)
A callback parameter passed to the callback function.

Field Documentation

- (1) i2c_master_transfer_t i2c_master_handle_t::transfer
- (2) size_t i2c_master_handle_t::transferSize
- (3) uint8_t i2c_master_handle_t::state

(4) `i2c_master_transfer_callback_t i2c_master_handle_t::completionCallback`

(5) `void* i2c_master_handle_t::userData`

13.2.3.4 struct `i2c_slave_config_t`

Data Fields

- `bool enableSlave`
Enables the I2C peripheral at initialization time.
- `uint16_t slaveAddress`
A slave address configuration.

Field Documentation

(1) `bool i2c_slave_config_t::enableSlave`

(2) `uint16_t i2c_slave_config_t::slaveAddress`

13.2.3.5 struct `i2c_slave_transfer_t`

Data Fields

- `i2c_slave_transfer_event_t event`
A reason that the callback is invoked.
- `uint8_t *volatile data`
A transfer buffer.
- `volatile size_t dataSize`
A transfer size.
- `status_t completionStatus`
Success or error code describing how the transfer completed.
- `size_t transferredCount`
A number of bytes actually transferred since the start or since the last repeated start.

Field Documentation

(1) `i2c_slave_transfer_event_t i2c_slave_transfer_t::event`

(2) `uint8_t* volatile i2c_slave_transfer_t::data`

(3) `volatile size_t i2c_slave_transfer_t::dataSize`

(4) `status_t i2c_slave_transfer_t::completionStatus`

Only applies for `kI2C_SlaveCompletionEvent`.

(5) `size_t i2c_slave_transfer_t::transferredCount`

13.2.3.6 struct _i2c_slave_handle

I2C slave handle typedef.

Data Fields

- volatile uint8_t [state](#)
A transfer state maintained during transfer.
- [i2c_slave_transfer_t](#) [transfer](#)
I2C slave transfer copy.
- uint32_t [eventMask](#)
A mask of enabled events.
- [i2c_slave_transfer_callback_t](#) [callback](#)
A callback function called at the transfer event.
- void * [userData](#)
A callback parameter passed to the callback.

Field Documentation

- (1) volatile uint8_t i2c_slave_handle_t::state
- (2) i2c_slave_transfer_t i2c_slave_handle_t::transfer
- (3) uint32_t i2c_slave_handle_t::eventMask
- (4) i2c_slave_transfer_callback_t i2c_slave_handle_t::callback
- (5) void* i2c_slave_handle_t::userData

13.2.4 Macro Definition Documentation

13.2.4.1 #define FSL_I2C_DRIVER_VERSION (MAKE_VERSION(2, 0, 7))

13.2.4.2 #define I2C_RETRY_TIMES 0U /* Define to zero means keep waiting until the flag is assert/deassert. */

13.2.5 Typedef Documentation

13.2.5.1 typedef void(* i2c_master_transfer_callback_t)(I2C_Type *base, i2c_master_handle_t *handle, status_t status, void *userData)

13.2.5.2 typedef void(* i2c_slave_transfer_callback_t)(I2C_Type *base, i2c_slave_transfer_t *xfer, void *userData)

13.2.6 Enumeration Type Documentation

13.2.6.1 anonymous enum

Enumerator

kStatus_I2C_Busy I2C is busy with current transfer.
kStatus_I2C_Idle Bus is Idle.
kStatus_I2C_Nak NAK received during transfer.
kStatus_I2C_ArbitrationLost Arbitration lost during transfer.
kStatus_I2C_Timeout Timeout polling status flags.
kStatus_I2C_Addr_Nak NAK received during the address probe.

13.2.6.2 enum_i2c_flags

The following status register flags can be cleared:

- [kI2C_ArbitrationLostFlag](#)
- [kI2C_IntPendingFlag](#)

Note

These enumerations are meant to be OR'd together to form a bit mask.

Enumerator

kI2C_ReceiveNakFlag I2C receive NAK flag.
kI2C_IntPendingFlag I2C interrupt pending flag.
kI2C_TransferDirectionFlag I2C transfer direction flag.
kI2C_ArbitrationLostFlag I2C arbitration lost flag.
kI2C_BusBusyFlag I2C bus busy flag.
kI2C_AddressMatchFlag I2C address match flag.
kI2C_TransferCompleteFlag I2C transfer complete flag.

13.2.6.3 enum_i2c_interrupt_enable

Enumerator

kI2C_GlobalInterruptEnable I2C global interrupt.

13.2.6.4 enum_i2c_direction_t

Enumerator

kI2C_Write Master transmits to the slave.
kI2C_Read Master receives from the slave.

13.2.6.5 enum `_i2c_master_transfer_flags`

Enumerator

kI2C_TransferDefaultFlag A transfer starts with a start signal, stops with a stop signal.

kI2C_TransferNoStartFlag A transfer starts without a start signal, only support write only or write+read with no start flag, do not support read only with no start flag.

kI2C_TransferRepeatedStartFlag A transfer starts with a repeated start signal.

kI2C_TransferNoStopFlag A transfer ends without a stop signal.

13.2.6.6 enum `i2c_slave_transfer_event_t`

These event enumerations are used for two related purposes. First, a bit mask created by OR'ing together events is passed to [I2C_SlaveTransferNonBlocking\(\)](#) to specify which events to enable. Then, when the slave callback is invoked, it is passed the current event through its *transfer* parameter.

Note

These enumerations are meant to be OR'd together to form a bit mask of events.

Enumerator

kI2C_SlaveAddressMatchEvent Received the slave address after a start or repeated start.

kI2C_SlaveTransmitEvent A callback is requested to provide data to transmit (slave-transmitter role).

kI2C_SlaveReceiveEvent A callback is requested to provide a buffer in which to place received data (slave-receiver role).

kI2C_SlaveTransmitAckEvent A callback needs to either transmit an ACK or NACK.

kI2C_SlaveCompletionEvent A stop was detected or finished transfer, completing the transfer.

kI2C_SlaveAllEvents A bit mask of all available events.

13.2.7 Function Documentation

13.2.7.1 void `I2C_MasterInit (I2C_Type * base, const i2c_master_config_t * masterConfig, uint32_t srcClock_Hz)`

Call this API to ungate the I2C clock and configure the I2C with master configuration.

Note

This API should be called at the beginning of the application. Otherwise, any operation to the I2C module can cause a hard fault because the clock is not enabled. The configuration structure can be custom filled or it can be set with default values by using the [I2C_MasterGetDefaultConfig\(\)](#). After calling this API, the master is ready to transfer. This is an example.

```

* i2c_master_config_t config = {
*   .enableMaster = true,
*   .baudRate_Bps = 100000
* };
* I2C_MasterInit(I2C0, &config, 12000000U);
*

```

Parameters

<i>base</i>	I2C base pointer
<i>masterConfig</i>	A pointer to the master configuration structure
<i>srcClock_Hz</i>	I2C peripheral clock frequency in Hz

13.2.7.2 void I2C_MasterDeinit (I2C_Type * *base*)

Call this API to gate the I2C clock. The I2C master module can't work unless the I2C_MasterInit is called.

Parameters

<i>base</i>	I2C base pointer
-------------	------------------

13.2.7.3 void I2C_MasterGetDefaultConfig (i2c_master_config_t * *masterConfig*)

The purpose of this API is to get the configuration structure initialized for use in the I2C_MasterInit(). Use the initialized structure unchanged in the I2C_MasterInit() or modify the structure before calling the I2C_MasterInit(). This is an example.

```

* i2c_master_config_t config;
* I2C_MasterGetDefaultConfig(&config);
*

```

Parameters

<i>masterConfig</i>	A pointer to the master configuration structure.
---------------------	--

13.2.7.4 void I2C_SlaveInit (I2C_Type * *base*, const i2c_slave_config_t * *slaveConfig*)

Call this API to ungate the I2C clock and initialize the I2C with the slave configuration.

Note

This API should be called at the beginning of the application. Otherwise, any operation to the I2C module can cause a hard fault because the clock is not enabled. The configuration structure can partly be set with default values by [I2C_SlaveGetDefaultConfig\(\)](#) or it can be custom filled by the user. This is an example.

```
* i2c_slave_config_t config = {
* .enableSlave = true,
* .slaveAddress = 0x1DU,
* };
* I2C_SlaveInit(I2C0, &config);
*
```

Parameters

<i>base</i>	I2C base pointer
<i>slaveConfig</i>	A pointer to the slave configuration structure

13.2.7.5 void I2C_SlaveDeinit (I2C_Type * *base*)

Calling this API gates the I2C clock. The I2C slave module can't work unless the I2C_SlaveInit is called to enable the clock.

Parameters

<i>base</i>	I2C base pointer
-------------	------------------

13.2.7.6 void I2C_SlaveGetDefaultConfig (i2c_slave_config_t * *slaveConfig*)

The purpose of this API is to get the configuration structure initialized for use in the [I2C_SlaveInit\(\)](#). Modify fields of the structure before calling the [I2C_SlaveInit\(\)](#). This is an example.

```
* i2c_slave_config_t config;
* I2C_SlaveGetDefaultConfig(&config);
*
```

Parameters

<i>slaveConfig</i>	A pointer to the slave configuration structure.
--------------------	---

13.2.7.7 static void I2C_Enable (I2C_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	I2C base pointer
<i>enable</i>	Pass true to enable and false to disable the module.

13.2.7.8 static uint32_t I2C_MasterGetStatusFlags (I2C_Type * *base*) [inline], [static]

Parameters

<i>base</i>	I2C base pointer
-------------	------------------

Returns

status flag, use status flag to AND [_i2c_flags](#) to get the related status.

13.2.7.9 static void I2C_MasterClearStatusFlags (I2C_Type * *base*, uint32_t *statusMask*) [inline], [static]

The following status register flags can be cleared kI2C_ArbitrationLostFlag and kI2C_IntPendingFlag.

Parameters

<i>base</i>	I2C base pointer
<i>statusMask</i>	The status flag mask, defined in type i2c_status_flag_t. The parameter can be any combination of the following values: <ul style="list-style-type: none"> • kI2C_ArbitrationLostFlag • kI2C_IntPendingFlag

13.2.7.10 static uint32_t I2C_SlaveGetStatusFlags (I2C_Type * *base*) [inline], [static]

Parameters

<i>base</i>	I2C base pointer
-------------	------------------

Returns

status flag, use status flag to AND [_i2c_flags](#) to get the related status.

13.2.7.11 static void I2C_SlaveClearStatusFlags (I2C_Type * *base*, uint32_t *statusMask*) [inline], [static]

The following status register flags can be cleared kI2C_ArbitrationLostFlag and kI2C_IntPendingFlag

Parameters

<i>base</i>	I2C base pointer
<i>statusMask</i>	The status flag mask, defined in type i2c_status_flag_t. The parameter can be any combination of the following values: <ul style="list-style-type: none"> • kI2C_IntPendingFlagFlag

13.2.7.12 void I2C_EnableInterrupts (I2C_Type * *base*, uint32_t *mask*)

Parameters

<i>base</i>	I2C base pointer
<i>mask</i>	interrupt source The parameter can be combination of the following source if defined: <ul style="list-style-type: none"> • kI2C_GlobalInterruptEnable • kI2C_StopDetectInterruptEnable/kI2C_StartDetectInterruptEnable • kI2C_SdaTimeoutInterruptEnable

13.2.7.13 void I2C_DisableInterrupts (I2C_Type * *base*, uint32_t *mask*)

Parameters

<i>base</i>	I2C base pointer
<i>mask</i>	interrupt source The parameter can be combination of the following source if defined: <ul style="list-style-type: none"> • kI2C_GlobalInterruptEnable • kI2C_StopDetectInterruptEnable/kI2C_StartDetectInterruptEnable • kI2C_SdaTimeoutInterruptEnable

13.2.7.14 void I2C_MasterSetBaudRate (I2C_Type * *base*, uint32_t *baudRate_Bps*,
uint32_t *srcClock_Hz*)

Parameters

<i>base</i>	I2C base pointer
<i>baudRate_Bps</i>	the baud rate value in bps
<i>srcClock_Hz</i>	Source clock

13.2.7.15 status_t I2C_MasterStart (I2C_Type * *base*, uint8_t *address*, i2c_direction_t *direction*)

This function is used to initiate a new master mode transfer by sending the START signal. The slave address is sent following the I2C START signal.

Parameters

<i>base</i>	I2C peripheral base pointer
<i>address</i>	7-bit slave device address.
<i>direction</i>	Master transfer directions(transmit/receive).

Return values

<i>kStatus_Success</i>	Successfully send the start signal.
<i>kStatus_I2C_Busy</i>	Current bus is busy.

13.2.7.16 status_t I2C_MasterStop (I2C_Type * *base*)

Return values

<i>kStatus_Success</i>	Successfully send the stop signal.
<i>kStatus_I2C_Timeout</i>	Send stop signal failed, timeout.

13.2.7.17 status_t I2C_MasterRepeatedStart (I2C_Type * *base*, uint8_t *address*, i2c_direction_t *direction*)

Parameters

<i>base</i>	I2C peripheral base pointer
<i>address</i>	7-bit slave device address.
<i>direction</i>	Master transfer directions(transmit/receive).

Return values

<i>kStatus_Success</i>	Successfully send the start signal.
<i>kStatus_I2C_Busy</i>	Current bus is busy but not occupied by current I2C master.

13.2.7.18 status_t I2C_MasterWriteBlocking (I2C_Type * *base*, const uint8_t * *txBuff*, size_t *txSize*, uint32_t *flags*)

Parameters

<i>base</i>	The I2C peripheral base pointer.
<i>txBuff</i>	The pointer to the data to be transferred.
<i>txSize</i>	The length in bytes of the data to be transferred.
<i>flags</i>	Transfer control flag to decide whether need to send a stop, use kI2C_TransferDefaultFlag to issue a stop and kI2C_TransferNoStop to not send a stop.

Return values

<i>kStatus_Success</i>	Successfully complete the data transmission.
<i>kStatus_I2C_Arbitration-Lost</i>	Transfer error, arbitration lost.
<i>kStatus_I2C_Nak</i>	Transfer error, receive NAK during transfer.

13.2.7.19 status_t I2C_MasterReadBlocking (I2C_Type * *base*, uint8_t * *rxBuff*, size_t *rxSize*, uint32_t *flags*)

Note

The I2C_MasterReadBlocking function stops the bus before reading the final byte. Without stopping the bus prior for the final read, the bus issues another read, resulting in garbage data being read into the data register.

Parameters

<i>base</i>	I2C peripheral base pointer.
<i>rxBuff</i>	The pointer to the data to store the received data.
<i>rxSize</i>	The length in bytes of the data to be received.
<i>flags</i>	Transfer control flag to decide whether need to send a stop, use kI2C_TransferDefaultFlag to issue a stop and kI2C_TransferNoStop to not send a stop.

Return values

<i>kStatus_Success</i>	Successfully complete the data transmission.
<i>kStatus_I2C_Timeout</i>	Send stop signal failed, timeout.

13.2.7.20 **status_t I2C_SlaveWriteBlocking (I2C_Type * *base*, const uint8_t * *txBuff*, size_t *txSize*)**

Parameters

<i>base</i>	The I2C peripheral base pointer.
<i>txBuff</i>	The pointer to the data to be transferred.
<i>txSize</i>	The length in bytes of the data to be transferred.

Return values

<i>kStatus_Success</i>	Successfully complete the data transmission.
<i>kStatus_I2C_Arbitration-Lost</i>	Transfer error, arbitration lost.
<i>kStatus_I2C_Nak</i>	Transfer error, receive NAK during transfer.

13.2.7.21 **status_t I2C_SlaveReadBlocking (I2C_Type * *base*, uint8_t * *rxBuff*, size_t *rxSize*)**

Parameters

<i>base</i>	I2C peripheral base pointer.
<i>rxBuff</i>	The pointer to the data to store the received data.
<i>rxSize</i>	The length in bytes of the data to be received.

13.2.7.22 **status_t I2C_MasterTransferBlocking (I2C_Type * *base*, i2c_master_transfer_t * *xfer*)**

Note

The API does not return until the transfer succeeds or fails due to arbitration lost or receiving a NAK.

Parameters

<i>base</i>	I2C peripheral base address.
<i>xfer</i>	Pointer to the transfer structure.

Return values

<i>kStatus_Success</i>	Successfully complete the data transmission.
<i>kStatus_I2C_Busy</i>	Previous transmission still not finished.
<i>kStatus_I2C_Timeout</i>	Transfer error, wait signal timeout.
<i>kStatus_I2C_Arbitration-Lost</i>	Transfer error, arbitration lost.
<i>kStatus_I2C_Nak</i>	Transfer error, receive NAK during transfer.

13.2.7.23 void I2C_MasterTransferCreateHandle (I2C_Type * *base*, i2c_master_handle_t * *handle*, i2c_master_transfer_callback_t *callback*, void * *userData*)

Parameters

<i>base</i>	I2C base pointer.
<i>handle</i>	pointer to i2c_master_handle_t structure to store the transfer state.
<i>callback</i>	pointer to user callback function.
<i>userData</i>	user parameter passed to the callback function.

13.2.7.24 status_t I2C_MasterTransferNonBlocking (I2C_Type * *base*, i2c_master_handle_t * *handle*, i2c_master_transfer_t * *xfer*)

Note

Calling the API returns immediately after transfer initiates. The user needs to call I2C_MasterGetTransferCount to poll the transfer status to check whether the transfer is finished. If the return status is not kStatus_I2C_Busy, the transfer is finished.

Parameters

<i>base</i>	I2C base pointer.
<i>handle</i>	pointer to i2c_master_handle_t structure which stores the transfer state.
<i>xfer</i>	pointer to i2c_master_transfer_t structure.

Return values

<i>kStatus_Success</i>	Successfully start the data transmission.
<i>kStatus_I2C_Busy</i>	Previous transmission still not finished.
<i>kStatus_I2C_Timeout</i>	Transfer error, wait signal timeout.

13.2.7.25 status_t I2C_MasterTransferGetCount (I2C_Type * *base*, i2c_master_handle_t * *handle*, size_t * *count*)

Parameters

<i>base</i>	I2C base pointer.
<i>handle</i>	pointer to i2c_master_handle_t structure which stores the transfer state.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Return values

<i>kStatus_InvalidArgument</i>	count is Invalid.
<i>kStatus_Success</i>	Successfully return the count.

13.2.7.26 status_t I2C_MasterTransferAbort (I2C_Type * *base*, i2c_master_handle_t * *handle*)

Note

This API can be called at any time when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	I2C base pointer.
<i>handle</i>	pointer to i2c_master_handle_t structure which stores the transfer state

Return values

<i>kStatus_I2C_Timeout</i>	Timeout during polling flag.
<i>kStatus_Success</i>	Successfully abort the transfer.

13.2.7.27 void I2C_MasterTransferHandleIRQ (I2C_Type * *base*, void * *i2cHandle*)

Parameters

<i>base</i>	I2C base pointer.
<i>i2cHandle</i>	pointer to i2c_master_handle_t structure.

13.2.7.28 void I2C_SlaveTransferCreateHandle (I2C_Type * *base*, i2c_slave_handle_t * *handle*, i2c_slave_transfer_callback_t *callback*, void * *userData*)

Parameters

<i>base</i>	I2C base pointer.
<i>handle</i>	pointer to i2c_slave_handle_t structure to store the transfer state.
<i>callback</i>	pointer to user callback function.
<i>userData</i>	user parameter passed to the callback function.

13.2.7.29 status_t I2C_SlaveTransferNonBlocking (I2C_Type * *base*, i2c_slave_handle_t * *handle*, uint32_t *eventMask*)

Call this API after calling the [I2C_SlaveInit\(\)](#) and [I2C_SlaveTransferCreateHandle\(\)](#) to start processing transactions driven by an I2C master. The slave monitors the I2C bus and passes events to the callback that was passed into the call to [I2C_SlaveTransferCreateHandle\(\)](#). The callback is always invoked from the interrupt context.

The set of events received by the callback is customizable. To do so, set the *eventMask* parameter to the OR'd combination of [i2c_slave_transfer_event_t](#) enumerators for the events you wish to receive. The [kI2C_SlaveTransmitEvent](#) and [kLPI2C_SlaveReceiveEvent](#) events are always enabled and do not need to be included in the mask. Alternatively, pass 0 to get a default set of only the transmit and receive events that are always enabled. In addition, the [kI2C_SlaveAllEvents](#) constant is provided as a convenient way to enable all events.

Parameters

<i>base</i>	The I2C peripheral base address.
<i>handle</i>	Pointer to <code>i2c_slave_handle_t</code> structure which stores the transfer state.
<i>eventMask</i>	Bit mask formed by OR'ing together <code>i2c_slave_transfer_event_t</code> enumerators to specify which events to send to the callback. Other accepted values are 0 to get a default set of only the transmit and receive events, and <code>kI2C_SlaveAllEvents</code> to enable all events.

Return values

<i>kStatus_Success</i>	Slave transfers were successfully started.
<i>kStatus_I2C_Busy</i>	Slave transfers have already been started on this handle.

13.2.7.30 void I2C_SlaveTransferAbort (I2C_Type * *base*, i2c_slave_handle_t * *handle*)

Note

This API can be called at any time to stop slave for handling the bus events.

Parameters

<i>base</i>	I2C base pointer.
<i>handle</i>	pointer to <code>i2c_slave_handle_t</code> structure which stores the transfer state.

13.2.7.31 status_t I2C_SlaveTransferGetCount (I2C_Type * *base*, i2c_slave_handle_t * *handle*, size_t * *count*)

Parameters

<i>base</i>	I2C base pointer.
<i>handle</i>	pointer to <code>i2c_slave_handle_t</code> structure.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Return values

<i>kStatus_InvalidArgument</i>	count is Invalid.
<i>kStatus_Success</i>	Successfully return the count.

13.2.7.32 void I2C_SlaveTransferHandleIRQ (I2C_Type * *base*, void * *i2cHandle*)

Parameters

<i>base</i>	I2C base pointer.
<i>i2cHandle</i>	pointer to i2c_slave_handle_t structure which stores the transfer state

13.3 I2C FreeRTOS Driver

13.3.1 Overview

Driver version

- #define `FSL_I2C_FREERTOS_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 7)`)
I2C FreeRTOS driver version.

I2C RTOS Operation

- `status_t I2C_RTOS_Init` (`i2c_rtos_handle_t *handle`, `I2C_Type *base`, `const i2c_master_config_t *masterConfig`, `uint32_t srcClock_Hz`)
Initializes I2C.
- `status_t I2C_RTOS_Deinit` (`i2c_rtos_handle_t *handle`)
Deinitializes the I2C.
- `status_t I2C_RTOS_Transfer` (`i2c_rtos_handle_t *handle`, `i2c_master_transfer_t *transfer`)
Performs the I2C transfer.

13.3.2 Macro Definition Documentation

13.3.2.1 #define FSL_I2C_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 0, 7))

13.3.3 Function Documentation

13.3.3.1 `status_t I2C_RTOS_Init (i2c_rtos_handle_t * handle, I2C_Type * base, const i2c_master_config_t * masterConfig, uint32_t srcClock_Hz)`

This function initializes the I2C module and the related RTOS context.

Parameters

<i>handle</i>	The RTOS I2C handle, the pointer to an allocated space for RTOS context.
<i>base</i>	The pointer base address of the I2C instance to initialize.
<i>masterConfig</i>	The configuration structure to set-up I2C in master mode.
<i>srcClock_Hz</i>	The frequency of an input clock of the I2C module.

Returns

status of the operation.

13.3.3.2 status_t I2C_RTOS_Deinit (i2c_rtos_handle_t * *handle*)

This function deinitializes the I2C module and the related RTOS context.

Parameters

<i>handle</i>	The RTOS I2C handle.
---------------	----------------------

13.3.3.3 status_t I2C_RTOS_Transfer (i2c_rtos_handle_t * *handle*, i2c_master_transfer_t * *transfer*)

This function performs the I2C transfer according to the data given in the transfer structure.

Parameters

<i>handle</i>	The RTOS I2C handle.
<i>transfer</i>	A structure specifying the transfer parameters.

Returns

status of the operation.

13.4 I2C CMSIS Driver

This section describes the programming interface of the I2C Cortex Microcontroller Software Interface Standard (CMSIS) driver. This driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method see <http://www.keil.com/pack/doc/cmsis/Driver/html/index.html>.

The I2C CMSIS driver includes transactional APIs.

Transactional APIs are transaction target high-level APIs. The transactional APIs can be used to enable the peripheral quickly and also in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code accessing the hardware registers.

13.4.1 I2C CMSIS Driver

13.4.1.1 Master Operation in interrupt transactional method

```
void I2C_MasterSignalEvent_t(uint32_t event)
{
    if (event == ARM_I2C_EVENT_TRANSFER_DONE)
    {
        g_MasterCompletionFlag = true;
    }
}

/*Init I2C1*/
Driver_I2C1.Initialize(I2C_MasterSignalEvent_t);

Driver_I2C1.PowerControl(ARM_POWER_FULL);

/*config transmit speed*/
Driver_I2C1.Control(ARM_I2C_BUS_SPEED, ARM_I2C_BUS_SPEED_STANDARD);

/*start transmit*/
Driver_I2C1.MasterTransmit(I2C_MASTER_SLAVE_ADDR, g_master_buff, I2C_DATA_LENGTH, false);

/* Wait for transfer completed. */
while (!g_MasterCompletionFlag)
{
}
g_MasterCompletionFlag = false;
```

13.4.1.2 Slave Operation in interrupt transactional method

```
void I2C_SlaveSignalEvent_t(uint32_t event)
{
    /* Transfer done */
    if (event == ARM_I2C_EVENT_TRANSFER_DONE)
    {
        g_SlaveCompletionFlag = true;
    }
}

/*Init I2C1*/
Driver_I2C1.Initialize(I2C_SlaveSignalEvent_t);
```

```
Driver_I2C1.PowerControl(ARM_POWER_FULL);

/*config slave addr*/
Driver_I2C1.Control(ARM_I2C_OWN_ADDRESS, I2C_MASTER_SLAVE_ADDR);

/*start transfer*/
Driver_I2C1.SlaveReceive(g_slave_buff, I2C_DATA_LENGTH);

/* Wait for transfer completed. */
while (!g_SlaveCompletionFlag)
{
}
g_SlaveCompletionFlag = false;
```


Chapter 14

PWM: Pulse Width Modulation Driver

14.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Pulse Width Modulation (PWM) module of MCUXpresso SDK devices.

14.2 PWM Driver

14.2.1 Initialization and deinitialization

The function `PWM_Init()` initializes the PWM with a specified configurations. The function `PWM_GetDefaultConfig()` gets the default configurations. The initialization function configures the PWM for the requested register update mode for registers with buffers.

The function `PWM_Deinit()` disables the PWM counter and turns off the module clock.

14.3 Typical use case

14.3.1 PWM output

Output PWM signal on PWM3 module with different dutycycles. Periodically update the PWM signal duty cycle. Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/pwm`

Enumerations

- enum `pwm_clock_source_t` {
 `kPWM_PeripheralClock` = 1U,
 `kPWM_HighFrequencyClock`,
 `kPWM_LowFrequencyClock` }
 PWM clock source select.
- enum `pwm_fifo_water_mark_t` {
 `kPWM_FIFOWaterMark_1` = 0U,
 `kPWM_FIFOWaterMark_2`,
 `kPWM_FIFOWaterMark_3`,
 `kPWM_FIFOWaterMark_4` }
 PWM FIFO water mark select.
- enum `pwm_byte_data_swap_t` {
 `kPWM_ByteNoSwap` = 0U,
 `kPWM_ByteSwap` }
 PWM byte data swap select.

- enum `pwm_half_word_data_swap_t` {
`kPWM_HalfWordNoSwap` = 0U,
`kPWM_HalfWordSwap` }
PWM half-word data swap select.
- enum `pwm_output_configuration_t` {
`kPWM_SetAtRolloverAndClearAtcomparison` = 0U,
`kPWM_ClearAtRolloverAndSetAtcomparison`,
`kPWM_NoConfigure` }
PWM Output Configuration.
- enum `pwm_sample_repeat_t` {
`kPWM_EachSampleOnce` = 0u,
`kPWM_EachSampletwice`,
`kPWM_EachSampleFourTimes`,
`kPWM_EachSampleEightTimes` }
PWM FIFO sample repeat It determines the number of times each sample from the FIFO is to be used.
- enum `pwm_interrupt_enable_t` {
`kPWM_FIFOEmptyInterruptEnable` = (1U << 0),
`kPWM_RolloverInterruptEnable` = (1U << 1),
`kPWM_CompareInterruptEnable` = (1U << 2) }
List of PWM interrupt options.
- enum `pwm_status_flags_t` {
`kPWM_FIFOEmptyFlag` = (1U << 3),
`kPWM_RolloverFlag` = (1U << 4),
`kPWM_CompareFlag` = (1U << 5),
`kPWM_FIFOWriteErrorFlag` }
List of PWM status flags.
- enum `pwm_fifo_available_t` {
`kPWM_NoDataInFIFOFlag` = 0U,
`kPWM_OneWordInFIFOFlag`,
`kPWM_TwoWordsInFIFOFlag`,
`kPWM_ThreeWordsInFIFOFlag`,
`kPWM_FourWordsInFIFOFlag` }
List of PWM FIFO available.

Functions

- static void `PWM_SoftwareReset` (PWM_Type *base)
Software reset.
- static void `PWM_SetPeriodValue` (PWM_Type *base, uint32_t value)
Sets the PWM period value.
- static uint32_t `PWM_GetPeriodValue` (PWM_Type *base)
Gets the PWM period value.
- static uint32_t `PWM_GetCounterValue` (PWM_Type *base)
Gets the PWM counter value.

Driver version

- #define `FSL_PWM_DRIVER_VERSION` (`MAKE_VERSION`(2, 0, 0))

Version 2.0.0.

Initialization and deinitialization

- `status_t PWM_Init` (PWM_Type *base, const pwm_config_t *config)
Ungates the PWM clock and configures the peripheral for basic operation.
- `void PWM_Deinit` (PWM_Type *base)
Gate the PWM submodule clock.
- `void PWM_GetDefaultConfig` (pwm_config_t *config)
Fill in the PWM config struct with the default settings.

PWM start and stop.

- `static void PWM_StartTimer` (PWM_Type *base)
Starts the PWM counter when the PWM is enabled.
- `static void PWM_StopTimer` (PWM_Type *base)
Stops the PWM counter when the pwm is disabled.

Interrupt Interface

- `static void PWM_EnableInterrupts` (PWM_Type *base, uint32_t mask)
Enables the selected PWM interrupts.
- `static void PWM_DisableInterrupts` (PWM_Type *base, uint32_t mask)
Disables the selected PWM interrupts.
- `static uint32_t PWM_GetEnabledInterrupts` (PWM_Type *base)
Gets the enabled PWM interrupts.

Status Interface

- `static uint32_t PWM_GetStatusFlags` (PWM_Type *base)
Gets the PWM status flags.
- `static void PWM_clearStatusFlags` (PWM_Type *base, uint32_t mask)
Clears the PWM status flags.
- `static uint32_t PWM_GetFIFOAvailable` (PWM_Type *base)
Gets the PWM FIFO available.

Sample Interface

- `static void PWM_SetSampleValue` (PWM_Type *base, uint32_t value)
Sets the PWM sample value.
- `static uint32_t PWM_GetSampleValue` (PWM_Type *base)
Gets the PWM sample value.

14.4 Enumeration Type Documentation

14.4.1 enum pwm_clock_source_t

Enumerator

kPWM_PeripheralClock The Peripheral clock is used as the clock.

kPWM_HighFrequencyClock High-frequency reference clock is used as the clock.

kPWM_LowFrequencyClock Low-frequency reference clock(32KHz) is used as the clock.

14.4.2 enum pwm_fifo_water_mark_t

Sets the data level at which the FIFO empty flag will be set

Enumerator

kPWM_FIFOWaterMark_1 FIFO empty flag is set when there are more than or equal to 1 empty slots.

kPWM_FIFOWaterMark_2 FIFO empty flag is set when there are more than or equal to 2 empty slots.

kPWM_FIFOWaterMark_3 FIFO empty flag is set when there are more than or equal to 3 empty slots.

kPWM_FIFOWaterMark_4 FIFO empty flag is set when there are more than or equal to 4 empty slots.

14.4.3 enum pwm_byte_data_swap_t

It determines the byte ordering of the 16-bit data when it goes into the FIFO from the sample register.

Enumerator

kPWM_ByteNoSwap byte ordering remains the same

kPWM_ByteSwap byte ordering is reversed

14.4.4 enum pwm_half_word_data_swap_t

Enumerator

kPWM_HalfWordNoSwap Half word swapping does not take place.

kPWM_HalfWordSwap Half word from write data bus are swapped.

14.4.5 enum pwm_output_configuration_t

Enumerator

kPWM_SetAtRolloverAndClearAtcomparison Output pin is set at rollover and cleared at comparison.

kPWM_ClearAtRolloverAndSetAtcomparison Output pin is cleared at rollover and set at comparison.

kPWM_NoConfigure PWM output is disconnected.

14.4.6 enum pwm_sample_repeat_t

Enumerator

kPWM_EachSampleOnce Use each sample once.

kPWM_EachSampletwice Use each sample twice.

kPWM_EachSampleFourTimes Use each sample four times.

kPWM_EachSampleEightTimes Use each sample eight times.

14.4.7 enum pwm_interrupt_enable_t

Enumerator

kPWM_FIFOEmptyInterruptEnable This bit controls the generation of the FIFO Empty interrupt.

kPWM_RolloverInterruptEnable This bit controls the generation of the Rollover interrupt.

kPWM_CompareInterruptEnable This bit controls the generation of the Compare interrupt.

14.4.8 enum pwm_status_flags_t

Enumerator

kPWM_FIFOEmptyFlag This bit indicates the FIFO data level in comparison to the water level set by FWM field in the control register.

kPWM_RolloverFlag This bit shows that a roll-over event has occurred.

kPWM_CompareFlag This bit shows that a compare event has occurred.

kPWM_FIFOWriteErrorFlag This bit shows that an attempt has been made to write FIFO when it is full.

14.4.9 enum pwm_fifo_available_t

Enumerator

kPWM_NoDataInFIFOFlag No data available.

kPWM_OneWordInFIFOFlag 1 word of data in FIFO

kPWM_TwoWordsInFIFOFlag 2 word of data in FIFO

kPWM_ThreeWordsInFIFOFlag 3 word of data in FIFO

kPWM_FourWordsInFIFOFlag 4 word of data in FIFO

14.5 Function Documentation

14.5.1 status_t PWM_Init (PWM_Type * *base*, const pwm_config_t * *config*)

Note

This API should be called at the beginning of the application using the PWM driver.

Parameters

<i>base</i>	PWM peripheral base address
<i>config</i>	Pointer to user's PWM config structure.

Returns

kStatus_Success means success; else failed.

14.5.2 void PWM_Deinit (PWM_Type * *base*)

Parameters

<i>base</i>	PWM peripheral base address
-------------	-----------------------------

14.5.3 void PWM_GetDefaultConfig (pwm_config_t * *config*)

The default values are:

```
* config->enableStopMode = false;
* config->enableDozeMode = false;
* config->enableWaitMode = false;
* config->enableDozeMode = false;
* config->clockSource = kPWM_LowFrequencyClock;
* config->prescale = 0U;
* config->outputConfig = kPWM_SetAtRolloverAndClearAtcomparison;
* config->fifoWater = kPWM_FIFOWaterMark_2;
* config->sampleRepeat = kPWM_EachSampleOnce;
* config->byteSwap = kPWM_ByteNoSwap;
* config->halfWordSwap = kPWM_HalfWordNoSwap;
*
```

Parameters

<i>config</i>	Pointer to user's PWM config structure.
---------------	---

14.5.4 static void PWM_StartTimer (PWM_Type * *base*) [inline], [static]

When the PWM is enabled, it begins a new period, the output pin is set to start a new period while the prescaler and counter are released and counting begins.

Parameters

<i>base</i>	PWM peripheral base address
-------------	-----------------------------

14.5.5 static void PWM_StopTimer (PWM_Type * *base*) [inline], [static]

Parameters

<i>base</i>	PWM peripheral base address
-------------	-----------------------------

14.5.6 static void PWM_SoftwareReset (PWM_Type * *base*) [inline], [static]

PWM is reset when this bit is set to 1. It is a self clearing bit. Setting this bit resets all the registers to their reset values except for the STOPEN, DOZEN, WAITEN, and DBGEN bits in this control register.

Parameters

<i>base</i>	PWM peripheral base address
-------------	-----------------------------

14.5.7 static void PWM_EnableInterrupts (PWM_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	PWM peripheral base address
<i>mask</i>	The interrupts to enable. This is a logical OR of members of the enumeration pwm_interrupt_enable_t

14.5.8 static void PWM_DisableInterrupts (PWM_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	PWM peripheral base address
<i>mask</i>	The interrupts to disable. This is a logical OR of members of the enumeration pwm_interrupt_enable_t

14.5.9 static uint32_t PWM_GetEnabledInterrupts (PWM_Type * *base*) [inline], [static]

Parameters

<i>base</i>	PWM peripheral base address
-------------	-----------------------------

Returns

The enabled interrupts. This is the logical OR of members of the enumeration [pwm_interrupt_enable_t](#)

14.5.10 static uint32_t PWM_GetStatusFlags (PWM_Type * *base*) [inline], [static]

Parameters

<i>base</i>	PWM peripheral base address
-------------	-----------------------------

Returns

The status flags. This is the logical OR of members of the enumeration [pwm_status_flags_t](#)

14.5.11 **static void PWM_clearStatusFlags (PWM_Type * *base*, uint32_t *mask*)**
 [inline], [static]

Parameters

<i>base</i>	PWM peripheral base address
<i>mask</i>	The status flags to clear. This is a logical OR of members of the enumeration pwm_status_flags_t

14.5.12 static uint32_t PWM_GetFIFOAvailable (PWM_Type * *base*) [inline], [static]

Parameters

<i>base</i>	PWM peripheral base address
-------------	-----------------------------

Returns

The status flags. This is the logical OR of members of the enumeration [pwm_fifo_available_t](#)

14.5.13 static void PWM_SetSampleValue (PWM_Type * *base*, uint32_t *value*) [inline], [static]

Parameters

<i>base</i>	PWM peripheral base address
<i>value</i>	The sample value. This is the input to the 4x16 FIFO. The value in this register denotes the value of the sample being currently used.

14.5.14 static uint32_t PWM_GetSampleValue (PWM_Type * *base*) [inline], [static]

Parameters

<i>base</i>	PWM peripheral base address
-------------	-----------------------------

Returns

The sample value. It can be read only when the PWM is enable.

14.5.15 **static void PWM_SetPeriodValue (PWM_Type * *base*, uint32_t *value*)**
 [inline], [static]

Parameters

<i>base</i>	PWM peripheral base address
<i>value</i>	The period value. The PWM period register (PWM_PWMPR) determines the period of the PWM output signal. Writing 0xFFFF to this register will achieve the same result as writing 0xFFFE. $PWMO\text{ (Hz)} = PCLK\text{(Hz)} / (\text{period} + 2)$

14.5.16 **static uint32_t PWM_GetPeriodValue (PWM_Type * *base*) [inline], [static]**

Parameters

<i>base</i>	PWM peripheral base address
-------------	-----------------------------

Returns

The period value. The PWM period register (PWM_PWMPR) determines the period of the PWM output signal.

14.5.17 **static uint32_t PWM_GetCounterValue (PWM_Type * *base*) [inline], [static]**

Parameters

<i>base</i>	PWM peripheral base address
-------------	-----------------------------

Returns

The counter value. The current count value.



Chapter 15

UART: Universal Asynchronous Receiver/Transmitter Driver

15.1 Overview

Modules

- [UART CMSIS Driver](#)
- [UART Driver](#)
- [UART FreeRTOS Driver](#)
- [UART SDMA Driver](#)

15.2 UART Driver

15.2.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Universal Asynchronous Receiver/Transmitter (UART) module of MCUXpresso SDK devices.

The UART driver includes functional APIs and transactional APIs.

Functional APIs are used for UART initialization/configuration/operation for the purpose of optimization/customization. Using the functional API requires the knowledge of the UART peripheral and how to organize functional APIs to meet the application requirements. All functional APIs use the peripheral base address as the first parameter. UART functional operation groups provide the functional API set.

Transactional APIs can be used to enable the peripheral quickly and in the application if the code size and performance of transactional APIs can satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code. All transactional APIs use the `uart_handle_t` as the second parameter. Initialize the handle by calling the [UART_TransferCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer, which means that the functions [UART_TransferSendNonBlocking\(\)](#) and [UART_TransferReceiveNonBlocking\(\)](#) set up an interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the `kStatus_UART_TxIdle` and `kStatus_UART_RxIdle`.

Transactional receive APIs support the ring buffer. Prepare the memory for the ring buffer and pass in the start address and size while calling the [UART_TransferCreateHandle\(\)](#). If passing NULL, the ring buffer feature is disabled. When the ring buffer is enabled, the received data is saved to the ring buffer in the background. The [UART_TransferReceiveNonBlocking\(\)](#) function first gets data from the ring buffer. If the ring buffer does not have enough data, the function first returns the data in the ring buffer and then saves the received data to user memory. When all data is received, the upper layer is informed through a callback with the `kStatus_UART_RxIdle`.

If the receive ring buffer is full, the upper layer is informed through a callback with the `kStatus_UART_RxRingBufferOverflow`. In the callback function, the upper layer reads data out from the ring buffer. If not, existing data is overwritten by the new data.

The ring buffer size is specified when creating the handle. Note that one byte is reserved for the ring buffer maintenance. When creating handle using the following code.

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/uart`. In this example, the buffer size is 32, but only 31 bytes are used for saving data.

15.2.2 Typical use case

15.2.2.1 UART Send/receive using a polling method

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/uart`

15.2.2.2 UART Send/receive using an interrupt method

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/uart

15.2.2.3 UART Receive using the ringbuffer feature

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/uart

15.2.2.4 UART automatic baud rate detect feature

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/uart

Data Structures

- struct [uart_config_t](#)
UART configuration structure. [More...](#)
- struct [uart_transfer_t](#)
UART transfer structure. [More...](#)
- struct [uart_handle_t](#)
UART handle structure. [More...](#)

Macros

- #define [UART_RETRY_TIMES](#) 0U /* Defining to zero means to keep waiting for the flag until it is assert/deassert. */
Retry times for waiting flag.

Typedefs

- typedef void(* [uart_transfer_callback_t](#))(UART_Type *base, uart_handle_t *handle, [status_t](#) status, void *userData)
UART transfer callback function.

Enumerations

- enum {
 - kStatus_UART_TxBusy = MAKE_STATUS(kStatusGroup_IUART, 0),
 - kStatus_UART_RxBusy = MAKE_STATUS(kStatusGroup_IUART, 1),
 - kStatus_UART_TxIdle = MAKE_STATUS(kStatusGroup_IUART, 2),
 - kStatus_UART_RxIdle = MAKE_STATUS(kStatusGroup_IUART, 3),
 - kStatus_UART_TxWatermarkTooLarge = MAKE_STATUS(kStatusGroup_IUART, 4),
 - kStatus_UART_RxWatermarkTooLarge = MAKE_STATUS(kStatusGroup_IUART, 5),
 - kStatus_UART_FlagCannotClearManually,
 - kStatus_UART_Error = MAKE_STATUS(kStatusGroup_IUART, 7),
 - kStatus_UART_RxRingBufferOverflow = MAKE_STATUS(kStatusGroup_IUART, 8),
 - kStatus_UART_RxHardwareOverflow = MAKE_STATUS(kStatusGroup_IUART, 9),
 - kStatus_UART_NoiseError = MAKE_STATUS(kStatusGroup_IUART, 10),
 - kStatus_UART_FramingError = MAKE_STATUS(kStatusGroup_IUART, 11),
 - kStatus_UART_ParityError = MAKE_STATUS(kStatusGroup_IUART, 12),
 - kStatus_UART_BaudrateNotSupport,
 - kStatus_UART_BreakDetect = MAKE_STATUS(kStatusGroup_IUART, 14),
 - kStatus_UART_Timeout = MAKE_STATUS(kStatusGroup_IUART, 15) }

Error codes for the UART driver.
- enum uart_data_bits_t {
 - kUART_SevenDataBits = 0x0U,
 - kUART_EightDataBits = 0x1U }

UART data bits count.
- enum uart_parity_mode_t {
 - kUART_ParityDisabled = 0x0U,
 - kUART_ParityEven = 0x2U,
 - kUART_ParityOdd = 0x3U }

UART parity mode.
- enum uart_stop_bit_count_t {
 - kUART_OneStopBit = 0x0U,
 - kUART_TwoStopBit = 0x1U }

UART stop bit count.
- enum uart_idle_condition_t {
 - kUART_IdleFor4Frames = 0x0U,
 - kUART_IdleFor8Frames = 0x1U,
 - kUART_IdleFor16Frames = 0x2U,
 - kUART_IdleFor32Frames = 0x3U }

UART idle condition detect.
- enum _uart_interrupt_enable
 - This structure contains the settings for all of the UART interrupt configurations.*
- enum {


```

kUART_RxCharReadyFlag = 0x0000000FU,
kUART_RxErrorFlag = 0x0000000EU,
kUART_RxOverrunErrorFlag = 0x0000000DU,
kUART_RxFrameErrorFlag = 0x0000000CU,
kUART_RxBreakDetectFlag = 0x0000000BU,
kUART_RxParityErrorFlag = 0x0000000AU,
kUART_ParityErrorFlag = 0x0094000FU,
kUART_RtsStatusFlag = 0x0094000EU,
kUART_TxReadyFlag = 0x0094000DU,
kUART_RtsDeltaFlag = 0x0094000CU,
kUART_EscapeFlag = 0x0094000BU,
kUART_FrameErrorFlag = 0x0094000AU,
kUART_RxReadyFlag = 0x00940009U,
kUART_AgingTimerFlag = 0x00940008U,
kUART_DtrDeltaFlag = 0x00940007U,
kUART_RxDsFlag = 0x00940006U,
kUART_tAirWakeFlag = 0x00940005U,
kUART_AwakeFlag = 0x00940004U,
kUART_Rs485SlaveAddrMatchFlag = 0x00940003U,
kUART_AutoBaudFlag = 0x0098000FU,
kUART_TxEmptyFlag = 0x0098000EU,
kUART_DtrFlag = 0x0098000DU,
kUART_IdleFlag = 0x0098000CU,
kUART_AutoBaudCntStopFlag = 0x0098000BU,
kUART_RiDeltaFlag = 0x0098000AU,
kUART_RiFlag = 0x00980009U,
kUART_IrFlag = 0x00980008U,
kUART_WakeFlag = 0x00980007U,
kUART_DcdDeltaFlag = 0x00980006U,
kUART_DcdFlag = 0x00980005U,
kUART_RtsFlag = 0x00980004U,
kUART_TxCompleteFlag = 0x00980003U,
kUART_BreakDetectFlag = 0x00980002U,
kUART_RxOverrunFlag = 0x00980001U,
kUART_RxDataReadyFlag = 0x00980000U }

```

UART status flags.

Functions

- `uint32_t UART_GetInstance (UART_Type *base)`
Get the UART instance from peripheral base address.

Variables

- void * [s_uartHandle](#) []
Pointers to uart handles for each instance.

Driver version

- #define [FSL_UART_DRIVER_VERSION](#) ([MAKE_VERSION](#)(2, 3, 1))
UART driver version.

Software Reset

- static void [UART_SoftwareReset](#) (UART_Type *base)
Resets the UART using software.

Initialization and deinitialization

- [status_t UART_Init](#) (UART_Type *base, const [uart_config_t](#) *config, uint32_t srcClock_Hz)
Initializes an UART instance with the user configuration structure and the peripheral clock.
- void [UART_Deinit](#) (UART_Type *base)
Deinitializes a UART instance.
- void [UART_GetDefaultConfig](#) ([uart_config_t](#) *config)
l
- [status_t UART_SetBaudRate](#) (UART_Type *base, uint32_t baudRate_Bps, uint32_t srcClock_Hz)
Sets the UART instance baud rate.
- static void [UART_Enable](#) (UART_Type *base)
This function is used to Enable the UART Module.
- static void [UART_SetIdleCondition](#) (UART_Type *base, [uart_idle_condition_t](#) condition)
This function is used to configure the IDLE line condition.
- static void [UART_Disable](#) (UART_Type *base)
This function is used to Disable the UART Module.

Status

- bool [UART_GetStatusFlag](#) (UART_Type *base, uint32_t flag)
This function is used to get the current status of specific UART status flag(including interrupt flag).
- void [UART_ClearStatusFlag](#) (UART_Type *base, uint32_t flag)
This function is used to clear the current status of specific UART status flag.

Interrupts

- void [UART_EnableInterrupts](#) (UART_Type *base, uint32_t mask)
Enables UART interrupts according to the provided mask.
- void [UART_DisableInterrupts](#) (UART_Type *base, uint32_t mask)

- *Disables the UART interrupts according to the provided mask.*
- `uint32_t UART_GetEnabledInterrupts (UART_Type *base)`
Gets enabled UART interrupts.

Bus Operations

- `static void UART_EnableTx (UART_Type *base, bool enable)`
Enables or disables the UART transmitter.
- `static void UART_EnableRx (UART_Type *base, bool enable)`
Enables or disables the UART receiver.
- `static void UART_WriteByte (UART_Type *base, uint8_t data)`
Writes to the transmitter register.
- `static uint8_t UART_ReadByte (UART_Type *base)`
Reads the receiver register.
- `status_t UART_WriteBlocking (UART_Type *base, const uint8_t *data, size_t length)`
Writes to the TX register using a blocking method.
- `status_t UART_ReadBlocking (UART_Type *base, uint8_t *data, size_t length)`
Read RX data register using a blocking method.

Transactional

- `void UART_TransferCreateHandle (UART_Type *base, uart_handle_t *handle, uart_transfer_callback_t callback, void *userData)`
Initializes the UART handle.
- `void UART_TransferStartRingBuffer (UART_Type *base, uart_handle_t *handle, uint8_t *ringBuffer, size_t ringBufferSize)`
Sets up the RX ring buffer.
- `void UART_TransferStopRingBuffer (UART_Type *base, uart_handle_t *handle)`
Aborts the background transfer and uninstalls the ring buffer.
- `size_t UART_TransferGetRxRingBufferLength (uart_handle_t *handle)`
Get the length of received data in RX ring buffer.
- `status_t UART_TransferSendNonBlocking (UART_Type *base, uart_handle_t *handle, uart_transfer_t *xfer)`
Transmits a buffer of data using the interrupt method.
- `void UART_TransferAbortSend (UART_Type *base, uart_handle_t *handle)`
Aborts the interrupt-driven data transmit.
- `status_t UART_TransferGetSendCount (UART_Type *base, uart_handle_t *handle, uint32_t *count)`
Gets the number of bytes written to the UART TX register.
- `status_t UART_TransferReceiveNonBlocking (UART_Type *base, uart_handle_t *handle, uart_transfer_t *xfer, size_t *receivedBytes)`
Receives a buffer of data using an interrupt method.
- `void UART_TransferAbortReceive (UART_Type *base, uart_handle_t *handle)`
Aborts the interrupt-driven data receiving.
- `status_t UART_TransferGetReceiveCount (UART_Type *base, uart_handle_t *handle, uint32_t *count)`
Gets the number of bytes that have been received.
- `void UART_TransferHandleIRQ (UART_Type *base, void *irqHandle)`

UART IRQ handle function.

DMA control functions.

- static void [UART_EnableTxDMA](#) (UART_Type *base, bool enable)
Enables or disables the UART transmitter DMA request.
- static void [UART_EnableRxDMA](#) (UART_Type *base, bool enable)
Enables or disables the UART receiver DMA request.

FIFO control functions.

- static void [UART_SetTxFifoWatermark](#) (UART_Type *base, uint8_t watermark)
This function is used to set the watermark of UART Tx FIFO.
- static void [UART_SetRxRTSWatermark](#) (UART_Type *base, uint8_t watermark)
This function is used to set the watermark of UART RTS deassertion.
- static void [UART_SetRxFifoWatermark](#) (UART_Type *base, uint8_t watermark)
This function is used to set the watermark of UART Rx FIFO.

Auto baud rate detection.

- static void [UART_EnableAutoBaudRate](#) (UART_Type *base, bool enable)
This function is used to set the enable condition of Automatic Baud Rate Detection feature.
- static bool [UART_IsAutoBaudRateComplete](#) (UART_Type *base)
This function is used to read if the automatic baud rate detection has finished.

15.2.3 Data Structure Documentation

15.2.3.1 struct uart_config_t

Data Fields

- uint32_t [baudRate_Bps](#)
UART baud rate.
- [uart_parity_mode_t](#) [parityMode](#)
Parity error check mode of this module.
- [uart_data_bits_t](#) [dataBitsCount](#)
Data bits count, eight (default), seven.
- [uart_stop_bit_count_t](#) [stopBitCount](#)
Number of stop bits in one frame.
- uint8_t [txFifoWatermark](#)
TX FIFO watermark.
- uint8_t [rxFifoWatermark](#)
RX FIFO watermark.
- uint8_t [rxRTSWatermark](#)
RX RTS watermark, RX FIFO data count being larger than this triggers RTS deassertion.

- bool [enableAutoBaudRate](#)
Enable automatic baud rate detection.
- bool [enableTx](#)
Enable TX.
- bool [enableRx](#)
Enable RX.
- bool [enableRxRTS](#)
RX RTS enable.
- bool [enableTxCTS](#)
TX CTS enable.

Field Documentation

- (1) `uint32_t uart_config_t::baudRate_Bps`
- (2) `uart_parity_mode_t uart_config_t::parityMode`
- (3) `uart_stop_bit_count_t uart_config_t::stopBitCount`

15.2.3.2 struct `uart_transfer_t`

Data Fields

- `size_t dataSize`
The byte count to be transfer.
- `uint8_t * data`
The buffer of data to be transfer.
- `uint8_t * rxData`
The buffer to receive data.
- `const uint8_t * txData`
The buffer of data to be sent.

Field Documentation

- (1) `uint8_t* uart_transfer_t::data`
- (2) `uint8_t* uart_transfer_t::rxData`
- (3) `const uint8_t* uart_transfer_t::txData`
- (4) `size_t uart_transfer_t::dataSize`

15.2.3.3 struct `_uart_handle`

Forward declaration of the handle typedef.

Data Fields

- `const uint8_t *volatile txData`
Address of remaining data to send.

- volatile size_t `txDataSize`
Size of the remaining data to send.
- size_t `txDataSizeAll`
Size of the data to send out.
- uint8_t *volatile `rxData`
Address of remaining data to receive.
- volatile size_t `rxDataSize`
Size of the remaining data to receive.
- size_t `rxDataSizeAll`
Size of the data to receive.
- uint8_t * `rxRingBuffer`
Start address of the receiver ring buffer.
- size_t `rxRingBufferSize`
Size of the ring buffer.
- volatile uint16_t `rxRingBufferHead`
Index for the driver to store received data into ring buffer.
- volatile uint16_t `rxRingBufferTail`
Index for the user to get data from the ring buffer.
- `uart_transfer_callback_t` `callback`
Callback function.
- void * `userData`
UART callback function parameter.
- volatile uint8_t `txState`
TX transfer state.
- volatile uint8_t `rxState`
RX transfer state.

Field Documentation

- (1) `const uint8_t* volatile uart_handle_t::txData`
- (2) `volatile size_t uart_handle_t::txDataSize`
- (3) `size_t uart_handle_t::txDataSizeAll`
- (4) `uint8_t* volatile uart_handle_t::rxData`
- (5) `volatile size_t uart_handle_t::rxDataSize`
- (6) `size_t uart_handle_t::rxDataSizeAll`
- (7) `uint8_t* uart_handle_t::rxRingBuffer`
- (8) `size_t uart_handle_t::rxRingBufferSize`
- (9) `volatile uint16_t uart_handle_t::rxRingBufferHead`
- (10) `volatile uint16_t uart_handle_t::rxRingBufferTail`
- (11) `uart_transfer_callback_t uart_handle_t::callback`

(12) `void* uart_handle_t::userData`

(13) `volatile uint8_t uart_handle_t::txState`

15.2.4 Macro Definition Documentation

15.2.4.1 `#define FSL_UART_DRIVER_VERSION (MAKE_VERSION(2, 3, 1))`

15.2.4.2 `#define UART_RETRY_TIMES 0U` /* Defining to zero means to keep waiting for the flag until it is assert/deassert. */

15.2.5 Typedef Documentation

15.2.5.1 `typedef void(* uart_transfer_callback_t)(UART_Type *base, uart_handle_t *handle, status_t status, void *userData)`

15.2.6 Enumeration Type Documentation

15.2.6.1 anonymous enum

Enumerator

kStatus_UART_TxBusy Transmitter is busy.
kStatus_UART_RxBusy Receiver is busy.
kStatus_UART_TxIdle UART transmitter is idle.
kStatus_UART_RxIdle UART receiver is idle.
kStatus_UART_TxWatermarkTooLarge TX FIFO watermark too large.
kStatus_UART_RxWatermarkTooLarge RX FIFO watermark too large.
kStatus_UART_FlagCannotClearManually UART flag can't be manually cleared.
kStatus_UART_Error Error happens on UART.
kStatus_UART_RxRingBufferOverflow UART RX software ring buffer overrun.
kStatus_UART_RxHardwareOverflow UART RX receiver overrun.
kStatus_UART_NoiseError UART noise error.
kStatus_UART_FramingError UART framing error.
kStatus_UART_ParityError UART parity error.
kStatus_UART_BaudrateNotSupport Baudrate is not support in current clock source.
kStatus_UART_BreakDetect Receiver detect BREAK signal.
kStatus_UART_Timeout UART times out.

15.2.6.2 enum uart_data_bits_t

Enumerator

kUART_SevenDataBits Seven data bit.

kUART_EightDataBits Eight data bit.

15.2.6.3 enum uart_parity_mode_t

Enumerator

kUART_ParityDisabled Parity disabled.

kUART_ParityEven Even error check is selected.

kUART_ParityOdd Odd error check is selected.

15.2.6.4 enum uart_stop_bit_count_t

Enumerator

kUART_OneStopBit One stop bit.

kUART_TwoStopBit Two stop bits.

15.2.6.5 enum uart_idle_condition_t

Enumerator

kUART_IdleFor4Frames Idle for more than 4 frames.

kUART_IdleFor8Frames Idle for more than 8 frames.

kUART_IdleFor16Frames Idle for more than 16 frames.

kUART_IdleFor32Frames Idle for more than 32 frames.

15.2.6.6 enum _uart_interrupt_enable

15.2.6.7 anonymous enum

This provides constants for the UART status flags for use in the UART functions.

Enumerator

kUART_RxCharReadyFlag Rx Character Ready Flag.

kUART_RxErrorFlag Rx Error Detect Flag.

kUART_RxOverrunErrorFlag Rx Overrun Flag.

kUART_RxFrameErrorFlag Rx Frame Error Flag.

kUART_RxBreakDetectFlag Rx Break Detect Flag.

kUART_RxParityErrorFlag Rx Parity Error Flag.

kUART_ParityErrorFlag Parity Error Interrupt Flag.

kUART_RtsStatusFlag RTS_B Pin Status Flag.

kUART_TxReadyFlag Transmitter Ready Interrupt/DMA Flag.
kUART_RtsDeltaFlag RTS Delta Flag.
kUART_EscapeFlag Escape Sequence Interrupt Flag.
kUART_FrameErrorFlag Frame Error Interrupt Flag.
kUART_RxReadyFlag Receiver Ready Interrupt/DMA Flag.
kUART_AgingTimerFlag Aging Timer Interrupt Flag.
kUART_DtrDeltaFlag DTR Delta Flag.
kUART_RxDsFlag Receiver IDLE Interrupt Flag.
kUART_tAirWakeFlag Asynchronous IR WAKE Interrupt Flag.
kUART_AwakeFlag Asynchronous WAKE Interrupt Flag.
kUART_Rs485SlaveAddrMatchFlag RS-485 Slave Address Detected Interrupt Flag.
kUART_AutoBaudFlag Automatic Baud Rate Detect Complete Flag.
kUART_TxEmptyFlag Transmit Buffer FIFO Empty.
kUART_DtrFlag DTR edge triggered interrupt flag.
kUART_IdleFlag Idle Condition Flag.
kUART_AutoBaudCntStopFlag Auto-baud Counter Stopped Flag.
kUART_RiDeltaFlag Ring Indicator Delta Flag.
kUART_RiFlag Ring Indicator Input Flag.
kUART_IrFlag Serial Infrared Interrupt Flag.
kUART_WakeFlag Wake Flag.
kUART_DcdDeltaFlag Data Carrier Detect Delta Flag.
kUART_DcdFlag Data Carrier Detect Input Flag.
kUART_RtsFlag RTS Edge Triggered Interrupt Flag.
kUART_TxCompleteFlag Transmitter Complete Flag.
kUART_BreakDetectFlag BREAK Condition Detected Flag.
kUART_RxOverrunFlag Overrun Error Flag.
kUART_RxDataReadyFlag Receive Data Ready Flag.

15.2.7 Function Documentation

15.2.7.1 uint32_t UART_GetInstance (UART_Type * *base*)

Parameters

<i>base</i>	UART peripheral base address.
-------------	-------------------------------

Returns

UART instance.

15.2.7.2 static void UART_SoftwareReset (UART_Type * *base*) [inline], [static]

This function resets the transmit and receive state machines, all FIFOs and register USR1, USR2, UBIR, UBMR, UBRC , URXD, UTXD and UTS[6-3]

Parameters

<i>base</i>	UART peripheral base address.
-------------	-------------------------------

15.2.7.3 `status_t UART_Init (UART_Type * base, const uart_config_t * config, uint32_t srcClock_Hz)`

This function configures the UART module with user-defined settings. Call the [UART_GetDefaultConfig\(\)](#) function to configure the configuration structure and get the default configuration. The example below shows how to use this API to configure the UART.

```
*  uart_config_t uartConfig;
*  uartConfig.baudRate_Bps = 115200U;
*  uartConfig.parityMode = kUART_ParityDisabled;
*  uartConfig.dataBitsCount = kUART_EightDataBits;
*  uartConfig.stopBitCount = kUART_OneStopBit;
*  uartConfig.txFifoWatermark = 2;
*  uartConfig.rxFifoWatermark = 1;
*  uartConfig.enableAutoBaudrate = false;
*  uartConfig.enableTx = true;
*  uartConfig.enableRx = true;
*  UART_Init(UART1, &uartConfig, 24000000U);
*
```

Parameters

<i>base</i>	UART peripheral base address.
<i>config</i>	Pointer to a user-defined configuration structure.
<i>srcClock_Hz</i>	UART clock source frequency in HZ.

Return values

<i>kStatus_Success</i>	UART initialize succeed
------------------------	-------------------------

15.2.7.4 `void UART_Deinit (UART_Type * base)`

This function waits for transmit to complete, disables TX and RX, and disables the UART clock.

Parameters

<i>base</i>	UART peripheral base address.
-------------	-------------------------------

15.2.7.5 void UART_GetDefaultConfig (uart_config_t * *config*)

Gets the default configuration structure.

This function initializes the UART configuration structure to a default value. The default values are:
: uartConfig->baudRate_Bps = 115200U; uartConfig->parityMode = kUART_ParityDisabled; uartConfig->dataBitsCount = kUART_EightDataBits; uartConfig->stopBitCount = kUART_OneStopBit; uartConfig->txFifoWatermark = 2; uartConfig->rxFifoWatermark = 1; uartConfig->enableAutoBaudrate = false; uartConfig->enableTx = false; uartConfig->enableRx = false;

Parameters

<i>config</i>	Pointer to a configuration structure.
---------------	---------------------------------------

15.2.7.6 status_t UART_SetBaudRate (UART_Type * *base*, uint32_t *baudRate_Bps*, uint32_t *srcClock_Hz*)

This function configures the UART module baud rate. This function is used to update the UART module baud rate after the UART module is initialized by the UART_Init.

```
* UART_SetBaudRate(UART1, 115200U, 200000000U);
*
```

Parameters

<i>base</i>	UART peripheral base address.
<i>baudRate_Bps</i>	UART baudrate to be set.
<i>srcClock_Hz</i>	UART clock source frequency in Hz.

Return values

<i>kStatus_UART_Baudrate-NotSupport</i>	Baudrate is not support in the current clock source.
---	--

<i>kStatus_Success</i>	Set baudrate succeeded.
------------------------	-------------------------

15.2.7.7 static void UART_Enable (UART_Type * *base*) [inline], [static]

Parameters

<i>base</i>	UART base pointer.
-------------	--------------------

15.2.7.8 static void UART_SetIdleCondition (UART_Type * *base*, uart_idle_condition_t *condition*) [inline], [static]

Parameters

<i>base</i>	UART base pointer.
<i>condition</i>	IDLE line detect condition of the enumerators in uart_idle_condition_t .

15.2.7.9 static void UART_Disable (UART_Type * *base*) [inline], [static]

Parameters

<i>base</i>	UART base pointer.
-------------	--------------------

15.2.7.10 bool UART_GetStatusFlag (UART_Type * *base*, uint32_t *flag*)

The available status flag can be select from [uart_status_flag_t](#) enumeration.

Parameters

<i>base</i>	UART base pointer.
<i>flag</i>	Status flag to check.

Return values

<i>current</i>	state of corresponding status flag.
----------------	-------------------------------------

15.2.7.11 void UART_ClearStatusFlag (UART_Type * *base*, uint32_t *flag*)

The available status flag can be select from `uart_status_flag_t` enumeration.

Parameters

<i>base</i>	UART base pointer.
<i>flag</i>	Status flag to clear.

15.2.7.12 void UART_EnableInterrupts (UART_Type * *base*, uint32_t *mask*)

This function enables the UART interrupts according to the provided mask. The mask is a logical OR of enumeration members. See [_uart_interrupt_enable](#). For example, to enable TX empty interrupt and RX data ready interrupt, do the following.

```
*   UART_EnableInterrupts(UART1, kUART_TxEmptyEnable | kUART_RxDataReadyEnable);
*
```

Parameters

<i>base</i>	UART peripheral base address.
<i>mask</i>	The interrupts to enable. Logical OR of _uart_interrupt_enable .

15.2.7.13 void UART_DisableInterrupts (UART_Type * *base*, uint32_t *mask*)

This function disables the UART interrupts according to the provided mask. The mask is a logical OR of enumeration members. See [_uart_interrupt_enable](#). For example, to disable TX empty interrupt and RX data ready interrupt do the following.

```
*   UART_EnableInterrupts(UART1, kUART_TxEmptyEnable | kUART_RxDataReadyEnable);
*
```

Parameters

<i>base</i>	UART peripheral base address.
<i>mask</i>	The interrupts to disable. Logical OR of _uart_interrupt_enable .

15.2.7.14 uint32_t UART_GetEnabledInterrupts (UART_Type * *base*)

This function gets the enabled UART interrupts. The enabled interrupts are returned as the logical OR value of the enumerators [_uart_interrupt_enable](#). To check a specific interrupt enable status, compare the return value with enumerators in [_uart_interrupt_enable](#). For example, to check whether the TX empty interrupt is enabled:

```
*   uint32_t enabledInterrupts = UART_GetEnabledInterrupts(UART1);
*
*   if (kUART_TxEmptyEnable & enabledInterrupts)
*   {
*       ...
*   }
*
```

Parameters

<i>base</i>	UART peripheral base address.
-------------	-------------------------------

Returns

UART interrupt flags which are logical OR of the enumerators in [_uart_interrupt_enable](#).

15.2.7.15 static void UART_EnableTx (UART_Type * *base*, bool *enable*) [inline], [static]

This function enables or disables the UART transmitter.

Parameters

<i>base</i>	UART peripheral base address.
<i>enable</i>	True to enable, false to disable.

15.2.7.16 static void UART_EnableRx (UART_Type * *base*, bool *enable*) [inline], [static]

This function enables or disables the UART receiver.

Parameters

<i>base</i>	UART peripheral base address.
<i>enable</i>	True to enable, false to disable.

15.2.7.17 static void UART_WriteByte (UART_Type * *base*, uint8_t *data*) [inline], [static]

This function is used to write data to transmitter register. The upper layer must ensure that the TX register is empty or that the TX FIFO has room before calling this function.

Parameters

<i>base</i>	UART peripheral base address.
<i>data</i>	Data write to the TX register.

15.2.7.18 static uint8_t UART_ReadByte (UART_Type * *base*) [inline], [static]

This function is used to read data from receiver register. The upper layer must ensure that the receiver register is full or that the RX FIFO has data before calling this function.

Parameters

<i>base</i>	UART peripheral base address.
-------------	-------------------------------

Returns

Data read from data register.

15.2.7.19 status_t UART_WriteBlocking (UART_Type * *base*, const uint8_t * *data*, size_t *length*)

This function polls the TX register, waits for the TX register to be empty or for the TX FIFO to have room and writes data to the TX buffer.

Parameters

<i>base</i>	UART peripheral base address.
<i>data</i>	Start address of the data to write.
<i>length</i>	Size of the data to write.

Return values

<i>kStatus_UART_Timeout</i>	Transmission timed out and was aborted.
<i>kStatus_Success</i>	Successfully wrote all data.

15.2.7.20 **status_t UART_ReadBlocking (UART_Type * *base*, uint8_t * *data*, size_t *length*)**

This function polls the RX register, waits for the RX register to be full or for RX FIFO to have data, and reads data from the TX register.

Parameters

<i>base</i>	UART peripheral base address.
<i>data</i>	Start address of the buffer to store the received data.
<i>length</i>	Size of the buffer.

Return values

<i>kStatus_UART_Rx-HardwareOverrun</i>	Receiver overrun occurred while receiving data.
<i>kStatus_UART_Noise-Error</i>	A noise error occurred while receiving data.
<i>kStatus_UART_Framing-Error</i>	A framing error occurred while receiving data.
<i>kStatus_UART_Parity-Error</i>	A parity error occurred while receiving data.
<i>kStatus_UART_Timeout</i>	Transmission timed out and was aborted.
<i>kStatus_Success</i>	Successfully received all data.

15.2.7.21 **void UART_TransferCreateHandle (UART_Type * *base*, uart_handle_t * *handle*, uart_transfer_callback_t *callback*, void * *userData*)**

This function initializes the UART handle which can be used for other UART transactional APIs. Usually, for a specified UART instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	UART handle pointer.
<i>callback</i>	The callback function.
<i>userData</i>	The parameter of the callback function.

15.2.7.22 void UART_TransferStartRingBuffer (UART_Type * *base*, uart_handle_t * *handle*, uint8_t * *ringBuffer*, size_t *ringBufferSize*)

This function sets up the RX ring buffer to a specific UART handle.

When the RX ring buffer is used, data received are stored into the ring buffer even when the user doesn't call the [UART_TransferReceiveNonBlocking\(\)](#) API. If data is already received in the ring buffer, the user can get the received data from the ring buffer directly.

Note

When using the RX ring buffer, one byte is reserved for internal use. In other words, if `ringBufferSize` is 32, only 31 bytes are used for saving data.

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	UART handle pointer.
<i>ringBuffer</i>	Start address of the ring buffer for background receiving. Pass NULL to disable the ring buffer.
<i>ringBufferSize</i>	Size of the ring buffer.

15.2.7.23 void UART_TransferStopRingBuffer (UART_Type * *base*, uart_handle_t * *handle*)

This function aborts the background transfer and uninstalls the ring buffer.

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	UART handle pointer.

15.2.7.24 **size_t UART_TransferGetRxRingBufferLength (uart_handle_t * *handle*)**

Parameters

<i>handle</i>	UART handle pointer.
---------------	----------------------

Returns

Length of received data in RX ring buffer.

15.2.7.25 **status_t UART_TransferSendNonBlocking (UART_Type * *base*, uart_handle_t * *handle*, uart_transfer_t * *xfer*)**

This function sends data using an interrupt method. This is a non-blocking function, which returns directly without waiting for all data to be written to the TX register. When all data is written to the TX register in the ISR, the UART driver calls the callback function and passes the [kStatus_UART_TxIdle](#) as status parameter.

Note

The [kStatus_UART_TxIdle](#) is passed to the upper layer when all data is written to the TX register. However, it does not ensure that all data is sent out. Before disabling the TX, check the [kUART_TransmissionCompleteFlag](#) to ensure that the TX is finished.

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	UART handle pointer.
<i>xfer</i>	UART transfer structure. See uart_transfer_t .

Return values

<i>kStatus_Success</i>	Successfully start the data transmission.
<i>kStatus_UART_TxBusy</i>	Previous transmission still not finished; data not all written to TX register yet.
<i>kStatus_InvalidArgument</i>	Invalid argument.

15.2.7.26 void UART_TransferAbortSend (UART_Type * *base*, uart_handle_t * *handle*)

This function aborts the interrupt-driven data sending. The user can get the remainBytes to find out how many bytes are not sent out.

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	UART handle pointer.

15.2.7.27 status_t UART_TransferGetSendCount (UART_Type * *base*, uart_handle_t * *handle*, uint32_t * *count*)

This function gets the number of bytes written to the UART TX register by using the interrupt method.

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	UART handle pointer.
<i>count</i>	Send bytes count.

Return values

<i>kStatus_NoTransferInProgress</i>	No send in progress.
<i>kStatus_InvalidArgument</i>	The parameter is invalid.
<i>kStatus_Success</i>	Get successfully through the parameter <i>count</i> ;

15.2.7.28 status_t UART_TransferReceiveNonBlocking (UART_Type * *base*, uart_handle_t * *handle*, uart_transfer_t * *xfer*, size_t * *receivedBytes*)

This function receives data using an interrupt method. This is a non-blocking function, which returns without waiting for all data to be received. If the RX ring buffer is used and not empty, the data in the ring buffer is copied and the parameter *receivedBytes* shows how many bytes are copied from the ring

buffer. After copying, if the data in the ring buffer is not enough to read, the receive request is saved by the UART driver. When the new data arrives, the receive request is serviced first. When all data is received, the UART driver notifies the upper layer through a callback function and passes the status parameter `kStatus_UART_RxIdle`. For example, the upper layer needs 10 bytes but there are only 5 bytes in the ring buffer. The 5 bytes are copied to the `xfer->data` and this function returns with the parameter `receivedBytes` set to 5. For the left 5 bytes, newly arrived data is saved from the `xfer->data[5]`. When 5 bytes are received, the UART driver notifies the upper layer. If the RX ring buffer is not enabled, this function enables the RX and RX interrupt to receive data to the `xfer->data`. When all data is received, the upper layer is notified.

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	UART handle pointer.
<i>xfer</i>	UART transfer structure, see uart_transfer_t .
<i>receivedBytes</i>	Bytes received from the ring buffer directly.

Return values

<i>kStatus_Success</i>	Successfully queue the transfer into transmit queue.
<i>kStatus_UART_RxBusy</i>	Previous receive request is not finished.
<i>kStatus_InvalidArgument</i>	Invalid argument.

15.2.7.29 void UART_TransferAbortReceive (UART_Type * *base*, uart_handle_t * *handle*)

This function aborts the interrupt-driven data receiving. The user can get the `remainBytes` to know how many bytes are not received yet.

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	UART handle pointer.

15.2.7.30 status_t UART_TransferGetReceiveCount (UART_Type * *base*, uart_handle_t * *handle*, uint32_t * *count*)

This function gets the number of bytes that have been received.

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	UART handle pointer.
<i>count</i>	Receive bytes count.

Return values

<i>kStatus_NoTransferInProgress</i>	No receive in progress.
<i>kStatus_InvalidArgument</i>	Parameter is invalid.
<i>kStatus_Success</i>	Get successfully through the parameter <code>count</code> ;

15.2.7.31 void UART_TransferHandleIRQ (UART_Type * *base*, void * *irqHandle*)

This function handles the UART transmit and receive IRQ request.

Parameters

<i>base</i>	UART peripheral base address.
<i>irqHandle</i>	UART handle pointer.

15.2.7.32 static void UART_EnableTxDMA (UART_Type * *base*, bool *enable*) [inline], [static]

This function enables or disables the transmit request when the transmitter has one or more slots available in the TxFIFO. The fill level in the TxFIFO that generates the DMA request is controlled by the TXTL bits.

Parameters

<i>base</i>	UART peripheral base address.
<i>enable</i>	True to enable, false to disable.

15.2.7.33 static void UART_EnableRxDMA (UART_Type * *base*, bool *enable*) [inline], [static]

This function enables or disables the receive request when the receiver has data in the Rx FIFO. The fill level in the Rx FIFO at which a DMA request is generated is controlled by the RXTL bits .

Parameters

<i>base</i>	UART peripheral base address.
<i>enable</i>	True to enable, false to disable.

15.2.7.34 static void UART_SetTxFifoWatermark (UART_Type * *base*, uint8_t *watermark*) [inline], [static]

A maskable interrupt is generated whenever the data level in the TxFIFO falls below the Tx FIFO watermark.

Parameters

<i>base</i>	UART base pointer.
<i>watermark</i>	The Tx FIFO watermark.

15.2.7.35 static void UART_SetRxRTSWatermark (UART_Type * *base*, uint8_t *watermark*) [inline], [static]

The RTS signal deasserts whenever the data count in RxFIFO reaches the Rx RTS watermark.

Parameters

<i>base</i>	UART base pointer.
<i>watermark</i>	The Rx RTS watermark.

15.2.7.36 static void UART_SetRxFifoWatermark (UART_Type * *base*, uint8_t *watermark*) [inline], [static]

A maskable interrupt is generated whenever the data level in the RxFIFO reaches the Rx FIFO watermark.

Parameters

<i>base</i>	UART base pointer.
-------------	--------------------

<i>watermark</i>	The Rx FIFO watermark.
------------------	------------------------

15.2.7.37 static void UART_EnableAutoBaudRate (UART_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	UART base pointer.
<i>enable</i>	Enable/Disable Automatic Baud Rate Detection feature. <ul style="list-style-type: none"> • true: Enable Automatic Baud Rate Detection feature. • false: Disable Automatic Baud Rate Detection feature.

15.2.7.38 static bool UART_IsAutoBaudRateComplete (UART_Type * *base*) [inline], [static]

Parameters

<i>base</i>	UART base pointer.
-------------	--------------------

Returns

- true: Automatic baud rate detection has finished.
- false: Automatic baud rate detection has not finished.

15.2.8 Variable Documentation

15.2.8.1 void* s_uartHandle[]

15.3 UART FreeRTOS Driver

15.3.1 Overview

Data Structures

- struct `uart_rtos_config_t`
UART configuration structure. [More...](#)

Driver version

- #define `FSL_UART_FREERTOS_DRIVER_VERSION` (`MAKE_VERSION(2, 1, 1)`)
UART FreeRTOS driver version 2.1.1.

UART RTOS Operation

- int `UART_RTOS_Init` (`uart_rtos_handle_t *handle`, `uart_handle_t *t_handle`, const `uart_rtos_config_t *cfg`)
Initializes a UART instance for operation in RTOS.
- int `UART_RTOS_Deinit` (`uart_rtos_handle_t *handle`)
Deinitializes a UART instance for operation.

UART transactional Operation

- int `UART_RTOS_Send` (`uart_rtos_handle_t *handle`, `uint8_t *buffer`, `uint32_t length`)
Sends data in the background.
- int `UART_RTOS_Receive` (`uart_rtos_handle_t *handle`, `uint8_t *buffer`, `uint32_t length`, `size_t *received`)
Receives data.

15.3.2 Data Structure Documentation

15.3.2.1 struct `uart_rtos_config_t`

Data Fields

- `UART_Type * base`
UART base address.
- `uint32_t srcclk`
UART source clock in Hz.
- `uint32_t baudrate`
Desired communication speed.
- `uart_parity_mode_t parity`
Parity setting.

- `uart_stop_bit_count_t stopbits`
Number of stop bits to use.
- `uint8_t * buffer`
Buffer for background reception.
- `uint32_t buffer_size`
Size of buffer for background reception.

15.3.3 Macro Definition Documentation

15.3.3.1 `#define FSL_UART_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 1, 1))`

15.3.4 Function Documentation

15.3.4.1 `int UART_RTOS_Init (uart_rtos_handle_t * handle, uart_handle_t * t_handle, const uart_rtos_config_t * cfg)`

Parameters

<i>handle</i>	The RTOS UART handle, the pointer to an allocated space for RTOS context.
<i>t_handle</i>	The pointer to the allocated space to store the transactional layer internal state.
<i>cfg</i>	The pointer to the parameters required to configure the UART after initialization.

Returns

0 succeed; otherwise fail.

15.3.4.2 `int UART_RTOS_Deinit (uart_rtos_handle_t * handle)`

This function deinitializes the UART module, sets all register values to reset value, and frees the resources.

Parameters

<i>handle</i>	The RTOS UART handle.
---------------	-----------------------

15.3.4.3 `int UART_RTOS_Send (uart_rtos_handle_t * handle, uint8_t * buffer, uint32_t length)`

This function sends data. It is a synchronous API. If the hardware buffer is full, the task is in the blocked state.

Parameters

<i>handle</i>	The RTOS UART handle.
<i>buffer</i>	The pointer to the buffer to send.
<i>length</i>	The number of bytes to send.

15.3.4.4 int UART_RTOS_Receive (uart_rtos_handle_t * *handle*, uint8_t * *buffer*, uint32_t *length*, size_t * *received*)

This function receives data from UART. It is a synchronous API. If data is immediately available, it is returned immediately and the number of bytes received.

Parameters

<i>handle</i>	The RTOS UART handle.
<i>buffer</i>	The pointer to the buffer to write received data.
<i>length</i>	The number of bytes to receive.
<i>received</i>	The pointer to a variable of size_t where the number of received data is filled.

15.4 UART SDMA Driver

15.4.1 Overview

Data Structures

- struct `uart_sdma_handle_t`
UART sDMA handle. [More...](#)

Typedefs

- typedef void(* `uart_sdma_transfer_callback_t`)(UART_Type *base, uart_sdma_handle_t *handle, `status_t` status, void *userData)
UART transfer callback function.

Driver version

- #define `FSL_UART_SDMA_DRIVER_VERSION` (`MAKE_VERSION`(2, 3, 0))
UART SDMA driver version.

sDMA transactional

- void `UART_TransferCreateHandleSDMA` (UART_Type *base, uart_sdma_handle_t *handle, `uart_sdma_transfer_callback_t` callback, void *userData, `sdma_handle_t` *txSdmaHandle, `sdma_handle_t` *rxSdmaHandle, uint32_t eventSourceTx, uint32_t eventSourceRx)
Initializes the UART handle which is used in transactional functions.
- `status_t` `UART_SendSDMA` (UART_Type *base, uart_sdma_handle_t *handle, `uart_transfer_t` *xfer)
Sends data using sDMA.
- `status_t` `UART_ReceiveSDMA` (UART_Type *base, uart_sdma_handle_t *handle, `uart_transfer_t` *xfer)
Receives data using sDMA.
- void `UART_TransferAbortSendSDMA` (UART_Type *base, uart_sdma_handle_t *handle)
Aborts the sent data using sDMA.
- void `UART_TransferAbortReceiveSDMA` (UART_Type *base, uart_sdma_handle_t *handle)
Aborts the receive data using sDMA.
- void `UART_TransferSdmaHandleIRQ` (UART_Type *base, void *uartSdmaHandle)
UART IRQ handle function.

15.4.2 Data Structure Documentation

15.4.2.1 struct _uart_sdma_handle

Data Fields

- [uart_sdma_transfer_callback_t](#) *callback*
Callback function.
- void * [userData](#)
UART callback function parameter.
- size_t [rxDataSizeAll](#)
Size of the data to receive.
- size_t [txDataSizeAll](#)
Size of the data to send out.
- [sdma_handle_t](#) * [txSdmaHandle](#)
The sDMA TX channel used.
- [sdma_handle_t](#) * [rxSdmaHandle](#)
The sDMA RX channel used.
- volatile uint8_t [txState](#)
TX transfer state.
- volatile uint8_t [rxState](#)
RX transfer state.

Field Documentation

- (1) [uart_sdma_transfer_callback_t](#) [uart_sdma_handle_t::callback](#)
- (2) void* [uart_sdma_handle_t::userData](#)
- (3) size_t [uart_sdma_handle_t::rxDataSizeAll](#)
- (4) size_t [uart_sdma_handle_t::txDataSizeAll](#)
- (5) [sdma_handle_t](#)* [uart_sdma_handle_t::txSdmaHandle](#)
- (6) [sdma_handle_t](#)* [uart_sdma_handle_t::rxSdmaHandle](#)
- (7) volatile uint8_t [uart_sdma_handle_t::txState](#)

15.4.3 Macro Definition Documentation

15.4.3.1 #define FSL_UART_SDMA_DRIVER_VERSION (MAKE_VERSION(2, 3, 0))

15.4.4 Typedef Documentation

15.4.4.1 typedef void(* [uart_sdma_transfer_callback_t](#))(UART_Type *base, [uart_sdma_handle_t](#) *handle, status_t status, void *userData)

15.4.5 Function Documentation

15.4.5.1 void UART_TransferCreateHandleSDMA (UART_Type * *base*,
uart_sdma_handle_t * *handle*, uart_sdma_transfer_callback_t *callback*, void *
userData, sdma_handle_t * *txSdmaHandle*, sdma_handle_t * *rxSdmaHandle*,
uint32_t *eventSourceTx*, uint32_t *eventSourceRx*)

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	Pointer to the <code>uart_sdma_handle_t</code> structure.
<i>callback</i>	UART callback, NULL means no callback.
<i>userData</i>	User callback function data.
<i>rxSdmaHandle</i>	User-requested DMA handle for RX DMA transfer.
<i>txSdmaHandle</i>	User-requested DMA handle for TX DMA transfer.
<i>eventSourceTx</i>	Eventsource for TX DMA transfer.
<i>eventSourceRx</i>	Eventsource for RX DMA transfer.

15.4.5.2 `status_t UART_SendSDMA (UART_Type * base, uart_sdma_handle_t * handle, uart_transfer_t * xfer)`

This function sends data using sDMA. This is a non-blocking function, which returns right away. When all data is sent, the send callback function is called.

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	UART handle pointer.
<i>xfer</i>	UART sDMA transfer structure. See uart_transfer_t .

Return values

<i>kStatus_Success</i>	if succeeded; otherwise failed.
<i>kStatus_UART_TxBusy</i>	Previous transfer ongoing.
<i>kStatus_InvalidArgument</i>	Invalid argument.

15.4.5.3 `status_t UART_ReceiveSDMA (UART_Type * base, uart_sdma_handle_t * handle, uart_transfer_t * xfer)`

This function receives data using sDMA. This is a non-blocking function, which returns right away. When all data is received, the receive callback function is called.

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	Pointer to the <code>uart_sdma_handle_t</code> structure.
<i>xfer</i>	UART sDMA transfer structure. See uart_transfer_t .

Return values

<i>kStatus_Success</i>	if succeeded; otherwise failed.
<i>kStatus_UART_RxBusy</i>	Previous transfer ongoing.
<i>kStatus_InvalidArgument</i>	Invalid argument.

15.4.5.4 void UART_TransferAbortSendSDMA (UART_Type * *base*, `uart_sdma_handle_t` * *handle*)

This function aborts sent data using sDMA.

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	Pointer to the <code>uart_sdma_handle_t</code> structure.

15.4.5.5 void UART_TransferAbortReceiveSDMA (UART_Type * *base*, `uart_sdma_handle_t` * *handle*)

This function aborts receive data using sDMA.

Parameters

<i>base</i>	UART peripheral base address.
<i>handle</i>	Pointer to the <code>uart_sdma_handle_t</code> structure.

15.4.5.6 void UART_TransferSdmaHandleIRQ (UART_Type * *base*, void * *uartSdmaHandle*)

This function handles the UART transmit complete IRQ request and invoke user callback.

Parameters

<i>base</i>	UART peripheral base address.
<i>uartSdma-Handle</i>	UART handle pointer.

15.5 UART CMSIS Driver

This section describes the programming interface of the UART Cortex Microcontroller Software Interface Standard (CMSIS) driver. And this driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method please refer to <http://www.keil.com/pack/doc/cmsis/Driver/html/index.html>.

The UART driver includes transactional APIs.

Transactional APIs can be used to enable the peripheral quickly and in the application if the code size and performance of transactional APIs can satisfy the requirements. If the code size and performance are critical requirements please write custom code.

15.5.1 Function groups

15.5.1.1 UART CMSIS GetVersion Operation

This function group will return the UART CMSIS Driver version to user.

15.5.1.2 UART CMSIS GetCapabilities Operation

This function group will return the capabilities of this driver.

15.5.1.3 UART CMSIS Initialize and Uninitialize Operation

This function will initialize and uninitialize the uart instance . And this API must be called before you configure an uart instance or after you Deinit an uart instance. The right steps to start an instance is that you must initialize the instance which been selected firstly, then you can power on the instance. After these all have been done, you can configure the instance by using control operation. If you want to Uninitialize the instance, you must power off the instance first.

15.5.1.4 UART CMSIS Transfer Operation

This function group controls the transfer, send/receive data.

15.5.1.5 UART CMSIS Status Operation

This function group gets the UART transfer status.

15.5.1.6 UART CMSIS Control Operation

This function can configure an instance ,set baudrate for uart, get current baudrate ,set transfer data bits and other control command.

Chapter 16

MU: Messaging Unit

16.1 Overview

The MCUXpresso SDK provides a driver for the MU module of MCUXpresso SDK devices.

16.2 Function description

The MU driver provides these functions:

- Functions to initialize the MU module.
- Functions to send and receive messages.
- Functions for MU flags for both MU sides.
- Functions for status flags and interrupts.
- Other miscellaneous functions.

16.2.1 MU initialization

The function [MU_Init\(\)](#) initializes the MU module and enables the MU clock. It should be called before any other MU functions.

The function [MU_Deinit\(\)](#) deinitializes the MU module and disables the MU clock. No MU functions can be called after this function.

16.2.2 MU message

The MU message must be sent when the transmit register is empty. The MU driver provides blocking API and non-blocking API to send message.

The [MU_SendMsgNonBlocking\(\)](#) function writes a message to the MU transmit register without checking the transmit register status. The upper layer should check that the transmit register is empty before calling this function. This function can be used in the ISR for better performance.

The [MU_SendMsg\(\)](#) function is a blocking function. It waits until the transmit register is empty and sends the message.

Correspondingly, there are blocking and non-blocking APIs for receiving a message. The [MU_ReadMsgNonBlocking\(\)](#) function is a non-blocking API. The [MU_ReadMsg\(\)](#) function is the blocking API.

16.2.3 MU flags

The MU driver provides 3-bit general purpose flags. When the flags are set on one side, they are reflected on the other side.

The MU flags must be set when the previous flags have been updated to the other side. The MU driver provides a non-blocking function and a blocking function. The blocking function [MU_SetFlags\(\)](#) waits until previous flags have been updated to the other side and then sets flags. The non-blocking function sets the flags directly. Ensure that the `kMU_FlagsUpdatingFlag` is not pending before calling this function.

The function [MU_GetFlags\(\)](#) gets the MU flags on the current side.

16.2.4 Status and interrupt

The function [MU_GetStatusFlags\(\)](#) returns all MU status flags. Use the `_mu_status_flags` to check for specific flags, for example, to check RX0 and RX1 register full, use the following code:

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/mu`. The receive full flags are cleared automatically after messages are read out. The transmit empty flags are cleared automatically after new messages are written to the transmit register. The general purpose interrupt flags must be cleared manually using the function [MU_ClearStatusFlags\(\)](#).

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/mu`. To enable or disable a specific interrupt, use [MU_EnableInterrupts\(\)](#) and [MU_DisableInterrupts\(\)](#) functions. The interrupts to enable or disable should be passed in as a bit mask of the `_mu_interrupt_enable`.

The [MU_TriggerInterrupts\(\)](#) function triggers general purpose interrupts and NMI to the other core. The interrupts to trigger are passed in as a bit mask of the `_mu_interrupt_trigger`. If previously triggered interrupts have not been processed by the other side, this function returns an error.

16.2.5 MU misc functions

The [MU_BootCoreB\(\)](#) and [MU_HoldCoreBReset\(\)](#) functions should only be used from A side. They are used to boot the core B or to hold core B in reset.

The [MU_ResetBothSides\(\)](#) function resets MU at both A and B sides. However, only the A side can call this function.

If a core enters stop mode, the platform clock of this core is disabled by default. The function [MU_SetClockOnOtherCoreEnable\(\)](#) forces the other core's platform clock to remain enabled even after that core has entered a stop mode. In this case, the other core's platform clock keeps running until the current core enters stop mode too.

Function [MU_GetOtherCorePowerMode\(\)](#) gets the power mode of the other core.

Enumerations

- enum `_mu_status_flags` {
`kMU_Tx0EmptyFlag` = (1U << (MU_SR_TEn_SHIFT + 3U)),
`kMU_Tx1EmptyFlag` = (1U << (MU_SR_TEn_SHIFT + 2U)),
`kMU_Tx2EmptyFlag` = (1U << (MU_SR_TEn_SHIFT + 1U)),
`kMU_Tx3EmptyFlag` = (1U << (MU_SR_TEn_SHIFT + 0U)),
`kMU_Rx0FullFlag` = (1U << (MU_SR_RFn_SHIFT + 3U)),
`kMU_Rx1FullFlag` = (1U << (MU_SR_RFn_SHIFT + 2U)),
`kMU_Rx2FullFlag` = (1U << (MU_SR_RFn_SHIFT + 1U)),
`kMU_Rx3FullFlag` = (1U << (MU_SR_RFn_SHIFT + 0U)),
`kMU_GenInt0Flag` = (1U << (MU_SR_GIPn_SHIFT + 3U)),
`kMU_GenInt1Flag` = (1U << (MU_SR_GIPn_SHIFT + 2U)),
`kMU_GenInt2Flag` = (1U << (MU_SR_GIPn_SHIFT + 1U)),
`kMU_GenInt3Flag` = (1U << (MU_SR_GIPn_SHIFT + 0U)),
`kMU_EventPendingFlag` = MU_SR_EP_MASK,
`kMU_FlagsUpdatingFlag` = MU_SR_FUP_MASK,
`kMU_OtherSideInResetFlag` = MU_SR_RS_MASK }
MU status flags.
- enum `_mu_interrupt_enable` {
`kMU_Tx0EmptyInterruptEnable` = (1U << (MU_CR_TIEEn_SHIFT + 3U)),
`kMU_Tx1EmptyInterruptEnable` = (1U << (MU_CR_TIEEn_SHIFT + 2U)),
`kMU_Tx2EmptyInterruptEnable` = (1U << (MU_CR_TIEEn_SHIFT + 1U)),
`kMU_Tx3EmptyInterruptEnable` = (1U << (MU_CR_TIEEn_SHIFT + 0U)),
`kMU_Rx0FullInterruptEnable` = (1U << (MU_CR_RIEEn_SHIFT + 3U)),
`kMU_Rx1FullInterruptEnable` = (1U << (MU_CR_RIEEn_SHIFT + 2U)),
`kMU_Rx2FullInterruptEnable` = (1U << (MU_CR_RIEEn_SHIFT + 1U)),
`kMU_Rx3FullInterruptEnable` = (1U << (MU_CR_RIEEn_SHIFT + 0U)),
`kMU_GenInt0InterruptEnable` = (int)(1U << (MU_CR_GIEEn_SHIFT + 3U)),
`kMU_GenInt1InterruptEnable` = (1U << (MU_CR_GIEEn_SHIFT + 2U)),
`kMU_GenInt2InterruptEnable` = (1U << (MU_CR_GIEEn_SHIFT + 1U)),
`kMU_GenInt3InterruptEnable` = (1U << (MU_CR_GIEEn_SHIFT + 0U)) }
MU interrupt source to enable.
- enum `_mu_interrupt_trigger` {
`kMU_GenInt0InterruptTrigger` = (1U << (MU_CR_GIRn_SHIFT + 3U)),
`kMU_GenInt1InterruptTrigger` = (1U << (MU_CR_GIRn_SHIFT + 2U)),
`kMU_GenInt2InterruptTrigger` = (1U << (MU_CR_GIRn_SHIFT + 1U)),
`kMU_GenInt3InterruptTrigger` = (1U << (MU_CR_GIRn_SHIFT + 0U)) }
MU interrupt that could be triggered to the other core.
- enum `mu_msg_reg_index_t`
MU message register.

Driver version

- #define `FSL_MU_DRIVER_VERSION` (`MAKE_VERSION`(2, 1, 0))
MU driver version.

MU initialization.

- void [MU_Init](#) (MU_Type *base)
Initializes the MU module.
- void [MU_Deinit](#) (MU_Type *base)
De-initializes the MU module.

MU Message

- static void [MU_SendMsgNonBlocking](#) (MU_Type *base, uint32_t regIndex, uint32_t msg)
Writes a message to the TX register.
- void [MU_SendMsg](#) (MU_Type *base, uint32_t regIndex, uint32_t msg)
Blocks to send a message.
- static uint32_t [MU_ReceiveMsgNonBlocking](#) (MU_Type *base, uint32_t regIndex)
Reads a message from the RX register.
- uint32_t [MU_ReceiveMsg](#) (MU_Type *base, uint32_t regIndex)
Blocks to receive a message.

MU Flags

- static void [MU_SetFlagsNonBlocking](#) (MU_Type *base, uint32_t flags)
Sets the 3-bit MU flags reflect on the other MU side.
- void [MU_SetFlags](#) (MU_Type *base, uint32_t flags)
Blocks setting the 3-bit MU flags reflect on the other MU side.
- static uint32_t [MU_GetFlags](#) (MU_Type *base)
Gets the current value of the 3-bit MU flags set by the other side.

Status and Interrupt.

- static uint32_t [MU_GetStatusFlags](#) (MU_Type *base)
Gets the MU status flags.
- static uint32_t [MU_GetInterruptsPending](#) (MU_Type *base)
Gets the MU IRQ pending status.
- static void [MU_ClearStatusFlags](#) (MU_Type *base, uint32_t mask)
Clears the specific MU status flags.
- static void [MU_EnableInterrupts](#) (MU_Type *base, uint32_t mask)
Enables the specific MU interrupts.
- static void [MU_DisableInterrupts](#) (MU_Type *base, uint32_t mask)
Disables the specific MU interrupts.
- [status_t](#) [MU_TriggerInterrupts](#) (MU_Type *base, uint32_t mask)
Triggers interrupts to the other core.

MU misc functions

- static void [MU_MaskHardwareReset](#) (MU_Type *base, bool mask)
Mask hardware reset by the other core.
- static mu_power_mode_t [MU_GetOtherCorePowerMode](#) (MU_Type *base)
Gets the power mode of the other core.

16.3 Macro Definition Documentation

16.3.1 #define FSL_MU_DRIVER_VERSION (MAKE_VERSION(2, 1, 0))

16.4 Enumeration Type Documentation

16.4.1 enum _mu_status_flags

Enumerator

kMU_Tx0EmptyFlag TX0 empty.
kMU_Tx1EmptyFlag TX1 empty.
kMU_Tx2EmptyFlag TX2 empty.
kMU_Tx3EmptyFlag TX3 empty.
kMU_Rx0FullFlag RX0 full.
kMU_Rx1FullFlag RX1 full.
kMU_Rx2FullFlag RX2 full.
kMU_Rx3FullFlag RX3 full.
kMU_GenInt0Flag General purpose interrupt 0 pending.
kMU_GenInt1Flag General purpose interrupt 0 pending.
kMU_GenInt2Flag General purpose interrupt 0 pending.
kMU_GenInt3Flag General purpose interrupt 0 pending.
kMU_EventPendingFlag MU event pending.
kMU_FlagsUpdatingFlag MU flags update is on-going.
kMU_OtherSideInResetFlag The other side is in reset.

16.4.2 enum _mu_interrupt_enable

Enumerator

kMU_Tx0EmptyInterruptEnable TX0 empty.
kMU_Tx1EmptyInterruptEnable TX1 empty.
kMU_Tx2EmptyInterruptEnable TX2 empty.
kMU_Tx3EmptyInterruptEnable TX3 empty.
kMU_Rx0FullInterruptEnable RX0 full.
kMU_Rx1FullInterruptEnable RX1 full.
kMU_Rx2FullInterruptEnable RX2 full.
kMU_Rx3FullInterruptEnable RX3 full.
kMU_GenInt0InterruptEnable General purpose interrupt 0.
kMU_GenInt1InterruptEnable General purpose interrupt 1.
kMU_GenInt2InterruptEnable General purpose interrupt 2.
kMU_GenInt3InterruptEnable General purpose interrupt 3.

16.4.3 enum _mu_interrupt_trigger

Enumerator

kMU_GenInt0InterruptTrigger General purpose interrupt 0.
kMU_GenInt1InterruptTrigger General purpose interrupt 1.
kMU_GenInt2InterruptTrigger General purpose interrupt 2.
kMU_GenInt3InterruptTrigger General purpose interrupt 3.

16.5 Function Documentation

16.5.1 void MU_Init (MU_Type * *base*)

This function enables the MU clock only.

Parameters

<i>base</i>	MU peripheral base address.
-------------	-----------------------------

16.5.2 void MU_Deinit (MU_Type * *base*)

This function disables the MU clock only.

Parameters

<i>base</i>	MU peripheral base address.
-------------	-----------------------------

16.5.3 static void MU_SendMsgNonBlocking (MU_Type * *base*, uint32_t *regIndex*, uint32_t *msg*) [inline], [static]

This function writes a message to the specific TX register. It does not check whether the TX register is empty or not. The upper layer should make sure the TX register is empty before calling this function. This function can be used in ISR for better performance.

```
* while (!(kMU_Tx0EmptyFlag & MU_GetStatusFlags(base))) { } Wait for TX0
  register empty.
* MU_SendMsgNonBlocking(base, kMU_MsgReg0, MSG_VAL); Write message to the TX0
  register.
*
```

Parameters

<i>base</i>	MU peripheral base address.
<i>regIndex</i>	TX register index, see mu_msg_reg_index_t .
<i>msg</i>	Message to send.

16.5.4 void MU_SendMsg (MU_Type * *base*, uint32_t *regIndex*, uint32_t *msg*)

This function waits until the TX register is empty and sends the message.

Parameters

<i>base</i>	MU peripheral base address.
<i>regIndex</i>	MU message register, see mu_msg_reg_index_t
<i>msg</i>	Message to send.

16.5.5 static uint32_t MU_ReceiveMsgNonBlocking (MU_Type * *base*, uint32_t *regIndex*) [inline], [static]

This function reads a message from the specific RX register. It does not check whether the RX register is full or not. The upper layer should make sure the RX register is full before calling this function. This function can be used in ISR for better performance.

```
* uint32_t msg;
* while (!(kMU_Rx0FullFlag & MU_GetStatusFlags(base)))
* {
* } Wait for the RX0 register full.
*
* msg = MU_ReceiveMsgNonBlocking(base, kMU_MsgReg0); Read message from RX0
* register.
*
```

Parameters

<i>base</i>	MU peripheral base address.
<i>RX</i>	register index, see mu_msg_reg_index_t .

Returns

The received message.

16.5.6 uint32_t MU_ReceiveMsg (MU_Type * *base*, uint32_t *regIndex*)

This function waits until the RX register is full and receives the message.

Parameters

<i>base</i>	MU peripheral base address.
<i>regIndex</i>	MU message register, see mu_msg_reg_index_t

Returns

The received message.

16.5.7 static void MU_SetFlagsNonBlocking (MU_Type * *base*, uint32_t *flags*) [inline], [static]

This function sets the 3-bit MU flags directly. Every time the 3-bit MU flags are changed, the status flag `kMU_FlagsUpdatingFlag` asserts indicating the 3-bit MU flags are updating to the other side. After the 3-bit MU flags are updated, the status flag `kMU_FlagsUpdatingFlag` is cleared by hardware. During the flags updating period, the flags cannot be changed. The upper layer should make sure the status flag `kMU_FlagsUpdatingFlag` is cleared before calling this function.

```
* while (kMU_FlagsUpdatingFlag & MU_GetStatusFlags(base))
* {
*   Wait for previous MU flags updating.
* }
* MU_SetFlagsNonBlocking(base, 0U); Set the mU flags.
*
```

Parameters

<i>base</i>	MU peripheral base address.
<i>flags</i>	The 3-bit MU flags to set.

16.5.8 void MU_SetFlags (MU_Type * *base*, uint32_t *flags*)

This function blocks setting the 3-bit MU flags. Every time the 3-bit MU flags are changed, the status flag `kMU_FlagsUpdatingFlag` asserts indicating the 3-bit MU flags are updating to the other side. After the 3-bit MU flags are updated, the status flag `kMU_FlagsUpdatingFlag` is cleared by hardware. During the flags updating period, the flags cannot be changed. This function waits for the MU status flag `kMU_FlagsUpdatingFlag` cleared and sets the 3-bit MU flags.

Parameters

<i>base</i>	MU peripheral base address.
<i>flags</i>	The 3-bit MU flags to set.

16.5.9 static uint32_t MU_GetFlags (MU_Type * *base*) [inline], [static]

This function gets the current 3-bit MU flags on the current side.

Parameters

<i>base</i>	MU peripheral base address.
-------------	-----------------------------

Returns

flags Current value of the 3-bit flags.

16.5.10 static uint32_t MU_GetStatusFlags (MU_Type * *base*) [inline], [static]

This function returns the bit mask of the MU status flags. See `_mu_status_flags`.

```
* uint32_t flags;
* flags = MU_GetStatusFlags(base); Get all status flags.
* if (kMU_Tx0EmptyFlag & flags)
* {
*     The TX0 register is empty. Message can be sent.
*     MU_SendMsgNonBlocking(base, kMU_MsgReg0, MSG0_VAL);
* }
* if (kMU_Tx1EmptyFlag & flags)
* {
*     The TX1 register is empty. Message can be sent.
*     MU_SendMsgNonBlocking(base, kMU_MsgReg1, MSG1_VAL);
* }
*
```

Parameters

<i>base</i>	MU peripheral base address.
-------------	-----------------------------

Returns

Bit mask of the MU status flags, see `_mu_status_flags`.

16.5.11 `static uint32_t MU_GetInterruptsPending (MU_Type * base) [inline],
[static]`

This function returns the bit mask of the pending MU IRQs.

Parameters

<i>base</i>	MU peripheral base address.
-------------	-----------------------------

Returns

Bit mask of the MU IRQs pending.

16.5.12 static void MU_ClearStatusFlags (MU_Type * *base*, uint32_t *mask*) [inline], [static]

This function clears the specific MU status flags. The flags to clear should be passed in as bit mask. See `_mu_status_flags`.

```
* Clear general interrupt 0 and general interrupt 1 pending flags.
* MU_ClearStatusFlags(base, kMU_GenInt0Flag |
    kMU_GenInt1Flag);
*
```

Parameters

<i>base</i>	MU peripheral base address.
<i>mask</i>	<p>Bit mask of the MU status flags. See <code>_mu_status_flags</code>. The following flags are cleared by hardware, this function could not clear them.</p> <ul style="list-style-type: none"> • kMU_Tx0EmptyFlag • kMU_Tx1EmptyFlag • kMU_Tx2EmptyFlag • kMU_Tx3EmptyFlag • kMU_Rx0FullFlag • kMU_Rx1FullFlag • kMU_Rx2FullFlag • kMU_Rx3FullFlag • kMU_EventPendingFlag • kMU_FlagsUpdatingFlag • kMU_OtherSideInResetFlag

16.5.13 static void MU_EnableInterrupts (MU_Type * *base*, uint32_t *mask*) [inline], [static]

This function enables the specific MU interrupts. The interrupts to enable should be passed in as bit mask. See `_mu_interrupt_enable`.

```

*   Enable general interrupt 0 and TX0 empty interrupt.
*   MU_EnableInterrupts(base, kMU_GenInt0InterruptEnable |
*       kMU_Tx0EmptyInterruptEnable);
*

```

Parameters

<i>base</i>	MU peripheral base address.
<i>mask</i>	Bit mask of the MU interrupts. See <code>_mu_interrupt_enable</code> .

16.5.14 static void MU_DisableInterrupts (MU_Type * *base*, uint32_t *mask*) [inline], [static]

This function disables the specific MU interrupts. The interrupts to disable should be passed in as bit mask. See `_mu_interrupt_enable`.

```

*   Disable general interrupt 0 and TX0 empty interrupt.
*   MU_DisableInterrupts(base, kMU_GenInt0InterruptEnable |
*       kMU_Tx0EmptyInterruptEnable);
*

```

Parameters

<i>base</i>	MU peripheral base address.
<i>mask</i>	Bit mask of the MU interrupts. See <code>_mu_interrupt_enable</code> .

16.5.15 status_t MU_TriggerInterrupts (MU_Type * *base*, uint32_t *mask*)

This function triggers the specific interrupts to the other core. The interrupts to trigger are passed in as bit mask. See `_mu_interrupt_trigger`. The MU should not trigger an interrupt to the other core when the previous interrupt has not been processed by the other core. This function checks whether the previous interrupts have been processed. If not, it returns an error.

```

*   if (kStatus_Success != MU_TriggerInterrupts(base,
*       kMU_GenInt0InterruptTrigger |
*       kMU_GenInt2InterruptTrigger))
*   {
*       Previous general purpose interrupt 0 or general purpose interrupt 2
*       has not been processed by the other core.
*   }
*

```


Parameters

<i>base</i>	MU peripheral base address.
<i>mask</i>	Bit mask of the interrupts to trigger. See <code>_mu_interrupt_trigger</code> .

Return values

<i>kStatus_Success</i>	Interrupts have been triggered successfully.
<i>kStatus_Fail</i>	Previous interrupts have not been accepted.

16.5.16 `static void MU_MaskHardwareReset (MU_Type * base, bool mask) [inline], [static]`

The other core could call `MU_HardwareResetOtherCore()` to reset current core. To mask the reset, call this function and pass in true.

Parameters

<i>base</i>	MU peripheral base address.
<i>mask</i>	Pass true to mask the hardware reset, pass false to unmask it.

16.5.17 `static mu_power_mode_t MU_GetOtherCorePowerMode (MU_Type * base) [inline], [static]`

This function gets the power mode of the other core.

Parameters

<i>base</i>	MU peripheral base address.
-------------	-----------------------------

Returns

Power mode of the other core.



Chapter 17

PDM: Microphone Interface

17.1 Overview

Modules

- [PDM Driver](#)
- [PDM SDMA Driver](#)

17.2 Typical use case

17.3 PDM Driver

17.3.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Microphone Interface (PDM) module of MCUXpresso SDK devices.

PDM driver includes functional APIs and transactional APIs.

Functional APIs target low-level APIs. Functional APIs can be used for PDM initialization, configuration, and operation for the optimization and customization purpose. Using the functional API requires the knowledge of the PDM peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. PDM functional operation groups provide the functional API set.

Transactional APIs target high-level APIs. Transactional APIs can be used to enable the peripheral and in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are a critical requirement, see the transactional API implementation and write a custom code. Initialize the handle by calling the [PDM_TransferCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer. This means that the functions [PDM_TransferReceiveNonBlocking\(\)](#) set up the interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with `kStatus_PDM_Idle` status.

17.3.2 Typical use case

17.3.2.1 PDM receive using an interrupt method

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/pdm-_interrupt`

17.3.2.2 PDM receive using a SDMA method

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/pdm/pdm-_sdma_transfer`

17.3.2.3 PDM receive using a EDMA method

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/pdm/pdm-_edma_transfer` Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/pdm/pdm_sai_edma` Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/pdm/pdm_sai_multi_channel_edma`

17.3.2.4 PDM receive using a transactional method

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/pdm/pdm-interrupt_transfer

Data Structures

- struct [pdm_channel_config_t](#)
PDM channel configurations. [More...](#)
- struct [pdm_config_t](#)
PDM user configuration structure. [More...](#)
- struct [pdm_hwvad_config_t](#)
PDM voice activity detector user configuration structure. [More...](#)
- struct [pdm_hwvad_noise_filter_t](#)
PDM voice activity detector noise filter user configuration structure. [More...](#)
- struct [pdm_hwvad_zero_cross_detector_t](#)
PDM voice activity detector zero cross detector configuration structure. [More...](#)
- struct [pdm_transfer_t](#)
PDM SDMA transfer structure. [More...](#)
- struct [pdm_handle_t](#)
PDM handle structure. [More...](#)

Macros

- #define [PDM_XFER_QUEUE_SIZE](#) (4U)
PDM XFER QUEUE SIZE.

Typedefs

- typedef void(* [pdm_transfer_callback_t](#))(PDM_Type *base, pdm_handle_t *handle, [status_t](#) status, void *userData)
PDM transfer callback prototype.

Enumerations

- enum {
[kStatus_PDM_Busy](#) = MAKE_STATUS(kStatusGroup_PDM, 0),
[kStatus_PDM_CLK_LOW](#) = MAKE_STATUS(kStatusGroup_PDM, 1),
[kStatus_PDM_FIFO_ERROR](#) = MAKE_STATUS(kStatusGroup_PDM, 2),
[kStatus_PDM_QueueFull](#) = MAKE_STATUS(kStatusGroup_PDM, 3),
[kStatus_PDM_Idle](#) = MAKE_STATUS(kStatusGroup_PDM, 4),
[kStatus_PDM_Output_ERROR](#) = MAKE_STATUS(kStatusGroup_PDM, 5),
[kStatus_PDM_ChannelConfig_Failed](#) = MAKE_STATUS(kStatusGroup_PDM, 6) }
PDM return status.

- enum `_pdm_interrupt_enable` {
`kPDM_ErrorInterruptEnable` = `PDM_CTRL_1_ERREN_MASK`,
`kPDM_FIFOInterruptEnable` = `PDM_CTRL_1_DISEL(2U)` }
The PDM interrupt enable flag.
- enum `_pdm_internal_status` {
`kPDM_StatusDfBusyFlag` = `(int)PDM_STAT_BSY_FIL_MASK`,
`kPDM_StatusFIRFilterReady` = `PDM_STAT_FIR_RDY_MASK`,
`kPDM_StatusFrequencyLow` = `PDM_STAT_LOWFREQF_MASK`,
`kPDM_StatusCh0FifoDataAvaliable` = `PDM_STAT_CH0F_MASK`,
`kPDM_StatusCh1FifoDataAvaliable` = `PDM_STAT_CH1F_MASK`,
`kPDM_StatusCh2FifoDataAvaliable` = `PDM_STAT_CH2F_MASK`,
`kPDM_StatusCh3FifoDataAvaliable` = `PDM_STAT_CH3F_MASK`,
`kPDM_StatusCh4FifoDataAvaliable` = `PDM_STAT_CH4F_MASK`,
`kPDM_StatusCh5FifoDataAvaliable` = `PDM_STAT_CH5F_MASK`,
`kPDM_StatusCh6FifoDataAvaliable` = `PDM_STAT_CH6F_MASK`,
`kPDM_StatusCh7FifoDataAvaliable` = `PDM_STAT_CH7F_MASK` }
The PDM status.
- enum `_pdm_channel_enable_mask` {
`kPDM_EnableChannel0` = `PDM_STAT_CH0F_MASK`,
`kPDM_EnableChannel1` = `PDM_STAT_CH1F_MASK`,
`kPDM_EnableChannel2` = `PDM_STAT_CH2F_MASK`,
`kPDM_EnableChannel3` = `PDM_STAT_CH3F_MASK`,
`kPDM_EnableChannel4` = `PDM_STAT_CH4F_MASK`,
`kPDM_EnableChannel5` = `PDM_STAT_CH5F_MASK`,
`kPDM_EnableChannel6` = `PDM_STAT_CH6F_MASK`,
`kPDM_EnableChannel7` = `PDM_STAT_CH7F_MASK` }
PDM channel enable mask.
- enum `_pdm_fifo_status` {
`kPDM_FifoStatusUnderflowCh0` = `PDM_FIFO_STAT_FIFOUND0_MASK`,
`kPDM_FifoStatusUnderflowCh1` = `PDM_FIFO_STAT_FIFOUND1_MASK`,
`kPDM_FifoStatusUnderflowCh2` = `PDM_FIFO_STAT_FIFOUND2_MASK`,
`kPDM_FifoStatusUnderflowCh3` = `PDM_FIFO_STAT_FIFOUND3_MASK`,
`kPDM_FifoStatusUnderflowCh4` = `PDM_FIFO_STAT_FIFOUND4_MASK`,
`kPDM_FifoStatusUnderflowCh5` = `PDM_FIFO_STAT_FIFOUND5_MASK`,
`kPDM_FifoStatusUnderflowCh6` = `PDM_FIFO_STAT_FIFOUND6_MASK`,
`kPDM_FifoStatusUnderflowCh7` = `PDM_FIFO_STAT_FIFOUND6_MASK`,
`kPDM_FifoStatusOverflowCh0` = `PDM_FIFO_STAT_FIFOOVF0_MASK`,
`kPDM_FifoStatusOverflowCh1` = `PDM_FIFO_STAT_FIFOOVF1_MASK`,
`kPDM_FifoStatusOverflowCh2` = `PDM_FIFO_STAT_FIFOOVF2_MASK`,
`kPDM_FifoStatusOverflowCh3` = `PDM_FIFO_STAT_FIFOOVF3_MASK`,
`kPDM_FifoStatusOverflowCh4` = `PDM_FIFO_STAT_FIFOOVF4_MASK`,
`kPDM_FifoStatusOverflowCh5` = `PDM_FIFO_STAT_FIFOOVF5_MASK`,
`kPDM_FifoStatusOverflowCh6` = `PDM_FIFO_STAT_FIFOOVF6_MASK`,
`kPDM_FifoStatusOverflowCh7` = `PDM_FIFO_STAT_FIFOOVF7_MASK` }
The PDM fifo status.
- enum `_pdm_range_status` {

```

kPDM_RangeStatusUnderFlowCh0 = PDM_RANGE_STAT_RANGEUNF0_MASK,
kPDM_RangeStatusUnderFlowCh1 = PDM_RANGE_STAT_RANGEUNF1_MASK,
kPDM_RangeStatusUnderFlowCh2 = PDM_RANGE_STAT_RANGEUNF2_MASK,
kPDM_RangeStatusUnderFlowCh3 = PDM_RANGE_STAT_RANGEUNF3_MASK,
kPDM_RangeStatusUnderFlowCh4 = PDM_RANGE_STAT_RANGEUNF4_MASK,
kPDM_RangeStatusUnderFlowCh5 = PDM_RANGE_STAT_RANGEUNF5_MASK,
kPDM_RangeStatusUnderFlowCh6 = PDM_RANGE_STAT_RANGEUNF6_MASK,
kPDM_RangeStatusUnderFlowCh7 = PDM_RANGE_STAT_RANGEUNF7_MASK,
kPDM_RangeStatusOverFlowCh0 = PDM_RANGE_STAT_RANGEOVF0_MASK,
kPDM_RangeStatusOverFlowCh1 = PDM_RANGE_STAT_RANGEOVF1_MASK,
kPDM_RangeStatusOverFlowCh2 = PDM_RANGE_STAT_RANGEOVF2_MASK,
kPDM_RangeStatusOverFlowCh3 = PDM_RANGE_STAT_RANGEOVF3_MASK,
kPDM_RangeStatusOverFlowCh4 = PDM_RANGE_STAT_RANGEOVF4_MASK,
kPDM_RangeStatusOverFlowCh5 = PDM_RANGE_STAT_RANGEOVF5_MASK,
kPDM_RangeStatusOverFlowCh6 = PDM_RANGE_STAT_RANGEOVF6_MASK,
kPDM_RangeStatusOverFlowCh7 = PDM_RANGE_STAT_RANGEOVF7_MASK }

```

The PDM output status.

- enum `pdm_dc_removal_t` {


```

kPDM_DcRemoverCutOff21Hz = 0U,
kPDM_DcRemoverCutOff83Hz = 1U,
kPDM_DcRemoverCutOff152Hz = 2U,
kPDM_DcRemoverBypass = 3U }

```

PDM DC remover configurations.

- enum `pdm_df_quality_mode_t` {


```

kPDM_QualityModeMedium = 0U,
kPDM_QualityModeHigh = 1U,
kPDM_QualityModeLow = 7U,
kPDM_QualityModeVeryLow0 = 6U,
kPDM_QualityModeVeryLow1 = 5U,
kPDM_QualityModeVeryLow2 = 4U }

```

PDM decimation filter quality mode.

- enum `_pdm_qulaity_mode_k_factor` {


```

kPDM_QualityModeHighKFactor = 1U,
kPDM_QualityModeMediumKFactor = 2U,
kPDM_QualityModeLowKFactor = 4U,
kPDM_QualityModeVeryLow2KFactor = 8U }

```

PDM quality mode K factor.

- enum `pdm_df_output_gain_t` {

```

kPDM_DfOutputGain0 = 0U,
kPDM_DfOutputGain1 = 1U,
kPDM_DfOutputGain2 = 2U,
kPDM_DfOutputGain3 = 3U,
kPDM_DfOutputGain4 = 4U,
kPDM_DfOutputGain5 = 5U,
kPDM_DfOutputGain6 = 6U,
kPDM_DfOutputGain7 = 7U,
kPDM_DfOutputGain8 = 8U,
kPDM_DfOutputGain9 = 9U,
kPDM_DfOutputGain10 = 0xAU,
kPDM_DfOutputGain11 = 0xBU,
kPDM_DfOutputGain12 = 0xCU,
kPDM_DfOutputGain13 = 0xDU,
kPDM_DfOutputGain14 = 0xEU,
kPDM_DfOutputGain15 = 0xFU }

```

PDM decimation filter output gain.

- enum `_pdm_data_width` {
`kPDM_DataWidth24` = 3U,
`kPDM_DataWidth32` = 4U }

PDM data width.

- enum `_pdm_hwvad_interrupt_enable` {
`kPDM_HwvadErrorInterruptEnable` = PDM_VAD0_CTRL_1_VADERIE_MASK,
`kPDM_HwvadInterruptEnable` = PDM_VAD0_CTRL_1_VADIE_MASK }

PDM voice activity detector interrupt type.

- enum `_pdm_hwvad_int_status` {
`kPDM_HwvadStatusInputSaturation` = PDM_VAD0_STAT_VADINSATF_MASK,
`kPDM_HwvadStatusVoiceDetectFlag` = PDM_VAD0_STAT_VADIF_MASK }

The PDM hwvad interrupt status flag.

- enum `pdm_hwvad_hpf_config_t` {
`kPDM_HwvadHpfBypassed` = 0x0U,
`kPDM_HwvadHpfCutOffFreq1750Hz` = 0x1U,
`kPDM_HwvadHpfCutOffFreq215Hz` = 0x2U,
`kPDM_HwvadHpfCutOffFreq102Hz` = 0x3U }

High pass filter configure cut-off frequency.

- enum `pdm_hwvad_filter_status_t` {
`kPDM_HwvadInternalFilterNormalOperation` = 0U,
`kPDM_HwvadInternalFilterInitial` = PDM_VAD0_CTRL_1_VADST10_MASK }

HWVAD internal filter status.

- enum `pdm_hwvad_zcd_result_t` {
`kPDM_HwvadResultOREnergyBasedDetection`,
`kPDM_HwvadResultANDEnergyBasedDetection` }

PDM voice activity detector zero cross detector result.

Driver version

- #define `FSL_PDM_DRIVER_VERSION` (`MAKE_VERSION(2, 6, 0)`)
Version 2.6.0.

Initialization and deinitialization

- void `PDM_Init` (`PDM_Type *base`, const `pdm_config_t *config`)
Initializes the PDM peripheral.
- void `PDM_Deinit` (`PDM_Type *base`)
De-initializes the PDM peripheral.
- static void `PDM_Reset` (`PDM_Type *base`)
Resets the PDM module.
- static void `PDM_Enable` (`PDM_Type *base`, bool enable)
Enables/disables PDM interface.
- static void `PDM_EnableDoze` (`PDM_Type *base`, bool enable)
Enables/disables DOZE.
- static void `PDM_EnableDebugMode` (`PDM_Type *base`, bool enable)
Enables/disables debug mode for PDM.
- static void `PDM_EnableInDebugMode` (`PDM_Type *base`, bool enable)
Enables/disables PDM interface in debug mode.
- static void `PDM_EnterLowLeakageMode` (`PDM_Type *base`, bool enable)
Enables/disables PDM interface disable/Low Leakage mode.
- static void `PDM_EnableChannel` (`PDM_Type *base`, uint8_t channel, bool enable)
Enables/disables the PDM channel.
- void `PDM_SetChannelConfig` (`PDM_Type *base`, uint32_t channel, const `pdm_channel_config_t *config`)
PDM one channel configurations.
- `status_t` `PDM_SetSampleRateConfig` (`PDM_Type *base`, uint32_t sourceClock_HZ, uint32_t sampleRate_HZ)
PDM set sample rate.
- `status_t` `PDM_SetSampleRate` (`PDM_Type *base`, uint32_t enableChannelMask, `pdm_df_quality_mode_t` qualityMode, uint8_t osr, uint32_t clkDiv)
PDM set sample rate.
- uint32_t `PDM_GetInstance` (`PDM_Type *base`)
Get the instance number for PDM.

Status

- static uint32_t `PDM_GetStatus` (`PDM_Type *base`)
Gets the PDM internal status flag.
- static uint32_t `PDM_GetFifoStatus` (`PDM_Type *base`)
Gets the PDM FIFO status flag.
- static uint32_t `PDM_GetRangeStatus` (`PDM_Type *base`)
Gets the PDM Range status flag.
- static void `PDM_ClearStatus` (`PDM_Type *base`, uint32_t mask)
Clears the PDM Tx status.
- static void `PDM_ClearFIFOStatus` (`PDM_Type *base`, uint32_t mask)

- Clears the PDM Tx status.
- static void [PDM_ClearRangeStatus](#) (PDM_Type *base, uint32_t mask)
Clears the PDM range status.

Interrupts

- void [PDM_EnableInterrupts](#) (PDM_Type *base, uint32_t mask)
Enables the PDM interrupt requests.
- static void [PDM_DisableInterrupts](#) (PDM_Type *base, uint32_t mask)
Disables the PDM interrupt requests.

DMA Control

- static void [PDM_EnableDMA](#) (PDM_Type *base, bool enable)
Enables/disables the PDM DMA requests.
- static uint32_t [PDM_GetDataRegisterAddress](#) (PDM_Type *base, uint32_t channel)
Gets the PDM data register address.

Bus Operations

- void [PDM_ReadFifo](#) (PDM_Type *base, uint32_t startChannel, uint32_t channelNums, void *buffer, size_t size, uint32_t dataWidth)
PDM read fifo.
- static uint32_t [PDM_ReadData](#) (PDM_Type *base, uint32_t channel)
Reads data from the PDM FIFO.

Voice Activity Detector

- void [PDM_SetHwvadConfig](#) (PDM_Type *base, const [pdm_hwvad_config_t](#) *config)
Configure voice activity detector.
- static void [PDM_ForceHwvadOutputDisable](#) (PDM_Type *base, bool enable)
PDM hwvad force output disable.
- static void [PDM_ResetHwvad](#) (PDM_Type *base)
PDM hwvad reset.
- static void [PDM_EnableHwvad](#) (PDM_Type *base, bool enable)
Enable/Disable Voice activity detector.
- static void [PDM_EnableHwvadInterrupts](#) (PDM_Type *base, uint32_t mask)
Enables the PDM Voice Detector interrupt requests.
- static void [PDM_DisableHwvadInterrupts](#) (PDM_Type *base, uint32_t mask)
Disables the PDM Voice Detector interrupt requests.
- static void [PDM_ClearHwvadInterruptStatusFlags](#) (PDM_Type *base, uint32_t mask)
Clears the PDM voice activity detector status flags.
- static uint32_t [PDM_GetHwvadInterruptStatusFlags](#) (PDM_Type *base)
Clears the PDM voice activity detector status flags.
- static uint32_t [PDM_GetHwvadInitialFlag](#) (PDM_Type *base)
Get the PDM voice activity detector initial flags.

- static uint32_t **PDM_GetHwvadVoiceDetectedFlag** (PDM_Type *base)
Get the PDM voice activity detector voice detected flags.
- static void **PDM_EnableHwvadSignalFilter** (PDM_Type *base, bool enable)
Enables/disables voice activity detector signal filter.
- void **PDM_SetHwvadSignalFilterConfig** (PDM_Type *base, bool enableMaxBlock, uint32_t signalGain)
Configure voice activity detector signal filter.
- void **PDM_SetHwvadNoiseFilterConfig** (PDM_Type *base, const **pdm_hwvad_noise_filter_t** *config)
Configure voice activity detector noise filter.
- static void **PDM_EnableHwvadZeroCrossDetector** (PDM_Type *base, bool enable)
Enables/disables voice activity detector zero cross detector.
- void **PDM_SetHwvadZeroCrossDetectorConfig** (PDM_Type *base, const **pdm_hwvad_zero_cross_detector_t** *config)
Configure voice activity detector zero cross detector.
- static uint16_t **PDM_GetNoiseData** (PDM_Type *base)
Reads noise data.
- static void **PDM_SetHwvadInternalFilterStatus** (PDM_Type *base, **pdm_hwvad_filter_status_t** status)
set hwvad internal filter status .
- void **PDM_SetHwvadInEnvelopeBasedMode** (PDM_Type *base, const **pdm_hwvad_config_t** *hwvadConfig, const **pdm_hwvad_noise_filter_t** *noiseConfig, const **pdm_hwvad_zero_cross_detector_t** *zcdConfig, uint32_t signalGain)
set HWVAD in envelope based mode .
- void **PDM_SetHwvadInEnergyBasedMode** (PDM_Type *base, const **pdm_hwvad_config_t** *hwvadConfig, const **pdm_hwvad_noise_filter_t** *noiseConfig, const **pdm_hwvad_zero_cross_detector_t** *zcdConfig, uint32_t signalGain)
brief set HWVAD in energy based mode .

Transactional

- void **PDM_TransferCreateHandle** (PDM_Type *base, **pdm_handle_t** *handle, **pdm_transfer_callback_t** callback, void *userData)
Initializes the PDM handle.
- **status_t** **PDM_TransferSetChannelConfig** (PDM_Type *base, **pdm_handle_t** *handle, uint32_t channel, const **pdm_channel_config_t** *config, uint32_t format)
PDM set channel transfer config.
- **status_t** **PDM_TransferReceiveNonBlocking** (PDM_Type *base, **pdm_handle_t** *handle, **pdm_transfer_t** *xfer)
Performs an interrupt non-blocking receive transfer on PDM.
- void **PDM_TransferAbortReceive** (PDM_Type *base, **pdm_handle_t** *handle)
Aborts the current IRQ receive.
- void **PDM_TransferHandleIRQ** (PDM_Type *base, **pdm_handle_t** *handle)
Tx interrupt handler.

17.3.3 Data Structure Documentation

17.3.3.1 struct pdm_channel_config_t

Data Fields

- [pdm_dc_remover_t cutOffFreq](#)
DC remover cut off frequency.
- [pdm_df_output_gain_t gain](#)
Decimation Filter Output Gain.

17.3.3.2 struct pdm_config_t

Data Fields

- bool [enableDoze](#)
This module will enter disable/low leakage mode if DOZEN is active with ipg_doze is asserted.
- uint8_t [fifoWatermark](#)
Watermark value for FIFO.
- [pdm_df_quality_mode_t qualityMode](#)
Quality mode.
- uint8_t [cicOverSampleRate](#)
CIC filter over sampling rate.

17.3.3.3 struct pdm_hwvad_config_t

Data Fields

- uint8_t [channel](#)
Which channel uses voice activity detector.
- uint8_t [initializeTime](#)
Number of frames or samples to initialize voice activity detector.
- uint8_t [cicOverSampleRate](#)
CIC filter over sampling rate.
- uint8_t [inputGain](#)
Voice activity detector input gain.
- uint32_t [frameTime](#)
Voice activity frame time.
- [pdm_hwvad_hpf_config_t cutOffFreq](#)
High pass filter cut off frequency.
- bool [enableFrameEnergy](#)
If frame energy enabled, true means enable.
- bool [enablePreFilter](#)
If pre-filter enabled.

Field Documentation

(1) uint8_t pdm_hwvad_config_t::initializeTime

17.3.3.4 struct pdm_hwvad_noise_filter_t

Data Fields

- bool [enableAutoNoiseFilter](#)
If noise filterer automatically activated, true means enable.
- bool [enableNoiseMin](#)
If Noise minimum block enabled, true means enabled.
- bool [enableNoiseDecimation](#)
If enable noise input decimation.
- bool [enableNoiseDetectOR](#)
Enables a OR logic in the output of minimum noise estimator block.
- uint32_t [noiseFilterAdjustment](#)
The adjustment value of the noise filter.
- uint32_t [noiseGain](#)
Gain value for the noise energy or envelope estimated.

17.3.3.5 struct pdm_hwvad_zero_cross_detector_t

Data Fields

- bool [enableAutoThreshold](#)
If ZCD auto-threshold enabled, true means enabled.
- [pdm_hwvad_zcd_result_t](#) [zcdAnd](#)
Is ZCD result is AND'ed with energy-based detection, false means OR'ed.
- uint32_t [threshold](#)
The adjustment value of the noise filter.
- uint32_t [adjustmentThreshold](#)
Gain value for the noise energy or envelope estimated.

Field Documentation

(1) bool pdm_hwvad_zero_cross_detector_t::enableAutoThreshold

17.3.3.6 struct pdm_transfer_t

Data Fields

- volatile uint8_t * [data](#)
Data start address to transfer.
- volatile size_t [dataSize](#)
Total Transfer bytes size.

Field Documentation

(1) volatile uint8_t* pdm_transfer_t::data

(2) volatile size_t pdm_transfer_t::dataSize

17.3.3.7 struct _pdm_handle

PDM handle.

Data Fields

- uint32_t [state](#)
Transfer status.
- [pdm_transfer_callback_t](#) [callback](#)
Callback function called at transfer event.
- void * [userData](#)
Callback parameter passed to callback function.
- [pdm_transfer_t](#) [pdmQueue](#) [PDM_XFER_QUEUE_SIZE]
Transfer queue storing queued transfer.
- size_t [transferSize](#) [PDM_XFER_QUEUE_SIZE]
Data bytes need to transfer.
- volatile uint8_t [queueUser](#)
Index for user to queue transfer.
- volatile uint8_t [queueDriver](#)
Index for driver to get the transfer data and size.
- uint32_t [format](#)
data format
- uint8_t [watermark](#)
Watermark value.
- uint8_t [startChannel](#)
end channel
- uint8_t [channelNums](#)
Enabled channel number.

17.3.4 Enumeration Type Documentation

17.3.4.1 anonymous enum

Enumerator

kStatus_PDM_Busy PDM is busy.
kStatus_PDM_CLK_LOW PDM clock frequency low.
kStatus_PDM_FIFO_ERROR PDM FIFO underrun or overflow.
kStatus_PDM_QueueFull PDM FIFO underrun or overflow.
kStatus_PDM_Idle PDM is idle.
kStatus_PDM_Output_ERROR PDM is output error.
kStatus_PDM_ChannelConfig_Failed PDM channel config failed.

17.3.4.2 enum _pdm_interrupt_enable

Enumerator

kPDM_ErrorInterruptEnable PDM channel error interrupt enable.
kPDM_FIFOInterruptEnable PDM channel FIFO interrupt.

17.3.4.3 enum _pdm_internal_status

Enumerator

kPDM_StatusDfBusyFlag Decimation filter is busy processing data.
kPDM_StatusFIRFilterReady FIR filter data is ready.
kPDM_StatusFrequencyLow Mic app clock frequency not high enough.
kPDM_StatusCh0FifoDataAvaliable channel 0 fifo data reached watermark level
kPDM_StatusCh1FifoDataAvaliable channel 1 fifo data reached watermark level
kPDM_StatusCh2FifoDataAvaliable channel 2 fifo data reached watermark level
kPDM_StatusCh3FifoDataAvaliable channel 3 fifo data reached watermark level
kPDM_StatusCh4FifoDataAvaliable channel 4 fifo data reached watermark level
kPDM_StatusCh5FifoDataAvaliable channel 5 fifo data reached watermark level
kPDM_StatusCh6FifoDataAvaliable channel 6 fifo data reached watermark level
kPDM_StatusCh7FifoDataAvaliable channel 7 fifo data reached watermark level

17.3.4.4 enum _pdm_channel_enable_mask

Enumerator

kPDM_EnableChannel0 channigel 0 enable mask
kPDM_EnableChannel1 channigel 1 enable mask
kPDM_EnableChannel2 channigel 2 enable mask
kPDM_EnableChannel3 channigel 3 enable mask
kPDM_EnableChannel4 channigel 4 enable mask
kPDM_EnableChannel5 channigel 5 enable mask
kPDM_EnableChannel6 channigel 6 enable mask
kPDM_EnableChannel7 channigel 7 enable mask

17.3.4.5 enum _pdm_fifo_status

Enumerator

kPDM_FifoStatusUnderflowCh0 channel0 fifo status underflow
kPDM_FifoStatusUnderflowCh1 channel1 fifo status underflow
kPDM_FifoStatusUnderflowCh2 channel2 fifo status underflow

kPDM_FifoStatusUnderflowCh3 channel3 fifo status underflow
kPDM_FifoStatusUnderflowCh4 channel4 fifo status underflow
kPDM_FifoStatusUnderflowCh5 channel5 fifo status underflow
kPDM_FifoStatusUnderflowCh6 channel6 fifo status underflow
kPDM_FifoStatusUnderflowCh7 channel7 fifo status underflow
kPDM_FifoStatusOverflowCh0 channel0 fifo status overflow
kPDM_FifoStatusOverflowCh1 channel1 fifo status overflow
kPDM_FifoStatusOverflowCh2 channel2 fifo status overflow
kPDM_FifoStatusOverflowCh3 channel3 fifo status overflow
kPDM_FifoStatusOverflowCh4 channel4 fifo status overflow
kPDM_FifoStatusOverflowCh5 channel5 fifo status overflow
kPDM_FifoStatusOverflowCh6 channel6 fifo status overflow
kPDM_FifoStatusOverflowCh7 channel7 fifo status overflow

17.3.4.6 enum _pdm_range_status

Enumerator

kPDM_RangeStatusUnderFlowCh0 channel0 range status underflow
kPDM_RangeStatusUnderFlowCh1 channel1 range status underflow
kPDM_RangeStatusUnderFlowCh2 channel2 range status underflow
kPDM_RangeStatusUnderFlowCh3 channel3 range status underflow
kPDM_RangeStatusUnderFlowCh4 channel4 range status underflow
kPDM_RangeStatusUnderFlowCh5 channel5 range status underflow
kPDM_RangeStatusUnderFlowCh6 channel6 range status underflow
kPDM_RangeStatusUnderFlowCh7 channel7 range status underflow
kPDM_RangeStatusOverFlowCh0 channel0 range status overflow
kPDM_RangeStatusOverFlowCh1 channel1 range status overflow
kPDM_RangeStatusOverFlowCh2 channel2 range status overflow
kPDM_RangeStatusOverFlowCh3 channel3 range status overflow
kPDM_RangeStatusOverFlowCh4 channel4 range status overflow
kPDM_RangeStatusOverFlowCh5 channel5 range status overflow
kPDM_RangeStatusOverFlowCh6 channel6 range status overflow
kPDM_RangeStatusOverFlowCh7 channel7 range status overflow

17.3.4.7 enum pdm_dc_removal_t

Enumerator

kPDM_DcRemoverCutOff21Hz DC remover cut off 21HZ.
kPDM_DcRemoverCutOff83Hz DC remover cut off 83HZ.
kPDM_DcRemoverCutOff152Hz DC remover cut off 152HZ.
kPDM_DcRemoverBypass DC remover bypass.

17.3.4.8 enum pdm_df_quality_mode_t

Enumerator

kPDM_QualityModeMedium quality mode medium
kPDM_QualityModeHigh quality mode high
kPDM_QualityModeLow quality mode low
kPDM_QualityModeVeryLow0 quality mode very low0
kPDM_QualityModeVeryLow1 quality mode very low1
kPDM_QualityModeVeryLow2 quality mode very low2

17.3.4.9 enum _pdm_qulaity_mode_k_factor

Enumerator

kPDM_QualityModeHighKFactor high quality mode K factor = 1 / 2
kPDM_QualityModeMediumKFactor medium/very low0 quality mode K factor = 2 / 2
kPDM_QualityModeLowKFactor low/very low1 quality mode K factor = 4 / 2
kPDM_QualityModeVeryLow2KFactor very low2 quality mode K factor = 8 / 2

17.3.4.10 enum pdm_df_output_gain_t

Enumerator

kPDM_DfOutputGain0 Decimation filter output gain 0.
kPDM_DfOutputGain1 Decimation filter output gain 1.
kPDM_DfOutputGain2 Decimation filter output gain 2.
kPDM_DfOutputGain3 Decimation filter output gain 3.
kPDM_DfOutputGain4 Decimation filter output gain 4.
kPDM_DfOutputGain5 Decimation filter output gain 5.
kPDM_DfOutputGain6 Decimation filter output gain 6.
kPDM_DfOutputGain7 Decimation filter output gain 7.
kPDM_DfOutputGain8 Decimation filter output gain 8.
kPDM_DfOutputGain9 Decimation filter output gain 9.
kPDM_DfOutputGain10 Decimation filter output gain 10.
kPDM_DfOutputGain11 Decimation filter output gain 11.
kPDM_DfOutputGain12 Decimation filter output gain 12.
kPDM_DfOutputGain13 Decimation filter output gain 13.
kPDM_DfOutputGain14 Decimation filter output gain 14.
kPDM_DfOutputGain15 Decimation filter output gain 15.

17.3.4.11 enum _pdm_data_width

Enumerator

kPDM_DataWwidth24 PDM data width 24bit.*kPDM_DataWwidth32* PDM data width 32bit.**17.3.4.12 enum _pdm_hwvad_interrupt_enable**

Enumerator

kPDM_HwvadErrorInterruptEnable PDM channel HWVAD error interrupt enable.*kPDM_HwvadInterruptEnable* PDM channel HWVAD interrupt.**17.3.4.13 enum _pdm_hwvad_int_status**

Enumerator

kPDM_HwvadStatusInputSaturation HWVAD saturation condition.*kPDM_HwvadStatusVoiceDetectFlag* HWVAD voice detect interrupt triggered.**17.3.4.14 enum pdm_hwvad_hpf_config_t**

Enumerator

kPDM_HwvadHpfBypassed High-pass filter bypass.*kPDM_HwvadHpfCutOffFreq1750Hz* High-pass filter cut off frequency 1750HZ.*kPDM_HwvadHpfCutOffFreq215Hz* High-pass filter cut off frequency 215HZ.*kPDM_HwvadHpfCutOffFreq102Hz* High-pass filter cut off frequency 102HZ.**17.3.4.15 enum pdm_hwvad_filter_status_t**

Enumerator

kPDM_HwvadInternalFilterNormalOperation internal filter ready for normal operation*kPDM_HwvadInternalFilterInitial* internal filter are initial**17.3.4.16 enum pdm_hwvad_zcd_result_t**

Enumerator

kPDM_HwvadResultOREnergyBasedDetection zero cross detector result will be OR with energy based detection

kPDM_HwvadResultANDEnergyBasedDetection zero cross detector result will be AND with energy based detection

17.3.5 Function Documentation

17.3.5.1 void PDM_Init (PDM_Type * *base*, const pdm_config_t * *config*)

Ungates the PDM clock, resets the module, and configures PDM with a configuration structure. The configuration structure can be custom filled or set with default values by PDM_GetDefaultConfig().

Note

This API should be called at the beginning of the application to use the PDM driver. Otherwise, accessing the PDM module can cause a hard fault because the clock is not enabled.

Parameters

<i>base</i>	PDM base pointer
<i>config</i>	PDM configuration structure.

17.3.5.2 void PDM_Deinit (PDM_Type * *base*)

This API gates the PDM clock. The PDM module can't operate unless PDM_Init is called to enable the clock.

Parameters

<i>base</i>	PDM base pointer
-------------	------------------

17.3.5.3 static void PDM_Reset (PDM_Type * *base*) [inline], [static]

Parameters

<i>base</i>	PDM base pointer
-------------	------------------

17.3.5.4 static void PDM_Enable (PDM_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>enable</i>	True means PDM interface is enabled, false means PDM interface is disabled.

17.3.5.5 static void PDM_EnableDoze (PDM_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>enable</i>	True means the module will enter Disable/Low Leakage mode when ipg_doze is asserted, false means the module will not enter Disable/Low Leakage mode when ipg_doze is asserted.

17.3.5.6 static void PDM_EnableDebugMode (PDM_Type * *base*, bool *enable*) [inline], [static]

The PDM interface cannot enter debug mode once in Disable/Low Leakage or Low Power mode.

Parameters

<i>base</i>	PDM base pointer
<i>enable</i>	True means PDM interface enter debug mode, false means PDM interface in normal mode.

17.3.5.7 static void PDM_EnableInDebugMode (PDM_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>enable</i>	True means PDM interface is enabled debug mode, false means PDM interface is disabled after after completing the current frame in debug mode.

17.3.5.8 static void PDM_EnterLowLeakageMode (PDM_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>enable</i>	True means PDM interface is in disable/low leakage mode, False means PDM interface is in normal mode.

17.3.5.9 static void PDM_EnableChannel (PDM_Type * *base*, uint8_t *channel*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>channel</i>	PDM channel number need to enable or disable.
<i>enable</i>	True means enable PDM channel, false means disable.

17.3.5.10 void PDM_SetChannelConfig (PDM_Type * *base*, uint32_t *channel*, const pdm_channel_config_t * *config*)

Parameters

<i>base</i>	PDM base pointer
<i>config</i>	PDM channel configurations.
<i>channel</i>	channel number. after completing the current frame in debug mode.

17.3.5.11 status_t PDM_SetSampleRateConfig (PDM_Type * *base*, uint32_t *sourceClock_HZ*, uint32_t *sampleRate_HZ*)

Note

This function is depend on the configuration of the PDM and PDM channel, so the correct call sequence is

```
* PDM_Init(base, pdmConfig)
* PDM_SetChannelConfig(base, channel, &channelConfig)
* PDM_SetSampleRateConfig(base, source, sampleRate)
*
```

Parameters

<i>base</i>	PDM base pointer
<i>sourceClock_HZ</i>	PDM source clock frequency.
<i>sampleRate_HZ</i>	PDM sample rate.

17.3.5.12 `status_t PDM_SetSampleRate (PDM_Type * base, uint32_t enableChannelMask, pdm_df_quality_mode_t qualityMode, uint8_t osr, uint32_t clkDiv)`

Deprecated Do not use this function. It has been superseded by [PDM_SetSampleRateConfig](#)

Parameters

<i>base</i>	PDM base pointer
<i>enable-ChannelMask</i>	PDM channel enable mask.
<i>qualityMode</i>	quality mode.
<i>osr</i>	cic oversample rate
<i>clkDiv</i>	clock divider

17.3.5.13 `uint32_t PDM_GetInstance (PDM_Type * base)`

Parameters

<i>base</i>	PDM base pointer.
-------------	-------------------

17.3.5.14 `static uint32_t PDM_GetStatus (PDM_Type * base) [inline], [static]`

Use the Status Mask in `_pdm_internal_status` to get the status value needed

Parameters

<i>base</i>	PDM base pointer
-------------	------------------

Returns

PDM status flag value.

17.3.5.15 **static uint32_t PDM_GetFifoStatus (PDM_Type * *base*) [inline], [static]**

Use the Status Mask in `_pdm_fifo_status` to get the status value needed

Parameters

<i>base</i>	PDM base pointer
-------------	------------------

Returns

FIFO status.

17.3.5.16 **static uint32_t PDM_GetRangeStatus (PDM_Type * *base*) [inline], [static]**

Use the Status Mask in `_pdm_range_status` to get the status value needed

Parameters

<i>base</i>	PDM base pointer
-------------	------------------

Returns

output status.

17.3.5.17 **static void PDM_ClearStatus (PDM_Type * *base*, uint32_t *mask*) [inline], [static]**

Parameters

<i>base</i>	PDM base pointer
<i>mask</i>	State mask. It can be a combination of the status between kPDM_StatusFrequency-Low and kPDM_StatusCh7FifoDataAvaliable.

17.3.5.18 static void PDM_ClearFIFOStatus (PDM_Type * *base*, uint32_t *mask*)
[inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>mask</i>	State mask. It can be a combination of the status in _pdm_fifo_status.

17.3.5.19 static void PDM_ClearRangeStatus (PDM_Type * *base*, uint32_t *mask*)
[inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>mask</i>	State mask. It can be a combination of the status in _pdm_range_status.

17.3.5.20 void PDM_EnableInterrupts (PDM_Type * *base*, uint32_t *mask*)

Parameters

<i>base</i>	PDM base pointer
<i>mask</i>	interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> • kPDM_ErrorInterruptEnable • kPDM_FIFOInterruptEnable

17.3.5.21 static void PDM_DisableInterrupts (PDM_Type * *base*, uint32_t *mask*)
[inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>mask</i>	interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> • kPDM_ErrorInterruptEnable • kPDM_FIFOInterruptEnable

17.3.5.22 static void PDM_EnableDMA (PDM_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>enable</i>	True means enable DMA, false means disable DMA.

17.3.5.23 static uint32_t PDM_GetDataRegisterAddress (PDM_Type * *base*, uint32_t *channel*) [inline], [static]

This API is used to provide a transfer address for the PDM DMA transfer configuration.

Parameters

<i>base</i>	PDM base pointer.
<i>channel</i>	Which data channel used.

Returns

data register address.

17.3.5.24 void PDM_ReadFifo (PDM_Type * *base*, uint32_t *startChannel*, uint32_t *channelNums*, void * *buffer*, size_t *size*, uint32_t *dataWidth*)

Note

: This function support 16 bit only for IP version that only supports 16bit.

Parameters

<i>base</i>	PDM base pointer.
<i>startChannel</i>	start channel number.
<i>channelNums</i>	total enabled channelnums.
<i>buffer</i>	received buffer address.
<i>size</i>	number of samples to read.
<i>dataWidth</i>	sample width.

17.3.5.25 `static uint32_t PDM_ReadData (PDM_Type * base, uint32_t channel)`
[inline], [static]

Parameters

<i>base</i>	PDM base pointer.
<i>channel</i>	Data channel used.

Returns

Data in PDM FIFO.

17.3.5.26 `void PDM_SetHwvadConfig (PDM_Type * base, const pdm_hwvad_config_t * config)`

Parameters

<i>base</i>	PDM base pointer
<i>config</i>	Voice activity detector configure structure pointer .

17.3.5.27 `static void PDM_ForceHwvadOutputDisable (PDM_Type * base, bool enable)`
[inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>enable</i>	true is output force disable, false is output not force.

17.3.5.28 static void PDM_ResetHwvad (PDM_Type * *base*) [inline], [static]

It will reset VADNDATA register and will clean all internal buffers, should be called when the PDM isn't running.

Parameters

<i>base</i>	PDM base pointer
-------------	------------------

17.3.5.29 static void PDM_EnableHwvad (PDM_Type * *base*, bool *enable*) [inline], [static]

Should be called when the PDM isn't running.

Parameters

<i>base</i>	PDM base pointer.
<i>enable</i>	True means enable voice activity detector, false means disable.

17.3.5.30 static void PDM_EnableHwvadInterrupts (PDM_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>mask</i>	interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> • kPDM_HWVADErrorInterruptEnable • kPDM_HWVADInterruptEnable

17.3.5.31 static void PDM_DisableHwvadInterrupts (PDM_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>mask</i>	interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> • kPDM_HWVADErrorInterruptEnable • kPDM_HWVADInterruptEnable

17.3.5.32 `static void PDM_ClearHwvadInterruptStatusFlags (PDM_Type * base, uint32_t mask) [inline], [static]`

Parameters

<i>base</i>	PDM base pointer
<i>mask</i>	State mask,reference _pdm_hwvad_int_status.

17.3.5.33 `static uint32_t PDM_GetHwvadInterruptStatusFlags (PDM_Type * base) [inline], [static]`

Parameters

<i>base</i>	PDM base pointer
-------------	------------------

Returns

status, reference _pdm_hwvad_int_status

17.3.5.34 `static uint32_t PDM_GetHwvadInitialFlag (PDM_Type * base) [inline], [static]`

Parameters

<i>base</i>	PDM base pointer
-------------	------------------

Returns

initial flag.

17.3.5.35 `static uint32_t PDM_GetHwvadVoiceDetectedFlag (PDM_Type * base)`
`[inline], [static]`

NOte: this flag is auto cleared when voice gone.

Parameters

<i>base</i>	PDM base pointer
-------------	------------------

Returns

voice detected flag.

17.3.5.36 static void PDM_EnableHwvadSignalFilter (PDM_Type * *base*, bool *enable*)
[inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>enable</i>	True means enable signal filter, false means disable.

17.3.5.37 void PDM_SetHwvadSignalFilterConfig (PDM_Type * *base*, bool *enableMaxBlock*, uint32_t *signalGain*)

Parameters

<i>base</i>	PDM base pointer
<i>enableMaxBlock</i>	If signal maximum block enabled.
<i>signalGain</i>	Gain value for the signal energy.

17.3.5.38 void PDM_SetHwvadNoiseFilterConfig (PDM_Type * *base*, const pdm_hwvad_noise_filter_t * *config*)

Parameters

<i>base</i>	PDM base pointer
<i>config</i>	Voice activity detector noise filter configure structure pointer .

17.3.5.39 static void PDM_EnableHwvadZeroCrossDetector (PDM_Type * *base*, bool *enable*)
[inline], [static]

Parameters

<i>base</i>	PDM base pointer
<i>enable</i>	True means enable zero cross detector, false means disable.

17.3.5.40 void PDM_SetHwvadZeroCrossDetectorConfig (PDM_Type * *base*, const pdm_hwvad_zero_cross_detector_t * *config*)

Parameters

<i>base</i>	PDM base pointer
<i>config</i>	Voice activity detector zero cross detector configure structure pointer .

17.3.5.41 static uint16_t PDM_GetNoiseData (PDM_Type * *base*) [inline], [static]

Parameters

<i>base</i>	PDM base pointer.
-------------	-------------------

Returns

Data in PDM noise data register.

17.3.5.42 static void PDM_SetHwvadInternalFilterStatus (PDM_Type * *base*, pdm_hwvad_filter_status_t *status*) [inline], [static]

Note: filter initial status should be asserted for two more cycles, then set it to normal operation.

Parameters

<i>base</i>	PDM base pointer.
<i>status</i>	internal filter status.

17.3.5.43 void PDM_SetHwvadInEnvelopeBasedMode (PDM_Type * *base*, const pdm_hwvad_config_t * *hwvadConfig*, const pdm_hwvad_noise_filter_t * *noiseConfig*, const pdm_hwvad_zero_cross_detector_t * *zcdConfig*, uint32_t *signalGain*)

Recommand configurations,

```

* static const pdm_hwvad_config_t hwvadConfig = {
*   .channel          = 0,
*   .initializeTime   = 10U,
*   .cicOverSampleRate = 0U,
*   .inputGain        = 0U,
*   .frameTime        = 10U,
*   .cutOffFreq       = kPDM_HwvadHpfBypassed,
*   .enableFrameEnergy = false,
*   .enablePreFilter   = true,
* };

* static const pdm_hwvad_noise_filter_t noiseFilterConfig = {
*   .enableAutoNoiseFilter = false,
*   .enableNoiseMin        = true,
*   .enableNoiseDecimation = true,
*   .noiseFilterAdjustment = 0U,
*   .noiseGain             = 7U,
*   .enableNoiseDetectOR   = true,
* };
*

```

Parameters

<i>base</i>	PDM base pointer.
<i>hwvadConfig</i>	internal filter status.
<i>noiseConfig</i>	Voice activity detector noise filter configure structure pointer.
<i>zcdConfig</i>	Voice activity detector zero cross detector configure structure pointer .
<i>signalGain</i>	signal gain value.

17.3.5.44 void PDM_SetHwvadInEnergyBasedMode (PDM_Type * *base*, const pdm_hwvad_config_t * *hwvadConfig*, const pdm_hwvad_noise_filter_t * *noiseConfig*, const pdm_hwvad_zero_cross_detector_t * *zcdConfig*, uint32_t *signalGain*)

Recommand configurations, code static const `pdm_hwvad_config_t` `hwvadConfig` = { `.channel` = 0, `.initializeTime` = 10U, `.cicOverSampleRate` = 0U, `.inputGain` = 0U, `.frameTime` = 10U, `.cutOffFreq` = `kPDM_HwvadHpfBypassed`, `.enableFrameEnergy` = true, `.enablePreFilter` = true, };

static const `pdm_hwvad_noise_filter_t` `noiseFilterConfig` = { `.enableAutoNoiseFilter` = true, `.enableNoiseMin` = false, `.enableNoiseDecimation` = false, `.noiseFilterAdjustment` = 0U, `.noiseGain` = 7U, `.enableNoiseDetectOR` = false, }; code param `base` PDM base pointer. param `hwvadConfig` internal filter status. param `noiseConfig` Voice activity detector noise filter configure structure pointer. param `zcdConfig` Voice activity detector zero cross detector configure structure pointer . param `signalGain` signal gain value, signal gain value should be properly according to application.

17.3.5.45 void PDM_TransferCreateHandle (PDM_Type * *base*, pdm_handle_t * *handle*,
pdm_transfer_callback_t *callback*, void * *userData*)

This function initializes the handle for the PDM transactional APIs. Call this function once to get the handle initialized.

Parameters

<i>base</i>	PDM base pointer.
<i>handle</i>	PDM handle pointer.
<i>callback</i>	Pointer to the user callback function.
<i>userData</i>	User parameter passed to the callback function.

17.3.5.46 `status_t PDM_TransferSetChannelConfig (PDM_Type * base, pdm_handle_t * handle, uint32_t channel, const pdm_channel_config_t * config, uint32_t format)`

Parameters

<i>base</i>	PDM base pointer.
<i>handle</i>	PDM handle pointer.
<i>channel</i>	PDM channel.
<i>config</i>	channel config.
<i>format</i>	data format, support data width configurations, _pdm_data_width.

Return values

<i>kStatus_PDM_Channel-Config_Failed</i>	or kStatus_Success.
--	---------------------

17.3.5.47 `status_t PDM_TransferReceiveNonBlocking (PDM_Type * base, pdm_handle_t * handle, pdm_transfer_t * xfer)`

Note

This API returns immediately after the transfer initiates. Call the PDM_RxGetTransferStatusIRQ to poll the transfer status and check whether the transfer is finished. If the return status is not kStatus_PDM_Busy, the transfer is finished.

Parameters

<i>base</i>	PDM base pointer
<i>handle</i>	Pointer to the <code>pdm_handle_t</code> structure which stores the transfer state.
<i>xfer</i>	Pointer to the pdm_transfer_t structure.

Return values

<i>kStatus_Success</i>	Successfully started the data receive.
<i>kStatus_PDM_Busy</i>	Previous receive still not finished.

17.3.5.48 void PDM_TransferAbortReceive (PDM_Type * *base*, `pdm_handle_t` * *handle*)

Note

This API can be called when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	PDM base pointer
<i>handle</i>	Pointer to the <code>pdm_handle_t</code> structure which stores the transfer state.

17.3.5.49 void PDM_TransferHandleIRQ (PDM_Type * *base*, `pdm_handle_t` * *handle*)

Parameters

<i>base</i>	PDM base pointer.
<i>handle</i>	Pointer to the <code>pdm_handle_t</code> structure.

17.4 PDM SDMA Driver

17.4.1 Typical use case

17.4.2 Overview

The SDMA multi fifo script support transfer data between multi peripheral fifos and memory, a typical user case is that receiving multi PDM channel data and put it into memory as

| channel 0 | channel 1 | channel 2 | channel 3 | channel 4 | |

Multi fifo script is target to implement above feature, it can supports 1.configurable fifo watermark range from $1 \sim (2^{12} - 1)$, it is a value of `fifo_watermark * channel_numbers` 2.configurable fifo numbers, support up to 15 continuous fifos 3.configurable fifo address offset, support address offset up to 64

```
/* load sdma script */
SDMA_LoadScript()
/* pdm multi channel configurations */
PDM_SetChannelConfigSDMA()
PDM_SetChannelConfigSDMA()
PDM_SetChannelConfigSDMA()
PDM_SetChannelConfigSDMA()
....

PDM_TransferReceiveSDMA
```

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/pdm/pdm-sai_sdma`

Data Structures

- struct `pdm_sdma_handle_t`
PDM DMA transfer handle, users should not touch the content of the handle. [More...](#)

Typedefs

- typedef void(* `pdm_sdma_callback_t`)(PDM_Type *base, pdm_sdma_handle_t *handle, `status_t` status, void *userData)
PDM eDMA transfer callback function for finish and error.

Driver version

- #define `FSL_PDM_SDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 6, 0)`)
Version 2.6.0.

eDMA Transactional

- void [PDM_TransferCreateHandleSDMA](#) (PDM_Type *base, pdm_sdma_handle_t *handle, [pdm_sdma_callback_t](#) callback, void *userData, [sdma_handle_t](#) *dmaHandle, uint32_t eventSource)
Initializes the PDM eDMA handle.
- [status_t PDM_TransferReceiveSDMA](#) (PDM_Type *base, pdm_sdma_handle_t *handle, [pdm_transfer_t](#) *xfer)
Performs a non-blocking PDM receive using eDMA.
- void [PDM_TransferAbortReceiveSDMA](#) (PDM_Type *base, pdm_sdma_handle_t *handle)
Aborts a PDM receive using eDMA.
- void [PDM_SetChannelConfigSDMA](#) (PDM_Type *base, pdm_sdma_handle_t *handle, uint32_t channel, const [pdm_channel_config_t](#) *config)
PDM channel configurations.

17.4.3 Data Structure Documentation

17.4.3.1 struct _pdm_sdma_handle

Data Fields

- [sdma_handle_t](#) * [dmaHandle](#)
DMA handler for PDM send.
- uint8_t [nbytes](#)
eDMA minor byte transfer count initially configured.
- uint8_t [fifoWidth](#)
fifo width
- uint8_t [endChannel](#)
The last enabled channel.
- uint8_t [channelNums](#)
total channel numbers
- uint32_t [count](#)
The transfer data count in a DMA request.
- uint32_t [state](#)
Internal state for PDM eDMA transfer.
- uint32_t [eventSource](#)
PDM event source number.
- [pdm_sdma_callback_t](#) [callback](#)
Callback for users while transfer finish or error occurs.
- void * [userData](#)
User callback parameter.
- [sdma_buffer_descriptor_t](#) [bdPool](#) [[PDM_XFER_QUEUE_SIZE](#)]
BD pool for SDMA transfer.
- [pdm_transfer_t](#) [pdmQueue](#) [[PDM_XFER_QUEUE_SIZE](#)]
Transfer queue storing queued transfer.
- size_t [transferSize](#) [[PDM_XFER_QUEUE_SIZE](#)]
Data bytes need to transfer.
- volatile uint8_t [queueUser](#)
Index for user to queue transfer.
- volatile uint8_t [queueDriver](#)

Index for driver to get the transfer data and size.

Field Documentation

- (1) `uint8_t pdm_sdma_handle_t::nbytes`
- (2) `sdma_buffer_descriptor_t pdm_sdma_handle_t::bdPool[PDM_XFER_QUEUE_SIZE]`
- (3) `pdm_transfer_t pdm_sdma_handle_t::pdmQueue[PDM_XFER_QUEUE_SIZE]`
- (4) `volatile uint8_t pdm_sdma_handle_t::queueUser`

17.4.4 Function Documentation

17.4.4.1 void PDM_TransferCreateHandleSDMA (PDM_Type * *base*, pdm_sdma_handle_t * *handle*, pdm_sdma_callback_t *callback*, void * *userData*, sdma_handle_t * *dmaHandle*, uint32_t *eventSource*)

This function initializes the PDM DMA handle, which can be used for other PDM master transactional APIs. Usually, for a specified PDM instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	PDM base pointer.
<i>handle</i>	PDM eDMA handle pointer.
<i>callback</i>	Pointer to user callback function.
<i>userData</i>	User parameter passed to the callback function.
<i>dmaHandle</i>	eDMA handle pointer, this handle shall be static allocated by users.
<i>eventSource</i>	PDM event source number.

17.4.4.2 status_t PDM_TransferReceiveSDMA (PDM_Type * *base*, pdm_sdma_handle_t * *handle*, pdm_transfer_t * *xfer*)

Note

This interface returns immediately after the transfer initiates. Call the PDM_GetReceiveRemaining-Bytes to poll the transfer status and check whether the PDM transfer is finished.

Parameters

<i>base</i>	PDM base pointer
<i>handle</i>	PDM eDMA handle pointer.
<i>xfer</i>	Pointer to DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a PDM eDMA receive successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.
<i>kStatus_RxBusy</i>	PDM is busy receiving data.

17.4.4.3 void PDM_TransferAbortReceiveSDMA (PDM_Type * *base*, pdm_sdma_handle_t * *handle*)

Parameters

<i>base</i>	PDM base pointer
<i>handle</i>	PDM eDMA handle pointer.

17.4.4.4 void PDM_SetChannelConfigSDMA (PDM_Type * *base*, pdm_sdma_handle_t * *handle*, uint32_t *channel*, const pdm_channel_config_t * *config*)

Parameters

<i>base</i>	PDM base pointer.
<i>handle</i>	PDM eDMA handle pointer.
<i>channel</i>	channel number.
<i>config</i>	channel configurations.

Chapter 18

RDC: Resource Domain Controller

18.1 Overview

The MCUXpresso SDK provides a driver for the RDC module of MCUXpresso SDK devices.

The Resource Domain Controller (RDC) provides robust support for the isolation of destination memory mapped locations such as peripherals and memory to a single core, a bus master, or set of cores and bus masters.

The RDC driver should be used together with the RDC_SEMA42 driver.

Data Structures

- struct [rdc_hardware_config_t](#)
RDC hardware configuration. [More...](#)
- struct [rdc_domain_assignment_t](#)
Master domain assignment. [More...](#)
- struct [rdc_periph_access_config_t](#)
Peripheral domain access permission configuration. [More...](#)
- struct [rdc_mem_access_config_t](#)
Memory region domain access control configuration. [More...](#)
- struct [rdc_mem_status_t](#)
Memory region access violation status. [More...](#)

Enumerations

- enum [_rdc_interrupts](#) { [kRDC_RestoreCompleteInterrupt](#) = RDC_INTCTRL_RCI_EN_MASK }
RDC interrupts.
- enum [_rdc_flags](#) { [kRDC_PowerDownDomainOn](#) = RDC_STAT_PDS_MASK }
RDC status.
- enum [_rdc_access_policy](#) {
 [kRDC_NoAccess](#) = 0,
 [kRDC_WriteOnly](#) = 1,
 [kRDC_ReadOnly](#) = 2,
 [kRDC_ReadWrite](#) = 3 }
Access permission policy.

Functions

- void [RDC_Init](#) (RDC_Type *base)
Initializes the RDC module.
- void [RDC_Deinit](#) (RDC_Type *base)
De-initializes the RDC module.
- void [RDC_GetHardwareConfig](#) (RDC_Type *base, [rdc_hardware_config_t](#) *config)
Gets the RDC hardware configuration.

- static void [RDC_EnableInterrupts](#) (RDC_Type *base, uint32_t mask)
Enable interrupts.
- static void [RDC_DisableInterrupts](#) (RDC_Type *base, uint32_t mask)
Disable interrupts.
- static uint32_t [RDC_GetInterruptStatus](#) (RDC_Type *base)
Get the interrupt pending status.
- static void [RDC_ClearInterruptStatus](#) (RDC_Type *base, uint32_t mask)
Clear interrupt pending status.
- static uint32_t [RDC_GetStatus](#) (RDC_Type *base)
Get RDC status.
- static void [RDC_ClearStatus](#) (RDC_Type *base, uint32_t mask)
Clear RDC status.
- void [RDC_SetMasterDomainAssignment](#) (RDC_Type *base, rdc_master_t master, const [rdc_domain_assignment_t](#) *domainAssignment)
Set master domain assignment.
- void [RDC_GetDefaultMasterDomainAssignment](#) ([rdc_domain_assignment_t](#) *domainAssignment)
Get default master domain assignment.
- static void [RDC_LockMasterDomainAssignment](#) (RDC_Type *base, rdc_master_t master)
Lock master domain assignment.
- void [RDC_SetPeriphAccessConfig](#) (RDC_Type *base, const [rdc_periph_access_config_t](#) *config)
Set peripheral access policy.
- void [RDC_GetDefaultPeriphAccessConfig](#) ([rdc_periph_access_config_t](#) *config)
Get default peripheral access policy.
- static void [RDC_LockPeriphAccessConfig](#) (RDC_Type *base, rdc_periph_t periph)
Lock peripheral access policy configuration.
- static uint8_t [RDC_GetPeriphAccessPolicy](#) (RDC_Type *base, rdc_periph_t periph, uint8_t domainId)
Get the peripheral access policy for specific domain.
- void [RDC_SetMemAccessConfig](#) (RDC_Type *base, const [rdc_mem_access_config_t](#) *config)
Set memory region access policy.
- void [RDC_GetDefaultMemAccessConfig](#) ([rdc_mem_access_config_t](#) *config)
Get default memory region access policy.
- static void [RDC_LockMemAccessConfig](#) (RDC_Type *base, rdc_mem_t mem)
Lock memory access policy configuration.
- static void [RDC_SetMemAccessValid](#) (RDC_Type *base, rdc_mem_t mem, bool valid)
Enable or disable memory access policy configuration.
- void [RDC_GetMemViolationStatus](#) (RDC_Type *base, rdc_mem_t mem, [rdc_mem_status_t](#) *status)
Get the memory region violation status.
- static void [RDC_ClearMemViolationFlag](#) (RDC_Type *base, rdc_mem_t mem)
Clear the memory region violation flag.
- static uint8_t [RDC_GetMemAccessPolicy](#) (RDC_Type *base, rdc_mem_t mem, uint8_t domainId)
Get the memory region access policy for specific domain.
- static uint8_t [RDC_GetCurrentMasterDomainId](#) (RDC_Type *base)
Gets the domain ID of the current bus master.

18.2 Data Structure Documentation

18.2.1 struct rdc_hardware_config_t

Data Fields

- uint32_t [domainNumber](#): 4
Number of domains.
- uint32_t [masterNumber](#): 8
Number of bus masters.
- uint32_t [periphNumber](#): 8
Number of peripherals.
- uint32_t [memNumber](#): 8
Number of memory regions.

Field Documentation

- (1) uint32_t rdc_hardware_config_t::domainNumber
- (2) uint32_t rdc_hardware_config_t::masterNumber
- (3) uint32_t rdc_hardware_config_t::periphNumber
- (4) uint32_t rdc_hardware_config_t::memNumber

18.2.2 struct rdc_domain_assignment_t

Data Fields

- uint32_t [domainId](#): 2U
Domain ID.
- uint32_t [__pad0__](#): 29U
Reserved.
- uint32_t [lock](#): 1U
Lock the domain assignment.

Field Documentation

- (1) uint32_t rdc_domain_assignment_t::domainId
- (2) uint32_t rdc_domain_assignment_t::__pad0__
- (3) uint32_t rdc_domain_assignment_t::lock

18.2.3 struct rdc_periph_access_config_t

Data Fields

- rdc_periph_t [periph](#)
Peripheral name.

- bool [lock](#)
Lock the permission until reset.
- bool [enableSema](#)
Enable semaphore or not, when enabled, master should call [RDC_SEMA42_Lock](#) to lock the semaphore gate accordingly before access the peripheral.
- uint16_t [policy](#)
Access policy.

Field Documentation

- (1) `rdc_periph_t rdc_periph_access_config_t::periph`
- (2) `bool rdc_periph_access_config_t::lock`
- (3) `bool rdc_periph_access_config_t::enableSema`
- (4) `uint16_t rdc_periph_access_config_t::policy`

18.2.4 struct `rdc_mem_access_config_t`

Note that when setting the [baseAddress](#) and [endAddress](#), should be aligned to the region resolution, see `rdc_mem_t` definitions.

Data Fields

- `rdc_mem_t` [mem](#)
Memory region descriptor name.
- bool [lock](#)
Lock the configuration.
- uint64_t [baseAddress](#)
Start address of the memory region.
- uint64_t [endAddress](#)
End address of the memory region.
- uint16_t [policy](#)
Access policy.

Field Documentation

- (1) `rdc_mem_t rdc_mem_access_config_t::mem`
- (2) `bool rdc_mem_access_config_t::lock`
- (3) `uint64_t rdc_mem_access_config_t::baseAddress`
- (4) `uint64_t rdc_mem_access_config_t::endAddress`
- (5) `uint16_t rdc_mem_access_config_t::policy`

18.2.5 struct rdc_mem_status_t

Data Fields

- bool [hasViolation](#)
Violating happens or not.
- uint8_t [domainID](#)
Violating Domain ID.
- uint64_t [address](#)
Violating Address.

Field Documentation

(1) bool rdc_mem_status_t::hasViolation

(2) uint8_t rdc_mem_status_t::domainID

(3) uint64_t rdc_mem_status_t::address

18.3 Enumeration Type Documentation

18.3.1 enum _rdc_interrupts

Enumerator

kRDC_RestoreCompleteInterrupt Interrupt generated when the RDC has completed restoring state to a recently re-powered memory regions.

18.3.2 enum _rdc_flags

Enumerator

kRDC_PowerDownDomainOn Power down domain is ON.

18.3.3 enum _rdc_access_policy

Enumerator

kRDC_NoAccess Could not read or write.
kRDC_WriteOnly Write only.
kRDC_ReadOnly Read only.
kRDC_ReadWrite Read and write.

18.4 Function Documentation

18.4.1 void RDC_Init (RDC_Type * *base*)

This function enables the RDC clock.

Parameters

<i>base</i>	RDC peripheral base address.
-------------	------------------------------

18.4.2 void RDC_Deinit (RDC_Type * *base*)

This function disables the RDC clock.

Parameters

<i>base</i>	RDC peripheral base address.
-------------	------------------------------

18.4.3 void RDC_GetHardwareConfig (RDC_Type * *base*, rdc_hardware_config_t * *config*)

This function gets the RDC hardware configurations, including number of bus masters, number of domains, number of memory regions and number of peripherals.

Parameters

<i>base</i>	RDC peripheral base address.
<i>config</i>	Pointer to the structure to get the configuration.

18.4.4 static void RDC_EnableInterrupts (RDC_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	RDC peripheral base address.
<i>mask</i>	Interrupts to enable, it is OR'ed value of enum _rdc_interrupts .

18.4.5 static void RDC_DisableInterrupts (RDC_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	RDC peripheral base address.
<i>mask</i>	Interrupts to disable, it is OR'ed value of enum _rdc_interrupts .

18.4.6 static uint32_t RDC_GetInterruptStatus (RDC_Type * *base*) [inline], [static]

Parameters

<i>base</i>	RDC peripheral base address.
-------------	------------------------------

Returns

Interrupts pending status, it is OR'ed value of enum [_rdc_interrupts](#).

18.4.7 static void RDC_ClearInterruptStatus (RDC_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	RDC peripheral base address.
<i>mask</i>	Status to clear, it is OR'ed value of enum _rdc_interrupts .

18.4.8 static uint32_t RDC_GetStatus (RDC_Type * *base*) [inline], [static]

Parameters

<i>base</i>	RDC peripheral base address.
-------------	------------------------------

Returns

mask RDC status, it is OR'ed value of enum [_rdc_flags](#).

18.4.9 static void RDC_ClearStatus (RDC_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	RDC peripheral base address.
<i>mask</i>	RDC status to clear, it is OR'ed value of enum _rdc_flags .

18.4.10 void RDC_SetMasterDomainAssignment (RDC_Type * *base*, rdc_master_t *master*, const rdc_domain_assignment_t * *domainAssignment*)

Parameters

<i>base</i>	RDC peripheral base address.
<i>master</i>	Which master to set.
<i>domain-Assignment</i>	Pointer to the assignment.

18.4.11 void RDC_GetDefaultMasterDomainAssignment (rdc_domain_assignment_t * *domainAssignment*)

The default configuration is:

```
assignment->domainId = 0U;
assignment->lock = 0U;
```

Parameters

<i>domain-Assignment</i>	Pointer to the assignment.
--------------------------	----------------------------

18.4.12 static void RDC_LockMasterDomainAssignment (RDC_Type * *base*, rdc_master_t *master*) [inline], [static]

Once locked, it could not be unlocked until next reset.

Parameters

<i>base</i>	RDC peripheral base address.
<i>master</i>	Which master to lock.

18.4.13 void RDC_SetPeriphAccessConfig (RDC_Type * *base*, const rdc_periph_access_config_t * *config*)

Parameters

<i>base</i>	RDC peripheral base address.
<i>config</i>	Pointer to the policy configuration.

18.4.14 void RDC_GetDefaultPeriphAccessConfig (rdc_periph_access_config_t * *config*)

The default configuration is:

```
config->lock = false;
config->enableSema = false;
config->policy = RDC_ACCESS_POLICY(0, kRDC_ReadWrite) |
                RDC_ACCESS_POLICY(1, kRDC_ReadWrite) |
                RDC_ACCESS_POLICY(2, kRDC_ReadWrite) |
                RDC_ACCESS_POLICY(3, kRDC_ReadWrite);
```

Parameters

<i>config</i>	Pointer to the policy configuration.
---------------	--------------------------------------

18.4.15 static void RDC_LockPeriphAccessConfig (RDC_Type * *base*, rdc_periph_t *periph*) [inline], [static]

Once locked, it could not be unlocked until reset.

Parameters

<i>base</i>	RDC peripheral base address.
-------------	------------------------------

<i>periph</i>	Which peripheral to lock.
---------------	---------------------------

18.4.16 static uint8_t RDC_GetPeriphAccessPolicy (RDC_Type * *base*, rdc_periph_t *periph*, uint8_t *domainId*) [inline], [static]

Parameters

<i>base</i>	RDC peripheral base address.
<i>periph</i>	Which peripheral to get.
<i>domainId</i>	Get policy for which domain.

Returns

Access policy, see [_rdc_access_policy](#).

18.4.17 void RDC_SetMemAccessConfig (RDC_Type * *base*, const rdc_mem_access_config_t * *config*)

Note that when setting the `baseAddress` and `endAddress` in `config`, should be aligned to the region resolution, see `rdc_mem_t` definitions.

Parameters

<i>base</i>	RDC peripheral base address.
<i>config</i>	Pointer to the policy configuration.

18.4.18 void RDC_GetDefaultMemAccessConfig (rdc_mem_access_config_t * *config*)

The default configuration is:

```
config->lock = false;
config->baseAddress = 0;
config->endAddress = 0;
config->policy = RDC_ACCESS_POLICY(0, kRDC_ReadWrite) |
                RDC_ACCESS_POLICY(1, kRDC_ReadWrite) |
                RDC_ACCESS_POLICY(2, kRDC_ReadWrite) |
                RDC_ACCESS_POLICY(3, kRDC_ReadWrite);
```

Parameters

<i>config</i>	Pointer to the policy configuration.
---------------	--------------------------------------

18.4.19 static void RDC_LockMemAccessConfig (RDC_Type * *base*, rdc_mem_t *mem*) [inline], [static]

Once locked, it could not be unlocked until reset. After locked, you can only call [RDC_SetMemAccessValid](#) to enable the configuration, but can not disable it or change other settings.

Parameters

<i>base</i>	RDC peripheral base address.
<i>mem</i>	Which memory region to lock.

18.4.20 static void RDC_SetMemAccessValid (RDC_Type * *base*, rdc_mem_t *mem*, bool *valid*) [inline], [static]

Parameters

<i>base</i>	RDC peripheral base address.
<i>mem</i>	Which memory region to operate.
<i>valid</i>	Pass in true to valid, false to invalid.

18.4.21 void RDC_GetMemViolationStatus (RDC_Type * *base*, rdc_mem_t *mem*, rdc_mem_status_t * *status*)

The first access violation is captured. Subsequent violations are ignored until the status register is cleared. Contents are cleared upon reading the register. Clearing of contents occurs only when the status is read by the memory region's associated domain ID(s).

Parameters

<i>base</i>	RDC peripheral base address.
-------------	------------------------------

<i>mem</i>	Which memory region to get.
<i>status</i>	The returned status.

18.4.22 `static void RDC_ClearMemViolationFlag (RDC_Type * base, rdc_mem_t mem) [inline], [static]`

Parameters

<i>base</i>	RDC peripheral base address.
<i>mem</i>	Which memory region to clear.

18.4.23 `static uint8_t RDC_GetMemAccessPolicy (RDC_Type * base, rdc_mem_t mem, uint8_t domainId) [inline], [static]`

Parameters

<i>base</i>	RDC peripheral base address.
<i>mem</i>	Which memory region to get.
<i>domainId</i>	Get policy for which domain.

Returns

Access policy, see [_rdc_access_policy](#).

18.4.24 `static uint8_t RDC_GetCurrentMasterDomainId (RDC_Type * base) [inline], [static]`

This function returns the domain ID of the current bus master.

Parameters

<i>base</i>	RDC peripheral base address.
-------------	------------------------------

Returns

Domain ID of current bus master.

Chapter 19

RDC_SEMA42: Hardware Semaphores Driver

19.1 Overview

The MCUXpresso SDK provides a driver for the RDC_SEMA42 module of MCUXpresso SDK devices.

The RDC_SEMA42 driver should be used together with RDC driver.

Before using the RDC_SEMA42, call the [RDC_SEMA42_Init\(\)](#) function to initialize the module. Note that this function only enables the clock but does not reset the gates because the module might be used by other processors at the same time. To reset the gates, call either the [RDC_SEMA42_ResetGate\(\)](#) or [RDC_SEMA42_ResetAllGates\(\)](#) functions. The function [RDC_SEMA42_Deinit\(\)](#) deinitializes the RDC_SEMA42.

The RDC_SEMA42 provides two functions to lock the RDC_SEMA42 gate. The function [RDC_SEMA42_TryLock\(\)](#) tries to lock the gate. If the gate has been locked by another processor, this function returns an error immediately. The function [RDC_SEMA42_Lock\(\)](#) is a blocking method, which waits until the gate is free and locks it.

The [RDC_SEMA42_Unlock\(\)](#) unlocks the RDC_SEMA42 gate. The gate can only be unlocked by the processor which locked it. If the gate is not locked by the current processor, this function takes no effect. The function [RDC_SEMA42_GetGateStatus\(\)](#) returns a status whether the gate is unlocked and which processor locks the gate. The function [RDC_SEMA42_GetLockDomainID\(\)](#) returns the ID of the domain which has locked the gate.

The RDC_SEMA42 gate can be reset to unlock forcefully. The function [RDC_SEMA42_ResetGate\(\)](#) resets a specific gate. The function [RDC_SEMA42_ResetAllGates\(\)](#) resets all gates.

Macros

- #define [RDC_SEMA42_GATE_NUM_RESET_ALL](#) (64U)
The number to reset all RDC_SEMA42 gates.
- #define [RDC_SEMA42_GATEn](#)(base, n) (((volatile uint8_t *)&((base)->GATE0)))[(n)]
RDC_SEMA42 gate n register address.
- #define [RDC_SEMA42_GATE_COUNT](#) (64U)
RDC_SEMA42 gate count.

Functions

- void [RDC_SEMA42_Init](#) (RDC_SEMAPHORE_Type *base)
Initializes the RDC_SEMA42 module.
- void [RDC_SEMA42_Deinit](#) (RDC_SEMAPHORE_Type *base)
De-initializes the RDC_SEMA42 module.
- [status_t](#) [RDC_SEMA42_TryLock](#) (RDC_SEMAPHORE_Type *base, uint8_t gateNum, uint8_t masterIndex, uint8_t domainId)
Tries to lock the RDC_SEMA42 gate.

- void [RDC_SEMA42_Lock](#) (RDC_SEMAPHORE_Type *base, uint8_t gateNum, uint8_t masterIndex, uint8_t domainId)
Locks the RDC_SEMA42 gate.
- static void [RDC_SEMA42_Unlock](#) (RDC_SEMAPHORE_Type *base, uint8_t gateNum)
Unlocks the RDC_SEMA42 gate.
- static int32_t [RDC_SEMA42_GetLockMasterIndex](#) (RDC_SEMAPHORE_Type *base, uint8_t gateNum)
Gets which master has currently locked the gate.
- int32_t [RDC_SEMA42_GetLockDomainID](#) (RDC_SEMAPHORE_Type *base, uint8_t gateNum)
Gets which domain has currently locked the gate.
- status_t [RDC_SEMA42_ResetGate](#) (RDC_SEMAPHORE_Type *base, uint8_t gateNum)
Resets the RDC_SEMA42 gate to an unlocked status.
- static status_t [RDC_SEMA42_ResetAllGates](#) (RDC_SEMAPHORE_Type *base)
Resets all RDC_SEMA42 gates to an unlocked status.

Driver version

- #define [FSL_RDC_SEMA42_DRIVER_VERSION](#) ([MAKE_VERSION](#)(2, 0, 3))
RDC_SEMA42 driver version.

19.2 Macro Definition Documentation

19.2.1 #define RDC_SEMA42_GATE_NUM_RESET_ALL (64U)

19.2.2 #define RDC_SEMA42_GATEn(base, n) (((volatile uint8_t *)(&((base)->GATE0)))[(n)])

19.2.3 #define RDC_SEMA42_GATE_COUNT (64U)

19.3 Function Documentation

19.3.1 void RDC_SEMA42_Init (RDC_SEMAPHORE_Type * base)

This function initializes the RDC_SEMA42 module. It only enables the clock but does not reset the gates because the module might be used by other processors at the same time. To reset the gates, call either RDC_SEMA42_ResetGate or RDC_SEMA42_ResetAllGates function.

Parameters

<i>base</i>	RDC_SEMA42 peripheral base address.
-------------	-------------------------------------

19.3.2 void RDC_SEMA42_Deinit (RDC_SEMAPHORE_Type * base)

This function de-initializes the RDC_SEMA42 module. It only disables the clock.

Parameters

<i>base</i>	RDC_SEMA42 peripheral base address.
-------------	-------------------------------------

19.3.3 **status_t RDC_SEMA42_TryLock (RDC_SEMAPHORE_Type * *base*, uint8_t *gateNum*, uint8_t *masterIndex*, uint8_t *domainId*)**

This function tries to lock the specific RDC_SEMA42 gate. If the gate has been locked by another processor, this function returns an error code.

Parameters

<i>base</i>	RDC_SEMA42 peripheral base address.
<i>gateNum</i>	Gate number to lock.
<i>masterIndex</i>	Current processor master index.
<i>domainId</i>	Current processor domain ID.

Return values

<i>kStatus_Success</i>	Lock the sema42 gate successfully.
<i>kStatus_Failed</i>	Sema42 gate has been locked by another processor.

19.3.4 **void RDC_SEMA42_Lock (RDC_SEMAPHORE_Type * *base*, uint8_t *gateNum*, uint8_t *masterIndex*, uint8_t *domainId*)**

This function locks the specific RDC_SEMA42 gate. If the gate has been locked by other processors, this function waits until it is unlocked and then lock it.

Parameters

<i>base</i>	RDC_SEMA42 peripheral base address.
<i>gateNum</i>	Gate number to lock.
<i>masterIndex</i>	Current processor master index.
<i>domainId</i>	Current processor domain ID.

19.3.5 static void RDC_SEMA42_Unlock (RDC_SEMAPHORE_Type * *base*, uint8_t *gateNum*) [inline], [static]

This function unlocks the specific RDC_SEMA42 gate. It only writes unlock value to the RDC_SEMA42 gate register. However, it does not check whether the RDC_SEMA42 gate is locked by the current processor or not. As a result, if the RDC_SEMA42 gate is not locked by the current processor, this function has no effect.

Parameters

<i>base</i>	RDC_SEMA42 peripheral base address.
<i>gateNum</i>	Gate number to unlock.

19.3.6 static int32_t RDC_SEMA42_GetLockMasterIndex (RDC_SEMAPHORE_Type * *base*, uint8_t *gateNum*) [inline], [static]

Parameters

<i>base</i>	RDC_SEMA42 peripheral base address.
<i>gateNum</i>	Gate number.

Returns

Return -1 if the gate is not locked by any master, otherwise return the master index.

19.3.7 int32_t RDC_SEMA42_GetLockDomainID (RDC_SEMAPHORE_Type * *base*, uint8_t *gateNum*)

Parameters

<i>base</i>	RDC_SEMA42 peripheral base address.
<i>gateNum</i>	Gate number.

Returns

Return -1 if the gate is not locked by any domain, otherwise return the domain ID.

19.3.8 `status_t RDC_SEMA42_ResetGate (RDC_SEMAPHORE_Type * base, uint8_t gateNum)`

This function resets a RDC_SEMA42 gate to an unlocked status.

Parameters

<i>base</i>	RDC_SEMA42 peripheral base address.
<i>gateNum</i>	Gate number.

Return values

<i>kStatus_Success</i>	RDC_SEMA42 gate is reset successfully.
<i>kStatus_Failed</i>	Some other reset process is ongoing.

19.3.9 static status_t RDC_SEMA42_ResetAllGates (RDC_SEMAPHORE_Type * *base*) [inline], [static]

This function resets all RDC_SEMA42 gate to an unlocked status.

Parameters

<i>base</i>	RDC_SEMA42 peripheral base address.
-------------	-------------------------------------

Return values

<i>kStatus_Success</i>	RDC_SEMA42 is reset successfully.
<i>kStatus_RDC_SEMA42_-Reseting</i>	Some other reset process is ongoing.

Chapter 20

SAI: Serial Audio Interface

20.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Serial Audio Interface (SAI) module of MCUXpresso SDK devices.

SAI driver includes functional APIs and transactional APIs.

Functional APIs target low-level APIs. Functional APIs can be used for SAI initialization, configuration and operation, and for optimization and customization purposes. Using the functional API requires the knowledge of the SAI peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. SAI functional operation groups provide the functional API set.

Transactional APIs target high-level APIs. Transactional APIs can be used to enable the peripheral and in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are a critical requirement, see the transactional API implementation and write a custom code. All transactional APIs use the `sai_handle_t` as the first parameter. Initialize the handle by calling the [SAI_TransferTxCreateHandle\(\)](#) or [SAI_TransferRxCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer. This means that the functions [SAI_TransferSendNonBlocking\(\)](#) and [SAI_TransferReceiveNonBlocking\(\)](#) set up the interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the `kStatus_SAI_TxIdle` and `kStatus_SAI_RxIdle` status.

20.2 Typical configurations

Bit width configuration

SAI driver support 8/16/24/32bits stereo/mono raw audio data transfer. SAI EDMA driver support 8/16/32bits stereo/mono raw audio data transfer, since the EDMA doesn't support 24bit data width, so application should pre-convert the 24bit data to 32bit. SAI DMA driver support 8/16/32bits stereo/mono raw audio data transfer, since the EDMA doesn't support 24bit data width, so application should pre-convert the 24bit data to 32bit. SAI SDMA driver support 8/16/24/32bits stereo/mono raw audio data transfer.

Frame configuration

SAI driver support I2S, DSP, Left justified, Right justified, TDM mode. Application can call the api directly: `SAI_GetClassicI2SConfig` `SAI_GetLeftJustifiedConfig` `SAI_GetRightJustifiedConfig` `SAI_GetTDMConfig` `SAI_GetDSPConfig`

20.3 Typical use case

20.3.1 SAI Send/receive using an interrupt method

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/sai

20.3.2 SAI Send/receive using a DMA method

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/sai

Modules

- [SAI Driver](#)
- [SAI SDMA Driver](#)

20.4 *Typical use case*

20.5 SAI Driver

20.5.1 Overview

Data Structures

- struct [sai_config_t](#)
SAI user configuration structure. [More...](#)
- struct [sai_transfer_format_t](#)
sai transfer format [More...](#)
- struct [sai_master_clock_t](#)
master clock configurations [More...](#)
- struct [sai_fifo_t](#)
sai fifo configurations [More...](#)
- struct [sai_bit_clock_t](#)
sai bit clock configurations [More...](#)
- struct [sai_frame_sync_t](#)
sai frame sync configurations [More...](#)
- struct [sai_serial_data_t](#)
sai serial data configurations [More...](#)
- struct [sai_transceiver_t](#)
sai transceiver configurations [More...](#)
- struct [sai_transfer_t](#)
SAI transfer structure. [More...](#)
- struct [sai_handle_t](#)
SAI handle structure. [More...](#)

Macros

- #define [SAI_XFER_QUEUE_SIZE](#) (4U)
SAI transfer queue size, user can refine it according to use case.
- #define [FSL_SAI_HAS_FIFO_EXTEND_FEATURE](#) 1
sai fifo feature

Typedefs

- typedef void(* [sai_transfer_callback_t](#))(I2S_Type *base, sai_handle_t *handle, [status_t](#) status, void *userData)
SAI transfer callback prototype.

Enumerations

- enum {
`kStatus_SAI_TxBusy` = MAKE_STATUS(kStatusGroup_SAI, 0),
`kStatus_SAI_RxBusy` = MAKE_STATUS(kStatusGroup_SAI, 1),
`kStatus_SAI_TxError` = MAKE_STATUS(kStatusGroup_SAI, 2),
`kStatus_SAI_RxError` = MAKE_STATUS(kStatusGroup_SAI, 3),
`kStatus_SAI_QueueFull` = MAKE_STATUS(kStatusGroup_SAI, 4),
`kStatus_SAI_TxIdle` = MAKE_STATUS(kStatusGroup_SAI, 5),
`kStatus_SAI_RxIdle` = MAKE_STATUS(kStatusGroup_SAI, 6) }
_sai_status_t, SAI return status.
- enum {
`kSAI_Channel0Mask` = 1 << 0U,
`kSAI_Channel1Mask` = 1 << 1U,
`kSAI_Channel2Mask` = 1 << 2U,
`kSAI_Channel3Mask` = 1 << 3U,
`kSAI_Channel4Mask` = 1 << 4U,
`kSAI_Channel5Mask` = 1 << 5U,
`kSAI_Channel6Mask` = 1 << 6U,
`kSAI_Channel7Mask` = 1 << 7U }
_sai_channel_mask, sai channel mask value, actual channel numbers is depend soc specific
- enum `sai_protocol_t` {
`kSAI_BusLeftJustified` = 0x0U,
`kSAI_BusRightJustified`,
`kSAI_BusI2S`,
`kSAI_BusPCMA`,
`kSAI_BusPCMB` }
Define the SAI bus type.
- enum `sai_master_slave_t` {
`kSAI_Master` = 0x0U,
`kSAI_Slave` = 0x1U,
`kSAI_Bclk_Master_FrameSync_Slave` = 0x2U,
`kSAI_Bclk_Slave_FrameSync_Master` = 0x3U }
Master or slave mode.
- enum `sai_mono_stereo_t` {
`kSAI_Stereo` = 0x0U,
`kSAI_MonoRight`,
`kSAI_MonoLeft` }
Mono or stereo audio format.
- enum `sai_data_order_t` {
`kSAI_DataLSB` = 0x0U,
`kSAI_DataMSB` }
SAI data order, MSB or LSB.
- enum `sai_clock_polarity_t` {

- kSAI_PolarityActiveHigh = 0x0U,
 - kSAI_PolarityActiveLow = 0x1U,
 - kSAI_SampleOnFallingEdge = 0x0U,
 - kSAI_SampleOnRisingEdge = 0x1U }

SAI clock polarity, active high or low.
- enum sai_sync_mode_t {
 - kSAI_ModeAsync = 0x0U,
 - kSAI_ModeSync }

Synchronous or asynchronous mode.
- enum sai_bclk_source_t {
 - kSAI_BclkSourceBusclk = 0x0U,
 - kSAI_BclkSourceMclkOption1 = 0x1U,
 - kSAI_BclkSourceMclkOption2 = 0x2U,
 - kSAI_BclkSourceMclkOption3 = 0x3U,
 - kSAI_BclkSourceMclkDiv = 0x1U,
 - kSAI_BclkSourceOtherSai0 = 0x2U,
 - kSAI_BclkSourceOtherSai1 = 0x3U }

Bit clock source.
- enum {
 - kSAI_WordStartInterruptEnable,
 - kSAI_SyncErrorInterruptEnable = I2S_TCSR_SEIE_MASK,
 - kSAI_FIFOWarningInterruptEnable = I2S_TCSR_FWIE_MASK,
 - kSAI_FIFOErrorInterruptEnable = I2S_TCSR_FEIE_MASK,
 - kSAI_FIFORequestInterruptEnable = I2S_TCSR_FRIE_MASK }

_sai_interrupt_enable_t, The SAI interrupt enable flag
- enum {
 - kSAI_FIFOWarningDMAEnable = I2S_TCSR_FWDE_MASK,
 - kSAI_FIFORequestDMAEnable = I2S_TCSR_FRDE_MASK }

_sai_dma_enable_t, The DMA request sources
- enum {
 - kSAI_WordStartFlag = I2S_TCSR_WSF_MASK,
 - kSAI_SyncErrorFlag = I2S_TCSR_SEF_MASK,
 - kSAI_FIFOErrorFlag = I2S_TCSR_FEF_MASK,
 - kSAI_FIFORequestFlag = I2S_TCSR_FRF_MASK,
 - kSAI_FIFOWarningFlag = I2S_TCSR_FWF_MASK }

_sai_flags, The SAI status flag
- enum sai_reset_type_t {
 - kSAI_ResetTypeSoftware = I2S_TCSR_SR_MASK,
 - kSAI_ResetTypeFIFO = I2S_TCSR_FR_MASK,
 - kSAI_ResetAll = I2S_TCSR_SR_MASK | I2S_TCSR_FR_MASK }

The reset type.
- enum sai_fifo_packing_t {
 - kSAI_FifoPackingDisabled = 0x0U,
 - kSAI_FifoPacking8bit = 0x2U,
 - kSAI_FifoPacking16bit = 0x3U }

The SAI packing mode The mode includes 8 bit and 16 bit packing.
- enum sai_sample_rate_t {

```

kSAI_SampleRate8KHz = 8000U,
kSAI_SampleRate11025Hz = 11025U,
kSAI_SampleRate12KHz = 12000U,
kSAI_SampleRate16KHz = 16000U,
kSAI_SampleRate22050Hz = 22050U,
kSAI_SampleRate24KHz = 24000U,
kSAI_SampleRate32KHz = 32000U,
kSAI_SampleRate44100Hz = 44100U,
kSAI_SampleRate48KHz = 48000U,
kSAI_SampleRate96KHz = 96000U,
kSAI_SampleRate192KHz = 192000U,
kSAI_SampleRate384KHz = 384000U }

```

Audio sample rate.

- enum `sai_word_width_t` {
`kSAI_WordWidth8bits` = 8U,
`kSAI_WordWidth16bits` = 16U,
`kSAI_WordWidth24bits` = 24U,
`kSAI_WordWidth32bits` = 32U }

Audio word width.

- enum `sai_data_pin_state_t` {
`kSAI_DataPinStateTriState`,
`kSAI_DataPinStateOutputZero` = 1U }

sai data pin state definition

- enum `sai_fifo_combine_t` {
`kSAI_FifoCombineDisabled` = 0U,
`kSAI_FifoCombineModeEnabledOnRead`,
`kSAI_FifoCombineModeEnabledOnWrite`,
`kSAI_FifoCombineModeEnabledOnReadWrite` }

sai fifo combine mode definition

- enum `sai_transceiver_type_t` {
`kSAI_Transmitter` = 0U,
`kSAI_Receiver` = 1U }

sai transceiver type

- enum `sai_frame_sync_len_t` {
`kSAI_FrameSyncLenOneBitClk` = 0U,
`kSAI_FrameSyncLenPerWordWidth` = 1U }

sai frame sync len

Driver version

- #define `FSL_SAI_DRIVER_VERSION` (`MAKE_VERSION(2, 3, 4)`)
Version 2.3.4.

Initialization and deinitialization

- void [SAI_TxInit](#) (I2S_Type *base, const [sai_config_t](#) *config)
Initializes the SAI Tx peripheral.
- void [SAI_RxInit](#) (I2S_Type *base, const [sai_config_t](#) *config)
Initializes the SAI Rx peripheral.
- void [SAI_TxGetDefaultConfig](#) ([sai_config_t](#) *config)
Sets the SAI Tx configuration structure to default values.
- void [SAI_RxGetDefaultConfig](#) ([sai_config_t](#) *config)
Sets the SAI Rx configuration structure to default values.
- void [SAI_Init](#) (I2S_Type *base)
Initializes the SAI peripheral.
- void [SAI_Deinit](#) (I2S_Type *base)
De-initializes the SAI peripheral.
- void [SAI_TxReset](#) (I2S_Type *base)
Resets the SAI Tx.
- void [SAI_RxReset](#) (I2S_Type *base)
Resets the SAI Rx.
- void [SAI_TxEnable](#) (I2S_Type *base, bool enable)
Enables/disables the SAI Tx.
- void [SAI_RxEnable](#) (I2S_Type *base, bool enable)
Enables/disables the SAI Rx.
- static void [SAI_TxSetBitClockDirection](#) (I2S_Type *base, [sai_master_slave_t](#) masterSlave)
Set Rx bit clock direction.
- static void [SAI_RxSetBitClockDirection](#) (I2S_Type *base, [sai_master_slave_t](#) masterSlave)
Set Rx bit clock direction.
- static void [SAI_RxSetFrameSyncDirection](#) (I2S_Type *base, [sai_master_slave_t](#) masterSlave)
Set Rx frame sync direction.
- static void [SAI_TxSetFrameSyncDirection](#) (I2S_Type *base, [sai_master_slave_t](#) masterSlave)
Set Tx frame sync direction.
- void [SAI_TxSetBitClockRate](#) (I2S_Type *base, uint32_t sourceClockHz, uint32_t sampleRate, uint32_t bitWidth, uint32_t channelNumbers)
Transmitter bit clock rate configurations.
- void [SAI_RxSetBitClockRate](#) (I2S_Type *base, uint32_t sourceClockHz, uint32_t sampleRate, uint32_t bitWidth, uint32_t channelNumbers)
Receiver bit clock rate configurations.
- void [SAI_TxSetBitclockConfig](#) (I2S_Type *base, [sai_master_slave_t](#) masterSlave, [sai_bit_clock_t](#) *config)
Transmitter Bit clock configurations.
- void [SAI_RxSetBitclockConfig](#) (I2S_Type *base, [sai_master_slave_t](#) masterSlave, [sai_bit_clock_t](#) *config)
Receiver Bit clock configurations.
- void [SAI_SetMasterClockConfig](#) (I2S_Type *base, [sai_master_clock_t](#) *config)
Master clock configurations.
- void [SAI_TxSetFifoConfig](#) (I2S_Type *base, [sai_fifo_t](#) *config)
SAI transmitter fifo configurations.
- void [SAI_RxSetFifoConfig](#) (I2S_Type *base, [sai_fifo_t](#) *config)
SAI receiver fifo configurations.
- void [SAI_TxSetFrameSyncConfig](#) (I2S_Type *base, [sai_master_slave_t](#) masterSlave, [sai_frame_sync_t](#) *config)

- *SAI transmitter Frame sync configurations.*
- void [SAI_RxSetFrameSyncConfig](#) (I2S_Type *base, [sai_master_slave_t](#) masterSlave, [sai_frame_sync_t](#) *config)
- *SAI receiver Frame sync configurations.*
- void [SAI_TxSetSerialDataConfig](#) (I2S_Type *base, [sai_serial_data_t](#) *config)
- *SAI transmitter Serial data configurations.*
- void [SAI_RxSetSerialDataConfig](#) (I2S_Type *base, [sai_serial_data_t](#) *config)
- *SAI receiver Serial data configurations.*
- void [SAI_TxSetConfig](#) (I2S_Type *base, [sai_transceiver_t](#) *config)
- *SAI transmitter configurations.*
- void [SAI_RxSetConfig](#) (I2S_Type *base, [sai_transceiver_t](#) *config)
- *SAI receiver configurations.*
- void [SAI_GetClassicI2SConfig](#) ([sai_transceiver_t](#) *config, [sai_word_width_t](#) bitWidth, [sai_mono_stereo_t](#) mode, uint32_t saiChannelMask)
- *Get classic I2S mode configurations.*
- void [SAI_GetLeftJustifiedConfig](#) ([sai_transceiver_t](#) *config, [sai_word_width_t](#) bitWidth, [sai_mono_stereo_t](#) mode, uint32_t saiChannelMask)
- *Get left justified mode configurations.*
- void [SAI_GetRightJustifiedConfig](#) ([sai_transceiver_t](#) *config, [sai_word_width_t](#) bitWidth, [sai_mono_stereo_t](#) mode, uint32_t saiChannelMask)
- *Get right justified mode configurations.*
- void [SAI_GetTDMConfig](#) ([sai_transceiver_t](#) *config, [sai_frame_sync_len_t](#) frameSyncWidth, [sai_word_width_t](#) bitWidth, uint32_t dataWordNum, uint32_t saiChannelMask)
- *Get TDM mode configurations.*
- void [SAI_GetDSPConfig](#) ([sai_transceiver_t](#) *config, [sai_frame_sync_len_t](#) frameSyncWidth, [sai_word_width_t](#) bitWidth, [sai_mono_stereo_t](#) mode, uint32_t saiChannelMask)
- *Get DSP mode configurations.*

Status

- static uint32_t [SAI_TxGetStatusFlag](#) (I2S_Type *base)
- *Gets the SAI Tx status flag state.*
- static void [SAI_TxClearStatusFlags](#) (I2S_Type *base, uint32_t mask)
- *Clears the SAI Tx status flag state.*
- static uint32_t [SAI_RxGetStatusFlag](#) (I2S_Type *base)
- *Gets the SAI Rx status flag state.*
- static void [SAI_RxClearStatusFlags](#) (I2S_Type *base, uint32_t mask)
- *Clears the SAI Rx status flag state.*
- void [SAI_TxSoftwareReset](#) (I2S_Type *base, [sai_reset_type_t](#) type)
- *Do software reset or FIFO reset .*
- void [SAI_RxSoftwareReset](#) (I2S_Type *base, [sai_reset_type_t](#) type)
- *Do software reset or FIFO reset .*
- void [SAI_TxSetChannelFIFOMask](#) (I2S_Type *base, uint8_t mask)
- *Set the Tx channel FIFO enable mask.*
- void [SAI_RxSetChannelFIFOMask](#) (I2S_Type *base, uint8_t mask)
- *Set the Rx channel FIFO enable mask.*
- void [SAI_TxSetDataOrder](#) (I2S_Type *base, [sai_data_order_t](#) order)
- *Set the Tx data order.*
- void [SAI_RxSetDataOrder](#) (I2S_Type *base, [sai_data_order_t](#) order)

- *Set the Rx data order.*
- void [SAI_TxSetBitClockPolarity](#) (I2S_Type *base, [sai_clock_polarity_t](#) polarity)
- *Set the Tx data order.*
- void [SAI_RxSetBitClockPolarity](#) (I2S_Type *base, [sai_clock_polarity_t](#) polarity)
- *Set the Rx data order.*
- void [SAI_TxSetFrameSyncPolarity](#) (I2S_Type *base, [sai_clock_polarity_t](#) polarity)
- *Set the Tx data order.*
- void [SAI_RxSetFrameSyncPolarity](#) (I2S_Type *base, [sai_clock_polarity_t](#) polarity)
- *Set the Rx data order.*
- void [SAI_TxSetFIFOPacking](#) (I2S_Type *base, [sai_fifo_packing_t](#) pack)
- *Set Tx FIFO packing feature.*
- void [SAI_RxSetFIFOPacking](#) (I2S_Type *base, [sai_fifo_packing_t](#) pack)
- *Set Rx FIFO packing feature.*
- static void [SAI_TxSetFIFOErrorContinue](#) (I2S_Type *base, bool isEnabled)
- *Set Tx FIFO error continue.*
- static void [SAI_RxSetFIFOErrorContinue](#) (I2S_Type *base, bool isEnabled)
- *Set Rx FIFO error continue.*

Interrupts

- static void [SAI_TxEnableInterrupts](#) (I2S_Type *base, uint32_t mask)
- *Enables the SAI Tx interrupt requests.*
- static void [SAI_RxEnableInterrupts](#) (I2S_Type *base, uint32_t mask)
- *Enables the SAI Rx interrupt requests.*
- static void [SAI_TxDisableInterrupts](#) (I2S_Type *base, uint32_t mask)
- *Disables the SAI Tx interrupt requests.*
- static void [SAI_RxDisableInterrupts](#) (I2S_Type *base, uint32_t mask)
- *Disables the SAI Rx interrupt requests.*

DMA Control

- static void [SAI_TxEnableDMA](#) (I2S_Type *base, uint32_t mask, bool enable)
- *Enables/disables the SAI Tx DMA requests.*
- static void [SAI_RxEnableDMA](#) (I2S_Type *base, uint32_t mask, bool enable)
- *Enables/disables the SAI Rx DMA requests.*
- static uint32_t [SAI_TxGetDataRegisterAddress](#) (I2S_Type *base, uint32_t channel)
- *Gets the SAI Tx data register address.*
- static uint32_t [SAI_RxGetDataRegisterAddress](#) (I2S_Type *base, uint32_t channel)
- *Gets the SAI Rx data register address.*

Bus Operations

- void [SAI_TxSetFormat](#) (I2S_Type *base, [sai_transfer_format_t](#) *format, uint32_t mclkSourceClockHz, uint32_t bclkSourceClockHz)
- *Configures the SAI Tx audio format.*
- void [SAI_RxSetFormat](#) (I2S_Type *base, [sai_transfer_format_t](#) *format, uint32_t mclkSourceClockHz, uint32_t bclkSourceClockHz)

- *Configures the SAI Rx audio format.*
- void [SAI_WriteBlocking](#) (I2S_Type *base, uint32_t channel, uint32_t bitWidth, uint8_t *buffer, uint32_t size)
- *Sends data using a blocking method.*
- void [SAI_WriteMultiChannelBlocking](#) (I2S_Type *base, uint32_t channel, uint32_t channelMask, uint32_t bitWidth, uint8_t *buffer, uint32_t size)
- *Sends data to multi channel using a blocking method.*
- static void [SAI_WriteData](#) (I2S_Type *base, uint32_t channel, uint32_t data)
- *Writes data into SAI FIFO.*
- void [SAI_ReadBlocking](#) (I2S_Type *base, uint32_t channel, uint32_t bitWidth, uint8_t *buffer, uint32_t size)
- *Receives data using a blocking method.*
- void [SAI_ReadMultiChannelBlocking](#) (I2S_Type *base, uint32_t channel, uint32_t channelMask, uint32_t bitWidth, uint8_t *buffer, uint32_t size)
- *Receives multi channel data using a blocking method.*
- static uint32_t [SAI_ReadData](#) (I2S_Type *base, uint32_t channel)
- *Reads data from the SAI FIFO.*

Transactional

- void [SAI_TransferTxCreateHandle](#) (I2S_Type *base, sai_handle_t *handle, sai_transfer_callback_t callback, void *userData)
- *Initializes the SAI Tx handle.*
- void [SAI_TransferRxCreateHandle](#) (I2S_Type *base, sai_handle_t *handle, sai_transfer_callback_t callback, void *userData)
- *Initializes the SAI Rx handle.*
- void [SAI_TransferTxSetConfig](#) (I2S_Type *base, sai_handle_t *handle, sai_transceiver_t *config)
- *SAI transmitter transfer configurations.*
- void [SAI_TransferRxSetConfig](#) (I2S_Type *base, sai_handle_t *handle, sai_transceiver_t *config)
- *SAI receiver transfer configurations.*
- [status_t](#) [SAI_TransferTxSetFormat](#) (I2S_Type *base, sai_handle_t *handle, sai_transfer_format_t *format, uint32_t mclkSourceClockHz, uint32_t bclkSourceClockHz)
- *Configures the SAI Tx audio format.*
- [status_t](#) [SAI_TransferRxSetFormat](#) (I2S_Type *base, sai_handle_t *handle, sai_transfer_format_t *format, uint32_t mclkSourceClockHz, uint32_t bclkSourceClockHz)
- *Configures the SAI Rx audio format.*
- [status_t](#) [SAI_TransferSendNonBlocking](#) (I2S_Type *base, sai_handle_t *handle, sai_transfer_t *xfer)
- *Performs an interrupt non-blocking send transfer on SAI.*
- [status_t](#) [SAI_TransferReceiveNonBlocking](#) (I2S_Type *base, sai_handle_t *handle, sai_transfer_t *xfer)
- *Performs an interrupt non-blocking receive transfer on SAI.*
- [status_t](#) [SAI_TransferGetSendCount](#) (I2S_Type *base, sai_handle_t *handle, size_t *count)
- *Gets a set byte count.*
- [status_t](#) [SAI_TransferGetReceiveCount](#) (I2S_Type *base, sai_handle_t *handle, size_t *count)
- *Gets a received byte count.*
- void [SAI_TransferAbortSend](#) (I2S_Type *base, sai_handle_t *handle)
- *Aborts the current send.*
- void [SAI_TransferAbortReceive](#) (I2S_Type *base, sai_handle_t *handle)

- *Aborts the current IRQ receive.*
- void [SAI_TransferTerminateSend](#) (I2S_Type *base, sai_handle_t *handle)
Terminate all SAI send.
- void [SAI_TransferTerminateReceive](#) (I2S_Type *base, sai_handle_t *handle)
Terminate all SAI receive.
- void [SAI_TransferTxHandleIRQ](#) (I2S_Type *base, sai_handle_t *handle)
Tx interrupt handler.
- void [SAI_TransferRxHandleIRQ](#) (I2S_Type *base, sai_handle_t *handle)
Rx interrupt handler.

20.5.2 Data Structure Documentation

20.5.2.1 struct sai_config_t

Data Fields

- [sai_protocol_t](#) protocol
Audio bus protocol in SAI.
- [sai_sync_mode_t](#) syncMode
SAI sync mode, control Tx/Rx clock sync.
- bool [mclkOutputEnable](#)
Master clock output enable, true means master clock divider enabled.
- [sai_bclk_source_t](#) bclkSource
Bit Clock source.
- [sai_master_slave_t](#) masterSlave
Master or slave.

20.5.2.2 struct sai_transfer_format_t

Data Fields

- uint32_t [sampleRate_Hz](#)
Sample rate of audio data.
- uint32_t [bitWidth](#)
Data length of audio data, usually 8/16/24/32 bits.
- [sai_mono_stereo_t](#) stereo
Mono or stereo.
- uint8_t [watermark](#)
Watermark value.
- uint8_t [channel](#)
Transfer start channel.
- uint8_t [channelMask](#)
enabled channel mask value, reference `_sai_channel_mask`
- uint8_t [endChannel](#)
end channel number
- uint8_t [channelNums](#)
Total enabled channel numbers.
- [sai_protocol_t](#) protocol

- Which audio protocol used.
- bool [isFrameSyncCompact](#)
True means Frame sync length is configurable according to bitWidth, false means frame sync length is 64 times of bit clock.

Field Documentation

(1) bool sai_transfer_format_t::isFrameSyncCompact

20.5.2.3 struct sai_master_clock_t

Data Fields

- bool [mclkOutputEnable](#)
master clock output enable
- uint32_t [mclkHz](#)
target mclk frequency
- uint32_t [mclkSourceClkHz](#)
mclk source frequency

20.5.2.4 struct sai_fifo_t

Data Fields

- bool [fifoContinueOnError](#)
fifo continues when error occur
- [sai_fifo_combine_t](#) [fifoCombine](#)
fifo combine mode
- [sai_fifo_packing_t](#) [fifoPacking](#)
fifo packing mode
- uint8_t [fifoWatermark](#)
fifo watermark

20.5.2.5 struct sai_bit_clock_t

Data Fields

- bool [bclkSrcSwap](#)
bit clock source swap
- bool [bclkInputDelay](#)
bit clock actually used by the transmitter is delayed by the pad output delay, this has effect of decreasing the data input setup time, but increasing the data output valid time .
- [sai_clock_polarity_t](#) [bclkPolarity](#)
bit clock polarity
- [sai_bclk_source_t](#) [bclkSource](#)
bit Clock source

Field Documentation

(1) `bool sai_bit_clock_t::bclkInputDelay`

20.5.2.6 struct `sai_frame_sync_t`

Data Fields

- `uint8_t frameSyncWidth`
frame sync width in number of bit clocks
- `bool frameSyncEarly`
TRUE is frame sync assert one bit before the first bit of frame FALSE is frame sync assert with the first bit of the frame.
- `sai_clock_polarity_t frameSyncPolarity`
frame sync polarity

20.5.2.7 struct `sai_serial_data_t`

Data Fields

- `sai_data_pin_state_t dataMode`
sai data pin state when slots masked or channel disabled
- `sai_data_order_t dataOrder`
configure whether the LSB or MSB is transmitted first
- `uint8_t dataWord0Length`
configure the number of bits in the first word in each frame
- `uint8_t dataWordNLength`
configure the number of bits in the each word in each frame, except the first word
- `uint8_t dataWordLength`
used to record the data length for dma transfer
- `uint8_t dataFirstBitShifted`
Configure the bit index for the first bit transmitted for each word in the frame.
- `uint8_t dataWordNum`
configure the number of words in each frame
- `uint32_t dataMaskedWord`
configure whether the transmit word is masked

20.5.2.8 struct `sai_transceiver_t`

Data Fields

- `sai_serial_data_t serialData`
serial data configurations
- `sai_frame_sync_t frameSync`
ws configurations
- `sai_bit_clock_t bitClock`
bit clock configurations
- `sai_fifo_t fifo`
fifo configurations
- `sai_master_slave_t masterSlave`
transceiver is master or slave

- [sai_sync_mode_t syncMode](#)
transceiver sync mode
- [uint8_t startChannel](#)
Transfer start channel.
- [uint8_t channelMask](#)
enabled channel mask value, reference `_sai_channel_mask`
- [uint8_t endChannel](#)
end channel number
- [uint8_t channelNums](#)
Total enabled channel numbers.

20.5.2.9 struct sai_transfer_t

Data Fields

- [uint8_t * data](#)
Data start address to transfer.
- [size_t dataSize](#)
Transfer size.

Field Documentation

(1) [uint8_t* sai_transfer_t::data](#)

(2) [size_t sai_transfer_t::dataSize](#)

20.5.2.10 struct _sai_handle

Data Fields

- [I2S_Type * base](#)
base address
- [uint32_t state](#)
Transfer status.
- [sai_transfer_callback_t callback](#)
Callback function called at transfer event.
- [void * userData](#)
Callback parameter passed to callback function.
- [uint8_t bitWidth](#)
Bit width for transfer, 8/16/24/32 bits.
- [uint8_t channel](#)
Transfer start channel.
- [uint8_t channelMask](#)
enabled channel mask value, refernece `_sai_channel_mask`
- [uint8_t endChannel](#)
end channel number
- [uint8_t channelNums](#)
Total enabled channel numbers.
- [sai_transfer_t saiQueue \[SAI_XFER_QUEUE_SIZE\]](#)
Transfer queue storing queued transfer.

- size_t **transferSize** [**SAI_XFER_QUEUE_SIZE**]
Data bytes need to transfer.
- volatile uint8_t **queueUser**
Index for user to queue transfer.
- volatile uint8_t **queueDriver**
Index for driver to get the transfer data and size.
- uint8_t **watermark**
Watermark value.

20.5.3 Macro Definition Documentation

20.5.3.1 #define SAI_XFER_QUEUE_SIZE (4U)

20.5.4 Enumeration Type Documentation

20.5.4.1 anonymous enum

Enumerator

kStatus_SAI_TxBusy SAI Tx is busy.
kStatus_SAI_RxBusy SAI Rx is busy.
kStatus_SAI_TxError SAI Tx FIFO error.
kStatus_SAI_RxError SAI Rx FIFO error.
kStatus_SAI_QueueFull SAI transfer queue is full.
kStatus_SAI_TxIdle SAI Tx is idle.
kStatus_SAI_RxIdle SAI Rx is idle.

20.5.4.2 anonymous enum

Enumerator

kSAI_Channel0Mask channel 0 mask value
kSAI_Channel1Mask channel 1 mask value
kSAI_Channel2Mask channel 2 mask value
kSAI_Channel3Mask channel 3 mask value
kSAI_Channel4Mask channel 4 mask value
kSAI_Channel5Mask channel 5 mask value
kSAI_Channel6Mask channel 6 mask value
kSAI_Channel7Mask channel 7 mask value

20.5.4.3 enum sai_protocol_t

Enumerator

kSAI_BusLeftJustified Uses left justified format.

kSAI_BusRightJustified Uses right justified format.

kSAI_BusI2S Uses I2S format.

kSAI_BusPCMA Uses I2S PCM A format.

kSAI_BusPCMB Uses I2S PCM B format.

20.5.4.4 enum sai_master_slave_t

Enumerator

kSAI_Master Master mode include bclk and frame sync.

kSAI_Slave Slave mode include bclk and frame sync.

kSAI_Bclk_Master_FrameSync_Slave bclk in master mode, frame sync in slave mode

kSAI_Bclk_Slave_FrameSync_Master bclk in slave mode, frame sync in master mode

20.5.4.5 enum sai_mono_stereo_t

Enumerator

kSAI_Stereo Stereo sound.

kSAI_MonoRight Only Right channel have sound.

kSAI_MonoLeft Only left channel have sound.

20.5.4.6 enum sai_data_order_t

Enumerator

kSAI_DataLSB LSB bit transferred first.

kSAI_DataMSB MSB bit transferred first.

20.5.4.7 enum sai_clock_polarity_t

Enumerator

kSAI_PolarityActiveHigh Drive outputs on rising edge.

kSAI_PolarityActiveLow Drive outputs on falling edge.

kSAI_SampleOnFallingEdge Sample inputs on falling edge.

kSAI_SampleOnRisingEdge Sample inputs on rising edge.

20.5.4.8 enum sai_sync_mode_t

Enumerator

- kSAI_ModeAsync* Asynchronous mode.
- kSAI_ModeSync* Synchronous mode (with receiver or transmit)

20.5.4.9 enum sai_bclk_source_t

Enumerator

- kSAI_BclkSourceBusclk* Bit clock using bus clock.
- kSAI_BclkSourceMclkOption1* Bit clock MCLK option 1.
- kSAI_BclkSourceMclkOption2* Bit clock MCLK option2.
- kSAI_BclkSourceMclkOption3* Bit clock MCLK option3.
- kSAI_BclkSourceMclkDiv* Bit clock using master clock divider.
- kSAI_BclkSourceOtherSai0* Bit clock from other SAI device.
- kSAI_BclkSourceOtherSai1* Bit clock from other SAI device.

20.5.4.10 anonymous enum

Enumerator

- kSAI_WordStartInterruptEnable* Word start flag, means the first word in a frame detected.
- kSAI_SyncErrorInterruptEnable* Sync error flag, means the sync error is detected.
- kSAI_FIFOWarningInterruptEnable* FIFO warning flag, means the FIFO is empty.
- kSAI_FIFOErrorInterruptEnable* FIFO error flag.
- kSAI_FIFORequestInterruptEnable* FIFO request, means reached watermark.

20.5.4.11 anonymous enum

Enumerator

- kSAI_FIFOWarningDMAEnable* FIFO warning caused by the DMA request.
- kSAI_FIFORequestDMAEnable* FIFO request caused by the DMA request.

20.5.4.12 anonymous enum

Enumerator

- kSAI_WordStartFlag* Word start flag, means the first word in a frame detected.
- kSAI_SyncErrorFlag* Sync error flag, means the sync error is detected.
- kSAI_FIFOErrorFlag* FIFO error flag.
- kSAI_FIFORequestFlag* FIFO request flag.
- kSAI_FIFOWarningFlag* FIFO warning flag.

20.5.4.13 enum sai_reset_type_t

Enumerator

kSAI_ResetTypeSoftware Software reset, reset the logic state.
kSAI_ResetTypeFIFO FIFO reset, reset the FIFO read and write pointer.
kSAI_ResetAll All reset.

20.5.4.14 enum sai_fifo_packing_t

Enumerator

kSAI_FifoPackingDisabled Packing disabled.
kSAI_FifoPacking8bit 8 bit packing enabled
kSAI_FifoPacking16bit 16bit packing enabled

20.5.4.15 enum sai_sample_rate_t

Enumerator

kSAI_SampleRate8KHz Sample rate 8000 Hz.
kSAI_SampleRate11025Hz Sample rate 11025 Hz.
kSAI_SampleRate12KHz Sample rate 12000 Hz.
kSAI_SampleRate16KHz Sample rate 16000 Hz.
kSAI_SampleRate22050Hz Sample rate 22050 Hz.
kSAI_SampleRate24KHz Sample rate 24000 Hz.
kSAI_SampleRate32KHz Sample rate 32000 Hz.
kSAI_SampleRate44100Hz Sample rate 44100 Hz.
kSAI_SampleRate48KHz Sample rate 48000 Hz.
kSAI_SampleRate96KHz Sample rate 96000 Hz.
kSAI_SampleRate192KHz Sample rate 192000 Hz.
kSAI_SampleRate384KHz Sample rate 384000 Hz.

20.5.4.16 enum sai_word_width_t

Enumerator

kSAI_WordWidth8bits Audio data width 8 bits.
kSAI_WordWidth16bits Audio data width 16 bits.
kSAI_WordWidth24bits Audio data width 24 bits.
kSAI_WordWidth32bits Audio data width 32 bits.

20.5.4.17 enum sai_data_pin_state_t

Enumerator

kSAI_DataPinStateTriState transmit data pins are tri-stated when slots are masked or channels are disabled

kSAI_DataPinStateOutputZero transmit data pins are never tri-stated and will output zero when slots are masked or channel disabled

20.5.4.18 enum sai_fifo_combine_t

Enumerator

kSAI_FifoCombineDisabled sai fifo combine mode disabled

kSAI_FifoCombineModeEnabledOnRead sai fifo combine mode enabled on FIFO reads

kSAI_FifoCombineModeEnabledOnWrite sai fifo combine mode enabled on FIFO write

kSAI_FifoCombineModeEnabledOnReadWrite sai fifo combined mode enabled on FIFO read/writes

20.5.4.19 enum sai_transceiver_type_t

Enumerator

kSAI_Transmitter sai transmitter

kSAI_Receiver sai receiver

20.5.4.20 enum sai_frame_sync_len_t

Enumerator

kSAI_FrameSyncLenOneBitClk 1 bit clock frame sync len for DSP mode

kSAI_FrameSyncLenPerWordWidth Frame sync length decided by word width.

20.5.5 Function Documentation**20.5.5.1 void SAI_TxInit (I2S_Type * *base*, const sai_config_t * *config*)**

Deprecated Do not use this function. It has been superseded by [SAI_Init](#)

Ungates the SAI clock, resets the module, and configures SAI Tx with a configuration structure. The configuration structure can be custom filled or set with default values by [SAI_TxGetDefaultConfig\(\)](#).

Note

This API should be called at the beginning of the application to use the SAI driver. Otherwise, accessing the SAIM module can cause a hard fault because the clock is not enabled.

Parameters

<i>base</i>	SAI base pointer
<i>config</i>	SAI configuration structure.

20.5.5.2 void SAI_RxInit (I2S_Type * *base*, const sai_config_t * *config*)

Deprecated Do not use this function. It has been superseded by [SAI_Init](#)

Ungates the SAI clock, resets the module, and configures the SAI Rx with a configuration structure. The configuration structure can be custom filled or set with default values by [SAI_RxGetDefaultConfig\(\)](#).

Note

This API should be called at the beginning of the application to use the SAI driver. Otherwise, accessing the SAI module can cause a hard fault because the clock is not enabled.

Parameters

<i>base</i>	SAI base pointer
<i>config</i>	SAI configuration structure.

20.5.5.3 void SAI_TxGetDefaultConfig (sai_config_t * *config*)

Deprecated Do not use this function. It has been superseded by [SAI_GetClassicI2SConfig](#), [SAI_GetLeftJustifiedConfig](#), [SAI_GetRightJustifiedConfig](#), [SAI_GetDSPConfig](#), [SAI_GetTDMConfig](#)

This API initializes the configuration structure for use in [SAI_TxConfig\(\)](#). The initialized structure can remain unchanged in [SAI_TxConfig\(\)](#), or it can be modified before calling [SAI_TxConfig\(\)](#). This is an example.

```
sai_config_t config;
SAI_TxGetDefaultConfig(&config);
```

Parameters

<i>config</i>	pointer to master configuration structure
---------------	---

20.5.5.4 void SAI_RxGetDefaultConfig (sai_config_t * *config*)

Deprecated Do not use this function. It has been superceded by [SAI_GetClassicI2SConfig](#), [SAI_GetLeft-JustifiedConfig](#) , [SAI_GetRightJustifiedConfig](#), [SAI_GetDSPConfig](#), [SAI_GetTDMConfig](#)

This API initializes the configuration structure for use in SAI_RxConfig(). The initialized structure can remain unchanged in SAI_RxConfig() or it can be modified before calling SAI_RxConfig(). This is an example.

```
sai_config_t config;
SAI_RxGetDefaultConfig(&config);
```

Parameters

<i>config</i>	pointer to master configuration structure
---------------	---

20.5.5.5 void SAI_Init (I2S_Type * *base*)

This API gates the SAI clock. The SAI module can't operate unless SAI_Init is called to enable the clock.

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

20.5.5.6 void SAI_Deinit (I2S_Type * *base*)

This API gates the SAI clock. The SAI module can't operate unless SAI_TxInit or SAI_RxInit is called to enable the clock.

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

20.5.5.7 void SAI_TxReset (I2S_Type * *base*)

This function enables the software reset and FIFO reset of SAI Tx. After reset, clear the reset bit.

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

20.5.5.8 void SAI_RxReset (I2S_Type * *base*)

This function enables the software reset and FIFO reset of SAI Rx. After reset, clear the reset bit.

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

20.5.5.9 void SAI_TxEnable (I2S_Type * *base*, bool *enable*)

Parameters

<i>base</i>	SAI base pointer.
<i>enable</i>	True means enable SAI Tx, false means disable.

20.5.5.10 void SAI_RxEnable (I2S_Type * *base*, bool *enable*)

Parameters

<i>base</i>	SAI base pointer.
<i>enable</i>	True means enable SAI Rx, false means disable.

20.5.5.11 static void SAI_TxSetBitClockDirection (I2S_Type * *base*, sai_master_slave_t *masterSlave*) [inline], [static]

Select bit clock direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

<i>masterSlave</i>	reference sai_master_slave_t.
--------------------	-------------------------------

20.5.5.12 static void SAI_RxSetBitClockDirection (I2S_Type * *base*, sai_master_slave_t *masterSlave*) [inline], [static]

Select bit clock direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	reference sai_master_slave_t.

20.5.5.13 static void SAI_RxSetFrameSyncDirection (I2S_Type * *base*, sai_master_slave_t *masterSlave*) [inline], [static]

Select frame sync direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	reference sai_master_slave_t.

20.5.5.14 static void SAI_TxSetFrameSyncDirection (I2S_Type * *base*, sai_master_slave_t *masterSlave*) [inline], [static]

Select frame sync direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	reference sai_master_slave_t.

20.5.5.15 void SAI_TxSetBitClockRate (I2S_Type * *base*, uint32_t *sourceClockHz*, uint32_t *sampleRate*, uint32_t *bitWidth*, uint32_t *channelNumbers*)

Parameters

<i>base</i>	SAI base pointer.
<i>sourceClockHz</i>	Bit clock source frequency.
<i>sampleRate</i>	Audio data sample rate.
<i>bitWidth</i>	Audio data bitWidth.
<i>channel-Numbers</i>	Audio channel numbers.

20.5.5.16 void SAI_RxSetBitClockRate (I2S_Type * *base*, uint32_t *sourceClockHz*, uint32_t *sampleRate*, uint32_t *bitWidth*, uint32_t *channelNumbers*)

Parameters

<i>base</i>	SAI base pointer.
<i>sourceClockHz</i>	Bit clock source frequency.
<i>sampleRate</i>	Audio data sample rate.
<i>bitWidth</i>	Audio data bitWidth.
<i>channel-Numbers</i>	Audio channel numbers.

20.5.5.17 void SAI_TxSetBitclockConfig (I2S_Type * *base*, sai_master_slave_t *masterSlave*, sai_bit_clock_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	bit clock other configurations, can be NULL in slave mode.

20.5.5.18 void SAI_RxSetBitclockConfig (I2S_Type * *base*, sai_master_slave_t *masterSlave*, sai_bit_clock_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	bit clock other configurations, can be NULL in slave mode.

20.5.5.19 void SAI_SetMasterClockConfig (I2S_Type * *base*, sai_master_clock_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	master clock configurations.

20.5.5.20 void SAI_TxSetFifoConfig (I2S_Type * *base*, sai_fifo_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	fifo configurations.

20.5.5.21 void SAI_RxSetFifoConfig (I2S_Type * *base*, sai_fifo_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	fifo configurations.

20.5.5.22 void SAI_TxSetFrameSyncConfig (I2S_Type * *base*, sai_master_slave_t *masterSlave*, sai_frame_sync_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	frame sync configurations, can be NULL in slave mode.

20.5.5.23 void SAI_RxSetFrameSyncConfig (I2S_Type * *base*, sai_master_slave_t *masterSlave*, sai_frame_sync_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	frame sync configurations, can be NULL in slave mode.

20.5.5.24 void SAI_TxSetSerialDataConfig (I2S_Type * *base*, sai_serial_data_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	serial data configurations.

20.5.5.25 void SAI_RxSetSerialDataConfig (I2S_Type * *base*, sai_serial_data_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	serial data configurations.

20.5.5.26 void SAI_TxSetConfig (I2S_Type * *base*, sai_transceiver_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	transmitter configurations.

20.5.5.27 void SAI_RxSetConfig (I2S_Type * *base*, sai_transceiver_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	receiver configurations.

20.5.5.28 void SAI_GetClassicI2SConfig (sai_transceiver_t * *config*, sai_word_width_t *bitWidth*, sai_mono_stereo_t *mode*, uint32_t *saiChannelMask*)

Parameters

<i>config</i>	transceiver configurations.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

20.5.5.29 void SAI_GetLeftJustifiedConfig (sai_transceiver_t * *config*, sai_word_width_t *bitWidth*, sai_mono_stereo_t *mode*, uint32_t *saiChannelMask*)

Parameters

<i>config</i>	transceiver configurations.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

20.5.5.30 void SAI_GetRightJustifiedConfig (sai_transceiver_t * *config*, sai_word_width_t *bitWidth*, sai_mono_stereo_t *mode*, uint32_t *saiChannelMask*)

Parameters

<i>config</i>	transceiver configurations.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

20.5.5.31 void SAI_GetTDMConfig (sai_transceiver_t * *config*, sai_frame_sync_len_t *frameSyncWidth*, sai_word_width_t *bitWidth*, uint32_t *dataWordNum*, uint32_t *saiChannelMask*)

Parameters

<i>config</i>	transceiver configurations.
<i>frameSync-Width</i>	length of frame sync.
<i>bitWidth</i>	audio data word width.
<i>dataWordNum</i>	word number in one frame.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

20.5.5.32 void SAI_GetDSPConfig (sai_transceiver_t * *config*, sai_frame_sync_len_t *frameSyncWidth*, sai_word_width_t *bitWidth*, sai_mono_stereo_t *mode*, uint32_t *saiChannelMask*)

Note

DSP mode is also called PCM mode which support MODE A and MODE B, DSP/PCM MODE A configuration flow. RX is similiar but uses SAI_RxSetConfig instead of SAI_TxSetConfig:

```
* SAI_GetDSPConfig(config, kSAI_FrameSyncLenOneBitClk, bitWidth,
    kSAI_Stereo, channelMask)
* config->frameSync.frameSyncEarly = true;
* SAI_TxSetConfig(base, config)
*
```

DSP/PCM MODE B configuration flow for TX. RX is similiar but uses SAI_RxSetConfig instead of SAI_TxSetConfig:

```
* SAI_GetDSPConfig(config, kSAI_FrameSyncLenOneBitClk, bitWidth,
    kSAI_Stereo, channelMask)
* SAI_TxSetConfig(base, config)
*
```

Parameters

<i>config</i>	transceiver configurations.
<i>frameSync-Width</i>	length of frame sync.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannel-Mask</i>	mask value of the channel to enable.

20.5.5.33 `static uint32_t SAI_TxGetStatusFlag (I2S_Type * base) [inline],
[static]`

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

Returns

SAI Tx status flag value. Use the Status Mask to get the status value needed.

20.5.5.34 `static void SAI_TxClearStatusFlags (I2S_Type * base, uint32_t mask)`
[inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	State mask. It can be a combination of the following source if defined: <ul style="list-style-type: none"> • kSAI_WordStartFlag • kSAI_SyncErrorFlag • kSAI_FIFOErrorFlag

20.5.5.35 `static uint32_t SAI_RxGetStatusFlag (I2S_Type * base)` **[inline],**
[static]

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

Returns

SAI Rx status flag value. Use the Status Mask to get the status value needed.

20.5.5.36 `static void SAI_RxClearStatusFlags (I2S_Type * base, uint32_t mask)`
[inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	State mask. It can be a combination of the following sources if defined. <ul style="list-style-type: none"> • kSAI_WordStartFlag • kSAI_SyncErrorFlag • kSAI_FIFOErrorFlag

20.5.5.37 void SAI_TxSoftwareReset (I2S_Type * *base*, sai_reset_type_t *type*)

FIFO reset means clear all the data in the FIFO, and make the FIFO pointer both to 0. Software reset means clear the Tx internal logic, including the bit clock, frame count etc. But software reset will not clear any configuration registers like TCR1~TCR5. This function will also clear all the error flags such as FIFO error, sync error etc.

Parameters

<i>base</i>	SAI base pointer
<i>type</i>	Reset type, FIFO reset or software reset

20.5.5.38 void SAI_RxSoftwareReset (I2S_Type * *base*, sai_reset_type_t *type*)

FIFO reset means clear all the data in the FIFO, and make the FIFO pointer both to 0. Software reset means clear the Rx internal logic, including the bit clock, frame count etc. But software reset will not clear any configuration registers like RCR1~RCR5. This function will also clear all the error flags such as FIFO error, sync error etc.

Parameters

<i>base</i>	SAI base pointer
<i>type</i>	Reset type, FIFO reset or software reset

20.5.5.39 void SAI_TxSetChannelFIFOMask (I2S_Type * *base*, uint8_t *mask*)

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	Channel enable mask, 0 means all channel FIFO disabled, 1 means channel 0 enabled, 3 means both channel 0 and channel 1 enabled.

20.5.5.40 void SAI_RxSetChannelFIFOMask (I2S_Type * *base*, uint8_t *mask*)

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	Channel enable mask, 0 means all channel FIFO disabled, 1 means channel 0 enabled, 3 means both channel 0 and channel 1 enabled.

20.5.5.41 void SAI_TxSetDataOrder (I2S_Type * *base*, sai_data_order_t *order*)

Parameters

<i>base</i>	SAI base pointer
<i>order</i>	Data order MSB or LSB

20.5.5.42 void SAI_RxSetDataOrder (I2S_Type * *base*, sai_data_order_t *order*)

Parameters

<i>base</i>	SAI base pointer
<i>order</i>	Data order MSB or LSB

20.5.5.43 void SAI_TxSetBitClockPolarity (I2S_Type * *base*, sai_clock_polarity_t *polarity*)

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

20.5.5.44 void SAI_RxSetBitClockPolarity (I2S_Type * *base*, sai_clock_polarity_t *polarity*)

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

20.5.5.45 void SAI_TxSetFrameSyncPolarity (I2S_Type * *base*, sai_clock_polarity_t *polarity*)

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

20.5.5.46 void SAI_RxSetFrameSyncPolarity (I2S_Type * *base*, sai_clock_polarity_t *polarity*)

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

20.5.5.47 void SAI_TxSetFIFOPacking (I2S_Type * *base*, sai_fifo_packing_t *pack*)

Parameters

<i>base</i>	SAI base pointer.
<i>pack</i>	FIFO pack type. It is element of sai_fifo_packing_t.

20.5.5.48 void SAI_RxSetFIFOPacking (I2S_Type * *base*, sai_fifo_packing_t *pack*)

Parameters

<i>base</i>	SAI base pointer.
<i>pack</i>	FIFO pack type. It is element of sai_fifo_packing_t.

**20.5.5.49 static void SAI_TxSetFIFOErrorContinue (I2S_Type * *base*, bool *isEnabled*)
[inline], [static]**

FIFO error continue mode means SAI will keep running while FIFO error occurred. If this feature not enabled, SAI will hang and users need to clear FEF flag in TCSR register.

Parameters

<i>base</i>	SAI base pointer.
<i>isEnabled</i>	Is FIFO error continue enabled, true means enable, false means disable.

20.5.5.50 static void SAI_RxSetFIFOErrorContinue (I2S_Type * *base*, bool *isEnabled*) [inline], [static]

FIFO error continue mode means SAI will keep running while FIFO error occurred. If this feature not enabled, SAI will hang and users need to clear FEF flag in RCSR register.

Parameters

<i>base</i>	SAI base pointer.
<i>isEnabled</i>	Is FIFO error continue enabled, true means enable, false means disable.

20.5.5.51 static void SAI_TxEnableInterrupts (I2S_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> • kSAI_WordStartInterruptEnable • kSAI_SyncErrorInterruptEnable • kSAI_FIFOWarningInterruptEnable • kSAI_FIFORequestInterruptEnable • kSAI_FIFOErrorInterruptEnable

20.5.5.52 static void SAI_RxEnableInterrupts (I2S_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> • kSAI_WordStartInterruptEnable • kSAI_SyncErrorInterruptEnable • kSAI_FIFOWarningInterruptEnable • kSAI_FIFORequestInterruptEnable • kSAI_FIFOErrorInterruptEnable

20.5.5.53 static void SAI_TxDisableInterrupts (I2S_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> • kSAI_WordStartInterruptEnable • kSAI_SyncErrorInterruptEnable • kSAI_FIFOWarningInterruptEnable • kSAI_FIFORequestInterruptEnable • kSAI_FIFOErrorInterruptEnable

20.5.5.54 static void SAI_RxDisableInterrupts (I2S_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> • kSAI_WordStartInterruptEnable • kSAI_SyncErrorInterruptEnable • kSAI_FIFOWarningInterruptEnable • kSAI_FIFORequestInterruptEnable • kSAI_FIFOErrorInterruptEnable

20.5.5.55 `static void SAI_TxEnableDMA (I2S_Type * base, uint32_t mask, bool enable)`
`[inline], [static]`

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	DMA source The parameter can be combination of the following sources if defined. <ul style="list-style-type: none"> • kSAI_FIFOWarningDMAEnable • kSAI_FIFOREquestDMAEnable
<i>enable</i>	True means enable DMA, false means disable DMA.

20.5.5.56 static void SAI_RxEnableDMA (I2S_Type * *base*, uint32_t *mask*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	DMA source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> • kSAI_FIFOWarningDMAEnable • kSAI_FIFOREquestDMAEnable
<i>enable</i>	True means enable DMA, false means disable DMA.

20.5.5.57 static uint32_t SAI_TxGetDataRegisterAddress (I2S_Type * *base*, uint32_t *channel*) [inline], [static]

This API is used to provide a transfer address for the SAI DMA transfer configuration.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Which data channel used.

Returns

data register address.

20.5.5.58 static uint32_t SAI_RxGetDataRegisterAddress (I2S_Type * *base*, uint32_t *channel*) [inline], [static]

This API is used to provide a transfer address for the SAI DMA transfer configuration.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Which data channel used.

Returns

data register address.

20.5.5.59 void SAI_TxSetFormat (I2S_Type * *base*, sai_transfer_format_t * *format*, uint32_t *mclkSourceClockHz*, uint32_t *bclkSourceClockHz*)

Deprecated Do not use this function. It has been superceded by [SAI_TxSetConfig](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	SAI base pointer.
<i>format</i>	Pointer to the SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If the bit clock source is a master clock, this value should equal the masterClockHz.

20.5.5.60 void SAI_RxSetFormat (I2S_Type * *base*, sai_transfer_format_t * *format*, uint32_t *mclkSourceClockHz*, uint32_t *bclkSourceClockHz*)

Deprecated Do not use this function. It has been superceded by [SAI_RxSetConfig](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	SAI base pointer.
<i>format</i>	Pointer to the SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If the bit clock source is a master clock, this value should equal the masterClockHz.

20.5.5.61 void SAI_WriteBlocking (I2S_Type * *base*, uint32_t *channel*, uint32_t *bitWidth*, uint8_t * *buffer*, uint32_t *size*)

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be written.
<i>size</i>	Bytes to be written.

20.5.5.62 void SAI_WriteMultiChannelBlocking (I2S_Type * *base*, uint32_t *channel*, uint32_t *channelMask*, uint32_t *bitWidth*, uint8_t * *buffer*, uint32_t *size*)

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>channelMask</i>	channel mask.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be written.
<i>size</i>	Bytes to be written.

**20.5.5.63 static void SAI_WriteData (I2S_Type * *base*, uint32_t *channel*, uint32_t *data*)
[inline], [static]**

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>data</i>	Data needs to be written.

20.5.5.64 void SAI_ReadBlocking (I2S_Type * *base*, uint32_t *channel*, uint32_t *bitWidth*, uint8_t * *buffer*, uint32_t *size*)

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be read.
<i>size</i>	Bytes to be read.

20.5.5.65 void SAI_ReadMultiChannelBlocking (I2S_Type * *base*, uint32_t *channel*, uint32_t *channelMask*, uint32_t *bitWidth*, uint8_t * *buffer*, uint32_t *size*)

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>channelMask</i>	channel mask.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be read.
<i>size</i>	Bytes to be read.

**20.5.5.66 static uint32_t SAI_ReadData (I2S_Type * *base*, uint32_t *channel*)
[inline], [static]**

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.

Returns

Data in SAI FIFO.

20.5.5.67 void SAI_TransferTxCreateHandle (I2S_Type * *base*, sai_handle_t * *handle*, sai_transfer_callback_t *callback*, void * *userData*)

This function initializes the Tx handle for the SAI Tx transactional APIs. Call this function once to get the handle initialized.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI handle pointer.
<i>callback</i>	Pointer to the user callback function.
<i>userData</i>	User parameter passed to the callback function

20.5.5.68 void SAI_TransferRxCreateHandle (I2S_Type * *base*, sai_handle_t * *handle*, sai_transfer_callback_t *callback*, void * *userData*)

This function initializes the Rx handle for the SAI Rx transactional APIs. Call this function once to get the handle initialized.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>callback</i>	Pointer to the user callback function.
<i>userData</i>	User parameter passed to the callback function.

20.5.5.69 void SAI_TransferTxSetConfig (I2S_Type * *base*, sai_handle_t * *handle*, sai_transceiver_t * *config*)

This function initializes the Tx, include bit clock, frame sync, master clock, serial data and fifo configurations.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>config</i>	transmitter configurations.

20.5.5.70 void SAI_TransferRxSetConfig (I2S_Type * *base*, sai_handle_t * *handle*, sai_transceiver_t * *config*)

This function initializes the Rx, include bit clock, frame sync, master clock, serial data and fifo configurations.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>config</i>	receiver configurations.

20.5.5.71 status_t SAI_TransferTxSetFormat (I2S_Type * *base*, sai_handle_t * *handle*, sai_transfer_format_t * *format*, uint32_t *mclkSourceClockHz*, uint32_t *bclkSourceClockHz*)

Deprecated Do not use this function. It has been superseded by [SAI_TransferTxSetConfig](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>format</i>	Pointer to the SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If a bit clock source is a master clock, this value should equal the masterClockHz in format.

Returns

Status of this function. Return value is the status_t.

20.5.5.72 `status_t SAI_TransferRxSetFormat (I2S_Type * base, sai_handle_t * handle, sai_transfer_format_t * format, uint32_t mclkSourceClockHz, uint32_t bclkSourceClockHz)`

Deprecated Do not use this function. It has been superseded by [SAI_TransferRxSetConfig](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>format</i>	Pointer to the SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If a bit clock source is a master clock, this value should equal the masterClockHz in format.

Returns

Status of this function. Return value is one of `status_t`.

20.5.5.73 `status_t SAI_TransferSendNonBlocking (I2S_Type * base, sai_handle_t * handle, sai_transfer_t * xfer)`

Note

This API returns immediately after the transfer initiates. Call the `SAI_TxGetTransferStatusIRQ` to poll the transfer status and check whether the transfer is finished. If the return status is not `kStatus_SAI_Busy`, the transfer is finished.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the <code>sai_handle_t</code> structure which stores the transfer state.
<i>xfer</i>	Pointer to the sai_transfer_t structure.

Return values

<i>kStatus_Success</i>	Successfully started the data receive.
<i>kStatus_SAI_TxBusy</i>	Previous receive still not finished.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

20.5.5.74 **status_t SAI_TransferReceiveNonBlocking (I2S_Type * *base*, sai_handle_t * *handle*, sai_transfer_t * *xfer*)**

Note

This API returns immediately after the transfer initiates. Call the SAI_RxGetTransferStatusIRQ to poll the transfer status and check whether the transfer is finished. If the return status is not kStatus_SAI_Busy, the transfer is finished.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>xfer</i>	Pointer to the sai_transfer_t structure.

Return values

<i>kStatus_Success</i>	Successfully started the data receive.
<i>kStatus_SAI_RxBusy</i>	Previous receive still not finished.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

20.5.5.75 **status_t SAI_TransferGetSendCount (I2S_Type * *base*, sai_handle_t * *handle*, size_t * *count*)**

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>count</i>	Bytes count sent.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferInProgress</i>	There is not a non-blocking transaction currently in progress.

20.5.5.76 **status_t SAI_TransferGetReceiveCount (I2S_Type * *base*, sai_handle_t * *handle*, size_t * *count*)**

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>count</i>	Bytes count received.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferInProgress</i>	There is not a non-blocking transaction currently in progress.

20.5.5.77 **void SAI_TransferAbortSend (I2S_Type * *base*, sai_handle_t * *handle*)**

Note

This API can be called any time when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.

20.5.5.78 **void SAI_TransferAbortReceive (I2S_Type * *base*, sai_handle_t * *handle*)**

Note

This API can be called when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.

20.5.5.79 void SAI_TransferTerminateSend (I2S_Type * *base*, sai_handle_t * *handle*)

This function will clear all transfer slots buffered in the sai queue. If users only want to abort the current transfer slot, please call SAI_TransferAbortSend.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

20.5.5.80 void SAI_TransferTerminateReceive (I2S_Type * *base*, sai_handle_t * *handle*)

This function will clear all transfer slots buffered in the sai queue. If users only want to abort the current transfer slot, please call SAI_TransferAbortReceive.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

20.5.5.81 void SAI_TransferTxHandleIRQ (I2S_Type * *base*, sai_handle_t * *handle*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure.

20.5.5.82 void SAI_TransferRxHandleIRQ (I2S_Type * *base*, sai_handle_t * *handle*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure.

20.6 SAI SDMA Driver

20.6.1 Typical use case

20.6.2 Overview

Multi fifo transfer use sai sdma driver

The SDMA multi fifo script support transfer data between multi peripheral fifos and memory, a typical user case is that receiving multi sai channel data and put it into memory as

| channel 0 | channel 1 | channel 2 | channel 3 | channel 4 | |

Multi fifo script is target to implement above feature, it can supports 1.configurable fifo watermark range from $1 \sim (2^{12}-1)$, it is a value of `fifo_watermark * channel_numbers` 2.configurable fifo numbers, support up to 15 continuous fifos 3.configurable fifo address offset, support address offset up to 64

```
/* load sdma script */
SDMA_LoadScript()
/* sai multi channel configurations */
SAI_GetClassicI2SConfig(&config, DEMO_AUDIO_BIT_WIDTH, kSAI_Stereo,
    kSAI_Channel0Mask | kSAI_Channel1Mask |
    kSAI_Channel2Mask | kSAI_Channel3Mask | kSAI_Channel4Mask);
SAI_TransferRxSetConfigSDMA(SAI, handle, &config);
SAI_TransferReceiveSDMA(SAI, handle, &config);
```

Transmitting data using multi fifo is same as above.

Data Structures

- struct [sai_sdma_handle_t](#)
SAI DMA transfer handle, users should not touch the content of the handle. [More...](#)

Typedefs

- typedef void(* [sai_sdma_callback_t](#))(I2S_Type *base, sai_sdma_handle_t *handle, [status_t](#) status, void *userData)
SAI SDMA transfer callback function for finish and error.

Driver version

- #define [FSL_SAI_SDMA_DRIVER_VERSION](#) ([MAKE_VERSION](#)(2, 4, 1))
Version 2.4.1.

SDMA Transactional

- void [SAI_TransferTxCreateHandleSDMA](#) (I2S_Type *base, sai_sdma_handle_t *handle, [sai_sdma_callback_t](#) callback, void *userData, [sdma_handle_t](#) *dmaHandle, uint32_t eventSource)
Initializes the SAI SDMA handle.
- void [SAI_TransferRxCreateHandleSDMA](#) (I2S_Type *base, sai_sdma_handle_t *handle, [sai_sdma_callback_t](#) callback, void *userData, [sdma_handle_t](#) *dmaHandle, uint32_t eventSource)
Initializes the SAI Rx SDMA handle.
- void [SAI_TransferTxSetFormatSDMA](#) (I2S_Type *base, sai_sdma_handle_t *handle, [sai_transfer_format_t](#) *format, uint32_t mclkSourceClockHz, uint32_t bclkSourceClockHz)
Configures the SAI Tx audio format.
- void [SAI_TransferRxSetFormatSDMA](#) (I2S_Type *base, sai_sdma_handle_t *handle, [sai_transfer_format_t](#) *format, uint32_t mclkSourceClockHz, uint32_t bclkSourceClockHz)
Configures the SAI Rx audio format.
- [status_t](#) [SAI_TransferSendSDMA](#) (I2S_Type *base, sai_sdma_handle_t *handle, [sai_transfer_t](#) *xfer)
Performs a non-blocking SAI transfer using DMA.
- [status_t](#) [SAI_TransferReceiveSDMA](#) (I2S_Type *base, sai_sdma_handle_t *handle, [sai_transfer_t](#) *xfer)
Performs a non-blocking SAI receive using SDMA.
- void [SAI_TransferAbortSendSDMA](#) (I2S_Type *base, sai_sdma_handle_t *handle)
Aborts a SAI transfer using SDMA.
- void [SAI_TransferAbortReceiveSDMA](#) (I2S_Type *base, sai_sdma_handle_t *handle)
Aborts a SAI receive using SDMA.
- void [SAI_TransferRxSetConfigSDMA](#) (I2S_Type *base, sai_sdma_handle_t *handle, [sai_transceiver_t](#) *saiConfig)
brief Configures the SAI RX.
- void [SAI_TransferTxSetConfigSDMA](#) (I2S_Type *base, sai_sdma_handle_t *handle, [sai_transceiver_t](#) *saiConfig)
brief Configures the SAI Tx.

20.6.3 Data Structure Documentation

20.6.3.1 struct_sai_sdma_handle

Data Fields

- [sdma_handle_t](#) * [dmaHandle](#)
DMA handler for SAI send.
- uint8_t [bytesPerFrame](#)
Bytes in a frame.
- uint8_t [channel](#)
start data channel
- uint8_t [channelNums](#)
total transfer channel numbers, used for multifo
- uint8_t [channelMask](#)
enabled channel mask value, refernece [_sai_channel_mask](#)
- uint8_t [fifoOffset](#)

- *fifo address offset between multifo*
uint32_t **count**
The transfer data count in a DMA request.
- uint32_t **state**
Internal state for SAI SDMA transfer.
- uint32_t **eventSource**
SAI event source number.
- sai_sdma_callback_t **callback**
Callback for users while transfer finish or error occurs.
- void * **userData**
User callback parameter.
- sdma_buffer_descriptor_t **bdPool** [SAI_XFER_QUEUE_SIZE]
BD pool for SDMA transfer.
- sai_transfer_t **saiQueue** [SAI_XFER_QUEUE_SIZE]
Transfer queue storing queued transfer.
- size_t **transferSize** [SAI_XFER_QUEUE_SIZE]
Data bytes need to transfer.
- volatile uint8_t **queueUser**
Index for user to queue transfer.
- volatile uint8_t **queueDriver**
Index for driver to get the transfer data and size.

Field Documentation

- (1) sdma_buffer_descriptor_t sai_sdma_handle_t::bdPool[SAI_XFER_QUEUE_SIZE]
- (2) sai_transfer_t sai_sdma_handle_t::saiQueue[SAI_XFER_QUEUE_SIZE]
- (3) volatile uint8_t sai_sdma_handle_t::queueUser

20.6.4 Function Documentation

20.6.4.1 void SAI_TransferTxCreateHandleSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_sdma_callback_t *callback*, void * *userData*, sdma_handle_t * *dmaHandle*, uint32_t *eventSource*)

This function initializes the SAI master DMA handle, which can be used for other SAI master transactional APIs. Usually, for a specified SAI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI SDMA handle pointer.

<i>base</i>	SAI peripheral base address.
<i>callback</i>	Pointer to user callback function.
<i>userData</i>	User parameter passed to the callback function.
<i>dmaHandle</i>	SDMA handle pointer, this handle shall be static allocated by users.
<i>eventSource</i>	SAI event source number.

20.6.4.2 void SAI_TransferRxCreateHandleSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_sdma_callback_t *callback*, void * *userData*, sdma_handle_t * *dmaHandle*, uint32_t *eventSource*)

This function initializes the SAI slave DMA handle, which can be used for other SAI master transactional APIs. Usually, for a specified SAI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI SDMA handle pointer.
<i>base</i>	SAI peripheral base address.
<i>callback</i>	Pointer to user callback function.
<i>userData</i>	User parameter passed to the callback function.
<i>dmaHandle</i>	SDMA handle pointer, this handle shall be static allocated by users.
<i>eventSource</i>	SAI event source number.

20.6.4.3 void SAI_TransferTxSetFormatSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_transfer_format_t * *format*, uint32_t *mclkSourceClockHz*, uint32_t *bclkSourceClockHz*)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred. This function also sets the SDMA parameter according to formatting requirements.

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

<i>handle</i>	SAI SDMA handle pointer.
<i>format</i>	Pointer to SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If bit clock source is master clock, this value should equals to masterClockHz in format.

Return values

<i>kStatus_Success</i>	Audio format set successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.

20.6.4.4 void SAI_TransferRxSetFormatSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_transfer_format_t * *format*, uint32_t *mclkSourceClockHz*, uint32_t *bclkSourceClockHz*)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred. This function also sets the SDMA parameter according to formatting requirements.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI SDMA handle pointer.
<i>format</i>	Pointer to SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If a bit clock source is the master clock, this value should equal to masterClockHz in format.

Return values

<i>kStatus_Success</i>	Audio format set successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.

20.6.4.5 status_t SAI_TransferSendSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_transfer_t * *xfer*)

Note

This interface returns immediately after the transfer initiates. Call SAI_GetTransferStatus to poll the transfer status and check whether the SAI transfer is finished.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI SDMA handle pointer.
<i>xfer</i>	Pointer to the DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a SAI SDMA send successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.
<i>kStatus_TxBusy</i>	SAI is busy sending data.

20.6.4.6 status_t SAI_TransferReceiveSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_transfer_t * *xfer*)

Note

This interface returns immediately after the transfer initiates. Call the SAI_GetReceiveRemaining-Bytes to poll the transfer status and check whether the SAI transfer is finished.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI SDMA handle pointer.
<i>xfer</i>	Pointer to DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a SAI SDMA receive successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.
<i>kStatus_RxBusy</i>	SAI is busy receiving data.

20.6.4.7 void SAI_TransferAbortSendSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI SDMA handle pointer.

20.6.4.8 void SAI_TransferAbortReceiveSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*)

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI SDMA handle pointer.

20.6.4.9 void SAI_TransferRxSetConfigSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_transceiver_t * *saiConfig*)

param base SAI base pointer. param handle SAI SDMA handle pointer. param saiConig sai configurations.

20.6.4.10 void SAI_TransferTxSetConfigSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_transceiver_t * *saiConfig*)

param base SAI base pointer. param handle SAI SDMA handle pointer. param saiConig sai configurations.

Chapter 21

SDMA: Smart Direct Memory Access (SDMA) Controller Driver

21.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Smart Direct Memory Access (SDMA) of devices.

21.2 Typical use case

21.2.1 SDMA Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/sdma

Data Structures

- struct [sdma_config_t](#)
SDMA global configuration structure. [More...](#)
- struct [sdma_multi_fifo_config_t](#)
SDMA multi fifo configurations. [More...](#)
- struct [sdma_sw_done_config_t](#)
SDMA sw done configurations. [More...](#)
- struct [sdma_p2p_config_t](#)
SDMA peripheral to peripheral R7 config. [More...](#)
- struct [sdma_transfer_config_t](#)
SDMA transfer configuration. [More...](#)
- struct [sdma_buffer_descriptor_t](#)
SDMA buffer descriptor structure. [More...](#)
- struct [sdma_channel_control_t](#)
SDMA channel control descriptor structure. [More...](#)
- struct [sdma_context_data_t](#)
SDMA context structure for each channel. [More...](#)
- struct [sdma_handle_t](#)
SDMA transfer handle structure. [More...](#)

Typedefs

- typedef void(* [sdma_callback](#))(struct _sdma_handle *handle, void *userData, bool transferDone, uint32_t bdIndex)
Define callback function for SDMA.

Enumerations

- enum `sdma_transfer_size_t` {
`kSDMA_TransferSize1Bytes` = 0x1U,
`kSDMA_TransferSize2Bytes` = 0x2U,
`kSDMA_TransferSize3Bytes` = 0x3U,
`kSDMA_TransferSize4Bytes` = 0x0U }
SDMA transfer configuration.
- enum `sdma_bd_status_t` {
`kSDMA_BDStatusDone` = 0x1U,
`kSDMA_BDStatusWrap` = 0x2U,
`kSDMA_BDStatusContinuous` = 0x4U,
`kSDMA_BDStatusInterrupt` = 0x8U,
`kSDMA_BDStatusError` = 0x10U,
`kSDMA_BDStatusLast`,
`kSDMA_BDStatusExtend` = 0x80U }
SDMA buffer descriptor status.
- enum `sdma_bd_command_t` {
`kSDMA_BDCommandSETDM` = 0x1U,
`kSDMA_BDCommandGETDM` = 0x2U,
`kSDMA_BDCommandSETPM` = 0x4U,
`kSDMA_BDCommandGETPM` = 0x6U,
`kSDMA_BDCommandSETCTX` = 0x7U,
`kSDMA_BDCommandGETCTX` = 0x3U }
SDMA buffer descriptor command.
- enum `sdma_context_switch_mode_t` {
`kSDMA_ContextSwitchModeStatic` = 0x0U,
`kSDMA_ContextSwitchModeDynamicLowPower`,
`kSDMA_ContextSwitchModeDynamicWithNoLoop`,
`kSDMA_ContextSwitchModeDynamic` }
SDMA context switch mode.
- enum `sdma_clock_ratio_t` {
`kSDMA_HalfARMClockFreq` = 0x0U,
`kSDMA_ARMClockFreq` }
SDMA core clock frequency ratio to the ARM DMA interface.
- enum `sdma_transfer_type_t` {
`kSDMA_MemoryToMemory` = 0x0U,
`kSDMA_PeripheralToMemory`,
`kSDMA_MemoryToPeripheral`,
`kSDMA_PeripheralToPeripheral` }
SDMA transfer type.
- enum `sdma_peripheral_t` {

```

kSDMA_PeripheralTypeMemory = 0x0,
kSDMA_PeripheralTypeUART,
kSDMA_PeripheralTypeUART_SP,
kSDMA_PeripheralTypeSPDIF,
kSDMA_PeripheralNormal,
kSDMA_PeripheralNormal_SP,
kSDMA_PeripheralMultiFifoPDM,
kSDMA_PeripheralMultiFifoSaiRX,
kSDMA_PeripheralMultiFifoSaiTX,
kSDMA_PeripheralASRCM2P,
kSDMA_PeripheralASRCP2M,
kSDMA_PeripheralASRCP2P }

```

Peripheral type use SDMA.

- enum {


```

kStatus_SDMA_ERROR = MAKE_STATUS(kStatusGroup_SDMA, 0),
kStatus_SDMA_Busy = MAKE_STATUS(kStatusGroup_SDMA, 1) }

```

_sdma_transfer_status SDMA transfer status
- enum {


```

kSDMA_MultiFifoWatermarkLevelMask = 0xFFFU,
kSDMA_MultiFifoNumsMask = 0xFU,
kSDMA_MultiFifoOffsetMask = 0xFU,
kSDMA_MultiFifoSwDoneMask = 0x1U,
kSDMA_MultiFifoSwDoneSelectorMask = 0xFU }

```

_sdma_multi_fifo_mask SDMA multi fifo mask
- enum {


```

kSDMA_MultiFifoWatermarkLevelShift = 0U,
kSDMA_MultiFifoNumsShift = 12U,
kSDMA_MultiFifoOffsetShift = 16U,
kSDMA_MultiFifoSwDoneShift = 23U,
kSDMA_MultiFifoSwDoneSelectorShift = 24U }

```

_sdma_multi_fifo_shift SDMA multi fifo shift
- enum {


```

kSDMA_DoneChannel0 = 0U,
kSDMA_DoneChannel1 = 1U,
kSDMA_DoneChannel2 = 2U,
kSDMA_DoneChannel3 = 3U,
kSDMA_DoneChannel4 = 4U,
kSDMA_DoneChannel5 = 5U,
kSDMA_DoneChannel6 = 6U,
kSDMA_DoneChannel7 = 7U }

```

_sdma_done_channel SDMA done channel
- enum `sdma_done_src_t` {

```

kSDMA_DoneSrcSW = 0U,
kSDMA_DoneSrcHwEvent0U = 1U,
kSDMA_DoneSrcHwEvent1U = 2U,
kSDMA_DoneSrcHwEvent2U = 3U,
kSDMA_DoneSrcHwEvent3U = 4U,
kSDMA_DoneSrcHwEvent4U = 5U,
kSDMA_DoneSrcHwEvent5U = 6U,
kSDMA_DoneSrcHwEvent6U = 7U,
kSDMA_DoneSrcHwEvent7U = 8U,
kSDMA_DoneSrcHwEvent8U = 9U,
kSDMA_DoneSrcHwEvent9U = 10U,
kSDMA_DoneSrcHwEvent10U = 11U,
kSDMA_DoneSrcHwEvent11U = 12U,
kSDMA_DoneSrcHwEvent12U = 13U,
kSDMA_DoneSrcHwEvent13U = 14U,
kSDMA_DoneSrcHwEvent14U = 15U,
kSDMA_DoneSrcHwEvent15U = 16U,
kSDMA_DoneSrcHwEvent16U = 17U,
kSDMA_DoneSrcHwEvent17U = 18U,
kSDMA_DoneSrcHwEvent18U = 19U,
kSDMA_DoneSrcHwEvent19U = 20U,
kSDMA_DoneSrcHwEvent20U = 21U,
kSDMA_DoneSrcHwEvent21U = 22U,
kSDMA_DoneSrcHwEvent22U = 23U,
kSDMA_DoneSrcHwEvent23U = 24U,
kSDMA_DoneSrcHwEvent24U = 25U,
kSDMA_DoneSrcHwEvent25U = 26U,
kSDMA_DoneSrcHwEvent26U = 27U,
kSDMA_DoneSrcHwEvent27U = 28U,
kSDMA_DoneSrcHwEvent28U = 29U,
kSDMA_DoneSrcHwEvent29U = 30U,
kSDMA_DoneSrcHwEvent30U = 31U,
kSDMA_DoneSrcHwEvent31U = 32U }

```

SDMA done source.

Driver version

- #define `FSL_SDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 3, 6)`)
SDMA driver version.

SDMA initialization and de-initialization

- void `SDMA_Init` (`SDMAARM_Type *base`, const `sdma_config_t *config`)
Initializes the SDMA peripheral.
- void `SDMA_Deinit` (`SDMAARM_Type *base`)
Deinitializes the SDMA peripheral.

- void [SDMA_GetDefaultConfig](#) ([sdma_config_t](#) *config)
Gets the SDMA default configuration structure.
- void [SDMA_ResetModule](#) ([SDMAARM_Type](#) *base)
Sets all SDMA core register to reset status.

SDMA Channel Operation

- static void [SDMA_EnableChannelErrorInterrupts](#) ([SDMAARM_Type](#) *base, [uint32_t](#) channel)
Enables the interrupt source for the SDMA error.
- static void [SDMA_DisableChannelErrorInterrupts](#) ([SDMAARM_Type](#) *base, [uint32_t](#) channel)
Disables the interrupt source for the SDMA error.

SDMA Buffer Descriptor Operation

- void [SDMA_ConfigBufferDescriptor](#) ([sdma_buffer_descriptor_t](#) *bd, [uint32_t](#) srcAddr, [uint32_t](#) destAddr, [sdma_transfer_size_t](#) busWidth, [size_t](#) bufferSize, bool isLast, bool enableInterrupt, bool isWrap, [sdma_transfer_type_t](#) type)
Sets buffer descriptor contents.

SDMA Channel Transfer Operation

- static void [SDMA_SetChannelPriority](#) ([SDMAARM_Type](#) *base, [uint32_t](#) channel, [uint8_t](#) priority)
Set SDMA channel priority.
- static void [SDMA_SetSourceChannel](#) ([SDMAARM_Type](#) *base, [uint32_t](#) source, [uint32_t](#) channel-Mask)
Set SDMA request source mapping channel.
- static void [SDMA_StartChannelSoftware](#) ([SDMAARM_Type](#) *base, [uint32_t](#) channel)
Start a SDMA channel by software trigger.
- static void [SDMA_StartChannelEvents](#) ([SDMAARM_Type](#) *base, [uint32_t](#) channel)
Start a SDMA channel by hardware events.
- static void [SDMA_StopChannel](#) ([SDMAARM_Type](#) *base, [uint32_t](#) channel)
Stop a SDMA channel.
- void [SDMA_SetContextSwitchMode](#) ([SDMAARM_Type](#) *base, [sdma_context_switch_mode_t](#) mode)
Set the SDMA context switch mode.

SDMA Channel Status Operation

- static [uint32_t](#) [SDMA_GetChannelInterruptStatus](#) ([SDMAARM_Type](#) *base)
Gets the SDMA interrupt status of all channels.
- static void [SDMA_ClearChannelInterruptStatus](#) ([SDMAARM_Type](#) *base, [uint32_t](#) mask)
Clear the SDMA channel interrupt status of specific channels.
- static [uint32_t](#) [SDMA_GetChannelStopStatus](#) ([SDMAARM_Type](#) *base)
Gets the SDMA stop status of all channels.
- static void [SDMA_ClearChannelStopStatus](#) ([SDMAARM_Type](#) *base, [uint32_t](#) mask)
Clear the SDMA channel stop status of specific channels.
- static [uint32_t](#) [SDMA_GetChannelPendStatus](#) ([SDMAARM_Type](#) *base)
Gets the SDMA channel pending status of all channels.
- static void [SDMA_ClearChannelPendStatus](#) ([SDMAARM_Type](#) *base, [uint32_t](#) mask)

- *Clear the SDMA channel pending status of specific channels.*
- static uint32_t [SDMA_GetErrorStatus](#) (SDMAARM_Type *base)
Gets the SDMA channel error status.
- bool [SDMA_GetRequestSourceStatus](#) (SDMAARM_Type *base, uint32_t source)
Gets the SDMA request source pending status.

SDMA Transactional Operation

- void [SDMA_CreateHandle](#) (sdma_handle_t *handle, SDMAARM_Type *base, uint32_t channel, sdma_context_data_t *context)
Creates the SDMA handle.
- void [SDMA_InstallBDMemory](#) (sdma_handle_t *handle, sdma_buffer_descriptor_t *BDPool, uint32_t BDCount)
Installs the BDs memory pool into the SDMA handle.
- void [SDMA_SetCallback](#) (sdma_handle_t *handle, sdma_callback callback, void *userData)
Installs a callback function for the SDMA transfer.
- void [SDMA_SetMultiFifoConfig](#) (sdma_transfer_config_t *config, uint32_t fifoNums, uint32_t fifoOffset)
multi fifo configurations.
- void [SDMA_EnableSwDone](#) (SDMAARM_Type *base, sdma_transfer_config_t *config, uint8_t sel, sdma_peripheral_t type)
enable sdma sw done feature.
- void [SDMA_SetDoneConfig](#) (SDMAARM_Type *base, sdma_transfer_config_t *config, sdma_peripheral_t type, sdma_done_src_t doneSrc)
sdma channel done configurations.
- void [SDMA_LoadScript](#) (SDMAARM_Type *base, uint32_t destAddr, void *srcAddr, size_t bufferSizeBytes)
load script to sdma program memory.
- void [SDMA_DumpScript](#) (SDMAARM_Type *base, uint32_t srcAddr, void *destAddr, size_t bufferSizeBytes)
dump script from sdma program memory.
- void [SDMA_PrepareTransfer](#) (sdma_transfer_config_t *config, uint32_t srcAddr, uint32_t destAddr, uint32_t srcWidth, uint32_t destWidth, uint32_t bytesEachRequest, uint32_t transferSize, uint32_t eventSource, sdma_peripheral_t peripheral, sdma_transfer_type_t type)
Prepares the SDMA transfer structure.
- void [SDMA_PrepareP2PTransfer](#) (sdma_transfer_config_t *config, uint32_t srcAddr, uint32_t destAddr, uint32_t srcWidth, uint32_t destWidth, uint32_t bytesEachRequest, uint32_t transferSize, uint32_t eventSource, uint32_t eventSource1, sdma_peripheral_t peripheral, sdma_p2p_config_t *p2p)
Prepares the SDMA P2P transfer structure.
- void [SDMA_SubmitTransfer](#) (sdma_handle_t *handle, const sdma_transfer_config_t *config)
Submits the SDMA transfer request.
- void [SDMA_StartTransfer](#) (sdma_handle_t *handle)
SDMA starts transfer.
- void [SDMA_StopTransfer](#) (sdma_handle_t *handle)
SDMA stops transfer.
- void [SDMA_AbortTransfer](#) (sdma_handle_t *handle)
SDMA aborts transfer.
- uint32_t [SDMA_GetTransferredBytes](#) (sdma_handle_t *handle)
Get transferred bytes while not using BD pools.

- bool [SDMA_IsPeripheralInSPBA](#) (uint32_t addr)
Judge if address located in SPBA.
- void [SDMA_HandleIRQ](#) (sdma_handle_t *handle)
SDMA IRQ handler for complete a buffer descriptor transfer.

21.3 Data Structure Documentation

21.3.1 struct sdma_config_t

Data Fields

- bool [enableRealTimeDebugPin](#)
If enable real-time debug pin, default is closed to reduce power consumption.
- bool [isSoftwareResetClearLock](#)
If software reset clears the LOCK bit which prevent writing SDMA scripts into SDMA.
- [sdma_clock_ratio_t](#) ratio
SDMA core clock ratio to ARM platform DMA interface.

Field Documentation

(1) bool sdma_config_t::enableRealTimeDebugPin

(2) bool sdma_config_t::isSoftwareResetClearLock

21.3.2 struct sdma_multi_fifo_config_t

Data Fields

- uint8_t [fifoNums](#)
fifo numbers
- uint8_t [fifoOffset](#)
offset between multi fifo data register address

21.3.3 struct sdma_sw_done_config_t

Data Fields

- bool [enableSwDone](#)
true is enable sw done, false is disable
- uint8_t [swDoneSel](#)
sw done channel number per peripheral type

21.3.4 struct sdma_p2p_config_t

Data Fields

- uint8_t [sourceWatermark](#)
lower watermark value
- uint8_t [destWatermark](#)
higher watermark value
- bool [continuousTransfer](#)
0: the amount of samples to be transferred is equal to the cont field of mode word 1: the amount of samples to be transferred is unknown and script will keep on transferring as long as both events are detected and script must be stopped by application.

Field Documentation

(1) bool sdma_p2p_config_t::continuousTransfer

21.3.5 struct sdma_transfer_config_t

This structure configures the source/destination transfer attribute.

Data Fields

- uint32_t [srcAddr](#)
Source address of the transfer.
- uint32_t [destAddr](#)
Destination address of the transfer.
- [sdma_transfer_size_t](#) [srcTransferSize](#)
Source data transfer size.
- [sdma_transfer_size_t](#) [destTransferSize](#)
Destination data transfer size.
- uint32_t [bytesPerRequest](#)
Bytes to transfer in a minor loop.
- uint32_t [transferSzie](#)
Bytes to transfer for this descriptor.
- uint32_t [scriptAddr](#)
SDMA script address located in SDMA ROM.
- uint32_t [eventSource](#)
Event source number for the channel.
- uint32_t [eventSource1](#)
event source 1
- bool [isEventIgnore](#)
True means software trigger, false means hardware trigger.
- bool [isSoftTriggerIgnore](#)
If ignore the HE bit, 1 means use hardware events trigger, 0 means software trigger.
- [sdma_transfer_type_t](#) [type](#)
Transfer type, transfer type used to decide the SDMA script.
- [sdma_multi_fifo_config_t](#) [multiFifo](#)

- *multi fifo configurations*
`sdma_sw_done_config_t swDone`
- *sw done selector*
`uint32_t watermarkLevel`
watermark level
- `uint32_t eventMask0`
event mask 0
- `uint32_t eventMask1`
event mask 1

Field Documentation

- (1) `sdma_transfer_size_t sdma_transfer_config_t::srcTransferSize`
- (2) `sdma_transfer_size_t sdma_transfer_config_t::destTransferSize`
- (3) `uint32_t sdma_transfer_config_t::scriptAddr`
- (4) `uint32_t sdma_transfer_config_t::eventSource`

0 means no event, use software trigger

- (5) `sdma_transfer_type_t sdma_transfer_config_t::type`

21.3.6 struct sdma_buffer_descriptor_t

This structure is a buffer descriptor, this structure describes the buffer start address and other options

Data Fields

- `uint32_t count`: 16
Bytes of the buffer length for this buffer descriptor.
- `uint32_t status`: 8
E,R,I,C,W,D status bits stored here.
- `uint32_t command`: 8
command mostly used for channel 0
- `uint32_t bufferAddr`
Buffer start address for this descriptor.
- `uint32_t extendBufferAddr`
External buffer start address, this is an optional for a transfer.

Field Documentation

- (1) `uint32_t sdma_buffer_descriptor_t::count`
- (2) `uint32_t sdma_buffer_descriptor_t::bufferAddr`
- (3) `uint32_t sdma_buffer_descriptor_t::extendBufferAddr`

21.3.7 struct sdma_channel_control_t

Data Fields

- uint32_t [currentBDAddr](#)
Address of current buffer descriptor processed.
- uint32_t [baseBDAddr](#)
The start address of the buffer descriptor array.
- uint32_t [channelDesc](#)
Optional for transfer.
- uint32_t [status](#)
Channel status.

21.3.8 struct sdma_context_data_t

This structure can be load into SDMA core, with this structure, SDMA scripts can start work.

Data Fields

- uint32_t [GeneralReg](#) [8]
8 general regsiters used for SDMA RISC core

21.3.9 struct sdma_handle_t

Data Fields

- [sdma_callback](#) [callback](#)
Callback function for major count exhausted.
- void * [userData](#)
Callback function parameter.
- SDMAARM_Type * [base](#)
SDMA peripheral base address.
- [sdma_buffer_descriptor_t](#) * [BDPool](#)
Pointer to memory stored BD arrays.
- uint32_t [bdCount](#)
How many buffer descriptor.
- uint32_t [bdIndex](#)
How many buffer descriptor.
- uint32_t [eventSource](#)
Event source count for the channel.
- uint32_t [eventSource1](#)
Event source 1 count for the channel.
- [sdma_context_data_t](#) * [context](#)
Channel context to exectute in SDMA.
- uint8_t [channel](#)

- `uint8_t priority` *SDMA channel number.*
- `uint8_t flags` *SDMA channel priority.*
- *The status of the current channel.*

Field Documentation

- (1) `sdma_callback sdma_handle_t::callback`
- (2) `void* sdma_handle_t::userData`
- (3) `SDMAARM_Type* sdma_handle_t::base`
- (4) `sdma_buffer_descriptor_t* sdma_handle_t::BDPool`
- (5) `uint8_t sdma_handle_t::channel`
- (6) `uint8_t sdma_handle_t::flags`

21.4 Macro Definition Documentation

21.4.1 `#define FSL_SDMA_DRIVER_VERSION (MAKE_VERSION(2, 3, 6))`

Version 2.3.6.

21.5 Typedef Documentation

21.5.1 `typedef void(* sdma_callback)(struct _sdma_handle *handle, void *userData, bool transferDone, uint32_t bdIndex)`

21.6 Enumeration Type Documentation

21.6.1 `enum sdma_transfer_size_t`

Enumerator

- | | |
|---------------------------------|--|
| <i>kSDMA_TransferSize1Bytes</i> | Source/Destination data transfer size is 1 byte every time. |
| <i>kSDMA_TransferSize2Bytes</i> | Source/Destination data transfer size is 2 bytes every time. |
| <i>kSDMA_TransferSize3Bytes</i> | Source/Destination data transfer size is 3 bytes every time. |
| <i>kSDMA_TransferSize4Bytes</i> | Source/Destination data transfer size is 4 bytes every time. |

21.6.2 `enum sdma_bd_status_t`

Enumerator

- | | |
|---------------------------|---|
| <i>kSDMA_BDStatusDone</i> | BD ownership, 0 means ARM core owns the BD, while 1 means SDMA owns BD. |
|---------------------------|---|

- kSDMA_BDStatusWrap* While this BD is last one, the next BD will be the first one.
- kSDMA_BDStatusContinuous* Buffer is allowed to transfer/receive to/from multiple buffers.
- kSDMA_BDStatusInterrupt* While this BD finished, send an interrupt.
- kSDMA_BDStatusError* Error occurred on buffer descriptor command.
- kSDMA_BDStatusLast* This BD is the last BD in this array. It means the transfer ended after this buffer
- kSDMA_BDStatusExtend* Buffer descriptor extend status for SDMA scripts.

21.6.3 enum sdma_bd_command_t

Enumerator

- kSDMA_BDCommandSETDM* Load SDMA data memory from ARM core memory buffer.
- kSDMA_BDCommandGETDM* Copy SDMA data memory to ARM core memory buffer.
- kSDMA_BDCommandSETPM* Load SDMA program memory from ARM core memory buffer.
- kSDMA_BDCommandGETPM* Copy SDMA program memory to ARM core memory buffer.
- kSDMA_BDCommandSETCTX* Load context for one channel into SDMA RAM from ARM platform memory buffer.
- kSDMA_BDCommandGETCTX* Copy context for one channel from SDMA RAM to ARM platform memory buffer.

21.6.4 enum sdma_context_switch_mode_t

Enumerator

- kSDMA_ContextSwitchModeStatic* SDMA context switch mode static.
- kSDMA_ContextSwitchModeDynamicLowPower* SDMA context switch mode dynamic with low power.
- kSDMA_ContextSwitchModeDynamicWithNoLoop* SDMA context switch mode dynamic with no loop.
- kSDMA_ContextSwitchModeDynamic* SDMA context switch mode dynamic.

21.6.5 enum sdma_clock_ratio_t

Enumerator

- kSDMA_HalfARMClockFreq* SDMA core clock frequency half of ARM platform.
- kSDMA_ARMClockFreq* SDMA core clock frequency equals to ARM platform.

21.6.6 enum sdma_transfer_type_t

Enumerator

kSDMA_MemoryToMemory Transfer from memory to memory.
kSDMA_PeripheralToMemory Transfer from peripheral to memory.
kSDMA_MemoryToPeripheral Transfer from memory to peripheral.
kSDMA_PeripheralToPeripheral Transfer from peripheral to peripheral.

21.6.7 enum sdma_peripheral_t

Enumerator

kSDMA_PeripheralTypeMemory Peripheral DDR memory.
kSDMA_PeripheralTypeUART UART use SDMA.
kSDMA_PeripheralTypeUART_SP UART instance in SPBA use SDMA.
kSDMA_PeripheralTypeSPDIF SPDIF use SDMA.
kSDMA_PeripheralNormal Normal peripheral use SDMA.
kSDMA_PeripheralNormal_SP Normal peripheral in SPBA use SDMA.
kSDMA_PeripheralMultiFifoPDM multi fifo PDM
kSDMA_PeripheralMultiFifoSaiRX multi fifo sai rx use SDMA
kSDMA_PeripheralMultiFifoSaiTX multi fifo sai tx use SDMA
kSDMA_PeripheralASRCM2P asrc m2p
kSDMA_PeripheralASRCP2M asrc p2m
kSDMA_PeripheralASRCP2P asrc p2p

21.6.8 anonymous enum

Enumerator

kStatus_SDMA_ERROR SDMA context error.
kStatus_SDMA_Busy Channel is busy and can't handle the transfer request.

21.6.9 anonymous enum

Enumerator

kSDMA_MultiFifoWatermarkLevelMask multi fifo watermark level mask
kSDMA_MultiFifoNumsMask multi fifo nums mask
kSDMA_MultiFifoOffsetMask multi fifo offset mask
kSDMA_MultiFifoSwDoneMask multi fifo sw done mask
kSDMA_MultiFifoSwDoneSelectorMask multi fifo sw done selector mask

21.6.10 anonymous enum

Enumerator

kSDMA_MultiFifoWatermarkLevelShift multi fifo watermark level shift
kSDMA_MultiFifoNumsShift multi fifo nums shift
kSDMA_MultiFifoOffsetShift multi fifo offset shift
kSDMA_MultiFifoSwDoneShift multi fifo sw done shift
kSDMA_MultiFifoSwDoneSelectorShift multi fifo sw done selector shift

21.6.11 anonymous enum

Enumerator

kSDMA_DoneChannel0 SDMA done channel 0.
kSDMA_DoneChannel1 SDMA done channel 1.
kSDMA_DoneChannel2 SDMA done channel 2.
kSDMA_DoneChannel3 SDMA done channel 3.
kSDMA_DoneChannel4 SDMA done channel 4.
kSDMA_DoneChannel5 SDMA done channel 5.
kSDMA_DoneChannel6 SDMA done channel 6.
kSDMA_DoneChannel7 SDMA done channel 7.

21.6.12 enum sdma_done_src_t

Enumerator

kSDMA_DoneSrcSW software done
kSDMA_DoneSrcHwEvent0U HW event 0 is used for DONE event.
kSDMA_DoneSrcHwEvent1U HW event 1 is used for DONE event.
kSDMA_DoneSrcHwEvent2U HW event 2 is used for DONE event.
kSDMA_DoneSrcHwEvent3U HW event 3 is used for DONE event.
kSDMA_DoneSrcHwEvent4U HW event 4 is used for DONE event.
kSDMA_DoneSrcHwEvent5U HW event 5 is used for DONE event.
kSDMA_DoneSrcHwEvent6U HW event 6 is used for DONE event.
kSDMA_DoneSrcHwEvent7U HW event 7 is used for DONE event.
kSDMA_DoneSrcHwEvent8U HW event 8 is used for DONE event.
kSDMA_DoneSrcHwEvent9U HW event 9 is used for DONE event.
kSDMA_DoneSrcHwEvent10U HW event 10 is used for DONE event.
kSDMA_DoneSrcHwEvent11U HW event 11 is used for DONE event.
kSDMA_DoneSrcHwEvent12U HW event 12 is used for DONE event.
kSDMA_DoneSrcHwEvent13U HW event 13 is used for DONE event.
kSDMA_DoneSrcHwEvent14U HW event 14 is used for DONE event.
kSDMA_DoneSrcHwEvent15U HW event 15 is used for DONE event.

kSDMA_DoneSrcHwEvent16U HW event 16 is used for DONE event.
kSDMA_DoneSrcHwEvent17U HW event 17 is used for DONE event.
kSDMA_DoneSrcHwEvent18U HW event 18 is used for DONE event.
kSDMA_DoneSrcHwEvent19U HW event 19 is used for DONE event.
kSDMA_DoneSrcHwEvent20U HW event 20 is used for DONE event.
kSDMA_DoneSrcHwEvent21U HW event 21 is used for DONE event.
kSDMA_DoneSrcHwEvent22U HW event 22 is used for DONE event.
kSDMA_DoneSrcHwEvent23U HW event 23 is used for DONE event.
kSDMA_DoneSrcHwEvent24U HW event 24 is used for DONE event.
kSDMA_DoneSrcHwEvent25U HW event 25 is used for DONE event.
kSDMA_DoneSrcHwEvent26U HW event 26 is used for DONE event.
kSDMA_DoneSrcHwEvent27U HW event 27 is used for DONE event.
kSDMA_DoneSrcHwEvent28U HW event 28 is used for DONE event.
kSDMA_DoneSrcHwEvent29U HW event 29 is used for DONE event.
kSDMA_DoneSrcHwEvent30U HW event 30 is used for DONE event.
kSDMA_DoneSrcHwEvent31U HW event 31 is used for DONE event.

21.7 Function Documentation

21.7.1 void SDMA_Init (SDMAARM_Type * *base*, const sdma_config_t * *config*)

This function ungates the SDMA clock and configures the SDMA peripheral according to the configuration structure.

Parameters

<i>base</i>	SDMA peripheral base address.
<i>config</i>	A pointer to the configuration structure, see "sdma_config_t".

Note

This function enables the minor loop map feature.

21.7.2 void SDMA_Deinit (SDMAARM_Type * *base*)

This function gates the SDMA clock.

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

21.7.3 void SDMA_GetDefaultConfig (sdma_config_t * *config*)

This function sets the configuration structure to default values. The default configuration is set to the following values.

```
*  config.enableRealTimeDebugPin = false;
*  config.isSoftwareResetClearLock = true;
*  config.ratio = kSDMA_HalfARMClockFreq;
*
```

Parameters

<i>config</i>	A pointer to the SDMA configuration structure.
---------------	--

21.7.4 void SDMA_ResetModule (SDMAARM_Type * *base*)

If only reset ARM core, SDMA register cannot return to reset value, shall call this function to reset all SDMA register to reset value. But the internal status cannot be reset.

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

21.7.5 static void SDMA_EnableChannelErrorInterrupts (SDMAARM_Type * *base*, uint32_t *channel*) [inline], [static]

Enable this will trigger an interrupt while SDMA occurs error while executing scripts.

Parameters

<i>base</i>	SDMA peripheral base address.
<i>channel</i>	SDMA channel number.

21.7.6 static void SDMA_DisableChannelErrorInterrupts (SDMAARM_Type * *base*, uint32_t *channel*) [inline], [static]

Parameters

<i>base</i>	SDMA peripheral base address.
<i>channel</i>	SDMA channel number.

21.7.7 void SDMA_ConfigBufferDescriptor (sdma_buffer_descriptor_t * *bd*, uint32_t *srcAddr*, uint32_t *destAddr*, sdma_transfer_size_t *busWidth*, size_t *bufferSize*, bool *isLast*, bool *enableInterrupt*, bool *isWrap*, sdma_transfer_type_t *type*)

This function sets the descriptor contents such as source, dest address and status bits.

Parameters

<i>bd</i>	Pointer to the buffer descriptor structure.
<i>srcAddr</i>	Source address for the buffer descriptor.
<i>destAddr</i>	Destination address for the buffer descriptor.
<i>busWidth</i>	The transfer width, it only can be a member of sdma_transfer_size_t.
<i>bufferSize</i>	Buffer size for this descriptor, this number shall less than 0xFFFF. If need to transfer a big size, shall divide into several buffer descriptors.
<i>isLast</i>	Is the buffer descriptor the last one for the channel to transfer. If only one descriptor used for the channel, this bit shall set to TRUE.
<i>enableInterrupt</i>	If trigger an interrupt while this buffer descriptor transfer finished.
<i>isWrap</i>	Is the buffer descriptor need to be wrapped. While this bit set to true, it will automatically wrap to the first buffer descriptor to do transfer.
<i>type</i>	Transfer type, memory to memory, peripheral to memory or memory to peripheral.

21.7.8 static void SDMA_SetChannelPriority (SDMAARM_Type * *base*, uint32_t *channel*, uint8_t *priority*) [inline], [static]

This function sets the channel priority. The default value is 0 for all channels, priority 0 will prevents channel from starting, so the priority must be set before start a channel.

Parameters

<i>base</i>	SDMA peripheral base address.
<i>channel</i>	SDMA channel number.
<i>priority</i>	SDMA channel priority.

21.7.9 static void SDMA_SetSourceChannel (SDMAARM_Type * *base*, uint32_t *source*, uint32_t *channelMask*) [inline], [static]

This function sets which channel will be triggered by the dma request source.

Parameters

<i>base</i>	SDMA peripheral base address.
<i>source</i>	SDMA dma request source number.
<i>channelMask</i>	SDMA channel mask. 1 means channel 0, 2 means channel 1, 4 means channel 3. SDMA supports an event trigger multi-channel. A channel can also be triggered by several source events.

21.7.10 static void SDMA_StartChannelSoftware (SDMAARM_Type * *base*, uint32_t *channel*) [inline], [static]

This function start a channel.

Parameters

<i>base</i>	SDMA peripheral base address.
<i>channel</i>	SDMA channel number.

21.7.11 static void SDMA_StartChannelEvents (SDMAARM_Type * *base*, uint32_t *channel*) [inline], [static]

This function start a channel.

Parameters

<i>base</i>	SDMA peripheral base address.
<i>channel</i>	SDMA channel number.

21.7.12 `static void SDMA_StopChannel (SDMAARM_Type * base, uint32_t channel) [inline], [static]`

This function stops a channel.

Parameters

<i>base</i>	SDMA peripheral base address.
<i>channel</i>	SDMA channel number.

**21.7.13 void SDMA_SetContextSwitchMode (SDMAARM_Type * *base*,
sdma_context_switch_mode_t *mode*)**

Parameters

<i>base</i>	SDMA peripheral base address.
<i>mode</i>	SDMA context switch mode.

**21.7.14 static uint32_t SDMA_GetChannelInterruptStatus (SDMAARM_Type * *base*
) [inline], [static]**

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

Returns

The interrupt status for all channels. Check the relevant bits for specific channel.

**21.7.15 static void SDMA_ClearChannelInterruptStatus (SDMAARM_Type * *base*,
uint32_t *mask*) [inline], [static]**

Parameters

<i>base</i>	SDMA peripheral base address.
<i>mask</i>	The interrupt status need to be cleared.

**21.7.16 static uint32_t SDMA_GetChannelStopStatus (SDMAARM_Type * *base*)
[inline], [static]**

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

Returns

The stop status for all channels. Check the relevant bits for specific channel.

**21.7.17 static void SDMA_ClearChannelStopStatus (SDMAARM_Type * *base*,
uint32_t *mask*) [inline], [static]**

Parameters

<i>base</i>	SDMA peripheral base address.
<i>mask</i>	The stop status need to be cleared.

**21.7.18 static uint32_t SDMA_GetChannelPendStatus (SDMAARM_Type * *base*)
[inline], [static]**

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

Returns

The pending status for all channels. Check the relevant bits for specific channel.

**21.7.19 static void SDMA_ClearChannelPendStatus (SDMAARM_Type * *base*,
uint32_t *mask*) [inline], [static]**

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

<i>mask</i>	The pending status need to be cleared.
-------------	--

21.7.20 static uint32_t SDMA_GetErrorStatus (SDMAARM_Type * *base*) [inline], [static]

SDMA channel error flag is asserted while an incoming DMA request was detected and it triggers a channel that is already pending or being serviced. This probably means there is an overflow of data for that channel.

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

Returns

The error status for all channels. Check the relevant bits for specific channel.

21.7.21 bool SDMA_GetRequestSourceStatus (SDMAARM_Type * *base*, uint32_t *source*)

Parameters

<i>base</i>	SDMA peripheral base address.
<i>source</i>	DMA request source number.

Returns

True means the request source is pending, otherwise not pending.

21.7.22 void SDMA_CreateHandle (sdma_handle_t * *handle*, SDMAARM_Type * *base*, uint32_t *channel*, sdma_context_data_t * *context*)

This function is called if using the transactional API for SDMA. This function initializes the internal state of the SDMA handle.

Parameters

<i>handle</i>	SDMA handle pointer. The SDMA handle stores callback function and parameters.
<i>base</i>	SDMA peripheral base address.
<i>channel</i>	SDMA channel number.
<i>context</i>	Context structure for the channel to download into SDMA. Users shall make sure the context located in a non-cacheable memory, or it will cause SDMA run fail. Users shall not touch the context contents, it only be filled by SDMA driver in SDMA_SubmitTransfer function.

21.7.23 void SDMA_InstallBDMemory (sdma_handle_t * *handle*, sdma_buffer_descriptor_t * *BDPool*, uint32_t *BDCount*)

This function is called after the SDMA_CreateHandle to use multi-buffer feature.

Parameters

<i>handle</i>	SDMA handle pointer.
<i>BDPool</i>	A memory pool to store BDs. It must be located in non-cacheable address.
<i>BDCount</i>	The number of BD slots.

21.7.24 void SDMA_SetCallback (sdma_handle_t * *handle*, sdma_callback *callback*, void * *userData*)

This callback is called in the SDMA IRQ handler. Use the callback to do something after the current major loop transfer completes.

Parameters

<i>handle</i>	SDMA handle pointer.
<i>callback</i>	SDMA callback function pointer.
<i>userData</i>	A parameter for the callback function.

21.7.25 void SDMA_SetMultiFifoConfig (sdma_transfer_config_t * *config*, uint32_t *fifoNums*, uint32_t *fifoOffset*)

This api is used to support multi fifo for SDMA, if user want to get multi fifo data, then this api should be called before submit transfer.

Parameters

<i>config</i>	transfer configurations.
<i>fifoNums</i>	fifo numbers that multi fifo operation perform, support up to 15 fifo numbers.
<i>fifoOffset</i>	fifoOffset = fifo address offset / sizeof(uint32_t) - 1.

21.7.26 void SDMA_EnableSwDone (SDMAARM_Type * *base*, sdma_transfer_config_t * *config*, uint8_t *sel*, sdma_peripheral_t *type*)

Deprecated Do not use this function. It has been superceded by [SDMA_SetDoneConfig](#).

Parameters

<i>base</i>	SDMA base.
<i>config</i>	transfer configurations.
<i>sel</i>	sw done selector.
<i>type</i>	peripheral type is used to determine the corresponding peripheral sw done selector bit.

21.7.27 void SDMA_SetDoneConfig (SDMAARM_Type * *base*, sdma_transfer_config_t * *config*, sdma_peripheral_t *type*, sdma_done_src_t *doneSrc*)

Parameters

<i>base</i>	SDMA base.
<i>config</i>	transfer configurations.
<i>type</i>	peripheral type.
<i>doneSrc</i>	reference sdma_done_src_t.

21.7.28 void SDMA_LoadScript (SDMAARM_Type * *base*, uint32_t *destAddr*, void * *srcAddr*, size_t *bufferSizeBytes*)

Parameters

<i>base</i>	SDMA base.
<i>destAddr</i>	dest script address, should be SDMA program memory address.
<i>srcAddr</i>	source address of target script.
<i>bufferSizeBytes</i>	bytes size of script.

21.7.29 void SDMA_DumpScript (SDMAARM_Type * *base*, uint32_t *srcAddr*, void * *destAddr*, size_t *bufferSizeBytes*)

Parameters

<i>base</i>	SDMA base.
<i>srcAddr</i>	should be SDMA program memory address.
<i>destAddr</i>	address to store scripts.
<i>bufferSizeBytes</i>	bytes size of script.

21.7.30 void SDMA_PrepareTransfer (sdma_transfer_config_t * *config*, uint32_t *srcAddr*, uint32_t *destAddr*, uint32_t *srcWidth*, uint32_t *destWidth*, uint32_t *bytesEachRequest*, uint32_t *transferSize*, uint32_t *eventSource*, sdma_peripheral_t *peripheral*, sdma_transfer_type_t *type*)

This function prepares the transfer configuration structure according to the user input.

Parameters

<i>config</i>	The user configuration structure of type <code>sdma_transfer_t</code> .
<i>srcAddr</i>	SDMA transfer source address.
<i>destAddr</i>	SDMA transfer destination address.
<i>srcWidth</i>	SDMA transfer source address width(bytes).
<i>destWidth</i>	SDMA transfer destination address width(bytes).
<i>bytesEachRequest</i>	SDMA transfer bytes per channel request.
<i>transferSize</i>	SDMA transfer bytes to be transferred.
<i>eventSource</i>	Event source number for the transfer, if use software trigger, just write 0.
<i>peripheral</i>	Peripheral type, used to decide if need to use some special scripts.
<i>type</i>	SDMA transfer type. Used to decide the correct SDMA script address in SDMA ROM.

Note

The data address and the data width must be consistent. For example, if the SRC is 4 bytes, the source address must be 4 bytes aligned, or it results in source address error.

21.7.31 `void SDMA_PrepareP2PTransfer (sdma_transfer_config_t * config, uint32_t srcAddr, uint32_t destAddr, uint32_t srcWidth, uint32_t destWidth, uint32_t bytesEachRequest, uint32_t transferSize, uint32_t eventSource, uint32_t eventSource1, sdma_peripheral_t peripheral, sdma_p2p_config_t * p2p)`

This function prepares the transfer configuration structure according to the user input.

Parameters

<i>config</i>	The user configuration structure of type <code>sdma_transfer_t</code> .
<i>srcAddr</i>	SDMA transfer source address.
<i>destAddr</i>	SDMA transfer destination address.
<i>srcWidth</i>	SDMA transfer source address width(bytes).
<i>destWidth</i>	SDMA transfer destination address width(bytes).
<i>bytesEachRequest</i>	SDMA transfer bytes per channel request.
<i>transferSize</i>	SDMA transfer bytes to be transferred.
<i>eventSource</i>	Event source number for the transfer.
<i>eventSource1</i>	Event source1 number for the transfer.
<i>peripheral</i>	Peripheral type, used to decide if need to use some special scripts.
<i>p2p</i>	sdma p2p configuration pointer.

Note

The data address and the data width must be consistent. For example, if the SRC is 4 bytes, the source address must be 4 bytes aligned, or it results in source address error.

21.7.32 void SDMA_SubmitTransfer (`sdma_handle_t` * *handle*, const `sdma_transfer_config_t` * *config*)

This function submits the SDMA transfer request according to the transfer configuration structure.

Parameters

<i>handle</i>	SDMA handle pointer.
<i>config</i>	Pointer to SDMA transfer configuration structure.

21.7.33 void SDMA_StartTransfer (`sdma_handle_t` * *handle*)

This function enables the channel request. Users can call this function after submitting the transfer request or before submitting the transfer request.

Parameters

<i>handle</i>	SDMA handle pointer.
---------------	----------------------

21.7.34 void SDMA_StopTransfer (sdma_handle_t * *handle*)

This function disables the channel request to pause the transfer. Users can call [SDMA_StartTransfer\(\)](#) again to resume the transfer.

Parameters

<i>handle</i>	SDMA handle pointer.
---------------	----------------------

21.7.35 void SDMA_AbortTransfer (sdma_handle_t * *handle*)

This function disables the channel request and clear transfer status bits. Users can submit another transfer after calling this API.

Parameters

<i>handle</i>	DMA handle pointer.
---------------	---------------------

21.7.36 uint32_t SDMA_GetTransferredBytes (sdma_handle_t * *handle*)

This function returns the buffer descriptor count value if not using buffer descriptor. While do a simple transfer, which only uses one descriptor, the SDMA driver inside handle the buffer descriptor. In uart receive case, it can tell users how many data already received, also it can tells users how many data transfferd while error occurred. Notice, the count would not change while transfer is on-going using default SDMA script.

Parameters

<i>handle</i>	DMA handle pointer.
---------------	---------------------

Returns

Transferred bytes.

21.7.37 bool SDMA_IsPeripheralInSPBA (uint32_t *addr*)

Parameters

<i>addr</i>	Address which need to judge.
-------------	------------------------------

Return values

<i>True</i>	means located in SPBA, false means not.
-------------	---

21.7.38 void SDMA_HandleIRQ (sdma_handle_t * *handle*)

This function clears the interrupt flags and also handle the CCB for the channel.

Parameters

<i>handle</i>	SDMA handle pointer.
---------------	----------------------

Chapter 22

SEMA4: Hardware Semaphores Driver

22.1 Overview

The MCUXpresso SDK provides a driver for the SEMA4 module of MCUXpresso SDK devices.

Macros

- #define [SEMA4_GATE_NUM_RESET_ALL](#) (64U)
The number to reset all SEMA4 gates.
- #define [SEMA4_GATEn](#)(base, n) (((volatile uint8_t *)(&((base)->Gate00)))[(n)])
SEMA4 gate n register address.

Functions

- void [SEMA4_Init](#) (SEMA4_Type *base)
Initializes the SEMA4 module.
- void [SEMA4_Deinit](#) (SEMA4_Type *base)
De-initializes the SEMA4 module.
- [status_t SEMA4_TryLock](#) (SEMA4_Type *base, uint8_t gateNum, uint8_t procNum)
Tries to lock the SEMA4 gate.
- void [SEMA4_Lock](#) (SEMA4_Type *base, uint8_t gateNum, uint8_t procNum)
Locks the SEMA4 gate.
- static void [SEMA4_Unlock](#) (SEMA4_Type *base, uint8_t gateNum)
Unlocks the SEMA4 gate.
- static int32_t [SEMA4_GetLockProc](#) (SEMA4_Type *base, uint8_t gateNum)
Gets the status of the SEMA4 gate.
- [status_t SEMA4_ResetGate](#) (SEMA4_Type *base, uint8_t gateNum)
Resets the SEMA4 gate to an unlocked status.
- static [status_t SEMA4_ResetAllGates](#) (SEMA4_Type *base)
Resets all SEMA4 gates to an unlocked status.
- static void [SEMA4_EnableGateNotifyInterrupt](#) (SEMA4_Type *base, uint8_t procNum, uint32_t mask)
Enable the gate notification interrupt.
- static void [SEMA4_DisableGateNotifyInterrupt](#) (SEMA4_Type *base, uint8_t procNum, uint32_t mask)
Disable the gate notification interrupt.
- static uint32_t [SEMA4_GetGateNotifyStatus](#) (SEMA4_Type *base, uint8_t procNum)
Get the gate notification flags.
- [status_t SEMA4_ResetGateNotify](#) (SEMA4_Type *base, uint8_t gateNum)
Resets the SEMA4 gate IRQ notification.
- static [status_t SEMA4_ResetAllGateNotify](#) (SEMA4_Type *base)
Resets all SEMA4 gates IRQ notification.

Driver version

- #define **FSL_SEMA4_DRIVER_VERSION** (**MAKE_VERSION**(2, 0, 2))
SEMA4 driver version.

22.2 Macro Definition Documentation

22.2.1 #define SEMA4_GATE_NUM_RESET_ALL (64U)

22.3 Function Documentation

22.3.1 void SEMA4_Init (SEMA4_Type * *base*)

This function initializes the SEMA4 module. It only enables the clock but does not reset the gates because the module might be used by other processors at the same time. To reset the gates, call either SEMA4_ResetGate or SEMA4_ResetAllGates function.

Parameters

<i>base</i>	SEMA4 peripheral base address.
-------------	--------------------------------

22.3.2 void SEMA4_Deinit (SEMA4_Type * *base*)

This function de-initializes the SEMA4 module. It only disables the clock.

Parameters

<i>base</i>	SEMA4 peripheral base address.
-------------	--------------------------------

22.3.3 status_t SEMA4_TryLock (SEMA4_Type * *base*, uint8_t *gateNum*, uint8_t *procNum*)

This function tries to lock the specific SEMA4 gate. If the gate has been locked by another processor, this function returns an error code.

Parameters

<i>base</i>	SEMA4 peripheral base address.
-------------	--------------------------------

<i>gateNum</i>	Gate number to lock.
<i>procNum</i>	Current processor number.

Return values

<i>kStatus_Success</i>	Lock the sema4 gate successfully.
<i>kStatus_Fail</i>	Sema4 gate has been locked by another processor.

22.3.4 void SEMA4_Lock (SEMA4_Type * *base*, uint8_t *gateNum*, uint8_t *procNum*)

This function locks the specific SEMA4 gate. If the gate has been locked by other processors, this function waits until it is unlocked and then lock it.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>gateNum</i>	Gate number to lock.
<i>procNum</i>	Current processor number.

22.3.5 static void SEMA4_Unlock (SEMA4_Type * *base*, uint8_t *gateNum*) [inline], [static]

This function unlocks the specific SEMA4 gate. It only writes unlock value to the SEMA4 gate register. However, it does not check whether the SEMA4 gate is locked by the current processor or not. As a result, if the SEMA4 gate is not locked by the current processor, this function has no effect.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>gateNum</i>	Gate number to unlock.

22.3.6 static int32_t SEMA4_GetLockProc (SEMA4_Type * *base*, uint8_t *gateNum*) [inline], [static]

This function checks the lock status of a specific SEMA4 gate.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>gateNum</i>	Gate number.

Returns

Return -1 if the gate is unlocked, otherwise return the processor number which has locked the gate.

22.3.7 **status_t SEMA4_ResetGate (SEMA4_Type * *base*, uint8_t *gateNum*)**

This function resets a SEMA4 gate to an unlocked status.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>gateNum</i>	Gate number.

Return values

<i>kStatus_Success</i>	SEMA4 gate is reset successfully.
<i>kStatus_Fail</i>	Some other reset process is ongoing.

22.3.8 **static status_t SEMA4_ResetAllGates (SEMA4_Type * *base*) [inline], [static]**

This function resets all SEMA4 gate to an unlocked status.

Parameters

<i>base</i>	SEMA4 peripheral base address.
-------------	--------------------------------

Return values

<i>kStatus_Success</i>	SEMA4 is reset successfully.
------------------------	------------------------------

<i>kStatus_Fail</i>	Some other reset process is ongoing.
---------------------	--------------------------------------

22.3.9 static void SEMA4_EnableGateNotifyInterrupt (SEMA4_Type * *base*, uint8_t *procNum*, uint32_t *mask*) [inline], [static]

Gate notification provides such feature, when core tried to lock the gate and failed, it could get notification when the gate is idle.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>procNum</i>	Current processor number.
<i>mask</i>	OR'ed value of the gate index, for example: (1<<0) (1<<1) means gate 0 and gate 1.

22.3.10 static void SEMA4_DisableGateNotifyInterrupt (SEMA4_Type * *base*, uint8_t *procNum*, uint32_t *mask*) [inline], [static]

Gate notification provides such feature, when core tried to lock the gate and failed, it could get notification when the gate is idle.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>procNum</i>	Current processor number.
<i>mask</i>	OR'ed value of the gate index, for example: (1<<0) (1<<1) means gate 0 and gate 1.

22.3.11 static uint32_t SEMA4_GetGateNotifyStatus (SEMA4_Type * *base*, uint8_t *procNum*) [inline], [static]

Gate notification provides such feature, when core tried to lock the gate and failed, it could get notification when the gate is idle. The status flags are cleared automatically when the gate is locked by current core or locked again before the other core.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>procNum</i>	Current processor number.

Returns

OR'ed value of the gate index, for example: $(1 \ll 0) \mid (1 \ll 1)$ means gate 0 and gate 1 flags are pending.

22.3.12 `status_t SEMA4_ResetGateNotify (SEMA4_Type * base, uint8_t gateNum)`

This function resets a SEMA4 gate IRQ notification.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>gateNum</i>	Gate number.

Return values

<i>kStatus_Success</i>	Reset successfully.
<i>kStatus_Fail</i>	Some other reset process is ongoing.

22.3.13 `static status_t SEMA4_ResetAllGateNotify (SEMA4_Type * base) [inline], [static]`

This function resets all SEMA4 gate IRQ notifications.

Parameters

<i>base</i>	SEMA4 peripheral base address.
-------------	--------------------------------

Return values

<i>kStatus_Success</i>	Reset successfully.
<i>kStatus_Fail</i>	Some other reset process is ongoing.

Chapter 23

TMU: Thermal Management Unit Driver

23.1 Overview

The MCUXpresso SDK provides a peripheral driver for the thermal management unit (TMU) module of MCUXpresso SDK devices.

23.2 Typical use case

23.2.1 Monitor and report Configuration

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/tmu`

Data Structures

- struct `tmu_threshold_config_t`
configuration for TMU threshold. [More...](#)
- struct `tmu_config_t`
Configuration for TMU module. [More...](#)

Macros

- #define `FSL_TMU_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 0)`)
TMU driver version.

Enumerations

- enum {
 `kTMU_ImmediateTemperature0InterruptEnable`,
 `kTMU_AverageTemperature0InterruptEnable`,
 `kTMU_AverageTemperature0CriticalInterruptEnable`,
 `kTMU_ImmediateTemperature1Interrupt1Enable`,
 `kTMU_AverageTemperature1Interrupt1Enable`,
 `kTMU_AverageTemperature1CriticalInterrupt1Enable` }
 TMU interrupt enable, `_tmu_interrupt_enable`.
- enum {
 `kTMU_ImmediateTemperature0InterruptStatusFlags`,
 `kTMU_AverageTemperature0InterruptStatusFlags`,
 `kTMU_AverageTemperature0CriticalInterruptStatusFlags`,
 `kTMU_ImmediateTemperature1Interrupt1StatusFlags`,
 `kTMU_AverageTemperature1Interrupt1StatusFlags`,
 `kTMU_AverageTemperature1CriticalInterrupt1StatusFlags` }
 TMU interrupt enable, `_tmu_interrupt_status_flags`.

- enum `tmu_probe_select_t` {
`kTMU_ProbeSelectMainProbe` = 1U << 0U,
`kTMU_ProbeSelectRemoteProbe` = 1U << 1U,
`kTMU_ProbeSelectBothProbes` = (1U << 0U) | (1U << 1U) }

Probe selection.

- enum `tmu_average_low_pass_filter_t` {
`kTMU_AverageLowPassFilter1_0` = 0U,
`kTMU_AverageLowPassFilter0_5` = 1U,
`kTMU_AverageLowPassFilter0_25` = 2U,
`kTMU_AverageLowPassFilter0_125` = 3U }

Average low pass filter setting.

Functions

- void `TMU_Init` (TMU_Type *base, const `tmu_config_t` *config)
Enable the access to TMU registers and Initialize TMU module.
- void `TMU_Deinit` (TMU_Type *base)
De-initialize TMU module and Disable the access to DCDC registers.
- void `TMU_Enable` (TMU_Type *base, bool enable)
Enable/disable TMU module.
- void `TMU_GetDefaultConfig` (`tmu_config_t` *config)
Gets the default configuration for TMU.
- static void `TMU_EnableInterrupts` (TMU_Type *base, uint32_t mask)
Enable the TMU interrupts.
- static void `TMU_DisableInterrupts` (TMU_Type *base, uint32_t mask)
Disable the TMU interrupts.
- static uint32_t `TMU_GetInterruptStatusFlags` (TMU_Type *base)
Get interrupt status flags.
- static void `TMU_ClearInterruptStatusFlags` (TMU_Type *base, uint32_t mask)
Clear interrupt status flags.
- `status_t` `TMU_GetImmediateTemperature` (TMU_Type *base, `tmu_probe_select_t` probe, int8_t *temperature)
Get the last immediate temperature at site.
- `status_t` `TMU_GetAverageTemperature` (TMU_Type *base, `tmu_probe_select_t` probe, int8_t *temperature)
Get the last average temperature at site.
- void `TMU_UpdateHighTemperatureThreshold` (TMU_Type *base, `tmu_probe_select_t` probe, const `tmu_threshold_config_t` *thresholdConfig)
Update the high temperature threshold value.

23.3 Data Structure Documentation

23.3.1 struct `tmu_threshold_config_t`

Data Fields

- bool `immediateThresholdEnable`
Enable high temperature immediate threshold.
- bool `AverageThresholdEnable`

- *Enable high temperature average threshold.*
bool [AverageCriticalThresholdEnable](#)
- *Enable high temperature average critical threshold.*
uint8_t [immediateThresholdValueOfMainProbe](#)
Range:-40~125.
- uint8_t [averageThresholdValueOfMainProbe](#)
Range:-40~125.
- uint8_t [averageCriticalThresholdValueOfMainProbe](#)
Range:-40~125.
- uint8_t [immediateThresholdValueOfRemoteProbe](#)
Range:-40~125.
- uint8_t [averageThresholdValueOfRemoteProbe](#)
Range:-40~125.
- uint8_t [averageCriticalThresholdValueOfRemoteProbe](#)
Range:-40~125.

Field Documentation

- (1) **bool tmu_threshold_config_t::immediateThresholdEnable**
- (2) **bool tmu_threshold_config_t::AverageThresholdEnable**
- (3) **bool tmu_threshold_config_t::AverageCriticalThresholdEnable**
- (4) **uint8_t tmu_threshold_config_t::immediateThresholdValueOfMainProbe**

Valid when corresponding threshold is enabled. High temperature immediate threshold value of main probe. Besides, bit-8 is sign bit: 1 means negative and 0 means positive.

- (5) **uint8_t tmu_threshold_config_t::averageThresholdValueOfMainProbe**

Valid when corresponding threshold is enabled. High temperature average threshold value of main probe. Besides, bit-8 is sign bit: 1 means negative and 0 means positive.

- (6) **uint8_t tmu_threshold_config_t::averageCriticalThresholdValueOfMainProbe**

Valid when corresponding threshold is enabled. High temperature average critical threshold value of main probe. Besides, bit-8 is sign bit: 1 means negative and 0 means positive.

- (7) **uint8_t tmu_threshold_config_t::immediateThresholdValueOfRemoteProbe**

Valid when corresponding threshold is enabled. High temperature immediate threshold value of remote probe. Besides, bit-8 is sign bit: 1 means negative and 0 means positive.

- (8) **uint8_t tmu_threshold_config_t::averageThresholdValueOfRemoteProbe**

Valid when corresponding threshold is enabled. High temperature average threshold value of remote probe. Besides, bit-8 is sign bit: 1 means negative and 0 means positive.

(9) uint8_t tmu_threshold_config_t::averageCriticalThresholdValueOfRemoteProbe

Valid when corresponding threshold is enabled. High temperature average critical threshold value of remote probe. Besides, bit-8 is sign bit: 1 means negative and 0 means positive.

23.3.2 struct tmu_config_t

Data Fields

- [tmu_probe_select_t probeSelect](#)
The temperature monitor probe select.
- [tmu_average_low_pass_filter_t averageLPF](#)
The average temperature is calculated as: $ALPF \times Current_Temp + (1 - ALPF) \times Average_Temp$.
- [tmu_threshold_config_t thresholdConfig](#)
The high temperature threshold configuration.

Field Documentation

(1) tmu_probe_select_t tmu_config_t::probeSelect

(2) tmu_average_low_pass_filter_t tmu_config_t::averageLPF

For proper operation, this field should only change when monitoring is disabled.

(3) tmu_threshold_config_t tmu_config_t::thresholdConfig

23.4 Macro Definition Documentation

23.4.1 #define FSL_TMU_DRIVER_VERSION (MAKE_VERSION(2, 0, 0))

Version 2.0.0.

23.5 Enumeration Type Documentation

23.5.1 anonymous enum

Enumerator

- kTMU_ImmediateTemperature0InterruptEnable** Immediate temperature threshold exceeded interrupt enable of probe0.
- kTMU_AverageTemperature0InterruptEnable** Average temperature threshold exceeded interrupt enable of probe0.
- kTMU_AverageTemperature0CriticalInterruptEnable** Average temperature critical threshold exceeded interrupt enable of probe0.
- kTMU_ImmediateTemperature1Interrupt1Enable** Immediate temperature threshold exceeded interrupt enable of probe1.

kTMU_AverageTemperature1Interrupt1Enable Average temperature threshold exceeded interrupt enable of probe1.

kTMU_AverageTemperature1CriticalInterrupt1Enable Average temperature critical threshold exceeded interrupt enable of probe1.

23.5.2 anonymous enum

Enumerator

kTMU_ImmediateTemperature0InterruptStausFlags Immediate temperature threshold exceeded interrupt status of probe0.

kTMU_AverageTemperature0InterruptStausFlags Average temperature threshold exceeded interrupt status of probe0.

kTMU_AverageTemperature0CriticalInterruptStausFlags Average temperature critical threshold exceeded interrupt status of probe0.

kTMU_ImmediateTemperature1Interrupt1StausFlags Immediate temperature threshold exceeded interrupt status of probe1.

kTMU_AverageTemperature1Interrupt1StausFlags Average temperature threshold exceeded interrupt status of probe1.

kTMU_AverageTemperature1CriticalInterrupt1StausFlags Average temperature critical threshold exceeded interrupt status of probe1.

23.5.3 enum tmu_probe_select_t

Enumerator

kTMU_ProbeSelectMainProbe Select the main probe only.

kTMU_ProbeSelectRemoteProbe Select the remote probe(near A53) only.

kTMU_ProbeSelectBothProbes Select both 2 probes.

23.5.4 enum tmu_average_low_pass_filter_t

Enumerator

kTMU_AverageLowPassFilter1_0 Average low pass filter = 1.

kTMU_AverageLowPassFilter0_5 Average low pass filter = 0.5.

kTMU_AverageLowPassFilter0_25 Average low pass filter = 0.25.

kTMU_AverageLowPassFilter0_125 Average low pass filter = 0.125.

23.6 Function Documentation

23.6.1 void TMU_Init (TMU_Type * *base*, const tmu_config_t * *config*)

Parameters

<i>base</i>	TMU peripheral base address.
<i>config</i>	Pointer to configuration structure. Refer to "tmu_config_t" structure.

23.6.2 void TMU_Deinit (TMU_Type * *base*)

Parameters

<i>base</i>	TMU peripheral base address.
-------------	------------------------------

23.6.3 void TMU_Enable (TMU_Type * *base*, bool *enable*)

Parameters

<i>base</i>	TMU peripheral base address.
<i>enable</i>	enable or disable TMU.

23.6.4 void TMU_GetDefaultConfig (tmu_config_t * *config*)

This function initializes the user configuration structure to default value. The default value are:

Example:

```

config.averageLPF          =
    kTMU_AverageLowPassFilter0_5;
config.probeSelect         =
    kTMU_ProbeSelectMainProbe;
config.thresholdConfig.immediateThresholdEnable = false;
config.thresholdConfig.immediateThresholdValue = DEMO_TMU_IMMEDIATE_THRESHOLD;
config.thresholdConfig.AverageThresholdEnable  = true;
config.thresholdConfig.averageThresholdValue   = DEMO_TMU_AVERAGE_THRESHOLD;
config.thresholdConfig.AverageCriticalThresholdEnable = false;
config.thresholdConfig.averageCriticalThresholdValue = DEMO_TMU_AVERAGE_CRITICAL_THRESHOLD;

```

Parameters

<i>config</i>	Pointer to TMU configuration structure.
---------------	---

23.6.5 static void TMU_EnableInterrupts (TMU_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	TMU peripheral base address.
<i>mask</i>	The interrupt mask. Refer to "_tmu_interrupt_enable" enumeration.

23.6.6 static void TMU_DisableInterrupts (TMU_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	TMU peripheral base address.
<i>mask</i>	The interrupt mask. Refer to "_tmu_interrupt_enable" enumeration.

23.6.7 static uint32_t TMU_GetInterruptStatusFlags (TMU_Type * *base*) [inline], [static]

Parameters

<i>base</i>	TMU peripheral base address.
-------------	------------------------------

Return values

<i>The</i>	current interrupt status.
------------	---------------------------

23.6.8 static void TMU_ClearInterruptStatusFlags (TMU_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	TMU peripheral base address.
<i>mask</i>	The mask of interrupt status flags. Refer to "_tmu_interrupt_status_flags" enumeration.

23.6.9 status_t TMU_GetImmediateTemperature (TMU_Type * *base*, tmu_probe_select_t *probe*, int8_t * *temperature*)

Parameters

<i>base</i>	TMU peripheral base address.
<i>probe</i>	probe selection, if select both 2 probes, return main probe temeperature by default. Refer to "tmu_probe_select_t" structure.
<i>temperature</i>	Last immediate temperature reading at site when V=1. besides, Bit-8 is sign bit: 1 means nagetive and 0 means positive.

Return values

<i>get</i>	immediate temperature status.
------------	-------------------------------

23.6.10 status_t TMU_GetAverageTemperature (TMU_Type * *base*, tmu_probe_select_t *probe*, int8_t * *temperature*)

Parameters

<i>base</i>	TMU peripheral base address.
<i>probe</i>	probe selection, if select both 2 probes, return main probe temeperature by default. Refer to "tmu_probe_select_t" structure.
<i>temperature</i>	Last average temperature reading at site; besides, Bit-8 is sign bit: 1 means nagetive and 0 means positive.

Return values

<i>get</i>	average temperature status.
------------	-----------------------------

**23.6.11 void TMU_UpdateHighTemperatureThreshold (TMU_Type *
base, tmu_probe_select_t *probe*, const tmu_threshold_config_t *
thresholdConfig)**

Parameters

<i>base</i>	TMU peripheral base address.
<i>probe</i>	probe selection, if select both 2 probes, set main probe path by default. Refer to "tmu_probe_select_t" structure.
<i>threshold-Config</i>	threshold configuration. Refer to "tmu_threshold_config_t" structure.

Chapter 24

WDOG: Watchdog Timer Driver

24.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Watchdog module (WDOG) of MCUXpresso SDK devices.

24.2 Typical use case

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/wdog

Data Structures

- struct [wdog_work_mode_t](#)
Defines WDOG work mode. [More...](#)
- struct [wdog_config_t](#)
Describes WDOG configuration structure. [More...](#)

Enumerations

- enum [_wdog_interrupt_enable](#) { [kWDOG_InterruptEnable](#) = WDOG_WICR_WIE_MASK }
- enum [_wdog_status_flags](#) {
[kWDOG_RunningFlag](#) = WDOG_WCR_WDE_MASK,
[kWDOG_PowerOnResetFlag](#) = WDOG_WRSR_POR_MASK,
[kWDOG_TimeoutResetFlag](#) = WDOG_WRSR_TOUT_MASK,
[kWDOG_SoftwareResetFlag](#) = WDOG_WRSR_SFTW_MASK,
[kWDOG_InterruptFlag](#) = WDOG_WICR_WTIS_MASK }
- WDOG status flags.*

Driver version

- #define [FSL_WDOG_DRIVER_VERSION](#) ([MAKE_VERSION](#)(2, 1, 1))
Defines WDOG driver version.

Refresh sequence

- #define [WDOG_REFRESH_KEY](#) (0xAAAA5555U)

WDOG Initialization and De-initialization.

- void [WDOG_GetDefaultConfig](#) ([wdog_config_t](#) *config)
Initializes the WDOG configuration structure.
- void [WDOG_Init](#) (WDOG_Type *base, const [wdog_config_t](#) *config)

- *Initializes the WDOG.*
- void [WDOG_Deinit](#) (WDOG_Type *base)
- *Shuts down the WDOG.*
- static void [WDOG_Enable](#) (WDOG_Type *base)
- *Enables the WDOG module.*
- static void [WDOG_Disable](#) (WDOG_Type *base)
- *Disables the WDOG module.*
- static void [WDOG_TriggerSystemSoftwareReset](#) (WDOG_Type *base)
- *Trigger the system software reset.*
- static void [WDOG_TriggerSoftwareSignal](#) (WDOG_Type *base)
- *Trigger an output assertion.*
- static void [WDOG_EnableInterrupts](#) (WDOG_Type *base, uint16_t mask)
- *Enables the WDOG interrupt.*
- uint16_t [WDOG_GetStatusFlags](#) (WDOG_Type *base)
- *Gets the WDOG all reset status flags.*
- void [WDOG_ClearInterruptStatus](#) (WDOG_Type *base, uint16_t mask)
- *Clears the WDOG flag.*
- static void [WDOG_SetTimeoutValue](#) (WDOG_Type *base, uint16_t timeoutCount)
- *Sets the WDOG timeout value.*
- static void [WDOG_SetInterruptTimeoutValue](#) (WDOG_Type *base, uint16_t timeoutCount)
- *Sets the WDOG interrupt count timeout value.*
- static void [WDOG_DisablePowerDownEnable](#) (WDOG_Type *base)
- *Disable the WDOG power down enable bit.*
- void [WDOG_Refresh](#) (WDOG_Type *base)
- *Refreshes the WDOG timer.*

24.3 Data Structure Documentation

24.3.1 struct wdog_work_mode_t

Data Fields

- bool [enableWait](#)
continue or suspend WDOG in wait mode
- bool [enableStop](#)
continue or suspend WDOG in stop mode
- bool [enableDebug](#)
continue or suspend WDOG in debug mode

24.3.2 struct wdog_config_t

Data Fields

- bool [enableWdog](#)
Enables or disables WDOG.
- [wdog_work_mode_t](#) [workMode](#)
Configures WDOG work mode in debug stop and wait mode.
- bool [enableInterrupt](#)

- *Enables or disables WDOG interrupt.*
uint16_t `timeoutValue`
Timeout value.
- uint16_t `interruptTimeValue`
Interrupt count timeout value.
- bool `softwareResetExtension`
software reset extension
- bool `enablePowerDown`
power down enable bit
- bool `enableTimeOutAssert`
Enable WDOG_B timeout assertion.

Field Documentation

(1) bool `wdog_config_t::enableTimeOutAssert`

24.4 Enumeration Type Documentation

24.4.1 enum `_wdog_interrupt_enable`

This structure contains the settings for all of the WDOG interrupt configurations.

Enumerator

kWDOG_InterruptEnable WDOG timeout generates an interrupt before reset.

24.4.2 enum `_wdog_status_flags`

This structure contains the WDOG status flags for use in the WDOG functions.

Enumerator

kWDOG_RunningFlag Running flag, set when WDOG is enabled.

kWDOG_PowerOnResetFlag Power On flag, set when reset is the result of a powerOnReset.

kWDOG_TimeoutResetFlag Timeout flag, set when reset is the result of a timeout.

kWDOG_SoftwareResetFlag Software flag, set when reset is the result of a software.

kWDOG_InterruptFlag interrupt flag, whether interrupt has occurred or not

24.5 Function Documentation

24.5.1 void `WDOG_GetDefaultConfig (wdog_config_t * config)`

This function initializes the WDOG configuration structure to default values. The default values are as follows.

```
* wdogConfig->enableWdog = true;
* wdogConfig->workMode.enableWait = true;
* wdogConfig->workMode.enableStop = false;
```

```

* wdogConfig->workMode.enableDebug = false;
* wdogConfig->enableInterrupt = false;
* wdogConfig->enablePowerdown = false;
* wdogConfig->resetExtension = false;
* wdogConfig->timeoutValue = 0xFFU;
* wdogConfig->interruptTimeValue = 0x04u;
*

```

Parameters

<i>config</i>	Pointer to the WDOG configuration structure.
---------------	--

See Also

[wdog_config_t](#)

24.5.2 void WDOG_Init (WDOG_Type * *base*, const wdog_config_t * *config*)

This function initializes the WDOG. When called, the WDOG runs according to the configuration.

This is an example.

```

* wdog_config_t config;
* WDOG_GetDefaultConfig(&config);
* config.timeoutValue = 0xffU;
* config->interruptTimeValue = 0x04u;
* WDOG_Init(wdog_base, &config);
*

```

Parameters

<i>base</i>	WDOG peripheral base address
<i>config</i>	The configuration of WDOG

24.5.3 void WDOG_Deinit (WDOG_Type * *base*)

This function shuts down the WDOG. Watchdog Enable bit is a write one once only bit. It is not possible to clear this bit by a software write, once the bit is set. This bit(WDE) can be set/reset only in debug mode(exception).

24.5.4 static void WDOG_Enable (WDOG_Type * *base*) [inline], [static]

This function writes a value into the WDOG_WCR register to enable the WDOG. This is a write one once only bit. It is not possible to clear this bit by a software write, once the bit is set. only debug mode exception.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

24.5.5 static void WDOG_Disable (WDOG_Type * *base*) [inline], [static]

This function writes a value into the WDOG_WCR register to disable the WDOG. This is a write one once only bit. It is not possible to clear this bit by a software write, once the bit is set. only debug mode exception

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

24.5.6 static void WDOG_TriggerSystemSoftwareReset (WDOG_Type * *base*) [inline], [static]

This function will write to the WCR[SRS] bit to trigger a software system reset. This bit will automatically resets to "1" after it has been asserted to "0". Note: Calling this API will reset the system right now, please using it with more attention.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

24.5.7 static void WDOG_TriggerSoftwareSignal (WDOG_Type * *base*) [inline], [static]

This function will write to the WCR[WDA] bit to trigger WDOG_B signal assertion. The WDOG_B signal can be routed to external pin of the chip, the output pin will turn to assertion along with WDOG_B signal. Note: The WDOG_B signal will remain assert until a power on reset occurred, so, please take more attention while calling it.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

24.5.8 static void WDOG_EnableInterrupts (WDOG_Type * *base*, uint16_t *mask*) [inline], [static]

This bit is a write once only bit. Once the software does a write access to this bit, it will get locked and cannot be reprogrammed until the next system reset assertion

Parameters

<i>base</i>	WDOG peripheral base address
<i>mask</i>	The interrupts to enable The parameter can be combination of the following source if defined. <ul style="list-style-type: none"> • kWDOG_InterruptEnable

24.5.9 uint16_t WDOG_GetStatusFlags (WDOG_Type * *base*)

This function gets all reset status flags.

```
* uint16_t status;
* status = WDOG_GetStatusFlags (wdog_base);
*
```

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

Returns

State of the status flag: asserted (true) or not-asserted (false).

See Also

[_wdog_status_flags](#)

- true: a related status flag has been set.
- false: a related status flag is not set.

24.5.10 void WDOG_ClearInterruptStatus (WDOG_Type * *base*, uint16_t *mask*)

This function clears the WDOG status flag.

This is an example for clearing the interrupt flag.

```
* WDOG_ClearStatusFlags (wdog_base, kWDOG_InterruptFlag);
*
```

Parameters

<i>base</i>	WDOG peripheral base address
<i>mask</i>	The status flags to clear. The parameter could be any combination of the following values. kWDOG_TimeoutFlag

24.5.11 static void WDOG_SetTimeoutValue (WDOG_Type * *base*, uint16_t *timeoutCount*) [inline], [static]

This function sets the timeout value. This function writes a value into WCR registers. The time-out value can be written at any point of time but it is loaded to the counter at the time when WDOG is enabled or after the service routine has been performed.

Parameters

<i>base</i>	WDOG peripheral base address
<i>timeoutCount</i>	WDOG timeout value; count of WDOG clock tick.

24.5.12 static void WDOG_SetInterruptTimeoutValue (WDOG_Type * *base*, uint16_t *timeoutCount*) [inline], [static]

This function sets the interrupt count timeout value. This function writes a value into WIC registers which are write-once. This field is write once only. Once the software does a write access to this field, it will get locked and cannot be reprogrammed until the next system reset assertion.

Parameters

<i>base</i>	WDOG peripheral base address
<i>timeoutCount</i>	WDOG timeout value; count of WDOG clock tick.

24.5.13 static void WDOG_DisablePowerDownEnable (WDOG_Type * *base*) [inline], [static]

This function disable the WDOG power down enable(PDE). This function writes a value into WMCR registers which are write-once. This field is write once only. Once software sets this bit it cannot be reset until the next system reset.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

24.5.14 void WDOG_Refresh (WDOG_Type * *base*)

This function feeds the WDOG. This function should be called before the WDOG timer is in timeout. Otherwise, a reset is asserted.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

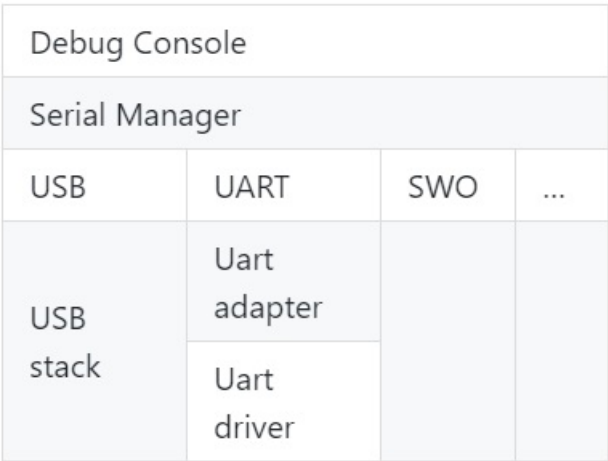
Chapter 25

Debug Console

25.1 Overview

This chapter describes the programming interface of the debug console driver.

The debug console enables debug log messages to be output via the specified peripheral with frequency of the peripheral source clock and base address at the specified baud rate. Additionally, it provides input and output functions to scan and print formatted data. The below picture shows the layout of debug console.



Debug console overview

25.2 Function groups

25.2.1 Initialization

To initialize the debug console, call the [DbgConsole_Init\(\)](#) function with these parameters. This function automatically enables the module and the clock.

```
status_t DbgConsole_Init(uint8_t instance, uint32_t baudRate,
    serial_port_type_t device, uint32_t clkSrcFreq);
```

Select the supported debug console hardware device type, such as

```
typedef enum _serial_port_type
{
    kSerialPort_Uart = 1U,
    kSerialPort_UsbCdc,
    kSerialPort_Swo,
} serial_port_type_t;
```

After the initialization is successful, stdout and stdin are connected to the selected peripheral.

This example shows how to call the `DbgConsole_Init()` given the user configuration structure.

```
DbgConsole_Init(BOARD_DEBUG_UART_INSTANCE, BOARD_DEBUG_UART_BAUDRATE, BOARD_DEBUG_UART_TYPE,
                BOARD_DEBUG_UART_CLK_FREQ);
```

25.2.2 Advanced Feature

The debug console provides input and output functions to scan and print formatted data.

- Support a format specifier for PRINTF following this prototype "`%[flags][width][.precision][length]specifier`", which is explained below

flags	Description
-	Left-justified within the given field width. Right-justified is the default.
+	Forces to precede the result with a plus or minus sign (+ or -) even for positive numbers. By default, only negative numbers are preceded with a - sign.
(space)	If no sign is written, a blank space is inserted before the value.
#	Used with o, x, or X specifiers the value is preceded with 0, 0x, or 0X respectively for values other than zero. Used with e, E and f, it forces the written output to contain a decimal point even if no digits would follow. By default, if no digits follow, no decimal point is written. Used with g or G the result is the same as with e or E but trailing zeros are not removed.
0	Left-pads the number with zeroes (0) instead of spaces, where padding is specified (see width sub-specifier).

Width	Description
(number)	A minimum number of characters to be printed. If the value to be printed is shorter than this number, the result is padded with blank spaces. The value is not truncated even if the result is larger.
*	The width is not specified in the format string, but as an additional integer value argument preceding the argument that has to be formatted.

.precision	Description
.number	For integer specifiers (d, i, o, u, x, X) precision specifies the minimum number of digits to be written. If the value to be written is shorter than this number, the result is padded with leading zeros. The value is not truncated even if the result is longer. A precision of 0 means that no character is written for the value 0. For e, E, and f specifiers this is the number of digits to be printed after the decimal point. For g and G specifiers This is the maximum number of significant digits to be printed. For s this is the maximum number of characters to be printed. By default, all characters are printed until the ending null character is encountered. For c type it has no effect. When no precision is specified, the default is 1. If the period is specified without an explicit value for precision, 0 is assumed.
.*	The precision is not specified in the format string, but as an additional integer value argument preceding the argument that has to be formatted.

length	Description
Do not support	

specifier	Description
d or i	Signed decimal integer
f	Decimal floating point
F	Decimal floating point capital letters
x	Unsigned hexadecimal integer
X	Unsigned hexadecimal integer capital letters
o	Signed octal
b	Binary value
p	Pointer address
u	Unsigned decimal integer
c	Character
s	String of characters
n	Nothing printed

- Support a format specifier for SCANF following this prototype " %[*][width][length]specifier", which is explained below

*	Description
	An optional starting asterisk indicates that the data is to be read from the stream but ignored. In other words, it is not stored in the corresponding argument.

width	Description
	This specifies the maximum number of characters to be read in the current reading operation.

length	Description
hh	The argument is interpreted as a signed character or unsigned character (only applies to integer specifiers: i, d, o, u, x, and X).
h	The argument is interpreted as a short integer or unsigned short integer (only applies to integer specifiers: i, d, o, u, x, and X).
l	The argument is interpreted as a long integer or unsigned long integer for integer specifiers (i, d, o, u, x, and X) and as a wide character or wide character string for specifiers c and s.
ll	The argument is interpreted as a long long integer or unsigned long long integer for integer specifiers (i, d, o, u, x, and X) and as a wide character or wide character string for specifiers c and s.
L	The argument is interpreted as a long double (only applies to floating point specifiers: e, E, f, g, and G).
j or z or t	Not supported

specifier	Qualifying Input	Type of argument
c	Single character: Reads the next character. If a width different from 1 is specified, the function reads width characters and stores them in the successive locations of the array passed as argument. No null character is appended at the end.	char *
i	Integer: : Number optionally preceded with a + or - sign	int *
d	Decimal integer: Number optionally preceded with a + or - sign	int *
a, A, e, E, f, F, g, G	Floating point: Decimal number containing a decimal point, optionally preceded by a + or - sign and optionally followed by the e or E character and a decimal number. Two examples of valid entries are -732.103 and 7.12e4	float *
o	Octal Integer:	int *
s	String of characters. This reads subsequent characters until a white space is found (white space characters are considered to be blank, newline, and tab).	char *
u	Unsigned decimal integer.	unsigned int *

The debug console has its own printf/scanf/putchar/getchar functions which are defined in the header file.

```
int DbgConsole_Printf(const char *fmt_s, ...);
int DbgConsole_Putchar(int ch);
int DbgConsole_Scanf(char *fmt_ptr, ...);
int DbgConsole_Getchar(void);
```

This utility supports selecting toolchain's printf/scanf or the MCUXpresso SDK printf/scanf.

```
#if SDK_DEBUGCONSOLE == DEBUGCONSOLE_DISABLE /* Disable debug console */
#define PRINTF
#define SCANF
#define PUTCHAR
#define GETCHAR
#elif SDK_DEBUGCONSOLE == DEBUGCONSOLE_REDIRECT_TO_SDK /* Select printf, scanf, putchar, getchar of SDK
```

```

        version. */
#define PRINTF DbgConsole_Printf
#define SCANF DbgConsole_Scanf
#define PUTCHAR DbgConsole_Putchar
#define GETCHAR DbgConsole_Getchar
#elif SDK_DEBUGCONSOLE == DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN /* Select printf, scanf, putchar, getchar of
        toolchain. */
#define PRINTF printf
#define SCANF scanf
#define PUTCHAR putchar
#define GETCHAR getchar
#endif /* SDK_DEBUGCONSOLE */

```

25.2.3 SDK_DEBUGCONSOLE and SDK_DEBUGCONSOLE_UART

There are two macros `SDK_DEBUGCONSOLE` and `SDK_DEBUGCONSOLE_UART` added to configure `PRINTF` and low level output peripheral.

- The macro `SDK_DEBUGCONSOLE` is used for frontend. Whether debug console redirect to toolchain or SDK or disabled, it decides which is the frontend of the debug console, Tool chain or SDK. The function can be set by the macro `SDK_DEBUGCONSOLE`.
- The macro `SDK_DEBUGCONSOLE_UART` is used for backend. It is used to decide whether provide low level IO implementation to toolchain `printf` and `scanf`. For example, within MCUXpresso, if the macro `SDK_DEBUGCONSOLE_UART` is defined, `__sys_write` and `__sys_readc` will be used when `__REDLIB__` is defined; `_write` and `_read` will be used in other cases. The macro does not specifically refer to the peripheral "UART". It refers to the external peripheral similar to UART, like as USB CDC, UART, SWO, etc. So if the macro `SDK_DEBUGCONSOLE_UART` is not defined when tool-chain `printf` is calling, the semihosting will be used.

The following matrix shows the effects of `SDK_DEBUGCONSOLE` and `SDK_DEBUGCONSOLE_UART` on `PRINTF` and `printf`. The green mark is the default setting of the debug console.

SDK_DEBUGCONSOLE	SDK_DEBUGCONSOLE_UART	PRINTF	printf
DEBUGCONSOLE_- REDIRECT_TO_SDK	defined	Low level peripheral*	Low level peripheral
DEBUGCONSOLE_- REDIRECT_TO_SDK	undefined	Low level peripheral*	semihost
DEBUGCONSOLE_- REDIRECT_TO_TO- OLCHAIN	defined	Low level peripheral*	Low level peripheral
DEBUGCONSOLE_- REDIRECT_TO_TO- OLCHAIN	undefined	semihost	semihost
DEBUGCONSOLE_- DISABLE	defined	No output	Low level peripheral
DEBUGCONSOLE_- DISABLE	undefined	No output	semihost

* the **low level peripheral** could be USB CDC, UART, or SWO, and so on.

25.3 Typical use case

Some examples use the **PUTCHAR & GETCHAR** function

```
ch = GETCHAR();
PUTCHAR(ch);
```

Some examples use the **PRINTF** function

Statement prints the string format.

```
PRINTF("%s %s\r\n", "Hello", "world!");
```

Statement prints the hexadecimal format/

```
PRINTF("0x%02X hexadecimal number equivalents 255", 255);
```

Statement prints the decimal floating point and unsigned decimal.

```
PRINTF("Execution timer: %s\n\rTime: %u ticks %2.5f milliseconds\n\rDONE\n\r", "1 day", 86400, 86.4);
```

Some examples use the **SCANF** function

```
PRINTF("Enter a decimal number: ");
SCANF("%d", &i);
PRINTF("\r\nYou have entered %d.\r\n", i, i);
PRINTF("Enter a hexadecimal number: ");
SCANF("%x", &i);
PRINTF("\r\nYou have entered 0x%X (%d).\r\n", i, i);
```

Print out failure messages using MCUXpresso SDK **__assert_func**:

```
void __assert_func(const char *file, int line, const char *func, const char *failedExpr)
{
    PRINTF("ASSERT ERROR \\" %s \": file \"%s\" Line \"%d\" function name \"%s\" \n", failedExpr, file
    , line, func);
    for (;;)
    {}
}
```

Note:

To use 'printf' and 'scanf' for GNUC Base, add file 'fsl_sbrk.c' in path: `..\{package}\devices\{subset}\utilities\fsl-
_sbrk.c` to your project.

Modules

- [SWO](#)
- [Semihosting](#)

Macros

- #define [DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN](#) 0U
Definition select redirect toolchain printf, scanf to uart or not.
- #define [DEBUGCONSOLE_REDIRECT_TO_SDK](#) 1U
Select SDK version printf, scanf.
- #define [DEBUGCONSOLE_DISABLE](#) 2U
Disable debugconsole function.
- #define [SDK_DEBUGCONSOLE](#) [DEBUGCONSOLE_REDIRECT_TO_SDK](#)
Definition to select sdk or toolchain printf, scanf.
- #define [PRINTF](#) [DbgConsole_Printf](#)
Definition to select redirect toolchain printf, scanf to uart or not.

Typedefs

- typedef void(* [printfCb](#))(char *buf, int32_t *indicator, char val, int len)
A function pointer which is used when format printf log.

Functions

- int [StrFormatPrintf](#) (const char *fmt, va_list ap, char *buf, [printfCb](#) cb)
This function outputs its parameters according to a formatted string.
- int [StrFormatScanf](#) (const char *line_ptr, char *format, va_list args_ptr)
Converts an input line of ASCII characters based upon a provided string format.

Variables

- [serial_handle_t](#) [g_serialHandle](#)
serial manager handle

Initialization

- [status_t](#) [DbgConsole_Init](#) (uint8_t instance, uint32_t baudRate, [serial_port_type_t](#) device, uint32_t clkSrcFreq)
Initializes the peripheral used for debug messages.
- [status_t](#) [DbgConsole_Deinit](#) (void)
De-initializes the peripheral used for debug messages.
- [status_t](#) [DbgConsole_EnterLowpower](#) (void)
Prepares to enter low power consumption.
- [status_t](#) [DbgConsole_ExitLowpower](#) (void)
Restores from low power consumption.
- int [DbgConsole_Printf](#) (const char *fmt_s,...)
Writes formatted output to the standard output stream.
- int [DbgConsole_Vprintf](#) (const char *fmt_s, va_list formatStringArg)
Writes formatted output to the standard output stream.
- int [DbgConsole_Putchar](#) (int ch)

- *Writes a character to stdout.*
- int [DbgConsole_Scanf](#) (char *fmt_s,...)
Reads formatted data from the standard input stream.
- int [DbgConsole_Getchar](#) (void)
Reads a character from standard input.
- int [DbgConsole_BlockingPrintf](#) (const char *fmt_s,...)
Writes formatted output to the standard output stream with the blocking mode.
- int [DbgConsole_BlockingVprintf](#) (const char *fmt_s, va_list formatStringArg)
Writes formatted output to the standard output stream with the blocking mode.
- [status_t DbgConsole_Flush](#) (void)
Debug console flush.

25.4 Macro Definition Documentation

25.4.1 #define DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN 0U

Select toolchain printf and scanf.

25.4.2 #define DEBUGCONSOLE_REDIRECT_TO_SDK 1U

25.4.3 #define DEBUGCONSOLE_DISABLE 2U

25.4.4 #define SDK_DEBUGCONSOLE DEBUGCONSOLE_REDIRECT_TO_SDK

The macro only support to be redefined in project setting.

25.4.5 #define PRINTF DbgConsole_Printf

if SDK_DEBUGCONSOLE defined to 0,it represents select toolchain printf, scanf. if SDK_DEBUGCONSOLE defined to 1,it represents select SDK version printf, scanf. if SDK_DEBUGCONSOLE defined to 2,it represents disable debugconsole function.

25.5 Function Documentation

25.5.1 status_t DbgConsole_Init (uint8_t instance, uint32_t baudRate, serial_port_type_t device, uint32_t clkSrcFreq)

Call this function to enable debug log messages to be output via the specified peripheral initialized by the serial manager module. After this function has returned, stdout and stdin are connected to the selected peripheral.

Parameters

<i>instance</i>	The instance of the module.If the device is kSerialPort_Uart, the instance is UART peripheral instance. The UART hardware peripheral type is determined by UART adapter. For example, if the instance is 1, if the lpuart_adapter.c is added to the current project, the UART peripheral is LPUART1. If the uart_adapter.c is added to the current project, the UART peripheral is UART1.
<i>baudRate</i>	The desired baud rate in bits per second.
<i>device</i>	Low level device type for the debug console, can be one of the following. <ul style="list-style-type: none"> • kSerialPort_Uart, • kSerialPort_UsbCdc
<i>clkSrcFreq</i>	Frequency of peripheral source clock.

Returns

Indicates whether initialization was successful or not.

Return values

<i>kStatus_Success</i>	Execution successfully
------------------------	------------------------

25.5.2 status_t DbgConsole_Deinit (void)

Call this function to disable debug log messages to be output via the specified peripheral initialized by the serial manager module.

Returns

Indicates whether de-initialization was successful or not.

25.5.3 status_t DbgConsole_EnterLowpower (void)

This function is used to prepare to enter low power consumption.

Returns

Indicates whether de-initialization was successful or not.

25.5.4 `status_t DbgConsole_ExitLowpower (void)`

This function is used to restore from low power consumption.

Returns

Indicates whether de-initialization was successful or not.

25.5.5 `int DbgConsole_Printf (const char * fmt_s, ...)`

Call this function to write a formatted output to the standard output stream.

Parameters

<i>fmt_s</i>	Format control string.
--------------	------------------------

Returns

Returns the number of characters printed or a negative value if an error occurs.

25.5.6 `int DbgConsole_Vprintf (const char * fmt_s, va_list formatStringArg)`

Call this function to write a formatted output to the standard output stream.

Parameters

<i>fmt_s</i>	Format control string.
<i>formatString-Arg</i>	Format arguments.

Returns

Returns the number of characters printed or a negative value if an error occurs.

25.5.7 `int DbgConsole_Putchar (int ch)`

Call this function to write a character to stdout.

Parameters

<i>ch</i>	Character to be written.
-----------	--------------------------

Returns

Returns the character written.

25.5.8 int DbgConsole_Scanf (char * *fmt_s*, ...)

Call this function to read formatted data from the standard input stream.

Note

Due the limitation in the BM OSA environment (CPU is blocked in the function, other tasks will not be scheduled), the function cannot be used when the `DEBUG_CONSOLE_TRANSFER_NON_BLOCKING` is set in the BM OSA environment. And an error is returned when the function called in this case. The suggestion is that polling the non-blocking function `DbgConsole_TryGetchar` to get the input char.

Parameters

<i>fmt_s</i>	Format control string.
--------------	------------------------

Returns

Returns the number of fields successfully converted and assigned.

25.5.9 int DbgConsole_Getchar (void)

Call this function to read a character from standard input.

Note

Due the limitation in the BM OSA environment (CPU is blocked in the function, other tasks will not be scheduled), the function cannot be used when the `DEBUG_CONSOLE_TRANSFER_NON_BLOCKING` is set in the BM OSA environment. And an error is returned when the function called in this case. The suggestion is that polling the non-blocking function `DbgConsole_TryGetchar` to get the input char.

Returns

Returns the character read.

25.5.10 int DbgConsole_BlockingPrintf (const char * *fmt_s*, ...)

Call this function to write a formatted output to the standard output stream with the blocking mode. The function will send data with blocking mode no matter the DEBUG_CONSOLE_TRANSFER_NON_BLOCKING set or not. The function could be used in system ISR mode with DEBUG_CONSOLE_TRANSFER_NON_BLOCKING set.

Parameters

<i>fmt_s</i>	Format control string.
--------------	------------------------

Returns

Returns the number of characters printed or a negative value if an error occurs.

25.5.11 int DbgConsole_BlockingVprintf (const char * *fmt_s*, va_list *formatStringArg*)

Call this function to write a formatted output to the standard output stream with the blocking mode. The function will send data with blocking mode no matter the DEBUG_CONSOLE_TRANSFER_NON_BLOCKING set or not. The function could be used in system ISR mode with DEBUG_CONSOLE_TRANSFER_NON_BLOCKING set.

Parameters

<i>fmt_s</i>	Format control string.
<i>formatStringArg</i>	Format arguments.

Returns

Returns the number of characters printed or a negative value if an error occurs.

25.5.12 status_t DbgConsole_Flush (void)

Call this function to wait the tx buffer empty. If interrupt transfer is using, make sure the global IRQ is enable before call this function This function should be called when 1, before enter power down mode 2, log is required to print to terminal immediately

Returns

Indicates whether wait idle was successful or not.

25.5.13 int StrFormatPrintf (const char * *fmt*, va_list *ap*, char * *buf*, printfCb *cb*)

Note

I/O is performed by calling given function pointer using following (*func_ptr)(c);

Parameters

in	<i>fmt</i>	Format string for printf.
in	<i>ap</i>	Arguments to printf.
in	<i>buf</i>	pointer to the buffer
	<i>cb</i>	print callbck function pointer

Returns

Number of characters to be print

25.5.14 int StrFormatScanf (const char * *line_ptr*, char * *format*, va_list *args_ptr*)

Parameters

in	<i>line_ptr</i>	The input line of ASCII data.
in	<i>format</i>	Format first points to the format string.
in	<i>args_ptr</i>	The list of parameters.

Returns

Number of input items converted and assigned.

Return values

<i>IO_EOF</i>	When line_ptr is empty string "".
---------------	-----------------------------------

25.6 Semihosting

Semihosting is a mechanism for ARM targets to communicate input/output requests from application code to a host computer running a debugger. This mechanism can be used, for example, to enable functions in the C library, such as `printf()` and `scanf()`, to use the screen and keyboard of the host rather than having a screen and keyboard on the target system.

25.6.1 Guide Semihosting for IAR

NOTE: After the setting both "printf" and "scanf" are available for debugging, if you want use PRINTF with semihosting, please make sure the `SDK_DEBUGCONSOLE` is `DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN`.

Step 1: Setting up the environment

1. To set debugger options, choose Project>Options. In the Debugger category, click the Setup tab.
2. Select Run to main and click OK. This ensures that the debug session starts by running the main function.
3. The project is now ready to be built.

Step 2: Building the project

1. Compile and link the project by choosing Project>Make or F7.
2. Alternatively, click the Make button on the tool bar. The Make command compiles and links those files that have been modified.

Step 3: Starting semihosting

1. Choose "Semihosting_IAR" project -> "Options" -> "Debugger" -> "J-Link/J-Trace".
2. Choose tab "J-Link/J-Trace" -> "Connection" tab -> "SWD".
3. Choose tab "General Options" -> "Library Configurations", select Semihosted, select Via semihosting. Please Make sure the `SDK_DEBUGCONSOLE_UART` is not defined in project settings.
4. Start the project by choosing Project>Download and Debug.
5. Choose View>Terminal I/O to display the output from the I/O operations.

25.6.2 Guide Semihosting for Keil µVision

NOTE: Semihosting is not support by MDK-ARM, use the retargeting functionality of MDK-ARM instead.

25.6.3 Guide Semihosting for MCUXpresso IDE

Step 1: Setting up the environment

1. To set debugger options, choose Project>Properties. select the setting category.
2. Select Tool Settings, unfold MCU C Compile.
3. Select Preprocessor item.
4. Set SDK_DEBUGCONSOLE=0, if set SDK_DEBUGCONSOLE=1, the log will be redirect to the UART.

Step 2: Building the project

1. Compile and link the project.

Step 3: Starting semihosting

1. Download and debug the project.
2. When the project runs successfully, the result can be seen in the Console window.

Semihosting can also be selected through the "Quick settings" menu in the left bottom window, Quick settings->SDK Debug Console->Semihost console.

25.6.4 Guide Semihosting for ARMGCC

Step 1: Setting up the environment

1. Turn on "J-LINK GDB Server" -> Select suitable "Target device" -> "OK".
2. Turn on "PuTTY". Set up as follows.
 - "Host Name (or IP address)" : localhost
 - "Port" :2333
 - "Connection type" : Telet.
 - Click "Open".
3. Increase "Heap/Stack" for GCC to 0x2000:

Add to "CMakeLists.txt"

```
SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "${CMAKE_EXE_LINKER_FLAGS_RELEASE}
--defsym=__stack_size__=0x2000")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} --
defsym=__stack_size__=0x2000")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} --
defsym=__heap_size__=0x2000")

SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "${CMAKE_EXE_LINKER_FLAGS_RELEASE}
--defsym=__heap_size__=0x2000")
```


Step 2: Building the project

1. Change "CMakeLists.txt":

Change "SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "\${CMAKE_EXE_LINKER_FLAGS_RELEASE} -specs=nano.specs")"

to "SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "\${CMAKE_EXE_LINKER_FLAGS_RELEASE} -specs=rdimon.specs")"

Replace paragraph

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} -fno-common")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} -ffunction-sections")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} -fdata-sections")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} -ffreestanding")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} -fno-builtin")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} -mthumb")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} -mapcs")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} -Xlinker")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} --gc-sections")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} -Xlinker")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} -static")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} -Xlinker")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} -z")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} -Xlinker")

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} muldefs")

To

SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "\${CMAKE_EXE_LINKER_FLAGS_DEBUG} --specs=rdimon.specs ")

Remove

target_link_libraries(semihosting_ARMGCC.elf debug nosys)

2. Run "build_debug.bat" to build project

Step 3: Starting semihosting

1. Download the image and set as follows.

```
cd D:\mcu-sdk-2.0-origin\boards\twrk64f120m\driver_examples\semihosting\armgcc\debug
d:
C:\PROGRA~2\GNUTOO~1\4BD65~1.920\bin\arm-none-eabi-gdb.exe
target remote localhost:2331
monitor reset
monitor semihosting enable
monitor semihosting thumbSWI 0xAB
monitor semihosting IOClient 1
monitor flash device = MK64FN1M0xxx12
load semihosting_ARMGCC.elf
monitor reg pc = (0x00000004)
monitor reg sp = (0x00000000)
continue
```

2. After the setting, press "enter". The PuTTY window now shows the printf() output.

25.7 SWO

Serial wire output is a mechanism for ARM targets to output signal from core through a single pin. Some IDEs also support SWO, such IAR and KEIL, both input and output are supported, see below for details.

25.7.1 Guide SWO for SDK

NOTE: After the setting both "printf" and "PRINTF" are available for debugging, JlinkSWOViewer can be used to capture the output log.

Step 1: Setting up the environment

1. Define SERIAL_PORT_TYPE_SWO in your project settings.
2. Prepare code, the port and baudrate can be decided by application, clkSrcFreq should be mcu core clock frequency:

```
DbgConsole_Init(instance, baudRate, kSerialPort_Swo, clkSrcFreq);
```

3. Use PRINTF or printf to print some thing in application.

Step 2: Building the project

Step 3: Download and run project

25.7.1.1 Guide SWO for IAR

NOTE: After the setting both "printf" and "scanf" are available for debugging.

Step 1: Setting up the environment

1. Choose project -> "Options" -> "Debugger" -> "J-Link/J-Trace".
2. Choose tab "J-Link/J-Trace" -> "Connection" tab -> "SWD".
3. Choose tab "General Options" -> "Library Configurations", select Semihosted, select Via SWO.
4. To configure the hardware's generation of trace data, click the SWO Configuration button available in the SWO Configuration dialog box. The value of the CPU clock option must reflect the frequency of the CPU clock speed at which the application executes. Note also that the settings you make are preserved between debug sessions. To decrease the amount of transmissions on the communication channel, you can disable the Timestamp option. Alternatively, set a lower rate for PC Sampling or use a higher SWO clock frequency.
5. Open the SWO Trace window from J-LINK, and click the Activate button to enable trace data collection.
6. There are three cases for this SDK_DEBUGCONSOLE_UART whether or not defined. a: if use uppercase PRINTF to output log, The SDK_DEBUGCONSOLE_UART defined or not defined will not effect debug function. b: if use lowercase printf to output log and defined SDK_DEBUGCONSOLE_UART to zero, then debug function ok. c: if use lowercase printf to output log and defined SDK_DEBUGCONSOLE_UART to one, then debug function ok.

NOTE: Case a or c only apply at example which enable swo function,the SDK_DEBUGCONSOLE_UART definition in fsl_debug_console.h. For case a and c, Do and not do the above third step will be not affect function.

1. Start the project by choosing Project>Download and Debug.

Step 2: Building the project

Step 3: Starting swo

1. Download and debug application.
2. Choose View -> Terminal I/O to display the output from the I/O operations.
3. Run application.

25.7.2 Guide SWO for Keil μ Vision

NOTE: After the setting both "printf" and "scanf" are available for debugging.

Step 1: Setting up the environment

1. There are three cases for this SDK_DEBUGCONSOLE_UART whether or not defined. a: if use uppercase PRINTF to output log,the SDK_DEBUGCONSOLE_UART definition does not affect the functionality and skip the second step directly. b: if use lowercase printf to output log and defined SDK_DEBUGCONSOLE_UART to zero,then start the second step. c: if use lowercase printf to output log and defined SDK_DEBUGCONSOLE_UART to one,then skip the second step directly.

NOTE: Case a or c only apply at example which enable swo function,the SDK_DEBUGCONSOLE_UART definition in fsl_debug_console.h.

1. In menu bar, click Management Run-Time Environment icon, select Compiler, unfold I/O, enable STDERR/STDIN/STDOUT and set the variant to ITM.
2. Open Project>Options for target or using Alt+F7 or click.
3. Select "Debug" tab, select "J-Link/J-Trace Cortex" and click "Setting button".
4. Select "Debug" tab and choose Port:SW, then select "Trace" tab, choose "Enable" and click O-K, please make sure the Core clock is set correctly, enable autodetect max SWO clk, enable ITM Stimulus Ports 0.

Step 3: Building the project

1. Compile and link the project by choosing Project>Build Target or using F7.

Step 4: Run the project

1. Choose "Debug" on menu bar or Ctrl F5.
2. In menu bar, choose "Serial Window" and click to "Debug (printf) Viewer".
3. Run line by line to see result in Console Window.

25.7.3 Guide SWO for MCUXpresso IDE

NOTE: MCUX support SWO for LPC-Link2 debug probe only.

25.7.4 Guide SWO for ARMGCC

NOTE: ARMGCC has no library support SWO.



Chapter 26

CODEC Driver

26.1 Overview

The MCUXpresso SDK provides a codec abstraction driver interface to access codec register.

Modules

- [CODEC Common Driver](#)
- [CODEC I2C Driver](#)
- [WM8960 Driver](#)

26.2 CODEC Common Driver

26.2.1 Overview

The codec common driver provides a codec control abstraction interface.

Modules

- [CODEC Adapter](#)
- [WM8960 Adapter](#)

Data Structures

- struct [codec_config_t](#)
Initialize structure of the codec. [More...](#)
- struct [codec_capability_t](#)
codec capability [More...](#)
- struct [codec_handle_t](#)
Codec handle definition. [More...](#)

Macros

- `#define CODEC_VOLUME_MAX_VALUE (100U)`
codec maximum volume range

Enumerations

- enum {
 [kStatus_CODEC_NotSupport](#) = MAKE_STATUS(kStatusGroup_CODEC, 0U),
 [kStatus_CODEC_DeviceNotRegistered](#) = MAKE_STATUS(kStatusGroup_CODEC, 1U),
 [kStatus_CODEC_I2CBusInitialFailed](#),
 [kStatus_CODEC_I2CCommandTransferFailed](#) }
 CODEC status.
- enum [codec_audio_protocol_t](#) {
 [kCODEC_BusI2S](#) = 0U,
 [kCODEC_BusLeftJustified](#) = 1U,
 [kCODEC_BusRightJustified](#) = 2U,
 [kCODEC_BusPCMA](#) = 3U,
 [kCODEC_BusPCMB](#) = 4U,
 [kCODEC_BusTDM](#) = 5U }
 AUDIO format definition.

- enum {
 - kCODEC_AudioSampleRate8KHz = 8000U,
 - kCODEC_AudioSampleRate11025Hz = 11025U,
 - kCODEC_AudioSampleRate12KHz = 12000U,
 - kCODEC_AudioSampleRate16KHz = 16000U,
 - kCODEC_AudioSampleRate22050Hz = 22050U,
 - kCODEC_AudioSampleRate24KHz = 24000U,
 - kCODEC_AudioSampleRate32KHz = 32000U,
 - kCODEC_AudioSampleRate44100Hz = 44100U,
 - kCODEC_AudioSampleRate48KHz = 48000U,
 - kCODEC_AudioSampleRate96KHz = 96000U,
 - kCODEC_AudioSampleRate192KHz = 192000U,
 - kCODEC_AudioSampleRate384KHz = 384000U }*audio sample rate definition*
- enum {
 - kCODEC_AudioBitWidth16bit = 16U,
 - kCODEC_AudioBitWidth20bit = 20U,
 - kCODEC_AudioBitWidth24bit = 24U,
 - kCODEC_AudioBitWidth32bit = 32U }*audio bit width*
- enum codec_module_t {
 - kCODEC_ModuleADC = 0U,
 - kCODEC_ModuleDAC = 1U,
 - kCODEC_ModulePGA = 2U,
 - kCODEC_ModuleHeadphone = 3U,
 - kCODEC_ModuleSpeaker = 4U,
 - kCODEC_ModuleLinein = 5U,
 - kCODEC_ModuleLineout = 6U,
 - kCODEC_ModuleVref = 7U,
 - kCODEC_ModuleMicbias = 8U,
 - kCODEC_ModuleMic = 9U,
 - kCODEC_ModuleI2SIn = 10U,
 - kCODEC_ModuleI2SOut = 11U,
 - kCODEC_ModuleMixer = 12U }*audio codec module*
- enum codec_module_ctrl_cmd_t { kCODEC_ModuleSwitchI2SInInterface = 0U }
 audio codec module control cmd
- enum {
 - kCODEC_ModuleI2SInInterfacePCM = 0U,
 - kCODEC_ModuleI2SInInterfaceDSD = 1U }*audio codec module digital interface*
- enum {
 - kCODEC_RecordSourceDifferentialLine = 1U,
 - kCODEC_RecordSourceLineInput = 2U,
 - kCODEC_RecordSourceDifferentialMic = 4U,
 - kCODEC_RecordSourceDigitalMic = 8U,


```
kCODEC_RecordSourceSingleEndMic = 16U }
```

audio codec module record source value

- enum {
 - kCODEC_RecordChannelLeft1 = 1U,
 - kCODEC_RecordChannelLeft2 = 2U,
 - kCODEC_RecordChannelLeft3 = 4U,
 - kCODEC_RecordChannelRight1 = 1U,
 - kCODEC_RecordChannelRight2 = 2U,
 - kCODEC_RecordChannelRight3 = 4U,
 - kCODEC_RecordChannelDifferentialPositive1 = 1U,
 - kCODEC_RecordChannelDifferentialPositive2 = 2U,
 - kCODEC_RecordChannelDifferentialPositive3 = 4U,
 - kCODEC_RecordChannelDifferentialNegative1 = 8U,
 - kCODEC_RecordChannelDifferentialNegative2 = 16U,
 - kCODEC_RecordChannelDifferentialNegative3 = 32U }

audio codec record channel

- enum {
 - kCODEC_PlaySourcePGA = 1U,
 - kCODEC_PlaySourceInput = 2U,
 - kCODEC_PlaySourceDAC = 4U,
 - kCODEC_PlaySourceMixerIn = 1U,
 - kCODEC_PlaySourceMixerInLeft = 2U,
 - kCODEC_PlaySourceMixerInRight = 4U,
 - kCODEC_PlaySourceAux = 8U }

audio codec module play source value

- enum {
 - kCODEC_PlayChannelHeadphoneLeft = 1U,
 - kCODEC_PlayChannelHeadphoneRight = 2U,
 - kCODEC_PlayChannelSpeakerLeft = 4U,
 - kCODEC_PlayChannelSpeakerRight = 8U,
 - kCODEC_PlayChannelLineOutLeft = 16U,
 - kCODEC_PlayChannelLineOutRight = 32U,
 - kCODEC_PlayChannelLeft0 = 1U,
 - kCODEC_PlayChannelRight0 = 2U,
 - kCODEC_PlayChannelLeft1 = 4U,
 - kCODEC_PlayChannelRight1 = 8U,
 - kCODEC_PlayChannelLeft2 = 16U,
 - kCODEC_PlayChannelRight2 = 32U,
 - kCODEC_PlayChannelLeft3 = 64U,
 - kCODEC_PlayChannelRight3 = 128U }

codec play channel

- enum {

```
kCODEC_VolumeHeadphoneLeft = 1U,  
kCODEC_VolumeHeadphoneRight = 2U,  
kCODEC_VolumeSpeakerLeft = 4U,  
kCODEC_VolumeSpeakerRight = 8U,  
kCODEC_VolumeLineOutLeft = 16U,  
kCODEC_VolumeLineOutRight = 32U,  
kCODEC_VolumeLeft0 = 1UL << 0U,  
kCODEC_VolumeRight0 = 1UL << 1U,  
kCODEC_VolumeLeft1 = 1UL << 2U,  
kCODEC_VolumeRight1 = 1UL << 3U,  
kCODEC_VolumeLeft2 = 1UL << 4U,  
kCODEC_VolumeRight2 = 1UL << 5U,  
kCODEC_VolumeLeft3 = 1UL << 6U,  
kCODEC_VolumeRight3 = 1UL << 7U,  
kCODEC_VolumeDAC = 1UL << 8U }
```

codec volume setting

- enum {

```

kCODEC_SupportModuleADC = 1U << 0U,
kCODEC_SupportModuleDAC = 1U << 1U,
kCODEC_SupportModulePGA = 1U << 2U,
kCODEC_SupportModuleHeadphone = 1U << 3U,
kCODEC_SupportModuleSpeaker = 1U << 4U,
kCODEC_SupportModuleLinein = 1U << 5U,
kCODEC_SupportModuleLineout = 1U << 6U,
kCODEC_SupportModuleVref = 1U << 7U,
kCODEC_SupportModuleMicbias = 1U << 8U,
kCODEC_SupportModuleMic = 1U << 9U,
kCODEC_SupportModuleI2SIn = 1U << 10U,
kCODEC_SupportModuleI2SOut = 1U << 11U,
kCODEC_SupportModuleMixer = 1U << 12U,
kCODEC_SupportModuleI2SInSwitchInterface = 1U << 13U,
kCODEC_SupportPlayChannelLeft0 = 1U << 0U,
kCODEC_SupportPlayChannelRight0 = 1U << 1U,
kCODEC_SupportPlayChannelLeft1 = 1U << 2U,
kCODEC_SupportPlayChannelRight1 = 1U << 3U,
kCODEC_SupportPlayChannelLeft2 = 1U << 4U,
kCODEC_SupportPlayChannelRight2 = 1U << 5U,
kCODEC_SupportPlayChannelLeft3 = 1U << 6U,
kCODEC_SupportPlayChannelRight3 = 1U << 7U,
kCODEC_SupportPlaySourcePGA = 1U << 8U,
kCODEC_SupportPlaySourceInput = 1U << 9U,
kCODEC_SupportPlaySourceDAC = 1U << 10U,
kCODEC_SupportPlaySourceMixerIn = 1U << 11U,
kCODEC_SupportPlaySourceMixerInLeft = 1U << 12U,
kCODEC_SupportPlaySourceMixerInRight = 1U << 13U,
kCODEC_SupportPlaySourceAux = 1U << 14U,
kCODEC_SupportRecordSourceDifferentialLine = 1U << 0U,
kCODEC_SupportRecordSourceLineInput = 1U << 1U,
kCODEC_SupportRecordSourceDifferentialMic = 1U << 2U,
kCODEC_SupportRecordSourceDigitalMic = 1U << 3U,
kCODEC_SupportRecordSourceSingleEndMic = 1U << 4U,
kCODEC_SupportRecordChannelLeft1 = 1U << 6U,
kCODEC_SupportRecordChannelLeft2 = 1U << 7U,
kCODEC_SupportRecordChannelLeft3 = 1U << 8U,
kCODEC_SupportRecordChannelRight1 = 1U << 9U,
kCODEC_SupportRecordChannelRight2 = 1U << 10U,
kCODEC_SupportRecordChannelRight3 = 1U << 11U }

```

audio codec capability

Functions

- `status_t CODEC_Init` (`codec_handle_t *handle`, `codec_config_t *config`)
Codec initialization.
- `status_t CODEC_Deinit` (`codec_handle_t *handle`)
Codec de-initialization.
- `status_t CODEC_SetFormat` (`codec_handle_t *handle`, `uint32_t mclk`, `uint32_t sampleRate`, `uint32_t bitWidth`)
set audio data format.
- `status_t CODEC_ModuleControl` (`codec_handle_t *handle`, `codec_module_ctrl_cmd_t cmd`, `uint32_t data`)
codec module control.
- `status_t CODEC_SetVolume` (`codec_handle_t *handle`, `uint32_t channel`, `uint32_t volume`)
set audio codec pl volume.
- `status_t CODEC_SetMute` (`codec_handle_t *handle`, `uint32_t channel`, `bool mute`)
set audio codec module mute.
- `status_t CODEC_SetPower` (`codec_handle_t *handle`, `codec_module_t module`, `bool powerOn`)
set audio codec power.
- `status_t CODEC_SetRecord` (`codec_handle_t *handle`, `uint32_t recordSource`)
codec set record source.
- `status_t CODEC_SetRecordChannel` (`codec_handle_t *handle`, `uint32_t leftRecordChannel`, `uint32_t rightRecordChannel`)
codec set record channel.
- `status_t CODEC_SetPlay` (`codec_handle_t *handle`, `uint32_t playSource`)
codec set play source.

Driver version

- `#define FSL_CODEC_DRIVER_VERSION` (`MAKE_VERSION(2, 3, 0)`)
CLOCK driver version 2.3.0.

26.2.2 Data Structure Documentation

26.2.2.1 struct codec_config_t

Data Fields

- `uint32_t codecDevType`
codec type
- `void * codecDevConfig`
Codec device specific configuration.

26.2.2.2 struct codec_capability_t

Data Fields

- uint32_t [codecModuleCapability](#)
codec module capability
- uint32_t [codecPlayCapability](#)
codec play capability
- uint32_t [codecRecordCapability](#)
codec record capability
- uint32_t [codecVolumeCapability](#)
codec volume capability

26.2.2.3 struct _codec_handle

codec handle declaration

- Application should allocate a buffer with CODEC_HANDLE_SIZE for handle definition, such as uint8_t codecHandleBuffer[CODEC_HANDLE_SIZE]; codec_handle_t *codecHandle = codecHandleBuffer;

Data Fields

- [codec_config_t](#) * [codecConfig](#)
codec configuration function pointer
- const [codec_capability_t](#) * [codecCapability](#)
codec capability
- uint8_t [codecDevHandle](#) [HAL_CODEC_HANDLER_SIZE]
codec device handle

26.2.3 Macro Definition Documentation

26.2.3.1 #define FSL_CODEC_DRIVER_VERSION (MAKE_VERSION(2, 3, 0))

26.2.4 Enumeration Type Documentation

26.2.4.1 anonymous enum

Enumerator

kStatus_CODEC_NotSupport CODEC not support status.

kStatus_CODEC_DeviceNotRegistered CODEC device register failed status.

kStatus_CODEC_I2CBusInitialFailed CODEC i2c bus initialization failed status.

kStatus_CODEC_I2CCommandTransferFailed CODEC i2c bus command transfer failed status.

26.2.4.2 enum codec_audio_protocol_t

Enumerator

kCODEC_BusI2S I2S type.
kCODEC_BusLeftJustified Left justified mode.
kCODEC_BusRightJustified Right justified mode.
kCODEC_BusPCMA DSP/PCM A mode.
kCODEC_BusPCMB DSP/PCM B mode.
kCODEC_BusTDM TDM mode.

26.2.4.3 anonymous enum

Enumerator

kCODEC_AudioSampleRate8KHz Sample rate 8000 Hz.
kCODEC_AudioSampleRate11025Hz Sample rate 11025 Hz.
kCODEC_AudioSampleRate12KHz Sample rate 12000 Hz.
kCODEC_AudioSampleRate16KHz Sample rate 16000 Hz.
kCODEC_AudioSampleRate22050Hz Sample rate 22050 Hz.
kCODEC_AudioSampleRate24KHz Sample rate 24000 Hz.
kCODEC_AudioSampleRate32KHz Sample rate 32000 Hz.
kCODEC_AudioSampleRate44100Hz Sample rate 44100 Hz.
kCODEC_AudioSampleRate48KHz Sample rate 48000 Hz.
kCODEC_AudioSampleRate96KHz Sample rate 96000 Hz.
kCODEC_AudioSampleRate192KHz Sample rate 192000 Hz.
kCODEC_AudioSampleRate384KHz Sample rate 384000 Hz.

26.2.4.4 anonymous enum

Enumerator

kCODEC_AudioBitWidth16bit audio bit width 16
kCODEC_AudioBitWidth20bit audio bit width 20
kCODEC_AudioBitWidth24bit audio bit width 24
kCODEC_AudioBitWidth32bit audio bit width 32

26.2.4.5 enum codec_module_t

Enumerator

kCODEC_ModuleADC codec module ADC
kCODEC_ModuleDAC codec module DAC
kCODEC_ModulePGA codec module PGA
kCODEC_ModuleHeadphone codec module headphone

kCODEC_ModuleSpeaker codec module speaker
kCODEC_ModuleLinein codec module linein
kCODEC_ModuleLineout codec module lineout
kCODEC_ModuleVref codec module VREF
kCODEC_ModuleMicbias codec module MIC BIAS
kCODEC_ModuleMic codec module MIC
kCODEC_ModuleI2SIn codec module I2S in
kCODEC_ModuleI2SOut codec module I2S out
kCODEC_ModuleMixer codec module mixer

26.2.4.6 enum codec_module_ctrl_cmd_t

Enumerator

kCODEC_ModuleSwitchI2SInInterface module digital interface swtch.

26.2.4.7 anonymous enum

Enumerator

kCODEC_ModuleI2SInInterfacePCM Pcm interface.
kCODEC_ModuleI2SInInterfaceDSD DSD interface.

26.2.4.8 anonymous enum

Enumerator

kCODEC_RecordSourceDifferentialLine record source from differential line
kCODEC_RecordSourceLineInput record source from line input
kCODEC_RecordSourceDifferentialMic record source from differential mic
kCODEC_RecordSourceDigitalMic record source from digital microphone
kCODEC_RecordSourceSingleEndMic record source from single microphone

26.2.4.9 anonymous enum

Enumerator

kCODEC_RecordChannelLeft1 left record channel 1
kCODEC_RecordChannelLeft2 left record channel 2
kCODEC_RecordChannelLeft3 left record channel 3
kCODEC_RecordChannelRight1 right record channel 1
kCODEC_RecordChannelRight2 right record channel 2
kCODEC_RecordChannelRight3 right record channel 3
kCODEC_RecordChannelDifferentialPositive1 differential positive record channel 1

<i>kCODEC_RecordChannelDifferentialPositive2</i>	differential positive record channel 2
<i>kCODEC_RecordChannelDifferentialPositive3</i>	differential positive record channel 3
<i>kCODEC_RecordChannelDifferentialNegative1</i>	differential negative record channel 1
<i>kCODEC_RecordChannelDifferentialNegative2</i>	differential negative record channel 2
<i>kCODEC_RecordChannelDifferentialNegative3</i>	differential negative record channel 3

26.2.4.10 anonymous enum

Enumerator

<i>kCODEC_PlaySourcePGA</i>	play source PGA, bypass ADC
<i>kCODEC_PlaySourceInput</i>	play source Input3
<i>kCODEC_PlaySourceDAC</i>	play source DAC
<i>kCODEC_PlaySourceMixerIn</i>	play source mixer in
<i>kCODEC_PlaySourceMixerInLeft</i>	play source mixer in left
<i>kCODEC_PlaySourceMixerInRight</i>	play source mixer in right
<i>kCODEC_PlaySourceAux</i>	play source mixer in AUx

26.2.4.11 anonymous enum

Enumerator

<i>kCODEC_PlayChannelHeadphoneLeft</i>	play channel headphone left
<i>kCODEC_PlayChannelHeadphoneRight</i>	play channel headphone right
<i>kCODEC_PlayChannelSpeakerLeft</i>	play channel speaker left
<i>kCODEC_PlayChannelSpeakerRight</i>	play channel speaker right
<i>kCODEC_PlayChannelLineOutLeft</i>	play channel lineout left
<i>kCODEC_PlayChannelLineOutRight</i>	play channel lineout right
<i>kCODEC_PlayChannelLeft0</i>	play channel left0
<i>kCODEC_PlayChannelRight0</i>	play channel right0
<i>kCODEC_PlayChannelLeft1</i>	play channel left1
<i>kCODEC_PlayChannelRight1</i>	play channel right1
<i>kCODEC_PlayChannelLeft2</i>	play channel left2
<i>kCODEC_PlayChannelRight2</i>	play channel right2
<i>kCODEC_PlayChannelLeft3</i>	play channel left3
<i>kCODEC_PlayChannelRight3</i>	play channel right3

26.2.4.12 anonymous enum

Enumerator

<i>kCODEC_VolumeHeadphoneLeft</i>	headphone left volume
<i>kCODEC_VolumeHeadphoneRight</i>	headphone right volume
<i>kCODEC_VolumeSpeakerLeft</i>	speaker left volume
<i>kCODEC_VolumeSpeakerRight</i>	speaker right volume

kCODEC_VolumeLineOutLeft lineout left volume
kCODEC_VolumeLineOutRight lineout right volume
kCODEC_VolumeLeft0 left0 volume
kCODEC_VolumeRight0 right0 volume
kCODEC_VolumeLeft1 left1 volume
kCODEC_VolumeRight1 right1 volume
kCODEC_VolumeLeft2 left2 volume
kCODEC_VolumeRight2 right2 volume
kCODEC_VolumeLeft3 left3 volume
kCODEC_VolumeRight3 right3 volume
kCODEC_VolumeDAC dac volume

26.2.4.13 anonymous enum

Enumerator

kCODEC_SupportModuleADC codec capability of module ADC
kCODEC_SupportModuleDAC codec capability of module DAC
kCODEC_SupportModulePGA codec capability of module PGA
kCODEC_SupportModuleHeadphone codec capability of module headphone
kCODEC_SupportModuleSpeaker codec capability of module speaker
kCODEC_SupportModuleLinein codec capability of module linein
kCODEC_SupportModuleLineout codec capability of module lineout
kCODEC_SupportModuleVref codec capability of module vref
kCODEC_SupportModuleMicbias codec capability of module mic bias
kCODEC_SupportModuleMic codec capability of module mic bias
kCODEC_SupportModuleI2SIn codec capability of module I2S in
kCODEC_SupportModuleI2SOut codec capability of module I2S out
kCODEC_SupportModuleMixer codec capability of module mixer
kCODEC_SupportModuleI2SInSwitchInterface codec capability of module I2S in switch interface

kCODEC_SupportPlayChannelLeft0 codec capability of play channel left 0
kCODEC_SupportPlayChannelRight0 codec capability of play channel right 0
kCODEC_SupportPlayChannelLeft1 codec capability of play channel left 1
kCODEC_SupportPlayChannelRight1 codec capability of play channel right 1
kCODEC_SupportPlayChannelLeft2 codec capability of play channel left 2
kCODEC_SupportPlayChannelRight2 codec capability of play channel right 2
kCODEC_SupportPlayChannelLeft3 codec capability of play channel left 3
kCODEC_SupportPlayChannelRight3 codec capability of play channel right 3
kCODEC_SupportPlaySourcePGA codec capability of set playback source PGA
kCODEC_SupportPlaySourceInput codec capability of set playback source INPUT
kCODEC_SupportPlaySourceDAC codec capability of set playback source DAC
kCODEC_SupportPlaySourceMixerIn codec capability of set play source Mixer in
kCODEC_SupportPlaySourceMixerInLeft codec capability of set play source Mixer in left
kCODEC_SupportPlaySourceMixerInRight codec capability of set play source Mixer in right

kCODEC_SupportPlaySourceAux codec capability of set play source aux

kCODEC_SupportRecordSourceDifferentialLine codec capability of record source differential line

kCODEC_SupportRecordSourceLineInput codec capability of record source line input

kCODEC_SupportRecordSourceDifferentialMic codec capability of record source differential mic

kCODEC_SupportRecordSourceDigitalMic codec capability of record digital mic

kCODEC_SupportRecordSourceSingleEndMic codec capability of single end mic

kCODEC_SupportRecordChannelLeft1 left record channel 1

kCODEC_SupportRecordChannelLeft2 left record channel 2

kCODEC_SupportRecordChannelLeft3 left record channel 3

kCODEC_SupportRecordChannelRight1 right record channel 1

kCODEC_SupportRecordChannelRight2 right record channel 2

kCODEC_SupportRecordChannelRight3 right record channel 3

26.2.5 Function Documentation

26.2.5.1 **status_t CODEC_Init (codec_handle_t * *handle*, codec_config_t * *config*)**

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configurations.

Returns

kStatus_Success is success, else de-initial failed.

26.2.5.2 **status_t CODEC_Deinit (codec_handle_t * *handle*)**

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus_Success is success, else de-initial failed.

26.2.5.3 **status_t CODEC_SetFormat (codec_handle_t * *handle*, uint32_t *mclk*, uint32_t *sampleRate*, uint32_t *bitWidth*)**

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus_Success is success, else configure failed.

26.2.5.4 status_t CODEC_ModuleControl (codec_handle_t * *handle*, codec_module_ctrl_cmd_t *cmd*, uint32_t *data*)

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature.

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus_Success is success, else configure failed.

26.2.5.5 status_t CODEC_SetVolume (codec_handle_t * *handle*, uint32_t *channel*, uint32_t *volume*)

Parameters

<i>handle</i>	codec handle.
<i>channel</i>	audio codec volume channel, can be a value or combine value of <code>_codec_volume_capability</code> or <code>_codec_play_channel</code> .
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

`kStatus_Success` is success, else configure failed.

26.2.5.6 `status_t CODEC_SetMute (codec_handle_t * handle, uint32_t channel, bool mute)`

Parameters

<i>handle</i>	codec handle.
<i>channel</i>	audio codec volume channel, can be a value or combine value of <code>_codec_volume_capability</code> or <code>_codec_play_channel</code> .
<i>mute</i>	true is mute, false is unmute.

Returns

`kStatus_Success` is success, else configure failed.

26.2.5.7 `status_t CODEC_SetPower (codec_handle_t * handle, codec_module_t module, bool powerOn)`

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

`kStatus_Success` is success, else configure failed.

26.2.5.8 `status_t CODEC_SetRecord (codec_handle_t * handle, uint32_t recordSource)`

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of <code>_codec_record_source</code> .

Returns

`kStatus_Success` is success, else configure failed.

26.2.5.9 `status_t CODEC_SetRecordChannel (codec_handle_t * handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)`

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference <code>_codec_record_channel</code> , can be a value combine of member in <code>_codec_record_channel</code> .
<i>rightRecord-Channel</i>	audio codec record channel, reference <code>_codec_record_channel</code> , can be a value combine of member in <code>_codec_record_channel</code> .

Returns

`kStatus_Success` is success, else configure failed.

26.2.5.10 `status_t CODEC_SetPlay (codec_handle_t * handle, uint32_t playSource)`

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of <code>_codec_play_source</code> .

Returns

`kStatus_Success` is success, else configure failed.

26.3 CODEC I2C Driver

The codec common driver provides a codec control abstraction interface.

26.4 WM8960 Driver

26.4.1 Overview

The wm8960 driver provides a codec control interface.

Data Structures

- struct [wm8960_audio_format_t](#)
wm8960 audio format [More...](#)
- struct [wm8960_master_sysclk_config_t](#)
wm8960 master system clock configuration [More...](#)
- struct [wm8960_config_t](#)
Initialize structure of WM8960. [More...](#)
- struct [wm8960_handle_t](#)
wm8960 codec handler [More...](#)

Macros

- #define [WM8960_I2C_HANDLER_SIZE](#) CODEC_I2C_MASTER_HANDLER_SIZE
wm8960 handle size
- #define [WM8960_LINVOL](#) 0x0U
Define the register address of WM8960.
- #define [WM8960_CACHEREGNUM](#) 56U
Cache register number.
- #define [WM8960_CLOCK2_BCLK_DIV_MASK](#) 0xFU
WM8960 CLOCK2 bits.
- #define [WM8960_IFACE1_FORMAT_MASK](#) 0x03U
WM8960_IFACE1 FORMAT bits.
- #define [WM8960_IFACE1_WL_MASK](#) 0x0CU
WM8960_IFACE1 WL bits.
- #define [WM8960_IFACE1_LRP_MASK](#) 0x10U
WM8960_IFACE1 LRP bit.
- #define [WM8960_IFACE1_DLR_SWAP_MASK](#) 0x20U
WM8960_IFACE1 DLR_SWAP bit.
- #define [WM8960_IFACE1_MS_MASK](#) 0x40U
WM8960_IFACE1 MS bit.
- #define [WM8960_IFACE1_BCLK_INV_MASK](#) 0x80U
WM8960_IFACE1 BCLK_INV bit.
- #define [WM8960_IFACE1_ALR_SWAP_MASK](#) 0x100U
WM8960_IFACE1 ALR_SWAP bit.
- #define [WM8960_POWER1_VREF_MASK](#) 0x40U
WM8960_POWER1.
- #define [WM8960_POWER2_DACL_MASK](#) 0x100U
WM8960_POWER2.
- #define [WM8960_I2C_ADDR](#) 0x1A
WM8960 I2C address.
- #define [WM8960_I2C_BAUDRATE](#) (100000U)

- *WM8960 I2C baudrate.*
- #define `WM8960_ADC_MAX_VOLUME_VALUE` 0xFFU
WM8960 maximum volume value.

Enumerations

- enum `wm8960_module_t` {
`kWM8960_ModuleADC` = 0,
`kWM8960_ModuleDAC` = 1,
`kWM8960_ModuleVREF` = 2,
`kWM8960_ModuleHP` = 3,
`kWM8960_ModuleMICB` = 4,
`kWM8960_ModuleMIC` = 5,
`kWM8960_ModuleLineIn` = 6,
`kWM8960_ModuleLineOut` = 7,
`kWM8960_ModuleSpeaker` = 8,
`kWM8960_ModuleOMIX` = 9 }
Modules in WM8960 board.
- enum {
`kWM8960_HeadphoneLeft` = 1,
`kWM8960_HeadphoneRight` = 2,
`kWM8960_SpeakerLeft` = 4,
`kWM8960_SpeakerRight` = 8 }
wm8960 play channel
- enum `wm8960_play_source_t` {
`kWM8960_PlaySourcePGA` = 1,
`kWM8960_PlaySourceInput` = 2,
`kWM8960_PlaySourceDAC` = 4 }
wm8960 play source
- enum `wm8960_route_t` {
`kWM8960_RouteBypass` = 0,
`kWM8960_RoutePlayback` = 1,
`kWM8960_RoutePlaybackandRecord` = 2,
`kWM8960_RouteRecord` = 5 }
WM8960 data route.
- enum `wm8960_protocol_t` {
`kWM8960_BusI2S` = 2,
`kWM8960_BusLeftJustified` = 1,
`kWM8960_BusRightJustified` = 0,
`kWM8960_BusPCMA` = 3,
`kWM8960_BusPCMB` = 3 | (1 << 4) }
The audio data transfer protocol choice.
- enum `wm8960_input_t` {


```

kWM8960_InputClosed = 0,
kWM8960_InputSingleEndedMic = 1,
kWM8960_InputDifferentialMicInput2 = 2,
kWM8960_InputDifferentialMicInput3 = 3,
kWM8960_InputLineINPUT2 = 4,
kWM8960_InputLineINPUT3 = 5 }
    wm8960 input source
• enum {
    kWM8960_AudioSampleRate8KHz = 8000U,
    kWM8960_AudioSampleRate11025Hz = 11025U,
    kWM8960_AudioSampleRate12KHz = 12000U,
    kWM8960_AudioSampleRate16KHz = 16000U,
    kWM8960_AudioSampleRate22050Hz = 22050U,
    kWM8960_AudioSampleRate24KHz = 24000U,
    kWM8960_AudioSampleRate32KHz = 32000U,
    kWM8960_AudioSampleRate44100Hz = 44100U,
    kWM8960_AudioSampleRate48KHz = 48000U,
    kWM8960_AudioSampleRate96KHz = 96000U,
    kWM8960_AudioSampleRate192KHz = 192000U,
    kWM8960_AudioSampleRate384KHz = 384000U }
    audio sample rate definition
• enum {
    kWM8960_AudioBitWidth16bit = 16U,
    kWM8960_AudioBitWidth20bit = 20U,
    kWM8960_AudioBitWidth24bit = 24U,
    kWM8960_AudioBitWidth32bit = 32U }
    audio bit width
• enum wm8960_sysclk_source_t {
    kWM8960_SysClkSourceMclk = 0U,
    kWM8960_SysClkSourceInternalPLL = 1U }
    wm8960 sysclk source

```

Functions

- `status_t WM8960_Init (wm8960_handle_t *handle, const wm8960_config_t *config)`
WM8960 initialize function.
- `status_t WM8960_Deinit (wm8960_handle_t *handle)`
Deinit the WM8960 codec.
- `status_t WM8960_SetDataRoute (wm8960_handle_t *handle, wm8960_route_t route)`
Set audio data route in WM8960.
- `status_t WM8960_SetLeftInput (wm8960_handle_t *handle, wm8960_input_t input)`
Set left audio input source in WM8960.
- `status_t WM8960_SetRightInput (wm8960_handle_t *handle, wm8960_input_t input)`
Set right audio input source in WM8960.
- `status_t WM8960_SetProtocol (wm8960_handle_t *handle, wm8960_protocol_t protocol)`
Set the audio transfer protocol.

- void [WM8960_SetMasterSlave](#) ([wm8960_handle_t](#) *handle, bool master)
Set WM8960 as master or slave.
- [status_t WM8960_SetVolume](#) ([wm8960_handle_t](#) *handle, [wm8960_module_t](#) module, [uint32_t](#) volume)
Set the volume of different modules in WM8960.
- [uint32_t WM8960_GetVolume](#) ([wm8960_handle_t](#) *handle, [wm8960_module_t](#) module)
Get the volume of different modules in WM8960.
- [status_t WM8960_SetMute](#) ([wm8960_handle_t](#) *handle, [wm8960_module_t](#) module, bool isEnabled)
Mute modules in WM8960.
- [status_t WM8960_SetModule](#) ([wm8960_handle_t](#) *handle, [wm8960_module_t](#) module, bool isEnabled)
Enable/disable expected devices.
- [status_t WM8960_SetPlay](#) ([wm8960_handle_t](#) *handle, [uint32_t](#) playSource)
SET the WM8960 play source.
- [status_t WM8960_ConfigDataFormat](#) ([wm8960_handle_t](#) *handle, [uint32_t](#) sysclk, [uint32_t](#) sample_rate, [uint32_t](#) bits)
Configure the data format of audio data.
- [status_t WM8960_SetJackDetect](#) ([wm8960_handle_t](#) *handle, bool isEnabled)
Enable/disable jack detect feature.
- [status_t WM8960_WriteReg](#) ([wm8960_handle_t](#) *handle, [uint8_t](#) reg, [uint16_t](#) val)
Write register to WM8960 using I2C.
- [status_t WM8960_ReadReg](#) ([uint8_t](#) reg, [uint16_t](#) *val)
Read register from WM8960 using I2C.
- [status_t WM8960_ModifyReg](#) ([wm8960_handle_t](#) *handle, [uint8_t](#) reg, [uint16_t](#) mask, [uint16_t](#) val)
Modify some bits in the register using I2C.

Driver version

- #define [FSL_WM8960_DRIVER_VERSION](#) ([MAKE_VERSION](#)(2, 2, 0))
CLOCK driver version 2.2.0.

26.4.2 Data Structure Documentation

26.4.2.1 struct [wm8960_audio_format_t](#)

Data Fields

- [uint32_t mclk_HZ](#)
master clock frequency
- [uint32_t sampleRate](#)
sample rate
- [uint32_t bitWidth](#)
bit width

26.4.2.2 struct wm8960_master_sysclk_config_t

Data Fields

- [wm8960_sysclk_source_t](#) sysclkSource
sysclk source
- [uint32_t](#) sysclkFreq
PLL output frequency value.

26.4.2.3 struct wm8960_config_t

Data Fields

- [wm8960_route_t](#) route
Audio data route.
- [wm8960_protocol_t](#) bus
Audio transfer protocol.
- [wm8960_audio_format_t](#) format
Audio format.
- [bool](#) master_slave
Master or slave.
- [wm8960_master_sysclk_config_t](#) masterClock
master clock configurations
- [bool](#) enableSpeaker
True means enable class D speaker as output, false means no.
- [wm8960_input_t](#) leftInputSource
Left input source for WM8960.
- [wm8960_input_t](#) rightInputSource
Right input source for wm8960.
- [wm8960_play_source_t](#) playSource
play source
- [uint8_t](#) slaveAddress
wm8960 device address
- [codec_i2c_config_t](#) i2cConfig
i2c configuration

Field Documentation

(1) [wm8960_route_t](#) wm8960_config_t::route

(2) [bool](#) wm8960_config_t::master_slave

26.4.2.4 struct wm8960_handle_t

Data Fields

- [const](#) [wm8960_config_t](#) * config
wm8904 config pointer
- [uint8_t](#) i2cHandle [WM8960_I2C_HANDLER_SIZE]
i2c handle

26.4.3 Macro Definition Documentation

26.4.3.1 **#define WM8960_LINVOL 0x0U**

26.4.3.2 **#define WM8960_I2C_ADDR 0x1A**

26.4.4 Enumeration Type Documentation

26.4.4.1 enum wm8960_module_t

Enumerator

kWM8960_ModuleADC ADC module in WM8960.

kWM8960_ModuleDAC DAC module in WM8960.

kWM8960_ModuleVREF VREF module.

kWM8960_ModuleHP Headphone.

kWM8960_ModuleMICB Mic bias.

kWM8960_ModuleMIC Input Mic.

kWM8960_ModuleLineIn Analog in PGA.

kWM8960_ModuleLineOut Line out module.

kWM8960_ModuleSpeaker Speaker module.

kWM8960_ModuleOMIX Output mixer.

26.4.4.2 anonymous enum

Enumerator

kWM8960_HeadphoneLeft wm8960 headphone left channel

kWM8960_HeadphoneRight wm8960 headphone right channel

kWM8960_SpeakerLeft wm8960 speaker left channel

kWM8960_SpeakerRight wm8960 speaker right channel

26.4.4.3 enum wm8960_play_source_t

Enumerator

kWM8960_PlaySourcePGA wm8960 play source PGA

kWM8960_PlaySourceInput wm8960 play source Input

kWM8960_PlaySourceDAC wm8960 play source DAC

26.4.4.4 enum wm8960_route_t

Only provide some typical data route, not all route listed. Note: Users cannot combine any routes, once a new route is set, the previous one would be replaced.

Enumerator

kWM8960_RouteBypass LINEIN->Headphone.
kWM8960_RoutePlayback I2SIN->DAC->Headphone.
kWM8960_RoutePlaybackandRecord I2SIN->DAC->Headphone, LINEIN->ADC->I2SOUT.
kWM8960_RouteRecord LINEIN->ADC->I2SOUT.

26.4.4.5 enum wm8960_protocol_t

WM8960 only supports I2S format and PCM format.

Enumerator

kWM8960_BusI2S I2S type.
kWM8960_BusLeftJustified Left justified mode.
kWM8960_BusRightJustified Right justified mode.
kWM8960_BusPCMA PCM A mode.
kWM8960_BusPCMB PCM B mode.

26.4.4.6 enum wm8960_input_t

Enumerator

kWM8960_InputClosed Input device is closed.
kWM8960_InputSingleEndedMic Input as single ended mic, only use L/RINPUT1.
kWM8960_InputDifferentialMicInput2 Input as differential mic, use L/RINPUT1 and L/RINPUT2.
kWM8960_InputDifferentialMicInput3 Input as differential mic, use L/RINPUT1 and L/RINPUT3.
kWM8960_InputLineINPUT2 Input as line input, only use L/RINPUT2.
kWM8960_InputLineINPUT3 Input as line input, only use L/RINPUT3.

26.4.4.7 anonymous enum

Enumerator

kWM8960_AudioSampleRate8KHz Sample rate 8000 Hz.
kWM8960_AudioSampleRate11025Hz Sample rate 11025 Hz.
kWM8960_AudioSampleRate12KHz Sample rate 12000 Hz.
kWM8960_AudioSampleRate16KHz Sample rate 16000 Hz.
kWM8960_AudioSampleRate22050Hz Sample rate 22050 Hz.
kWM8960_AudioSampleRate24KHz Sample rate 24000 Hz.
kWM8960_AudioSampleRate32KHz Sample rate 32000 Hz.
kWM8960_AudioSampleRate44100Hz Sample rate 44100 Hz.
kWM8960_AudioSampleRate48KHz Sample rate 48000 Hz.

kWM8960_AudioSampleRate96KHz Sample rate 96000 Hz.
kWM8960_AudioSampleRate192KHz Sample rate 192000 Hz.
kWM8960_AudioSampleRate384KHz Sample rate 384000 Hz.

26.4.4.8 anonymous enum

Enumerator

kWM8960_AudioBitWidth16bit audio bit width 16
kWM8960_AudioBitWidth20bit audio bit width 20
kWM8960_AudioBitWidth24bit audio bit width 24
kWM8960_AudioBitWidth32bit audio bit width 32

26.4.4.9 enum wm8960_sysclk_source_t

Enumerator

kWM8960_SysClkSourceMclk sysclk source from external MCLK
kWM8960_SysClkSourceInternalPLL sysclk source from internal PLL

26.4.5 Function Documentation

26.4.5.1 status_t WM8960_Init (wm8960_handle_t * *handle*, const wm8960_config_t * *config*)

The second parameter is NULL to WM8960 in this version. If users want to change the settings, they have to use wm8960_write_reg() or wm8960_modify_reg() to set the register value of WM8960. Note: If the codec_config is NULL, it would initialize WM8960 using default settings. The default setting: codec_config->route = kWM8960_RoutePlaybackandRecord codec_config->bus = kWM8960_BusI2S codec_config->master = slave

Parameters

<i>handle</i>	WM8960 handle structure.
<i>config</i>	WM8960 configuration structure.

26.4.5.2 status_t WM8960_Deinit (wm8960_handle_t * *handle*)

This function close all modules in WM8960 to save power.

Parameters

<i>handle</i>	WM8960 handle structure pointer.
---------------	----------------------------------

26.4.5.3 **status_t WM8960_SetDataRoute (wm8960_handle_t * *handle*, wm8960_route_t *route*)**

This function would set the data route according to route. The route cannot be combined, as all route would enable different modules. Note: If a new route is set, the previous route would not work.

Parameters

<i>handle</i>	WM8960 handle structure.
<i>route</i>	Audio data route in WM8960.

26.4.5.4 **status_t WM8960_SetLeftInput (wm8960_handle_t * *handle*, wm8960_input_t *input*)**

Parameters

<i>handle</i>	WM8960 handle structure.
<i>input</i>	Audio input source.

26.4.5.5 **status_t WM8960_SetRightInput (wm8960_handle_t * *handle*, wm8960_input_t *input*)**

Parameters

<i>handle</i>	WM8960 handle structure.
<i>input</i>	Audio input source.

26.4.5.6 **status_t WM8960_SetProtocol (wm8960_handle_t * *handle*, wm8960_protocol_t *protocol*)**

WM8960 only supports I2S, left justified, right justified, PCM A, PCM B format.

Parameters

<i>handle</i>	WM8960 handle structure.
<i>protocol</i>	Audio data transfer protocol.

26.4.5.7 void WM8960_SetMasterSlave (wm8960_handle_t * *handle*, bool *master*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>master</i>	1 represent master, 0 represent slave.

26.4.5.8 status_t WM8960_SetVolume (wm8960_handle_t * *handle*, wm8960_module_t *module*, uint32_t *volume*)

This function would set the volume of WM8960 modules. Uses need to appoint the module. The function assume that left channel and right channel has the same volume.

Module:kWM8960_ModuleADC, volume range value: 0 is mute, 1-255 is -97db to 30db Module:kWM8960_ModuleDAC, volume range value: 0 is mute, 1-255 is -127db to 0db Module:kWM8960_ModuleHP, volume range value: 0 - 2F is mute, 0x30 - 0x7F is -73db to 6db Module:kWM8960_ModuleLineIn, volume range value: 0 - 0x3F is -17.25db to 30db Module:kWM8960_ModuleSpeaker, volume range value: 0 - 2F is mute, 0x30 - 0x7F is -73db to 6db

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Module to set volume, it can be ADC, DAC, Headphone and so on.
<i>volume</i>	Volume value need to be set.

26.4.5.9 uint32_t WM8960_GetVolume (wm8960_handle_t * *handle*, wm8960_module_t *module*)

This function gets the volume of WM8960 modules. Uses need to appoint the module. The function assume that left channel and right channel has the same volume.

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Module to set volume, it can be ADC, DAC, Headphone and so on.

Returns

Volume value of the module.

26.4.5.10 **status_t WM8960_SetMute (wm8960_handle_t * *handle*, wm8960_module_t *module*, bool *isEnabled*)**

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Modules need to be mute.
<i>isEnabled</i>	Mute or unmute, 1 represent mute.

26.4.5.11 **status_t WM8960_SetModule (wm8960_handle_t * *handle*, wm8960_module_t *module*, bool *isEnabled*)**

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Module expected to enable.
<i>isEnabled</i>	Enable or disable moudles.

26.4.5.12 **status_t WM8960_SetPlay (wm8960_handle_t * *handle*, uint32_t *playSource*)**

Parameters

<i>handle</i>	WM8960 handle structure.
<i>playSource</i>	play source , can be a value combine of kWM8960_ModuleHeadphoneSourcePGA, kWM8960_ModuleHeadphoneSourceDAC, kWM8960_ModulePlaySourceInput, kWM8960_ModulePlayMonoRight, kWM8960_ModulePlayMonoLeft.

Returns

kStatus_WM8904_Success if successful, different code otherwise..

26.4.5.13 `status_t WM8960_ConfigDataFormat (wm8960_handle_t * handle, uint32_t sysclk, uint32_t sample_rate, uint32_t bits)`

This function would configure the registers about the sample rate, bit depths.

Parameters

<i>handle</i>	WM8960 handle structure pointer.
<i>sysclk</i>	system clock of the codec which can be generated by MCLK or PLL output.
<i>sample_rate</i>	Sample rate of audio file running in WM8960. WM8960 now supports 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k and 96k sample rate.
<i>bits</i>	Bit depth of audio file (WM8960 only supports 16bit, 20bit, 24bit and 32 bit in HW).

26.4.5.14 `status_t WM8960_SetJackDetect (wm8960_handle_t * handle, bool isEnabled)`

Parameters

<i>handle</i>	WM8960 handle structure.
<i>isEnabled</i>	Enable or disable moudles.

26.4.5.15 `status_t WM8960_WriteReg (wm8960_handle_t * handle, uint8_t reg, uint16_t val)`

Parameters

<i>handle</i>	WM8960 handle structure.
<i>reg</i>	The register address in WM8960.
<i>val</i>	Value needs to write into the register.

26.4.5.16 `status_t WM8960_ReadReg (uint8_t reg, uint16_t * val)`

Parameters

<i>reg</i>	The register address in WM8960.
<i>val</i>	Value written to.

26.4.5.17 `status_t WM8960_ModifyReg (wm8960_handle_t * handle, uint8_t reg, uint16_t mask, uint16_t val)`

Parameters

<i>handle</i>	WM8960 handle structure.
<i>reg</i>	The register address in WM8960.
<i>mask</i>	The mask code for the bits want to write. The bit you want to write should be 0.
<i>val</i>	Value needs to write into the register.

26.4.6 WM8960 Adapter

26.4.6.1 Overview

The wm8960 adapter provides a codec unify control interface.

Macros

- #define `HAL_CODEC_WM8960_HANDLER_SIZE` (`WM8960_I2C_HANDLER_SIZE` + 4)
codec handler size

Functions

- `status_t HAL_CODEC_WM8960_Init` (void *handle, void *config)
Codec initialization.
- `status_t HAL_CODEC_WM8960_Deinit` (void *handle)
Codec de-initialization.
- `status_t HAL_CODEC_WM8960_SetFormat` (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)
set audio data format.
- `status_t HAL_CODEC_WM8960_SetVolume` (void *handle, uint32_t playChannel, uint32_t volume)
set audio codec module volume.
- `status_t HAL_CODEC_WM8960_SetMute` (void *handle, uint32_t playChannel, bool isMute)
set audio codec module mute.
- `status_t HAL_CODEC_WM8960_SetPower` (void *handle, uint32_t module, bool powerOn)
set audio codec module power.
- `status_t HAL_CODEC_WM8960_SetRecord` (void *handle, uint32_t recordSource)
codec set record source.
- `status_t HAL_CODEC_WM8960_SetRecordChannel` (void *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)
codec set record channel.
- `status_t HAL_CODEC_WM8960_SetPlay` (void *handle, uint32_t playSource)
codec set play source.
- `status_t HAL_CODEC_WM8960_ModuleControl` (void *handle, uint32_t cmd, uint32_t data)
codec module control.
- static `status_t HAL_CODEC_Init` (void *handle, void *config)
Codec initialization.
- static `status_t HAL_CODEC_Deinit` (void *handle)
Codec de-initialization.
- static `status_t HAL_CODEC_SetFormat` (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)
set audio data format.
- static `status_t HAL_CODEC_SetVolume` (void *handle, uint32_t playChannel, uint32_t volume)
set audio codec module volume.
- static `status_t HAL_CODEC_SetMute` (void *handle, uint32_t playChannel, bool isMute)
set audio codec module mute.
- static `status_t HAL_CODEC_SetPower` (void *handle, uint32_t module, bool powerOn)

- *set audio codec module power.*
static [status_t HAL_CODEC_SetRecord](#) (void *handle, uint32_t recordSource)
- *codec set record source.*
static [status_t HAL_CODEC_SetRecordChannel](#) (void *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)
- *codec set record channel.*
static [status_t HAL_CODEC_SetPlay](#) (void *handle, uint32_t playSource)
- *codec set play source.*
static [status_t HAL_CODEC_ModuleControl](#) (void *handle, uint32_t cmd, uint32_t data)
- *codec module control.*

26.4.6.2 Function Documentation

26.4.6.2.1 status_t HAL_CODEC_WM8960_Init (void * *handle*, void * *config*)

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus_Success is success, else initial failed.

26.4.6.2.2 status_t HAL_CODEC_WM8960_Deinit (void * *handle*)

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus_Success is success, else de-initial failed.

26.4.6.2.3 status_t HAL_CODEC_WM8960_SetFormat (void * *handle*, uint32_t *mclk*, uint32_t *sampleRate*, uint32_t *bitWidth*)

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus_Success is success, else configure failed.

26.4.6.2.4 status_t HAL_CODEC_WM8960_SetVolume (void * *handle*, uint32_t *playChannel*, uint32_t *volume*)

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus_Success is success, else configure failed.

26.4.6.2.5 status_t HAL_CODEC_WM8960_SetMute (void * *handle*, uint32_t *playChannel*, bool *isMute*)

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus_Success is success, else configure failed.

26.4.6.2.6 status_t HAL_CODEC_WM8960_SetPower (void * *handle*, uint32_t *module*, bool *powerOn*)

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus_Success is success, else configure failed.

26.4.6.2.7 status_t HAL_CODEC_WM8960_SetRecord (void * *handle*, uint32_t *recordSource*)

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus_Success is success, else configure failed.

26.4.6.2.8 status_t HAL_CODEC_WM8960_SetRecordChannel (void * *handle*, uint32_t *leftRecordChannel*, uint32_t *rightRecordChannel*)

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus_Success is success, else configure failed.

26.4.6.2.9 status_t HAL_CODEC_WM8960_SetPlay (void * *handle*, uint32_t *playSource*)

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of <code>_codec_play_source</code> .

Returns

`kStatus_Success` is success, else configure failed.

26.4.6.2.10 `status_t HAL_CODEC_WM8960_ModuleControl (void * handle, uint32_t cmd, uint32_t data)`

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference <code>_codec_module_ctrl_cmd</code> .
<i>data</i>	value to write, when cmd is <code>kCODEC_ModuleRecordSourceChannel</code> , the data should be a value combine of channel and source, please reference macro <code>CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN)</code> , reference codec specific driver for detail configurations.

Returns

`kStatus_Success` is success, else configure failed.

26.4.6.2.11 `static status_t HAL_CODEC_Init (void * handle, void * config) [inline], [static]`

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

`kStatus_Success` is success, else initial failed.

26.4.6.2.12 `static status_t HAL_CODEC_Deinit (void * handle) [inline], [static]`

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus_Success is success, else de-initial failed.

26.4.6.2.13 `static status_t HAL_CODEC_SetFormat (void * handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth) [inline], [static]`

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus_Success is success, else configure failed.

26.4.6.2.14 `static status_t HAL_CODEC_SetVolume (void * handle, uint32_t playChannel, uint32_t volume) [inline], [static]`

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus_Success is success, else configure failed.

26.4.6.2.15 `static status_t HAL_CODEC_SetMute (void * handle, uint32_t playChannel, bool isMute) [inline], [static]`

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of <code>_codec_play_channel</code> .
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus_Success is success, else configure failed.

26.4.6.2.16 `static status_t HAL_CODEC_SetPower (void * handle, uint32_t module, bool powerOn) [inline], [static]`

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus_Success is success, else configure failed.

26.4.6.2.17 `static status_t HAL_CODEC_SetRecord (void * handle, uint32_t recordSource) [inline], [static]`

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of <code>_codec_record_source</code> .

Returns

kStatus_Success is success, else configure failed.

26.4.6.2.18 `static status_t HAL_CODEC_SetRecordChannel (void * handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel) [inline], [static]`

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference <code>_codec_record_channel</code> , can be a value or combine value of member in <code>_codec_record_channel</code> .
<i>rightRecord-Channel</i>	audio codec record channel, reference <code>_codec_record_channel</code> , can be a value or combine of member in <code>_codec_record_channel</code> .

Returns

`kStatus_Success` is success, else configure failed.

26.4.6.2.19 `static status_t HAL_CODEC_SetPlay (void * handle, uint32_t playSource)`
[inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of <code>_codec_play_source</code> .

Returns

`kStatus_Success` is success, else configure failed.

26.4.6.2.20 `static status_t HAL_CODEC_ModuleControl (void * handle, uint32_t cmd, uint32_t data)`
[inline], [static]

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference <code>_codec_module_ctrl_cmd</code> .
<i>data</i>	value to write, when cmd is <code>kCODEC_ModuleRecordSourceChannel</code> , the data should be a value combine of channel and source, please reference macro <code>CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN)</code> , reference codec specific driver for detail configurations.

Returns

`kStatus_Success` is success, else configure failed.

Chapter 27

Serial Manager

27.1 Overview

This chapter describes the programming interface of the serial manager component.

The serial manager component provides a series of APIs to operate different serial port types. The port types it supports are UART, USB CDC and SWO.

Modules

- [Serial Port SWO](#)
- [Serial Port Uart](#)

Data Structures

- struct [serial_manager_config_t](#)
serial manager config structure [More...](#)
- struct [serial_manager_callback_message_t](#)
Callback message structure. [More...](#)

Macros

- #define [SERIAL_MANAGER_NON_BLOCKING_MODE](#) (0U)
Enable or disable serial manager non-blocking mode (1 - enable, 0 - disable)
- #define [SERIAL_MANAGER_RING_BUFFER_FLOWCONTROL](#) (0U)
Enable or ring buffer flow control (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_UART](#) (0U)
Enable or disable uart port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_UART_DMA](#) (0U)
Enable or disable uart dma port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_USBCDC](#) (0U)
Enable or disable USB CDC port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_SWO](#) (0U)
Enable or disable SWO port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_VIRTUAL](#) (0U)
Enable or disable USB CDC virtual port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_RPMSG](#) (0U)
Enable or disable rPMSG port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_SPI_MASTER](#) (0U)
Enable or disable SPI Master port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_SPI_SLAVE](#) (0U)
Enable or disable SPI Slave port (1 - enable, 0 - disable)
- #define [SERIAL_MANAGER_TASK_HANDLE_TX](#) (0U)
Enable or disable SerialManager_Task() handle TX to prevent recursive calling.
- #define [SERIAL_MANAGER_WRITE_TIME_DELAY_DEFAULT_VALUE](#) (1U)

- Set the default delay time in ms used by `SerialManager_WriteTimeDelay()`.
• #define `SERIAL_MANAGER_READ_TIME_DELAY_DEFAULT_VALUE` (1U)
- Set the default delay time in ms used by `SerialManager_ReadTimeDelay()`.
• #define `SERIAL_MANAGER_TASK_HANDLE_RX_AVAILABLE_NOTIFY` (0U)
- Enable or disable `SerialManager_Task()` handle RX data available notify.
• #define `SERIAL_MANAGER_WRITE_HANDLE_SIZE` (4U)
- Set serial manager write handle size.
• #define `SERIAL_MANAGER_USE_COMMON_TASK` (0U)
- `SERIAL_PORT_UART_HANDLE_SIZE/SERIAL_PORT_USB_CDC_HANDLE_SIZE + serial manager dedicated size.`
• #define `SERIAL_MANAGER_HANDLE_SIZE` (`SERIAL_MANAGER_HANDLE_SIZE_TEMP + 12U`)
- Macro to determine whether use common task.
• #define `SERIAL_MANAGER_HANDLE_DEFINE`(name) `uint32_t name[((SERIAL_MANAGER_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]`
- Defines the serial manager handle.
• #define `SERIAL_MANAGER_WRITE_HANDLE_DEFINE`(name) `uint32_t name[((SERIAL_MANAGER_WRITE_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]`
- Defines the serial manager write handle.
• #define `SERIAL_MANAGER_READ_HANDLE_DEFINE`(name) `uint32_t name[((SERIAL_MANAGER_READ_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]`
- Defines the serial manager read handle.
• #define `SERIAL_MANAGER_TASK_PRIORITY` (2U)
- Macro to set serial manager task priority.
• #define `SERIAL_MANAGER_TASK_STACK_SIZE` (1000U)
- Macro to set serial manager task stack size.

Typedefs

- typedef void * `serial_handle_t`
The handle of the serial manager module.
- typedef void * `serial_write_handle_t`
The write handle of the serial manager module.
- typedef void * `serial_read_handle_t`
The read handle of the serial manager module.
- typedef void(* `serial_manager_callback_t`)(void *callbackParam, `serial_manager_callback_message_t` *message, `serial_manager_status_t` status)
callback function

Enumerations

- enum `serial_port_type_t` {
`kSerialPort_Uart` = 1U,
`kSerialPort_UsbCdc`,
`kSerialPort_Swo`,
`kSerialPort_Virtual`,
`kSerialPort_Rpmsg`,
`kSerialPort_UartDma`,
`kSerialPort_SpiMaster`,
`kSerialPort_SpiSlave`,
`kSerialPort_None` }
serial port type
- enum `serial_manager_type_t` {
`kSerialManager_NonBlocking` = 0x0U,
`kSerialManager_Blocking` = 0x8F41U }
serial manager type
- enum `serial_manager_status_t` {
`kStatus_SerialManager_Success` = `kStatus_Success`,
`kStatus_SerialManager_Error` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 1)`,
`kStatus_SerialManager_Busy` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 2)`,
`kStatus_SerialManager_Notify` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 3)`,
`kStatus_SerialManager_Canceled`,
`kStatus_SerialManager_HandleConflict` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 5)`,
`kStatus_SerialManager_RingBufferOverflow`,
`kStatus_SerialManager_NotConnected` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 7)` }
serial manager error code

Functions

- `serial_manager_status_t SerialManager_Init (serial_handle_t serialHandle, const serial_manager_config_t *config)`
Initializes a serial manager module with the serial manager handle and the user configuration structure.
- `serial_manager_status_t SerialManager_Deinit (serial_handle_t serialHandle)`
De-initializes the serial manager module instance.
- `serial_manager_status_t SerialManager_OpenWriteHandle (serial_handle_t serialHandle, serial_write_handle_t writeHandle)`
Opens a writing handle for the serial manager module.
- `serial_manager_status_t SerialManager_CloseWriteHandle (serial_write_handle_t writeHandle)`
Closes a writing handle for the serial manager module.
- `serial_manager_status_t SerialManager_OpenReadHandle (serial_handle_t serialHandle, serial_read_handle_t readHandle)`
Opens a reading handle for the serial manager module.
- `serial_manager_status_t SerialManager_CloseReadHandle (serial_read_handle_t readHandle)`
Closes a reading for the serial manager module.

- `serial_manager_status_t` `SerialManager_WriteBlocking` (`serial_write_handle_t` writeHandle, `uint8_t` *buffer, `uint32_t` length)
Transmits data with the blocking mode.
- `serial_manager_status_t` `SerialManager_ReadBlocking` (`serial_read_handle_t` readHandle, `uint8_t` *buffer, `uint32_t` length)
Reads data with the blocking mode.
- `serial_manager_status_t` `SerialManager_EnterLowpower` (`serial_handle_t` serialHandle)
Prepares to enter low power consumption.
- `serial_manager_status_t` `SerialManager_ExitLowpower` (`serial_handle_t` serialHandle)
Restores from low power consumption.
- static bool `SerialManager_needPollingIsr` (void)
Check if need polling ISR.

27.2 Data Structure Documentation

27.2.1 struct serial_manager_config_t

Data Fields

- `uint8_t` * `ringBuffer`
Ring buffer address, it is used to buffer data received by the hardware.
- `uint32_t` `ringBufferSize`
The size of the ring buffer.
- `serial_port_type_t` type
Serial port type.
- `serial_manager_type_t` blockType
Serial manager port type.
- void * `portConfig`
Serial port configuration.

Field Documentation

(1) `uint8_t* serial_manager_config_t::ringBuffer`

Besides, the memory space cannot be free during the lifetime of the serial manager module.

27.2.2 struct serial_manager_callback_message_t

Data Fields

- `uint8_t` * `buffer`
Transferred buffer.
- `uint32_t` `length`
Transferred data length.

27.3 Macro Definition Documentation

27.3.1 #define SERIAL_MANAGER_WRITE_TIME_DELAY_DEFAULT_VALUE (1U)

27.3.2 #define SERIAL_MANAGER_READ_TIME_DELAY_DEFAULT_VALUE (1U)

27.3.3 #define SERIAL_MANAGER_USE_COMMON_TASK (0U)

Macro to determine whether use common task.

27.3.4 #define SERIAL_MANAGER_HANDLE_SIZE (SERIAL_MANAGER_HANDLE_SIZE_TEMP + 12U)

Definition of serial manager handle size.

**27.3.5 #define SERIAL_MANAGER_HANDLE_DEFINE(*name*) uint32_t
name[(((SERIAL_MANAGER_HANDLE_SIZE + sizeof(uint32_t) - 1U) /
sizeof(uint32_t)))]**

This macro is used to define a 4 byte aligned serial manager handle. Then use "(serial_handle_t)name" to get the serial manager handle.

The macro should be global and could be optional. You could also define serial manager handle by yourself.

This is an example,

```
* SERIAL_MANAGER_HANDLE_DEFINE(serialManagerHandle);
*
```

Parameters

<i>name</i>	The name string of the serial manager handle.
-------------	---

**27.3.6 #define SERIAL_MANAGER_WRITE_HANDLE_DEFINE(*name*) uint32_t
name[(((SERIAL_MANAGER_WRITE_HANDLE_SIZE + sizeof(uint32_t) -
1U) / sizeof(uint32_t)))]**

This macro is used to define a 4 byte aligned serial manager write handle. Then use "(serial_write_handle_t)name" to get the serial manager write handle.

The macro should be global and could be optional. You could also define serial manager write handle by yourself.

This is an example,

```
* SERIAL_MANAGER_WRITE_HANDLE_DEFINE(serialManagerwriteHandle);
*
```

Parameters

<i>name</i>	The name string of the serial manager write handle.
-------------	---

**27.3.7 #define SERIAL_MANAGER_READ_HANDLE_DEFINE(*name*) uint32_t
name[(((SERIAL_MANAGER_READ_HANDLE_SIZE + sizeof(uint32_t) - 1U) /
sizeof(uint32_t))]**

This macro is used to define a 4 byte aligned serial manager read handle. Then use "(serial_read_handle-
_t)name" to get the serial manager read handle.

The macro should be global and could be optional. You could also define serial manager read handle by
yourself.

This is an example,

```
* SERIAL_MANAGER_READ_HANDLE_DEFINE(serialManagerReadHandle);
*
```

Parameters

<i>name</i>	The name string of the serial manager read handle.
-------------	--

27.3.8 #define SERIAL_MANAGER_TASK_PRIORITY (2U)

27.3.9 #define SERIAL_MANAGER_TASK_STACK_SIZE (1000U)

27.4 Enumeration Type Documentation

27.4.1 enum serial_port_type_t

Enumerator

kSerialPort_Uart Serial port UART.
kSerialPort_UsbCdc Serial port USB CDC.
kSerialPort_Swo Serial port SWO.
kSerialPort_Virtual Serial port Virtual.
kSerialPort_Rpmsg Serial port RPMSG.
kSerialPort_UartDma Serial port UART DMA.
kSerialPort_SpiMaster Serial port SPIMASTER.

kSerialPort_SpiSlave Serial port SPISLAVE.

kSerialPort_None Serial port is none.

27.4.2 enum serial_manager_type_t

Enumerator

kSerialManager_NonBlocking None blocking handle.

kSerialManager_Blocking Blocking handle.

27.4.3 enum serial_manager_status_t

Enumerator

kStatus_SerialManager_Success Success.

kStatus_SerialManager_Error Failed.

kStatus_SerialManager_Busy Busy.

kStatus_SerialManager_Notify Ring buffer is not empty.

kStatus_SerialManager_Canceled the non-blocking request is canceled

kStatus_SerialManager_HandleConflict The handle is opened.

kStatus_SerialManager_RingBufferOverflow The ring buffer is overflowed.

kStatus_SerialManager_NotConnected The host is not connected.

27.5 Function Documentation

27.5.1 serial_manager_status_t SerialManager_Init (serial_handle_t *serialHandle*, const serial_manager_config_t * *config*)

This function configures the Serial Manager module with user-defined settings. The user can configure the configuration structure. The parameter *serialHandle* is a pointer to point to a memory space of size [SERIAL_MANAGER_HANDLE_SIZE](#) allocated by the caller. The Serial Manager module supports three types of serial port, UART (includes UART, USART, LPSCI, LPUART, etc), USB CDC and swo. Please refer to [serial_port_type_t](#) for serial port setting. These three types can be set by using [serial_manager_config_t](#).

Example below shows how to use this API to configure the Serial Manager. For UART,

```
* #define SERIAL_MANAGER_RING_BUFFER_SIZE (256U)
* static SERIAL_MANAGER_HANDLE_DEFINE(s_serialHandle);
* static uint8_t s_ringBuffer[SERIAL_MANAGER_RING_BUFFER_SIZE];
*
* serial_manager_config_t config;
* serial_port_uart_config_t uartConfig;
* config.type = kSerialPort_Uart;
* config.ringBuffer = &s_ringBuffer[0];
* config.ringBufferSize = SERIAL_MANAGER_RING_BUFFER_SIZE;
* uartConfig.instance = 0;
```

```

*   uartConfig.clockRate = 24000000;
*   uartConfig.baudRate = 115200;
*   uartConfig.parityMode = kSerialManager_UartParityDisabled;
*   uartConfig.stopBitCount = kSerialManager_UartOneStopBit;
*   uartConfig.enableRx = 1;
*   uartConfig.enableTx = 1;
*   uartConfig.enableRxRTS = 0;
*   uartConfig.enableTxCTS = 0;
*   config.portConfig = &uartConfig;
*   SerialManager_Init((serial_handle_t)s_serialHandle, &config);
*

```

For USB CDC,

```

*   #define SERIAL_MANAGER_RING_BUFFER_SIZE (256U)
*   static SERIAL_MANAGER_HANDLE_DEFINE(s_serialHandle);
*   static uint8_t s_ringBuffer[SERIAL_MANAGER_RING_BUFFER_SIZE];
*
*   serial_manager_config_t config;
*   serial_port_usb_cdc_config_t usbCdcConfig;
*   config.type = kSerialPort_UsbCdc;
*   config.ringBuffer = &s_ringBuffer[0];
*   config.ringBufferSize = SERIAL_MANAGER_RING_BUFFER_SIZE;
*   usbCdcConfig.controllerIndex = kSerialManager_UsbControllerKhci0;
*   config.portConfig = &usbCdcConfig;
*   SerialManager_Init((serial_handle_t)s_serialHandle, &config);
*

```

Parameters

<i>serialHandle</i>	Pointer to point to a memory space of size SERIAL_MANAGER_HANDLE_SIZE allocated by the caller. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: SERIAL_MANAGER_HANDLE_DEFINE(serialHandle) ; or <code>uint32_t serialHandle[((SERIAL_MANAGER_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))];</code>
<i>config</i>	Pointer to user-defined configuration structure.

Return values

<i>kStatus_SerialManager_Error</i>	An error occurred.
<i>kStatus_SerialManager_Success</i>	The Serial Manager module initialization succeed.

27.5.2 serial_manager_status_t SerialManager_Deinit (serial_handle_t serialHandle)

This function de-initializes the serial manager module instance. If the opened writing or reading handle is not closed, the function will return `kStatus_SerialManager_Busy`.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer.
---------------------	---

Return values

<i>kStatus_SerialManager_Success</i>	The serial manager de-initialization succeed.
<i>kStatus_SerialManager_Busy</i>	Opened reading or writing handle is not closed.

27.5.3 serial_manager_status_t SerialManager_OpenWriteHandle (serial_handle_t serialHandle, serial_write_handle_t writeHandle)

This function Opens a writing handle for the serial manager module. If the serial manager needs to be used in different tasks, the task should open a dedicated write handle for itself by calling [SerialManager_OpenWriteHandle](#). Since there can only one buffer for transmission for the writing handle at the same time, multiple writing handles need to be opened when the multiple transmission is needed for a task.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices.
<i>writeHandle</i>	The serial manager module writing handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: SERIAL_MANAGER_WRITE_HANDLE_DEFINE(writeHandle) ; or <code>uint32_t writeHandle[((SERIAL_MANAGER_WRITE_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))];</code>

Return values

<i>kStatus_SerialManager_Error</i>	An error occurred.
<i>kStatus_SerialManager_HandleConflict</i>	The writing handle was opened.

<i>kStatus_SerialManager_Success</i>	The writing handle is opened.
--------------------------------------	-------------------------------

Example below shows how to use this API to write data. For task 1,

```
*  static SERIAL_MANAGER_WRITE_HANDLE_DEFINE(s_serialWriteHandle1);
*  static uint8_t s_nonBlockingWelcome1[] = "This is non-blocking writing log for task1!\r\n";
*  SerialManager_OpenWriteHandle((serial_handle_t)serialHandle
*      , (serial_write_handle_t)s_serialWriteHandle1);
*  SerialManager_InstallTxCallback((serial_write_handle_t)s_serialWriteHandle1,
*      Task1_SerialManagerTxCallback,
*      s_serialWriteHandle1);
*  SerialManager_WriteNonBlocking((serial_write_handle_t)s_serialWriteHandle1,
*      s_nonBlockingWelcome1,
*      sizeof(s_nonBlockingWelcome1) - 1U);
*
```

For task 2,

```
*  static SERIAL_MANAGER_WRITE_HANDLE_DEFINE(s_serialWriteHandle2);
*  static uint8_t s_nonBlockingWelcome2[] = "This is non-blocking writing log for task2!\r\n";
*  SerialManager_OpenWriteHandle((serial_handle_t)serialHandle
*      , (serial_write_handle_t)s_serialWriteHandle2);
*  SerialManager_InstallTxCallback((serial_write_handle_t)s_serialWriteHandle2,
*      Task2_SerialManagerTxCallback,
*      s_serialWriteHandle2);
*  SerialManager_WriteNonBlocking((serial_write_handle_t)s_serialWriteHandle2,
*      s_nonBlockingWelcome2,
*      sizeof(s_nonBlockingWelcome2) - 1U);
*
```

27.5.4 serial_manager_status_t SerialManager_CloseWriteHandle (serial_write_handle_t writeHandle)

This function Closes a writing handle for the serial manager module.

Parameters

<i>writeHandle</i>	The serial manager module writing handle pointer.
--------------------	---

Return values

<i>kStatus_SerialManager_Success</i>	The writing handle is closed.
--------------------------------------	-------------------------------

27.5.5 serial_manager_status_t SerialManager_OpenReadHandle (serial_handle_t serialHandle, serial_read_handle_t readHandle)

This function Opens a reading handle for the serial manager module. The reading handle can not be opened multiple at the same time. The error code `kStatus_SerialManager_Busy` would be returned when

the previous reading handle is not closed. And there can only be one buffer for receiving for the reading handle at the same time.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices.
<i>readHandle</i>	The serial manager module reading handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: SERIAL_MANAGER_READ_HANDLE_DEFINE(readHandle) ; or <code>uint32_t readHandle[(((SERIAL_MANAGER_READ_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t)))]</code> ;

Return values

<i>kStatus_SerialManager_Error</i>	An error occurred.
<i>kStatus_SerialManager_Success</i>	The reading handle is opened.
<i>kStatus_SerialManager_Busy</i>	Previous reading handle is not closed.

Example below shows how to use this API to read data.

```
*  static SERIAL_MANAGER_READ_HANDLE_DEFINE(s_serialReadHandle);
*  SerialManager_OpenReadHandle((serial_handle_t)serialHandle,
*    (serial_read_handle_t)s_serialReadHandle);
*  static uint8_t s_nonBlockingBuffer[64];
*  SerialManager_InstallRxCallback((serial_read_handle_t)s_serialReadHandle,
*    APP_SerialManagerRxCallback,
*    s_serialReadHandle);
*  SerialManager_ReadNonBlocking((serial_read_handle_t)s_serialReadHandle,
*    s_nonBlockingBuffer,
*    sizeof(s_nonBlockingBuffer));
*
```

27.5.6 serial_manager_status_t SerialManager_CloseReadHandle (serial_read_handle_t readHandle)

This function Closes a reading for the serial manager module.

Parameters

<i>readHandle</i>	The serial manager module reading handle pointer.
-------------------	---

Return values

<i>kStatus_SerialManager_Success</i>	The reading handle is closed.
--------------------------------------	-------------------------------

27.5.7 serial_manager_status_t SerialManager_WriteBlocking (serial_manager_write_handle_t writeHandle, uint8_t * buffer, uint32_t length)

This is a blocking function, which polls the sending queue, waits for the sending queue to be empty. This function sends data using an interrupt method. The interrupt of the hardware could not be disabled. And There can only one buffer for transmission for the writing handle at the same time.

Note

The function [SerialManager_WriteBlocking](#) and the function [SerialManager_WriteNonBlocking](#) cannot be used at the same time. And, the function [SerialManager_CancelWriting](#) cannot be used to abort the transmission of this function.

Parameters

<i>writeHandle</i>	The serial manager module handle pointer.
<i>buffer</i>	Start address of the data to write.
<i>length</i>	Length of the data to write.

Return values

<i>kStatus_SerialManager_Success</i>	Successfully sent all data.
<i>kStatus_SerialManager_Busy</i>	Previous transmission still not finished; data not all sent yet.
<i>kStatus_SerialManager_Error</i>	An error occurred.

27.5.8 serial_manager_status_t SerialManager_ReadBlocking (serial_manager_read_handle_t readHandle, uint8_t * buffer, uint32_t length)

This is a blocking function, which polls the receiving buffer, waits for the receiving buffer to be full. This function receives data using an interrupt method. The interrupt of the hardware could not be disabled. And There can only one buffer for receiving for the reading handle at the same time.

Note

The function [SerialManager_ReadBlocking](#) and the function `SerialManager_ReadNonBlocking` cannot be used at the same time. And, the function `SerialManager_CancelReading` cannot be used to abort the transmission of this function.

Parameters

<i>readHandle</i>	The serial manager module handle pointer.
<i>buffer</i>	Start address of the data to store the received data.
<i>length</i>	The length of the data to be received.

Return values

<i>kStatus_SerialManager_- Success</i>	Successfully received all data.
<i>kStatus_SerialManager_- Busy</i>	Previous transmission still not finished; data not all received yet.
<i>kStatus_SerialManager_- Error</i>	An error occurred.

27.5.9 serial_manager_status_t SerialManager_EnterLowpower (serial_handle_t serialHandle)

This function is used to prepare to enter low power consumption.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer.
---------------------	---

Return values

<i>kStatus_SerialManager_- Success</i>	Successful operation.
--	-----------------------

27.5.10 serial_manager_status_t SerialManager_ExitLowpower (serial_handle_t serialHandle)

This function is used to restore from low power consumption.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer.
---------------------	---

Return values

<i>kStatus_SerialManager_Success</i>	Successful operation.
--------------------------------------	-----------------------

27.5.11 static bool SerialManager_needPollingIsr (void) [inline], [static]

This function is used to check if need polling ISR.

Return values

<i>TRUE</i>	if need polling.
-------------	------------------

27.6 Serial Port Uart

27.6.1 Overview

Macros

- #define `SERIAL_PORT_UART_DMA_RECEIVE_DATA_LENGTH` (64U)
serial port uart handle size
- #define `SERIAL_USE_CONFIGURE_STRUCTURE` (0U)
Enable or disable the configure structure pointer.

Enumerations

- enum `serial_port_uart_parity_mode_t` {
 `kSerialManager_UartParityDisabled` = 0x0U,
 `kSerialManager_UartParityEven` = 0x2U,
 `kSerialManager_UartParityOdd` = 0x3U }
serial port uart parity mode
- enum `serial_port_uart_stop_bit_count_t` {
 `kSerialManager_UartOneStopBit` = 0U,
 `kSerialManager_UartTwoStopBit` = 1U }
serial port uart stop bit count

27.6.2 Enumeration Type Documentation

27.6.2.1 enum serial_port_uart_parity_mode_t

Enumerator

kSerialManager_UartParityDisabled Parity disabled.
kSerialManager_UartParityEven Parity even enabled.
kSerialManager_UartParityOdd Parity odd enabled.

27.6.2.2 enum serial_port_uart_stop_bit_count_t

Enumerator

kSerialManager_UartOneStopBit One stop bit.
kSerialManager_UartTwoStopBit Two stop bits.

27.7 Serial Port SWO

27.7.1 Overview

Data Structures

- struct [serial_port_swo_config_t](#)
serial port swo config struct [More...](#)

Macros

- #define [SERIAL_PORT_SWO_HANDLE_SIZE](#) (12U)
serial port swo handle size

Enumerations

- enum [serial_port_swo_protocol_t](#) {
 [kSerialManager_SwoProtocolManchester](#) = 1U,
 [kSerialManager_SwoProtocolNrz](#) = 2U }
serial port swo protocol

27.7.2 Data Structure Documentation

27.7.2.1 struct serial_port_swo_config_t

Data Fields

- uint32_t [clockRate](#)
clock rate
- uint32_t [baudRate](#)
baud rate
- uint32_t [port](#)
Port used to transfer data.
- [serial_port_swo_protocol_t](#) [protocol](#)
SWO protocol.

27.7.3 Enumeration Type Documentation

27.7.3.1 enum serial_port_swo_protocol_t

Enumerator

kSerialManager_SwoProtocolManchester SWO Manchester protocol.
kSerialManager_SwoProtocolNrz SWO UART/NRZ protocol.

27.7.4 CODEC Adapter

27.7.4.1 Overview

Enumerations

- enum {
[kCODEC_WM8904](#),
[kCODEC_WM8960](#),
[kCODEC_WM8524](#),
[kCODEC_SGTL5000](#),
[kCODEC_DA7212](#),
[kCODEC_CS42888](#),
[kCODEC_CS42448](#),
[kCODEC_AK4497](#),
[kCODEC_AK4458](#),
[kCODEC_TFA9XXX](#),
[kCODEC_TFA9896](#) }
codec type

27.7.4.2 Enumeration Type Documentation

27.7.4.2.1 anonymous enum

Enumerator

kCODEC_WM8904 wm8904
kCODEC_WM8960 wm8960
kCODEC_WM8524 wm8524
kCODEC_SGTL5000 sgtl5000
kCODEC_DA7212 da7212
kCODEC_CS42888 CS42888.
kCODEC_CS42448 CS42448.
kCODEC_AK4497 AK4497.
kCODEC_AK4458 ak4458
kCODEC_TFA9XXX tfa9xxx
kCODEC_TFA9896 tfa9896

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