Birla Institute of Technology and Science, Pilani

Work Integrated Learning Programmes Division
M. Tech. (Data Science and Engineering)
First Semester 2018 - 2019
Mid-Semester Examination (Makeup)

Course Number	: DSEABZG516/ DSEAHZG516/ DSEADZG516
Course Title	: Computer Organization & Software Systems
Type of Exam	: Closed Book
Weightage	: 30 %
Duration	: 90 minutes
Date of Exam	: 6/1/2019 Session: FN

Number of questions: 04
Number of Pages: 02

Instruction:

a) Read and follow all the instructions given on the cover page of the answer script.

b) **Answer the questions in the order in which they appear in the question paper.**

b) For problem based questions, show relevant calculations.

c) Assume missing data if any.

Q1 **Answer the following** **2 + 2 + 3 = 7M**

A Consider a computer system which has a CPU with a word length of 64 bits, 32 internal registers and an address bus of width 35 bits. The system's main memory is 1 GB.

i. What is the total memory occupied by the CPU internal register in Bytes?

ii. What modifications are needed to upgrade the main memory system to 32 GB?

B Implement the following using stack related addressing mode.

A+ B x C + D

C Which type of pipeline hazard results in Von-Neumann bottleneck? Is there a solution to overcome this problem? If yes, then explain the solution.

Q2 **Answer the following.** **2 + 1 + 4 = 7M**

A Consider a direct mapped cache with four cache lines. Suppose that the reference pattern of a program is such that it accesses the following sequence of blocks: 0, 4, 8, 0, 4, 4, 8, 2, 1. Compute the following :

i. To which cache line, block 5 maps to?

ii. What is the Hit ratio?

B Consider a system with cache, main memory and I/O device. Is it possible for the CPU to read or write to the cache, while I/O device is reading main memory? Justify your answer.

C Consider a machine with byte addressable main memory of 4 Mbytes and a direct mapped cache of 1024 lines. The main memory block size is 32 bytes. Answer the following questions by specifying clearly the formulae used:

i. What is the number of bits needed for representing a main memory address?
ii. What is the size of each cache line?
iii. Specify the number of bits needed for tag, line and word offset.
iv. To which cache line, the main memory address 33A9FFH is mapped to?

Q3 **Answer the following.** **4 + 4 = 8M**

A ~~Mr. Joel wants to configure a system with 15 external devices. He would like to use Interrupt driven data transfer scheme. To support the scheme he wishes to use 8259 interrupt controller. With a neat diagram, explain how 82C59A Interrupt Controller can be used to connect 15 external devices?~~

B State whether the following statements are **True** or **False** with proper justification. Answers without proper justification will not be given any marks.

i. A generic RISC instruction has a 6 bit operations code (OPCODE), a 5 bit source register 1 (Rs1), a 5 bit source register 2 (Rs2) and a 5 bit destination register (Rd), and an optional 11 bit field. The previous statement implies that the CPU has 32 general purpose registers and each is capable of storing 32 bits.
ii. CISC machine uses Harvard architecture, whereas RISC uses Stanford architecture.

Q4 **Answer the following.** **5 + 3 = 8M**

A Consider the following sequence of instructions:

I1: add R1, R0, #20 (R1← R0 + 20)
I2: mul R2, R3, #2 (R2← R3*2)
I3: and R4, R1, R2 (R4← R1 and R2)
I4: add R5, R4, R2 (R5← R4 + R2)

These instructions are executed in a computer that has a four stage pipeline (**F**etch, **D**ecode, **E**xecute, **W**rite). Assume that all stages for all instructions requires one cycle each, except the Execution stage of multiply instruction which requires two cycles. Draw a diagram to describe the operation being performed by each pipeline stage during each clock cycle. Show the stalls in the pipeline, if any.

B Consider a 5 stage pipeline with stages, taking 2, 1, 1.5, 2, 1 units of time and inter stage buffer takes 1 unit of time. What is the speed up and throughput of the pipeline for executing 100 tasks?