Birla Institute of Technology and Science, Pilani

Work Integrated Learning Programmes Division
M. Tech. (Data Science and Engineering)
First Semester 2018 - 2019
Comprehensive Examination (Makeup)

Course Number	: DSEABZG516/ DSEAHZG516/ DSEADZG516
Course Title	: Computer Organization & Software Systems
Type of Exam	: Open Book
Weightage	: 40 %
Duration	: 150 minutes
Date of Exam	: 7/4/2019 Session: FN

Number of questions: 05
Number of Pages: 04

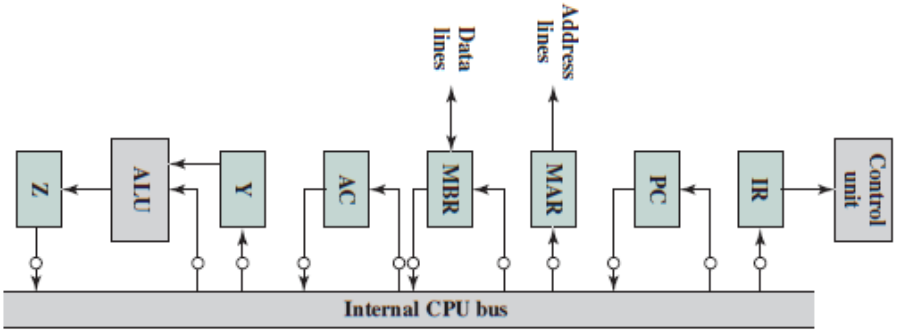
Instruction:

Start each answer from a fresh page.
All parts of a question should be answered consecutively.
Assume missing data if any.

Q1	**Answer the following.**		**8M**
	A	Consider two different implementations of machines, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 6 GHz and M2 has a clock rate of 3 GHz. Compiler "C1" is designed using an available instruction set. C1 instruction usage and the CPI for each instruction class on M1 and M2 is given in the following table: Class | CPI on M1 | CPI on M2 | C1 Usage A | 2 | 1 | 40% B | 3 | 2 | 40% C | 5 | 2 | 20% i. For C1 compiler, what is the average CPI of M1 and M2? ii. Using C1 compiler on both M1 and M2, how much faster is M1 than M2?	**2M**
	B	State whether the following statements are **True** or **False** with proper justification. Answers without proper justification will not be given any marks. i. DMA to main memory is given higher priority than CPU access to main memory. ii. Temporal locality of reference suggests the use of LRU (Least Recently Used) replacement policy for cache memory.	**2M**
	C	A byte addressable computer has on-chip data cache with eight lines (L0 to L7). Each cache line is capable of storing 4 bytes. The mapping function used is direct mapped. The following address sequence is generated by the CPU (hex notation) during the program execution : 212, 215, 236, 231, 2F5 i. Identify the main memory block number and line number to which each address corresponds to.	**4M**

		ii. Assume that the above pattern is repeated twice. What will be the final contents of L0 – L7 cache lines? (Indicate the contents of each line in terms of block number). iii. The access time of the cache is 5ns, and it has an 80 percent hit rate. The access time of the main memory is 100 ns. What is the average access time of the hierarchy?	
Q2		**Answer the following.**	**8M**

	A	i. A certain processor executes the following set of machine instructions sequentially.
		
		MOV R_0, # 0
		MOV R_1, 100(R_0)
		ADD R_1, 200(R_0)
		MOV 100(R_0), R_1
		
		Assuming that memory location 100 contains the value 35H, the memory location 200 contains the value A4H, R0 contains 10H and R1 contains 5H, what could be the final result?
		ii. If the same program is passed through simple 6 stage instruction pipeline containing FI, DI, CO, FO, EI, and WO stages, what could be the final result?
		iii. What is the speedup factor of the pipeline if the processor clock frequency is 1 MHz?
			3M

	B	A computer has 32-bit instructions and 12-bit addresses. Opcode field of the instruction has fixed number of bits. i. There are 245 two address instructions. How many one address instructions can be formulated? ii. Draw instruction format for one address instruction and two address instruction.	**2M**
	C	The figure shows the CPU with internal bus. Assume that propagation delay along the bus and through the ALU are 20 ns and 100 ns, respectively. The time required for a register to copy data from the bus is 10 ns. What is the time that must be allowed for i. transferring data from one register to another? ii. incrementing the program counter?  CPU with Internal Bus	**3M**
Q3		**Answer the following.**	**8M**
	A	The following program consists of 3 concurrent processes and 3 binary semaphores. The semaphores are initialized as S0 = 1, S1 = 0, S2 = 0.	**3M**

Process P0	Process P1	Process P2

While(true){
wait(S0);
print '0';
signal(S1);
signal (S2);
}
	Wait(S1);
	signal (S0);
		Wait(S2);
		signal (S0);

i. Assuming that the processes are scheduled as follows:
P1, P2, P0, P0, P2, P0
How many times will process P0 print '0'?

ii. What will be the values of S0, S1 and S2, at the end of execution of above sequence?

B Consider an operating system that uses a preemptive, priority based scheduling algorithm. The priorities, arrival times, and CPU and I/O burst times (CPU burst time is underlined) for four processes are given below. **5M**

Process	Arrival time	Priority	CPU – I/0 Burst	Finish time	Turnaround Time	Waiting Time
A	0	4	4+2+1			
B	3	2	3+2+4			
C	5	1	2+3+3			
D	8	3	2+4+3			

Lower numbers denote higher priorities. Assume that all I/O requests are for different devices. Note: Order of preference for process insertion at the ready queue in case of a tie: job queue process (newly arriving process, process that completed I/O, preempted process).

i. Draw the Gantt chart for the processes

ii. Compute finish time, turnaround time and waiting time. Present your answer in the table format shown above.

Q4 **Answer the following.** **8M**

A Consider the following sequence of addresses (represented in decimal): **2M**
0100, 0500, 1101, 1999, 3000, 3500, 1024, 2048
Assume 500 byte page. Find out the reference string representing page numbers.

B Following is the snapshot of the memory using Buddy system after allocating processes A, B and C. **3M**

A(624 B)		B(1025B)	C(3KB)	
1KB	1KB	2KB	4KB	4KB

Show the memory allocation of each of the following (provide a diagram for each step).
Free (B)
Allocate (D : 3KB)
Allocate (E : 512 B)
Allocate (F: 1KB)

C Consider a system with 8-bit virtual address, 10-bit physical address and a page size of 64 bytes. Answer the following questions: **3M**

i. How many pages are there in virtual memory?

ii. How many frames are there in physical memory?
iii. Consider a page table with the entries[2, 5, 1, 8]. What is the physical address for virtual address 241? Note that the address is in decimal number system.

Q5 **Answer the following.** **8M**

A **2M**

There are three processes (P1, P2, P3) currently running in the system. There are four resources (R1, R2, R3, R4) each having single instance. Following is the snapshot of current allocation/request.

1. P1 is using R3
2. P1 is requesting for R1 and R2
3. P2 is using R1
4. P2 is requesting for R4
5. P3 is using R4
6. P3 is requesting for R3

Model this state of the system using proper data structure and check whether deadlock is there in the system or not.

B **2M**

State whether the following statements are **True** or **False** with proper justification. Answers without proper justification will not be given any marks.

i. A system consists of a 32-bit physical address space and a 32-bit virtual address space. The logical address generated by the CPU is the same as the one generated by the MMU.
ii. Sequential access method is suitable for database files.

C **4M**

Consider the following snapshot of the system with four processes P0 to P3 and 3 resource types A (5 Instances), B (3Instances), and C (8 Instances).

	ALLOCATION				REQUEST			AVAILABLE		
Process	**A**	**B**	**C**		**A**	**B**	**C**	**A**	**B**	**C**
P0	**1**	**0**	**2**		**0**	**0**	**1**	**0**	**0**	**0**
P1	**2**	**1**	**1**		**1**	**0**	**2**			
P2	**1**	**0**	**3**		**0**	**0**	**0**			
P3	**1**	**2**	**2**		**3**	**3**	**0**			

Answer the following questions with reference to Deadlock Detection Algorithm.

i. Check whether the system is in deadlock or not.
ii. If the system is in safe state, then give safe sequence or else provide the process no(s) which is causing the deadlock.