Birla Institute of Technology & Science, Pilani
Work Integrated Learning Programmes Division
Second Semester 2019-2020
M.Tech (Data Science and Engineering)
Mid-Semester Exam (EC-2 Regular)

Course No.	: DSEIDZG516
Course Title	: Computer Organization and Software Systems
Nature of Exam	: Open Book
Weightage	: 30%
Duration	: 90 minutes
Date of Exam	: 28/06/2020 (FN), 10:00 am to 11:30 am

No. of Pages = 3
No. of Questions = 4

Note to Students:

1. **All parts of a question should be answered consecutively. Each answer should start from a fresh page.**
2. **Assumptions** made if any, should be stated clearly at the beginning of your answer.
3. For all problems **relevant steps** are to be shown.

Q1: Answer the following questions. **[8 MARKS]**

A. "Mybenchmark" is a performance benchmarking organization that does benchmarking of CPUs before they are released for commercial use. Their benchmarking programs consists of arithmetic operations apart from memory operations. They run in a controlled environment with prescribed configuration so that results can be analyzed and compared across CPUs. "Mybenchmark" business model is to sell their analysis to CPU manufacturers so that they can improve their designs.
In 2019, a new processor was designed with frequency of 5 GHz. The table below gives instruction frequencies as well as number of cycles the instructions take, for the different classes of instructions. It is assumed that the processor only executes one instruction at a time. This exercise is tuned to execute exactly 100 instructions. Following table summarizes the break-up:

Instruction Type	Purpose	Frequency	Cycles
Load & Store	Memory access instructions take higher number of cycles ; added to benchmark programs to simulate industry scenarios	40%	5 cycles
Arithmetic Instructions	Floating point and integer arithmetic instructions are predominantly used in business transactions and programs	40%	3 cycles
All others	These are instructions such as program control transfer	20%	4 cycles

This exercise of benchmarking looks at few critical parameters such as CPI, MIPS and cycle time, and the organization wants you to answer the following so that they can validate their results.

i. Calculate the CPI . [1]

CPI = (40*5)+(40*3)+(20*4)=200+120+80=400 Cycles/100 Instructions

therefore 4 cycles per instruction

ii. What is the "MIPS" processor speed for the benchmark in millions of instructions per second? [1]

MIPS = Clock rate/(CPI * 10^6)

The clock rate is 500MHz so...

MIPS = (5 * 10^9)/(4 * 10^6) = **1250**

iii. The hardware expert says that if you double the number of registers, the cycle time must be increased by 30%. What would the new clock speed be (in GHz)? [2]

Cycle Time = 1/(5 * 10^9) =2 *10^{-10}

The cycle time is then increased by 30%

$(2 * 10^{-10}) * .3 + 2 * 10^{-10} = 2.6 * 10^{-10}$

The new clock rate is=1/(2.6*10^-10) = 3.846 GHz

Marks Distribution: Cycle time : 1 Marks
Clock Rate : 1marks

B. About 2.5 quintillion bytes of data created each day at our current pace, but that pace is only accelerating with the growth of social media, and Internet of Things (IoT). The data gets stored in various storage devices and subsequently gets analyzed for business decisions. Magnetic disk drive continues to lead the market share. Size of data stored and access time continues to be a critical performance metrics of storage devices.
"Bgate" company which manufactures Magnetic Disk Drives seeks your help in evaluating critical performance metrics using the following inputs:
Magnetic Disc pack has 32 surfaces, 256 tracks per surface and 512 sectors per track. There are 512 bytes per sector.

i. What is the capacity of disk pack? [1]

Capacity of disk pack

= Total number of surfaces x Number of tracks per surface x Number of sectors per track x Number of bytes per sector

32 X 256 X 512 X 512 (2^5 X 2^8 X 2^9 X 2^9)

$= 2^{31}$ bytes

= 2 GB or 2.147 GB

ii. What is the number of bits required to address a sector? [1]

Total number of sectors

= Total number of surfaces x Number of tracks per surface x Number of sectors per track

= 32 x 256 X 512 sectors (2^5 X 2^8 X 2^9)

$= 2^{22}$ sectors

Thus, Number of bits required to address the sector = 22 bits

iii. If the disk is rotating at 60 RPS (revolutions per second), what is the data transfer rate? [2]

Number of rotations in one second = 60

Now, Data transfer rate

= Number of surfaces x Capacity of one track x Number of rotations in one second

= 32 X (512 X 512) X 60

$= 2^5 \times 2^9 \times 2^9 \times 60$ bytes/sec

$= 60 \times 2^{23}$ bytes/sec

= 480 MBps

2 marks

Q2 . Answer the following questions. **[8 MARKS]**

A. A computer program is developed to run the DBSCAN algorithm on a processor with L1 cache and main memory organization with hit ratio of 67%. The processor supports 64-bit address bus, an 8-bit

data bus and has a 256 KByte data cache memory with 4-way set associativity. The main memory is logically divided into a block size of 256 Bytes. Each cache line entry contains, in addition to address tag, 1 dirty bit.

i. What is the number of bits in the tag field of an address? [2]

Number of lines in the cache = 256 KB / 256 B = 2^10 = 1 K lines
4 way = 4 lines per set
Therefore Number of sets = 1K/ 4 = 256 sets = 2^8
Number of bits needed to address sets = 8 bits
Number bits needed to address a word in the block : 256 = 2^8 ➔ 8 bits
Tag bit = 64 – 8 -8 = 48 bits

Final answer is correct = 2 marks (need to look at the steps)
Final answer is wrong then 0.5 marks for each step (#lines , # sets, bits for block)

ii. If the associativity in the above problem, is changed to 8-way, do you see any performance gain and/ or drawback? Comment. [2]

There is a performance gain in terms number of HITS

Tag comparison circuit becomes complex

1 marks for each reason

B. Indian Meteorological Department's computer data scientists contemplating the preference of using LFU and FIFO replacement algorithms. The associative cache is having 4 lines and the address block generated by the CPU is 2,3,6,4,3,2,5,7,6,5.
Help these Data scientists to choose the better of the two replacement algorithms. Justify your selection with the help of the following table. [2+2 = 4]

Note: In LFU, in case of tie between cache lines for replacement, select the line which has been there for longer time in the cache.

Solution: FIFO is better as it results in hit rate of 4/10 compared to LFU whose hit rate is 2/10

LFU HR.=2/10

Time	0	1	2	3	4	5	6	7	8	9
Addr	2	3	6	4	3	2	5	7	6	5
L0	2,1	2,1	2,1	2,1	2,1	2,2	2,2	2,2	2,2	2,2
L1	-	3,1	3,1	3,1	3,2	3,2	3,2	3,2	3,2	3,2
L2	-	-	6,1	6,1	6,1	6,1 *	5,1	5,1*	6,1	6,1
L3	-	-	-	4,1	4,1	4,1	4,1*	7,1	7,1	5,1
Hit/Miss	M	M	M	M	H	H	M	M	M	M

FIFO HR=4/10

Time	0	1	2	3	4	5	6	7	8	9
Addr	2	3	6	4	3	2	5	7	6	5
L0	2,0	2,0	2,0	2,0	2,0	2,0	5,6	5,6	5,6	5,6
L1	-	3,1	3,1	3,1	3,1	3,1	3,1	7,7	7,7	7,7
L2	-	-	6,2	6,2	6,2	6,2	6,2	6,2	6,2	6,2
L3	-	-	-	4,3	4,3	4,3	4,3	4,3	4,3	4,3
Hit/Miss	M	M	M	M	H	H	M	M	H	H

2 marks for correct last line
Up to 7th line correct 1.5 marks
Up to 5th line is correct 1.0 marks
Up to 3rd line is correct 0.5 marks

Q3. Answer the following Questions. [7 Marks]

A. A RISC based CPU is to be designed to have 32 opcodes, source and destination operands referring to 64 registers, and a displacement of value such as 2ABCH. Specify the instruction format mentioning the various fields and bits required by them. [2]

ANS:

Opcode [5 bits]	Source operand [6bits]	Destination operand [6 bits]	Displacement [16 Bits]

0.5 marks for each

B. Consider a program with 50 instructions to be executed by a processor with two pipeline configurations Mode 1 and Mode 2.
Mode 1 pipeline configuration consists of 5 stages: Instruction Fetch(IF), Instruction Decode(ID), Fetch Operand(FO), Execution(EX), and Write Back(WB) with 12, 10, 25, 20 and 8 nano seconds (ns) respectively. The inter-stage delay between each stage is 3 ns.
Mode 2 pipeline configuration is similar to that of Mode1 except the FO stage is divided into FO1, FO2, FO3 with time duration 10ns, 8 ns, 7ns respectively and 3ns delay between stages.

i. Find out the time taken by the program using Mode1 pipeline configuration [1.5]

Ans: T = max {12,10,25,20 and 8 } + 3
= 28 ns
Time taken by the mode 1 pipeline = (K+(n-1)) T
= (5+(50-1)) 28
=1512ns

0.5 marks for clock
1 marks for second part

ii. Find out the time taken by the program using Mode2 pipeline configuration [1.5]

T = max {12,10,10,8, 7, 20 and 8 } + 3
= 23ns
Time taken by the mode 2 pipeline = (K+(n-1)) T
= (7+(50-1)) 23
=1288ns

0.5 marks for clock
1 marks for second part

iii. Find out and comment on the speedup achieved by mode2 configuration over mode1configuration. [2]

Speedup = Tmode1/Tmode2

= 1512/1288ns = 1.17

Since in mode 2 FO stage is further divided results clock time reduction. Hence performance gain

1 marks for calculation.

1 marks for reason

Q4: Answer the following questions. **[7 Marks]**

The single cycle implementation of MIPS is as shown below. Answer the following questions with reference to "beq $S1, $S2, 8H" instruction. Assume that the contents of the registers S1 = 10 H, S2 = 10H, and PC = 16H, pointing to the instruction under consideration.

i. What is the addressing mode of the instruction? [1]

Ans: Relative Addressing mode

ii. Which part of the instruction format, address of S1 and S2 are stored? [1]

Ans: rs stores address of S1 and **rt** stores address of S2

iii. What is the status of different control signals to execute the instruction? Answer should be presented in the form of table given below. Indicate **Don't care** as X. [3.5]

Signal	Status
RegDst	X
Branch	1
MemRead	0
MemtoReg	X
ALUOp	01
ALUSrc	0
RegWrite	0

0.5 marks each

iv. What is the value of Zero Flag ? [0.5]

Value of Zero Flag : 1

v. What is the value of PC, after the execution of the instruction? [1]

Ans: 3A