3.8 A BJT-Based CMOS Temperature Sensor Achieving an Inaccuracy of ±0.45°C (3σ) from -50°C to 180°C and a Resolution-FoM of 7.2pJ·K² at 150°C

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Integrated temperature sensors for industrial digital transformation such as turbine and bearing monitoring should exhibit low power consumption and high energy efficiency with moderate inaccuracy over a wide sensing range (e.g., >150°C) to achieve autonomous operation under a limited energy budget. Even though resistor-based temperature sensors can achieve a superior sub-pJ·K² resolution-FoM [1], they typically require a 2-point trim together with a high-order nonlinearity correction (6th-order in [2]), inevitably burdening the processing cost. In contrast, BJT-based temperature sensors in bulk or SOI CMOS can achieve accurate sensing at high temperature with only 1-point trim and simple digital processing [3,4]. However, they can suffer from a degraded energy efficiency at high temperature for ensuring the sensing resolution and/or accuracy (e.g., ~3× increase in bias current for improving the 3σ-inaccuracy from ±0.6°C to ±0.4°C in [3]). This paper describes a BJT-based temperature sensor capable of wide-range operation from -50°C to 180°C. By employing a nonlinear readout and the proposed subranging, double-sampling, and constant-biasing techniques, this work achieves a high resolution-FoM over the entire sensing range (9.7pJ·K² at room temperature and 7.2pJ·K² at 150°C), corresponding to a 6-to-10× improvement when compared with prior BJT-based wide-range designs [3,4]. We further employ dynamic error-correction [5] and switch-leakage compensation to effectively suppress the mismatch- and leakage-induced errors, resulting in a high precision of ±0.45°C (3σ).

Figure 3.8.1 depicts the system diagram of the proposed CMOS temperature sensor, consisting of a BJT-core, a switched-capacitor (SC) ΔΣ-ADC, and a digital controller. Instead of using a proportional-to-absolute-temperature (PTAT) current that can double the sensor's power consumption from -50°C to 180°C, we only devote the beta-cancellation circuit for BJT biasing, while employing a temperature-compensated peaking current source (total 0.26μA) for system use. The dominant noise source from the beta-cancellation circuit, which mostly appears at the $V_{BE0,1}$ output as a common-mode noise, can only be suppressed during ΔV_{BE} sampling but not when sampling V_{BE0}. Consequently, unlike the readout schemes in [3,6], we employ a nonlinear readout scheme with $X_T=k\cdot\Delta V_{BE}/V_{BE0}$, which effectively reduces the number of V_{BE0} samples per conversion while relaxing the resolution requirement at high temperature. Specifically, for a target resolution of 15m°C, this nonlinear readout should achieve a 16-bit effective noise level (referenced to V_{BE0}) at -50°C, which reduces to only 13.5-bit at 180°C. To optimize the energy efficiency over the entire sensing range, this work performs subranging using k_1=6 at low temperature (low-T) and k_2=3 at high temperature (high-T), with consideration of both the ADC's maximum stable amplitude (<0.8) and a transition temperature of T_r~100°C. As a result, it can relax the required ADC input-referred noise power by a factor of 4 and 2.5 in the two subranges, respectively. Using two gains ($k_{1,2}$) does not affect the linearized sensor output $\mu_T=\alpha/(\alpha+k/X_T)$ as the ratio k_1/k_2 can be precisely defined at room temperature (RT) by converting the same temperature twice with different gain settings ($k_1/k_2=X_{T1}/X_{T2}$), thus still allowing 1-point α-trim to compensate for the V_{BE0} spread. In addition, we employ double sampling with a single DAC to further improve the sensor energy efficiency by 2×.

Figure 3.8.2 shows the implementation of beta-cancellation biasing [4] with dynamic error-correction [5] in the sensor front-end. We employ small PNP BJTs (2μm×2μm) to maintain a high linearity in $V_{BE0,1}$ (<0.05°C error over full range) with a moderate emitter bias current of I_{PT}=150nA at RT. The 94dB-gain folded-cascode error amplifier (A_E) consumes 0.45μA, with its offset and 1/f noise up-modulated by chopping ($f_{cp}=f_s/36$). The four-wire connections at the BJT outputs prevent accuracy degradation in $V_{BE0,1}$ due to the varied voltage drop across the DEM switches (transmission gates). To suppress the switch-leakage-induced nonlinearity in $V_{BE0,1}$ at high-T (body-leakage dominant), the PMOS drain/source diffusion area is 3.6× larger than that of the NMOS to achieve a 1st-order body-leakage compensation. Diffusion areas of a switch pair are shared whenever possible to further reduce the body leakage. This results in a measured average leakage reduction of a transmission-gate pair from 640pA to 190pA at 180°C, corresponding to a <0.1°C overall linearity error in $V_{BE0,1}$.

Figure 3.8.3 shows the sensor readout with a 2nd-order feedforward double-sampled ΔΣ-ADC. The two sampling paths consisting of $C_{s1,2}$ ($C_{s1}=C_{s2}$) operate at f_s=40kHz, with the 1-bit quantizer clocked at $2\cdot f_s$. When the output bitstream (BS) is high, either one of the $\Phi_{1d,1dd,2d,2dd}$ falling edges triggers the feedback DAC consisting of C_{fb} for charge-balancing, depending on the active sampling path and the current DAC state. This feedback control as triggered by different clock edges can minimize signal-dependent errors introduced by the DAC. The use of only one DAC feedback path also avoids quantization-noise folding due to DAC mismatch. The varying common-mode voltages for V_{BE0} or ΔV_{BE} sampling are canceled by shorting the respective sampling plates of $C_{s1/s2/fb}$ during charge redistribution. To implement k_1=6 and k_2=3 while achieving the target resolution, we size $C_{s1,s2}/C_{fb}$ to be $6C_u/1C_u$ and $12C_u/4C_u$ (with a unit capacitance C_u=260fF) in the two subranges, respectively. The 1st-integrator gain is set to 1/3 ($C_{int1}=3C_u/12C_u$ in the two subranges) to balance the thermal noise contribution between the front-end and the ADC. Subranging decision is achieved by checking the polarity of $6\cdot(8\Delta V_{BE}-V_{BE0})$, in which the 6× gain can reduce the T_r variations as induced by the comparator offset. The sensor then runs for 162 ΔΣ cycles (324 output bits). System-level chopping (f_{sys}, once per conversion) suppresses the residue 1/f noise by inverting the input polarity and averaging the decimated output.

The 1st integrator in Fig. 3.8.3 consists of two ~80dB-gain chopped current-reuse amplifier slices ($A_{1,1,2}$) with different transistor bias conditions to maximize their respective output swings in the two subranges while consuming 0.8μA and 1.65μA, respectively. Despite the reduced settling requirement, $A_{1,2}$ designed for the high-T range consumes more power due to the 2× larger C_s and the degraded transistor g_m/I_d efficiency. The 2nd-integrator, which has a much-relaxed noise requirement, draws 170nA, and is bypassed during the subrange decision phase. We employ T-switches [4] with body-leakage compensation in the sensor readout to minimize its influence on $V_{BE0,1}$ during sampling. Notice that applying the conventional DEM to $C_{s1,s2,fb}$ requires a total of 336 switches for the 56 unit capacitors. Consequently, as the ratio k_1/k_2 can be determined at RT, we just perform a local DEM at low-T by involving all unit capacitors of $C_{s1,s2,fb}$ within one conversion to minimize the spread of k_1 and the layout-dependent ratio error of k_1/k_2. The DEM of C_{fb} is controlled by BS to ensure all unit capacitors can equally contribute to the feedback operation, at the cost of a small temperature-dependent noise tone in the BS output.

This 0.42mm² sensor was fabricated in a standard 0.18μm CMOS process. The die micrograph is shown in Fig.3.8.7. We implement the sinc³ decimation filter off-chip for testing flexibility. Clocked at 40kHz, the sensor employs a customized clock-gated digital controller using HVT devices, drawing 2.5μA at RT, and 3.8μA at 150°C from a 1.5V supply. The current consumption further increases to 5.7μA (~2μA from digital) at 180°C. Figure 3.8.4 shows the sensor output PSD, indicating a suppressed 1/f noise corner of <150mHz. With dynamic error correction, the best achieved kT/C-limited resolution is 17.6mK$_{rms}$ (with local DEM enabled) under a conversion time of 8.325ms at RT, corresponding to a resolution-FoM of 9.7pJ·K². By exploiting a nonlinear readout, subranging technique, double sampling, and constant-biasing method, this work further demonstrates a resolution-FoM of 7.2pJ·K² at 150°C. The measured supply sensitivity is 0.44°C/V from 1.5V to 2V. Figure 3.8.5 presents the measured performance with a total of 25 samples from -50°C to 180°C. Note that hysteresis around T_r (the transition region) will not affect the temperature reconstruction. As observed, the untrimmed inaccuracy is ±1.8°C (3σ). After 1-point α-trim and k_1/k_2 ratio correction at RT, the inaccuracy improves to ±0.45°C (3σ), ultimately limited by process spreads instead of nonlinearity at high-T. Figure 3.8.6 benchmarks this work with the state-of-the-art wide-range smart temperature sensors. Except from the resistor-based design [1], which requires high-order nonlinearity cancellation, this work in bulk CMOS achieves a 6-to-10× higher energy efficiency than prior BJT-based works [3,4] with comparable sensing resolution and trimming effort.

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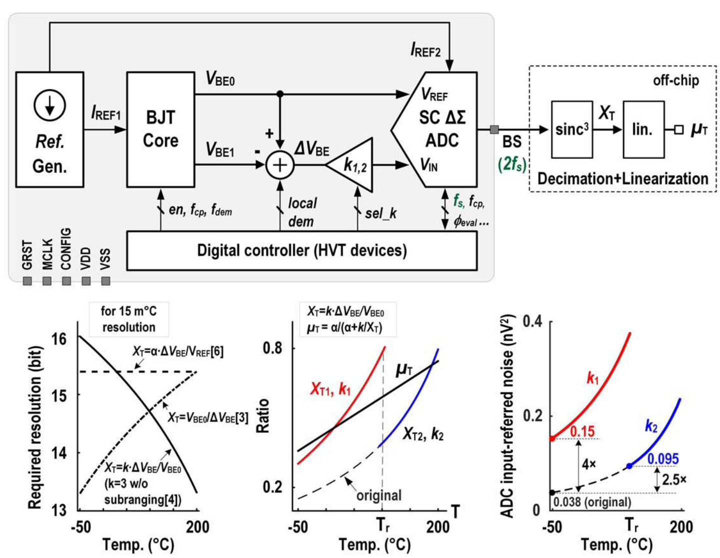

Figure 3.8.1: Proposed subranging temperature sensor with double-sampled SC ΔΣ-ADC for wide-range operation and energy-efficiency optimization.

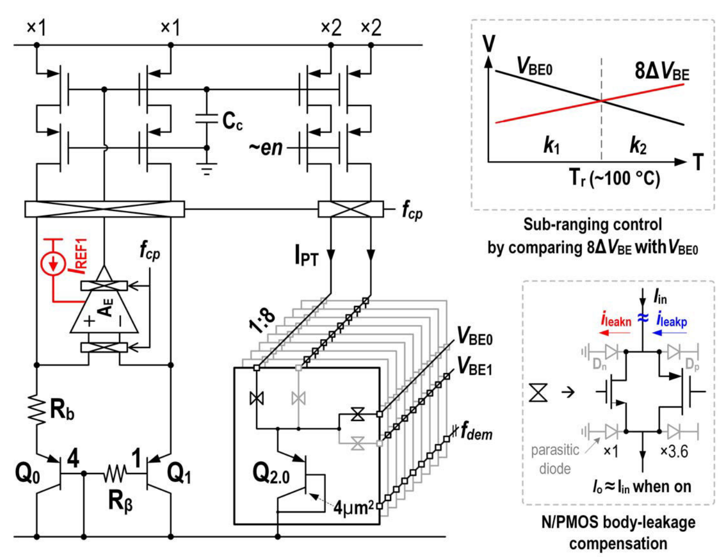

Figure 3.8.2: Sensor front-end with four-wire BJT output connection and switch body-leakage compensation to maintain signal linearity at high temperatures.

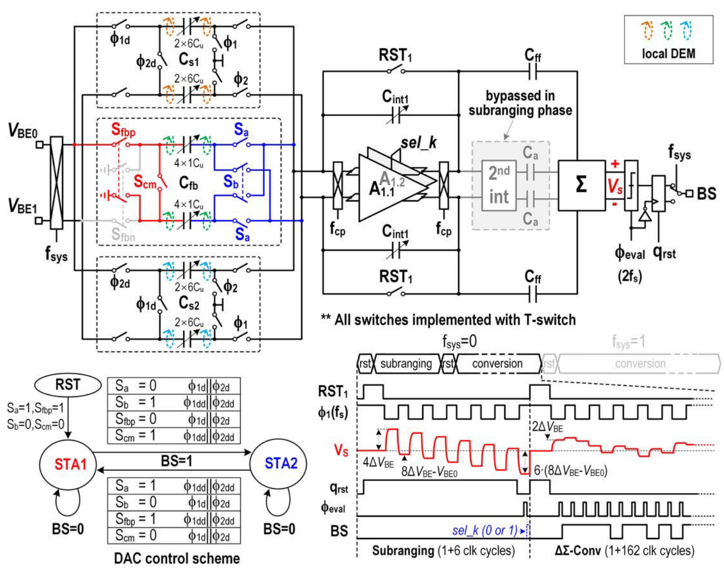

Figure 3.8.3: Double-sampled ΔΣ-ADC using a single DAC and with local DEM to reduce k_1/k_2 spread (top); DAC control and readout timing at f_{sys}=0 (bottom).

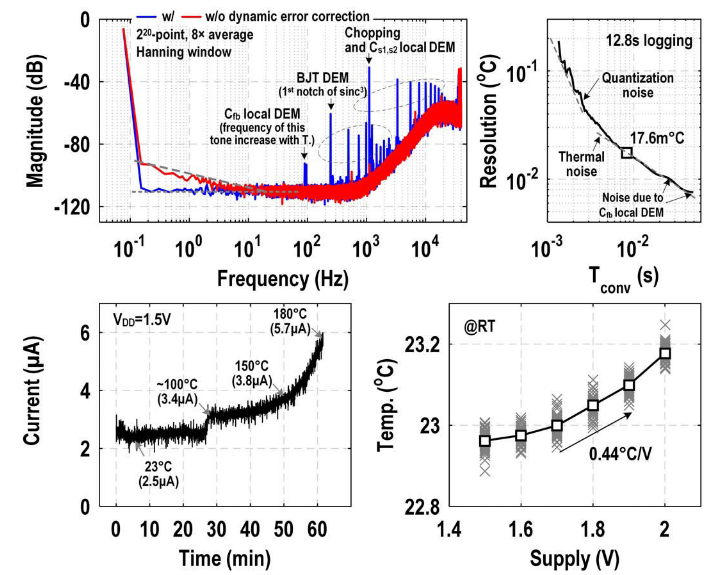

Figure 3.8.4: PSD of the output BS and resolution over time (top); logged sensor current with increasing ambient temperature and supply sensitivity (bottom).

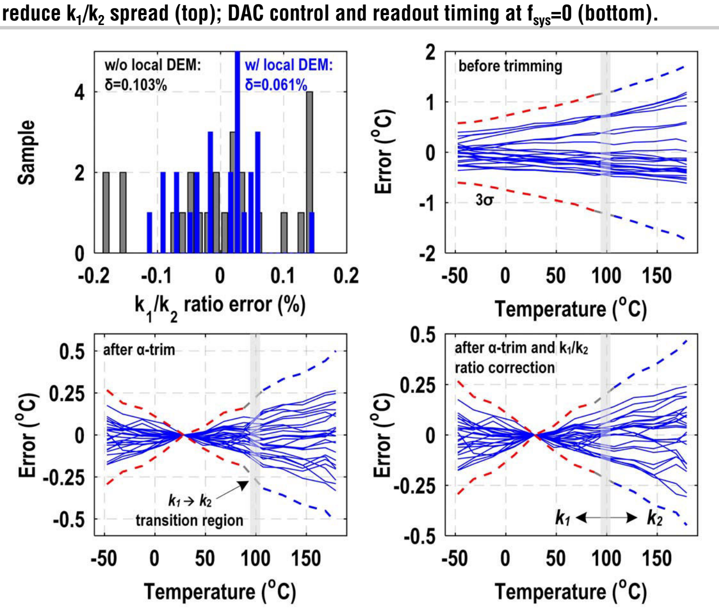

Figure 3.8.5: Measured k_1/k_2 spread and untrimmed temperature error (top); error after α-trim and both α-trim and k_1/k_2 ratio correction (bottom).

	ISSCC'19 [2]	ESSCIRC'13 [3]	JSSC'20 [4]	ISSCC'17 [5]	This work	
Technology	0.18 μm	0.16 μm SOI	0.16 μm	28 nm	**0.18 μm**	
Sensor Type	Resistor	BJT	BJT	BJT	**BJT**	
Area	0.12 mm^2	0.1 mm^2	0.15 mm^2	0.01 mm^2	**0.42 mm^2**	
Samples	20	7	24	76	**25**	
Supply Voltage	1.8 V	1.6 ~ 2 V	1.8 V	1.8 V	**1.5 ~ 2 V**	
Sensing Range	−40 °C to 180 °C	−55 °C to 200 °C	−40 °C to 180 °C	−25 °C to 125 °C	**−50 °C to 180 °C**	
3σ Inaccuracy (Trim points)	±0.4 °C (1-pt)[a] ±0.11 °C (2-pt)[a]	±0.4 °C (1-pt)	±0.2 °C (1-pt) ±0.25 °C (vcal)	±1.85 °C (0-pt)	**±1.8 °C (0-pt) ±0.45 °C (1-pt)**	
Relative Inaccuracy[b]	0.36% (1-pt) 0.1% (2-pt)	0.31% (1-pt)	0.18% (1-pt) 0.23% (vcal)	2.47% (0-pt)	**1.57% (0-pt) 0.39% (1-pt)**	
T_{conv}	10 ms	4.2 ms	20 ms	8.2 ms	**8.3 ms**	
Power (at RT)	52 μW	35.2 μW	9.8 μW	18.8 μW	**RT** **3.8 μW**	**150 °C** **5.7 μW**
Resolution	0.46 m°C	20 m°C	23 m°C	150 m°C	**17.6 m°C**	**12.3 m°C**
Res. FoM[c]	0.1 pJ·K^2	59 pJ·K^2	103 pJ·K^2	3500 pJ·K^2	**9.7 pJ·K^2**	**7.2 pJ·K^2**

a: 6th-order nonlinearity removal

b: Relative inaccuracy (%) = Max error / specified sensing range ×100

c: Res. FoM = Energy/Conversion×Resolution^2

Figure 3.8.6: Performance summary and benchmark with state of the art.

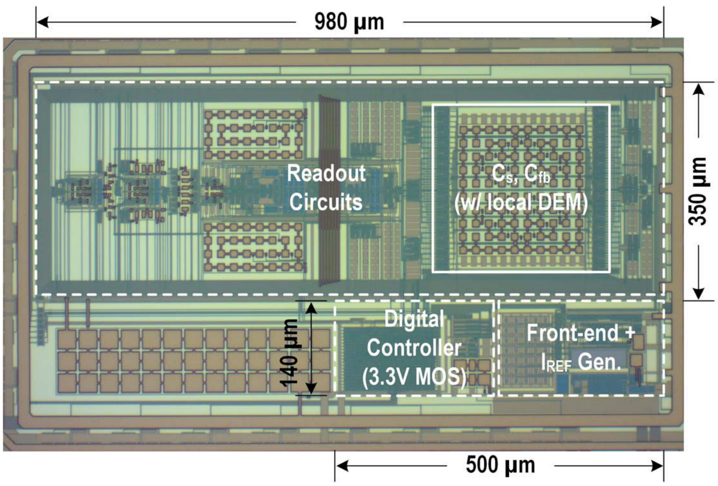

Figure 3.8.7: Die micrograph of the designed temperature sensor in 0.18µm 1.8/3.3V 1P6M CMOS process.