Midterm Review

ECE4514 - Spring 2017

Midterm Format

Structure:

- T/F
- Multiple Choice
- Short problems

Focus on lecture material

Closed note, closed book, closed computer, closed smartphone, closed Apple Watch

Review

Question sets discussed in class

Question sets posted on Canvas

Book Chapters:

1,2,3, 9,12,14

Logic Technology, No SystemVerilog (yet)

Logic Technologies

- Programmable Logic
  - Programmable Logic Devices (PLDs)
  - Field Programmable Gate Arrays (FPGAs)
- Pure ASIC
  - Gate Arrays (Mask Programmable) (MPGAs)
  - Standard Cell (Semi-Custom)
  - Full Custom

Performance

- High-Throughput Architectures
- Low-Latency Architectures
- Timing Optimizations
  - Adding Register Layers
  - Parallel Structures
  - Flatten Logic Structures
  - Register Balancing
  - Reorder Paths

Area

1. Rolling up the pipeline can optimize the area of pipelined designs with duplicated logic in the pipeline stages.
2. Controls can be used to direct the reuse of logic when the shared logic is larger than the control logic.
3. For compact designs where area is the primary requirement, search for resources that have similar counterparts in other modules that can be brought to a global point in the hierarchy and shared between multiple functional areas.
4. An improper reset strategy can create an unnecessarily large design and inhibit certain area optimizations.
5. An optimized FPGA resource will not be used if an incompatible reset is assigned to it. The function will be implemented with generic elements and will occupy more area.
6. Improperly resetting a RAM can have a catastrophic impact on the area.
7. Using set and reset can prevent certain combinatorial logic optimizations.

Power

- Source of power consumption, and what is in your control as a designer
- The impact of clock control on dynamic power consumption
- Glitches
- Problems with clock gating
- Input control for power minimization
- Dual-edge triggered flip-flops

Synthesis

- Creating efficient decision trees
  - Trade-offs between priority and parallel structures
  - Dangers of multiple control branches
- Coding style traps
  - Usage of blocking and nonblocking assignments
  - Proper and improper usage of FOR-loops
  - Inference of combinatorial loops and latches
- Design partitioning and organization.
  - Organizing data path and control structures
  - Modular design
- Parameterizing a design for reuse
- Understanding relationship between HDL and resulting circuit

Floating Point

- Dynamic range, number density, and precision
- General floating point format
- IEEE 754 format
- Exponent bias
- Conversion
- Floating point arithmetic
  - Multiplication
  - Addition
  - Other

Synthesis Constraints

- Role of an SDC file
- Temporal constraints
- Resource constraints
  - E.g., resource sharing
- Technology-dependent constraints
  - Retiming, logic balancing

Clocks and PLLs

- Clock problems
- Clock distribution
- PLL principles, applications, limitations
- Pseudo arbitrary frequency generation

MORE EXAMPLE QUESTIONS

Example True or False

T or F: If pipeline registers can be added to a computation without incurring timing overhead, 6 pipeline stages would have higher or equal throughput than 5 stages.

T or F: A single 4-input LUT cannot be programmed to calculate the odd parity of a 4-bit number.

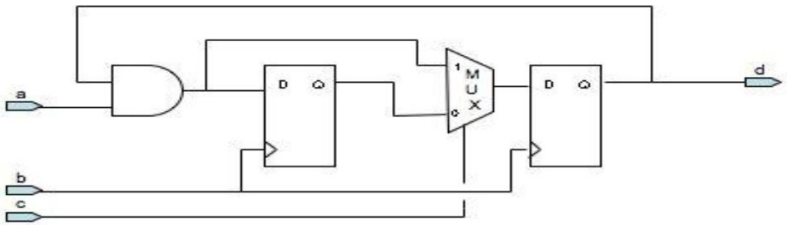
Example Multiple Choice

As a HDL designer, which of the following factors do you have the least control over?

- Dynamic power consumption
- Leakage power consumption
- Power consumption due to glitches
- Throughput
- Latency
- Circuit size

Example Short Answer

(3 points) Create a behavioral Verilog model for the circuit below. In your model, do not use the `assign` keyword. Also, refrain from using structural instantiations.




```
module circuit1 (
    input a,  input b, input c,
    output reg d );

endmodule
```