ASICs and ASIC Alternatives

ECE4514

Big Picture

Can implement a design with many different implementation technologies - different implementation technologies offer different tradeoffs

– *Verilog Synthesis* offers an easy way to target a model towards different implementations

ASIC Design Options

PROGRAMMABLE

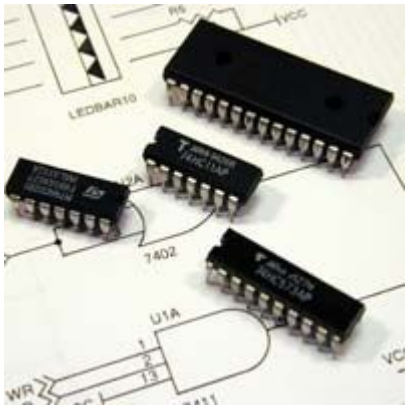
- Programmable Logic Devices (PLDs & CPLDs)
- Field Programmable Gate Arrays (FPGAs)

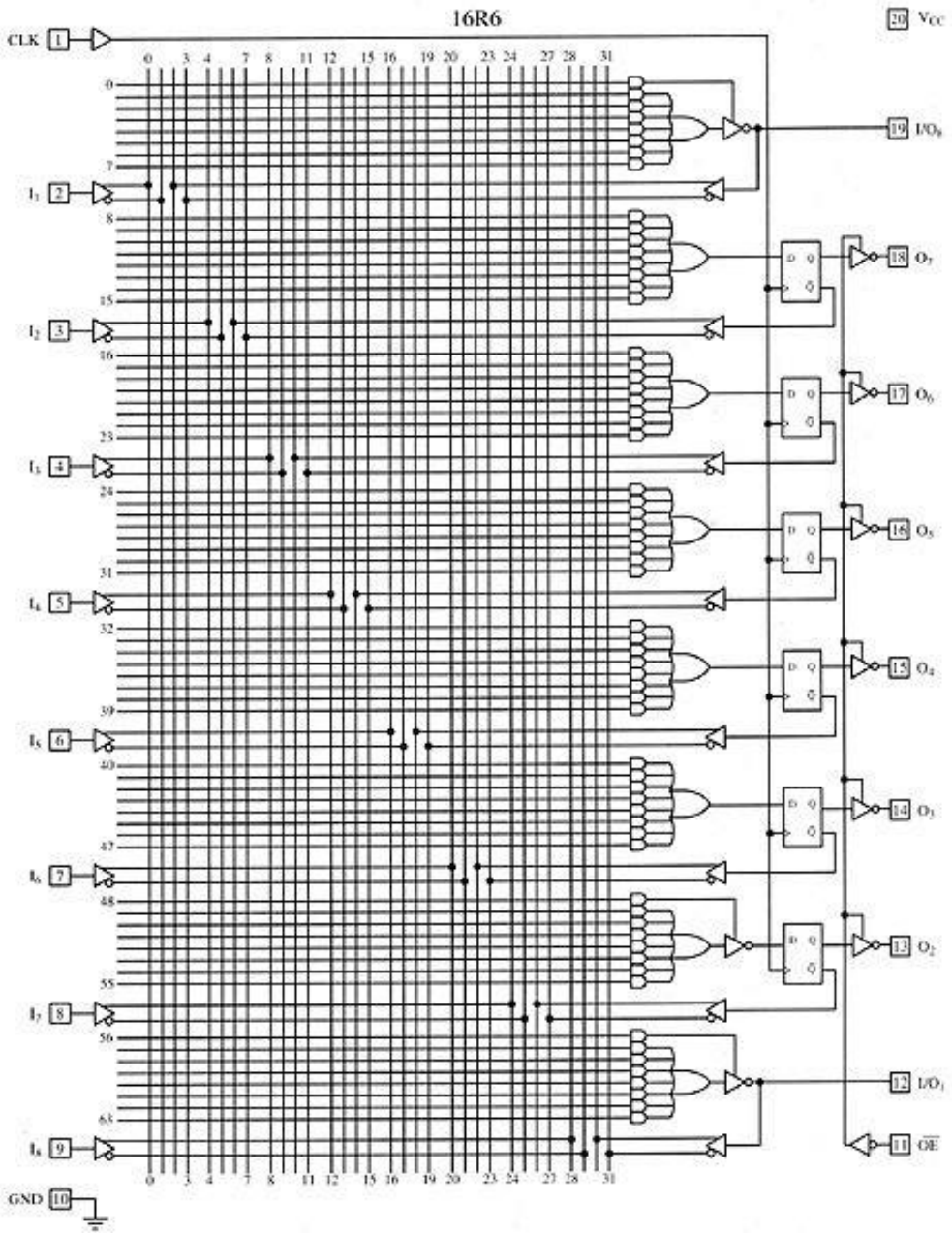
ASICs

- Gate Arrays (Mask Programmable) (MPGAs)
- Standard Cell (Semi-Custom)
- Full Custom

PLDs

- Programmable Logic Devices emerged in the 1970's
- Most effective for implementing logic where complex combinational logic functions terminate at a flip-flop, e.g. state machines
- Complex PLDs (CPLDs) available for implementing more complicated systems. Non-volitile.



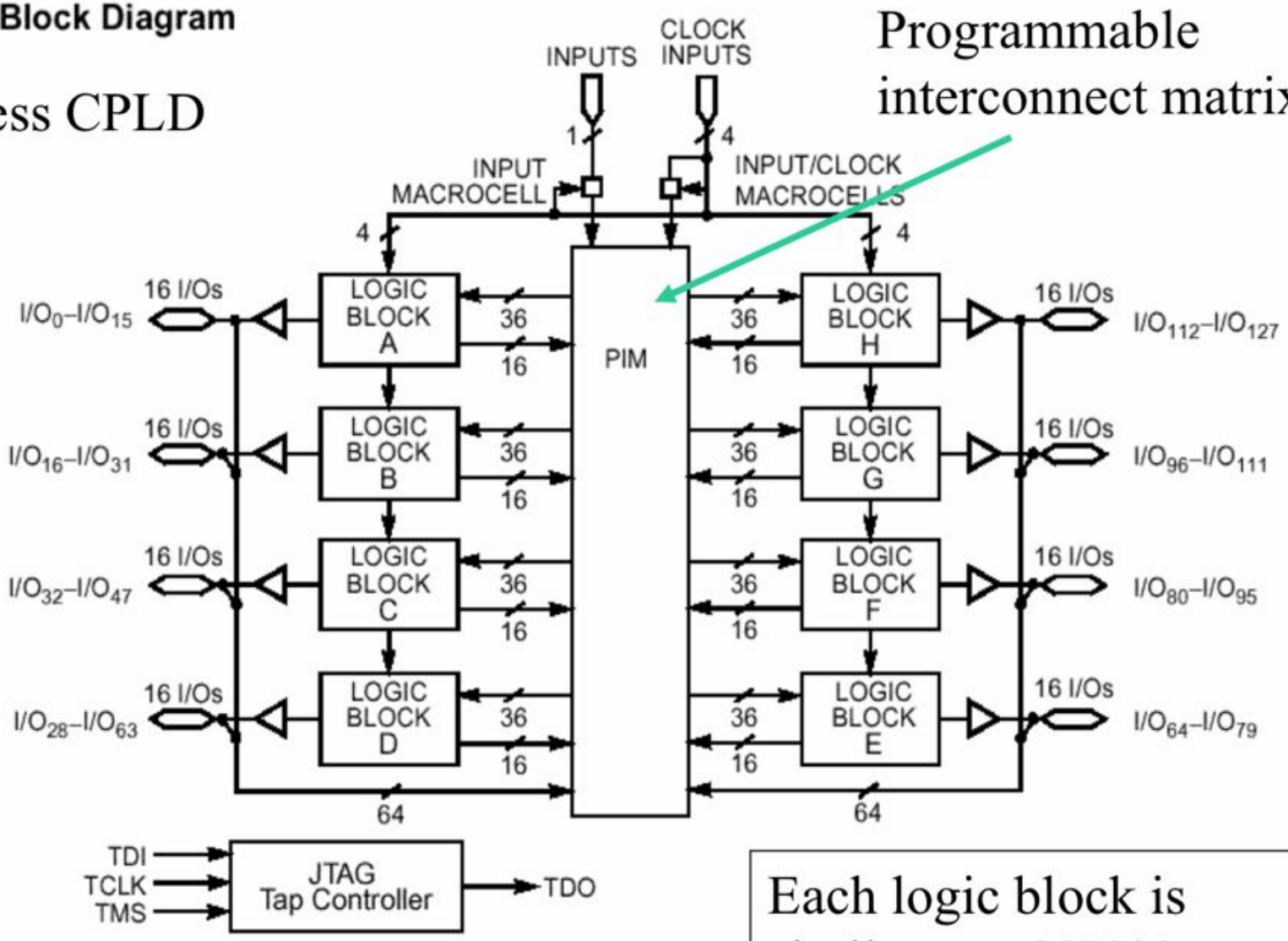

16R6
CLK
GND
20 VCC
19 I/O8
18 O7
17 O6
16 O5
15 O4
14 O3
13 O2
12 I/O1
11 OE

AMD PAL 16R6

Logic Block Diagram

Cypress CPLD

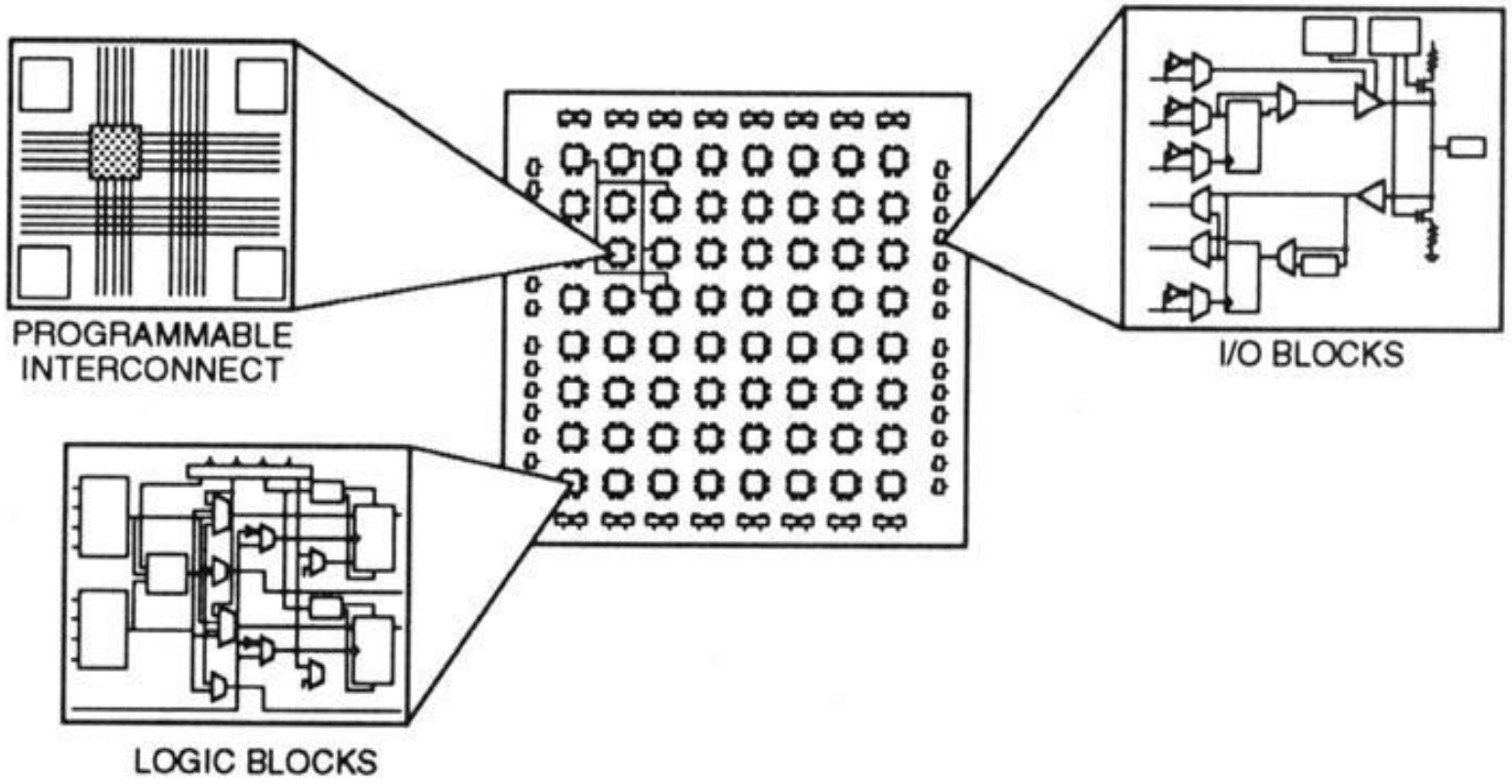
Programmable interconnect matrix.



Each logic block is similar to a 22V10.

FPGAs

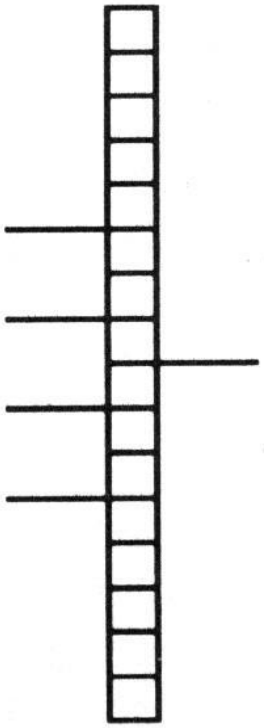
- Field Programmable Gate Arrays emerged in the 1980's
- Have a higher ratio of FFs to Gates than PLDs
- Programmable interconnect & I/O
- Better suited for designs with lots of registers, wide data busses, and MUXes.



FPGAs

Chip function controlled by SRAM control bits

Three Important Programmable Logical Elements

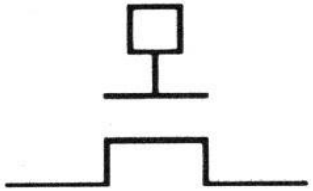


a

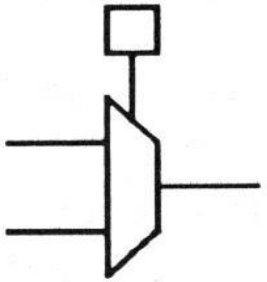
a) Lookup Table (RAM)

b) Programmable Interconnection Point (PIP)

c) Control MUX

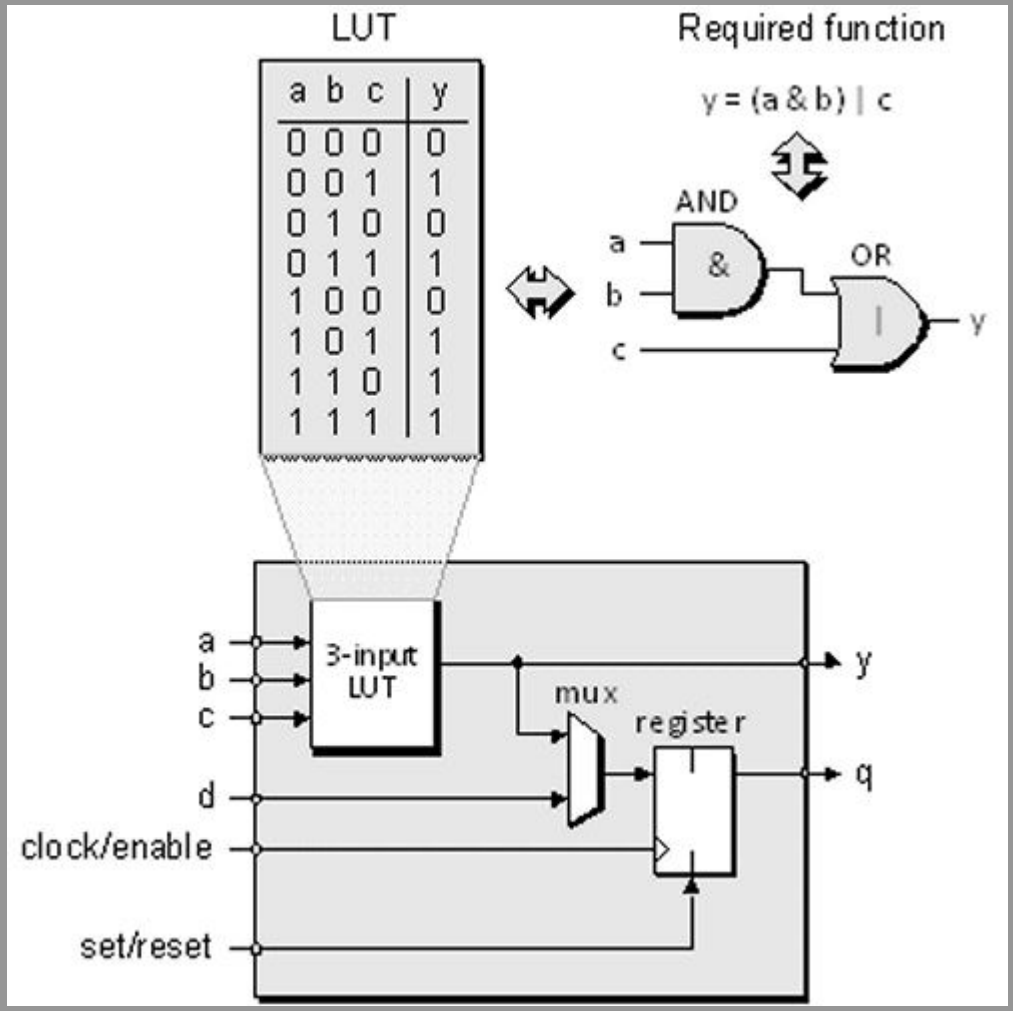


b

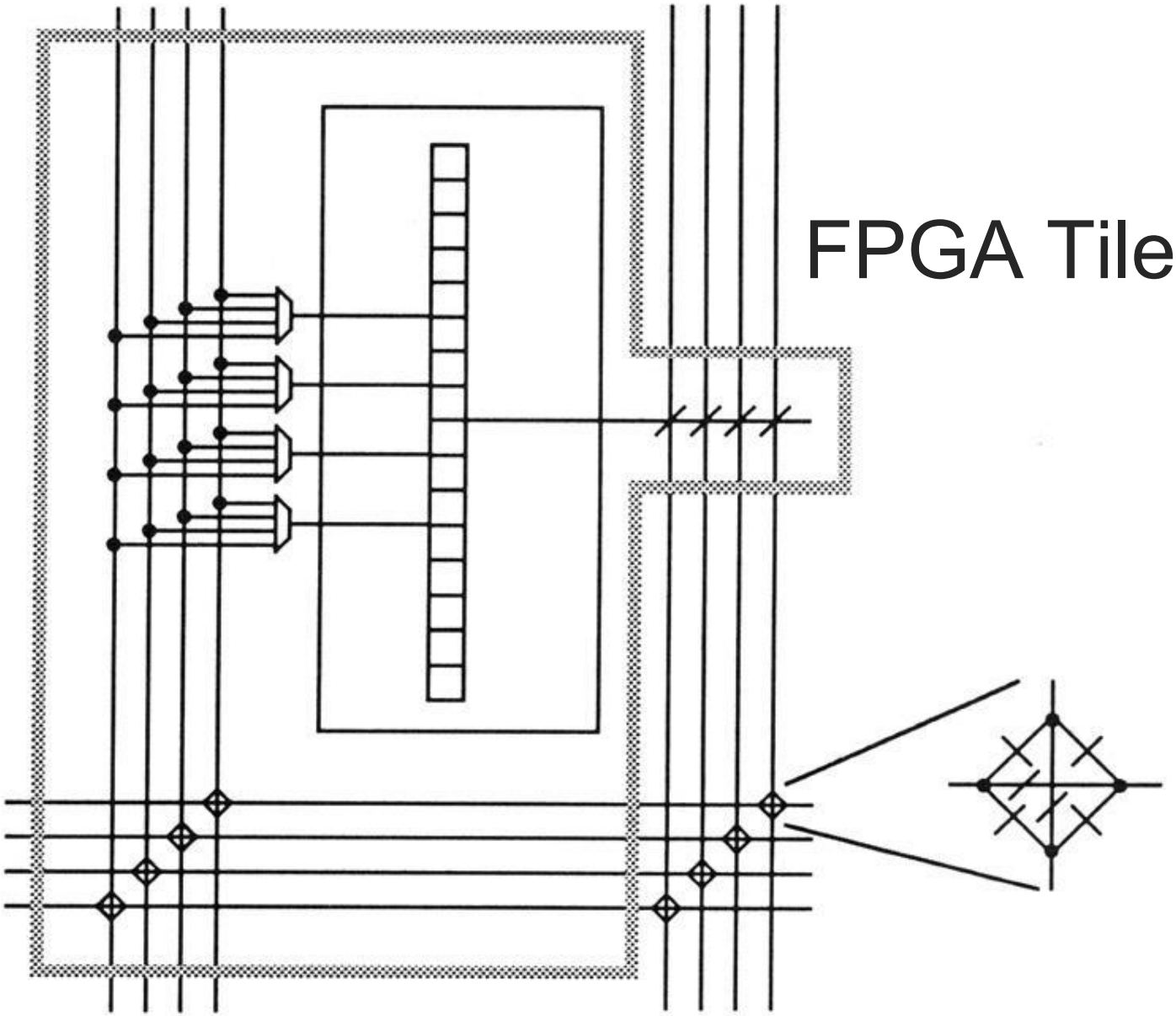


c

Look-up Table (LUT)



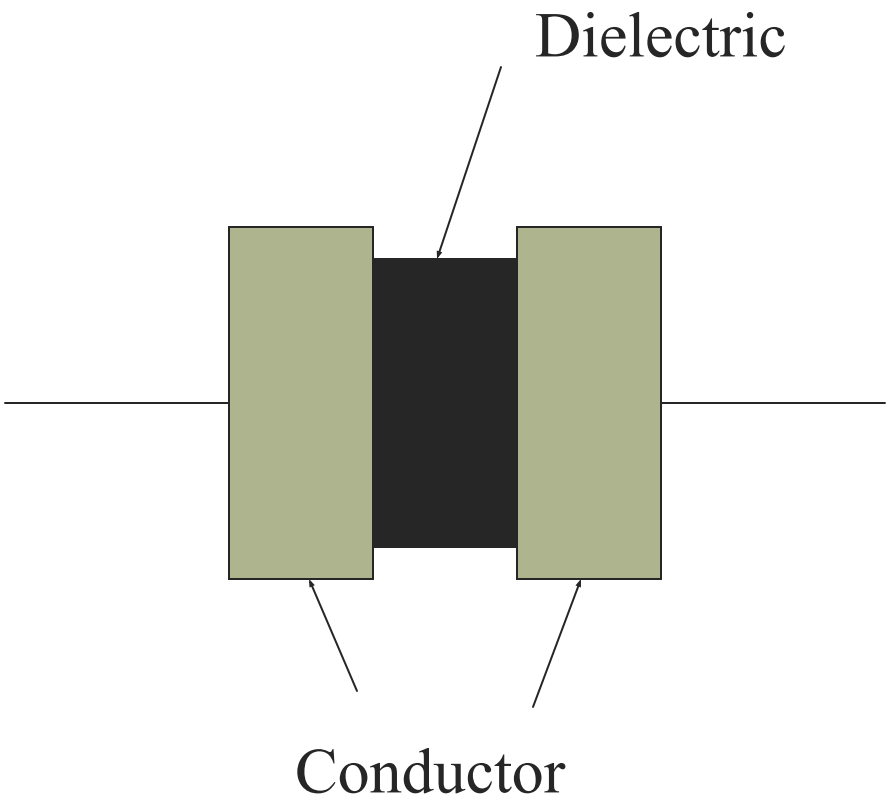
FPGA Tile



Switch Options

- SRAM
- Anti-fuse
- EPROM
- EEPROM / FLASH

Anti-fuse



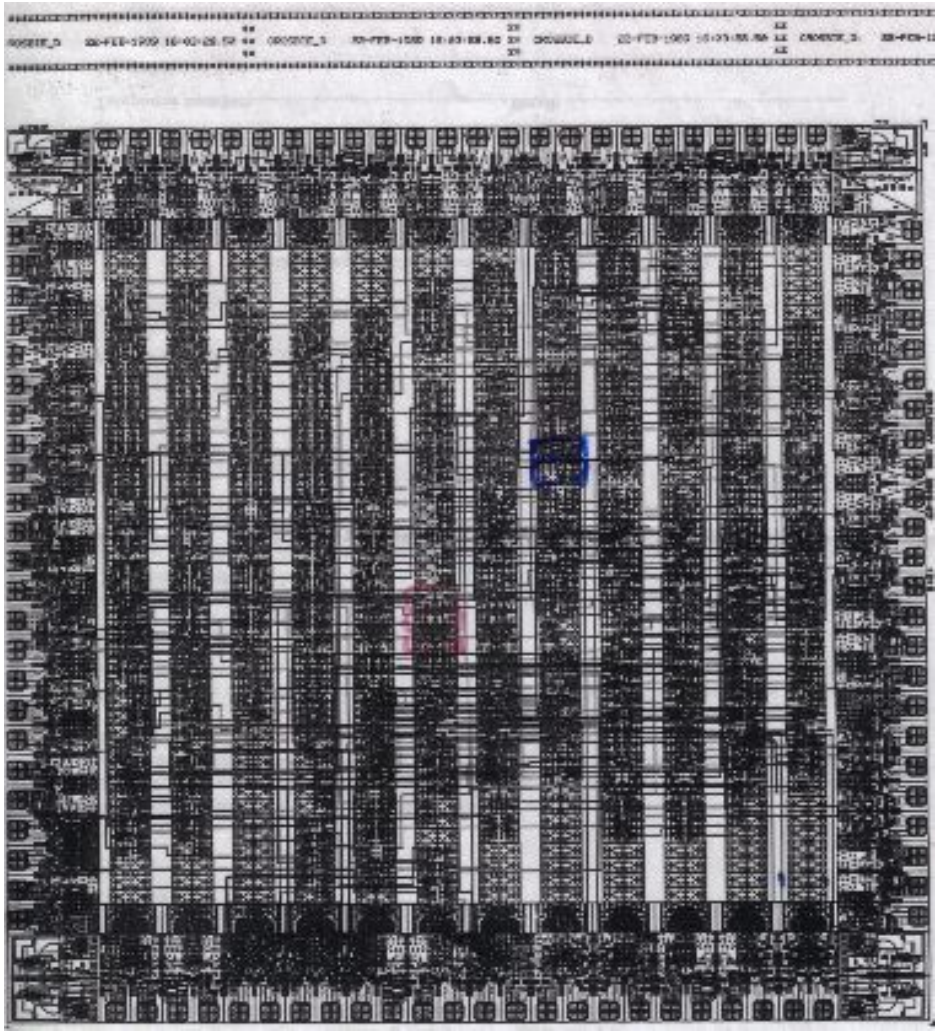
Switch Alternatives

Technology	Volatile	Re-Prog	Area	R(ohm)	C(ff)
SRAM	Yes	In-circuit	Large	1-2K	10-20
Anti-Fuse	No	No	Small	300-500	3-5
EPROM	No	Out of circuit	Small	2-4K	10-20
EEPROM	No	In-circuit	2*EPROM	2-4K	10-20

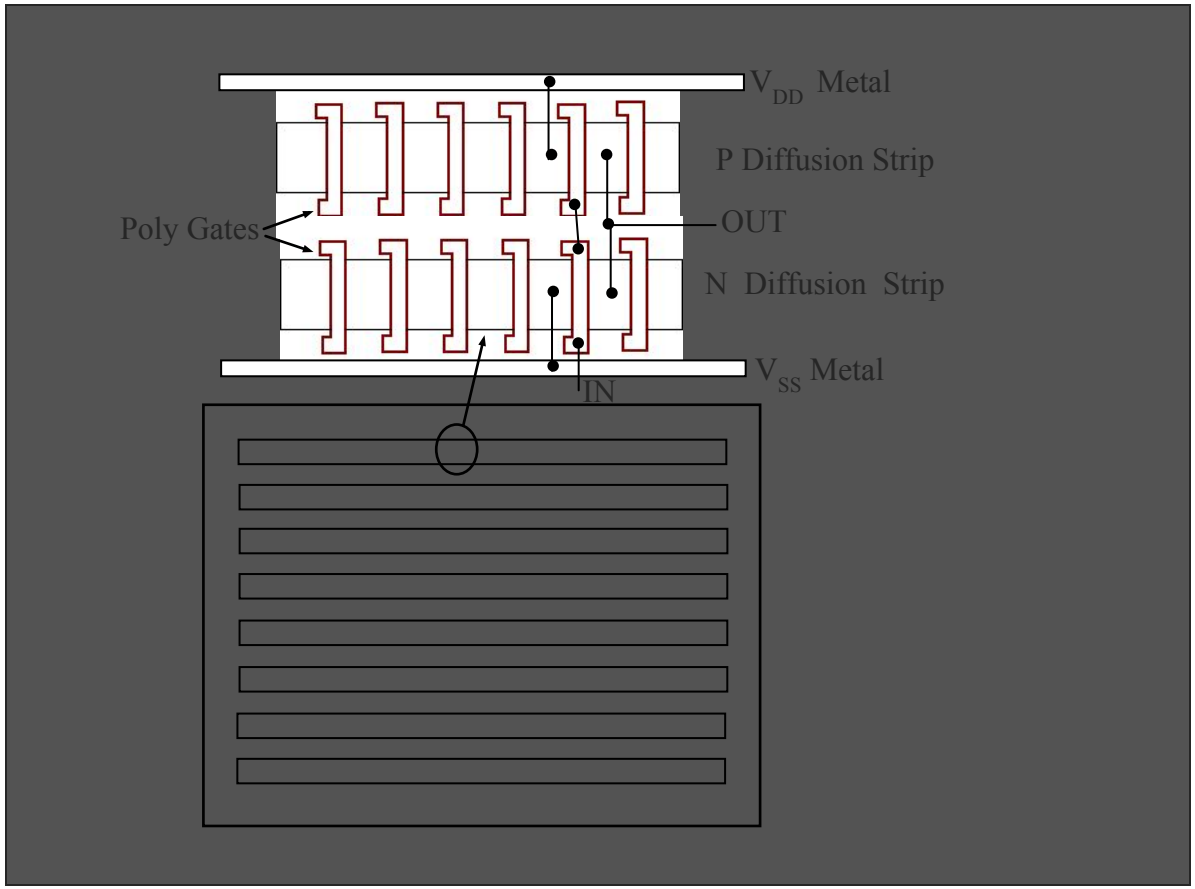
FPGAs?

- Performance is usually several factors to an order of magnitude lower than standard cell. Performance depends heavily on quality of FPGA technology.
- Design time advantages are the same as for standard cell (use same type of cell/macro library).
- Densities are an order of magnitude lower than standard cell but an order of magnitude higher than normal PLDs.
- Very good for prototyping designs:
  - Reusable
  - Low start-up costs

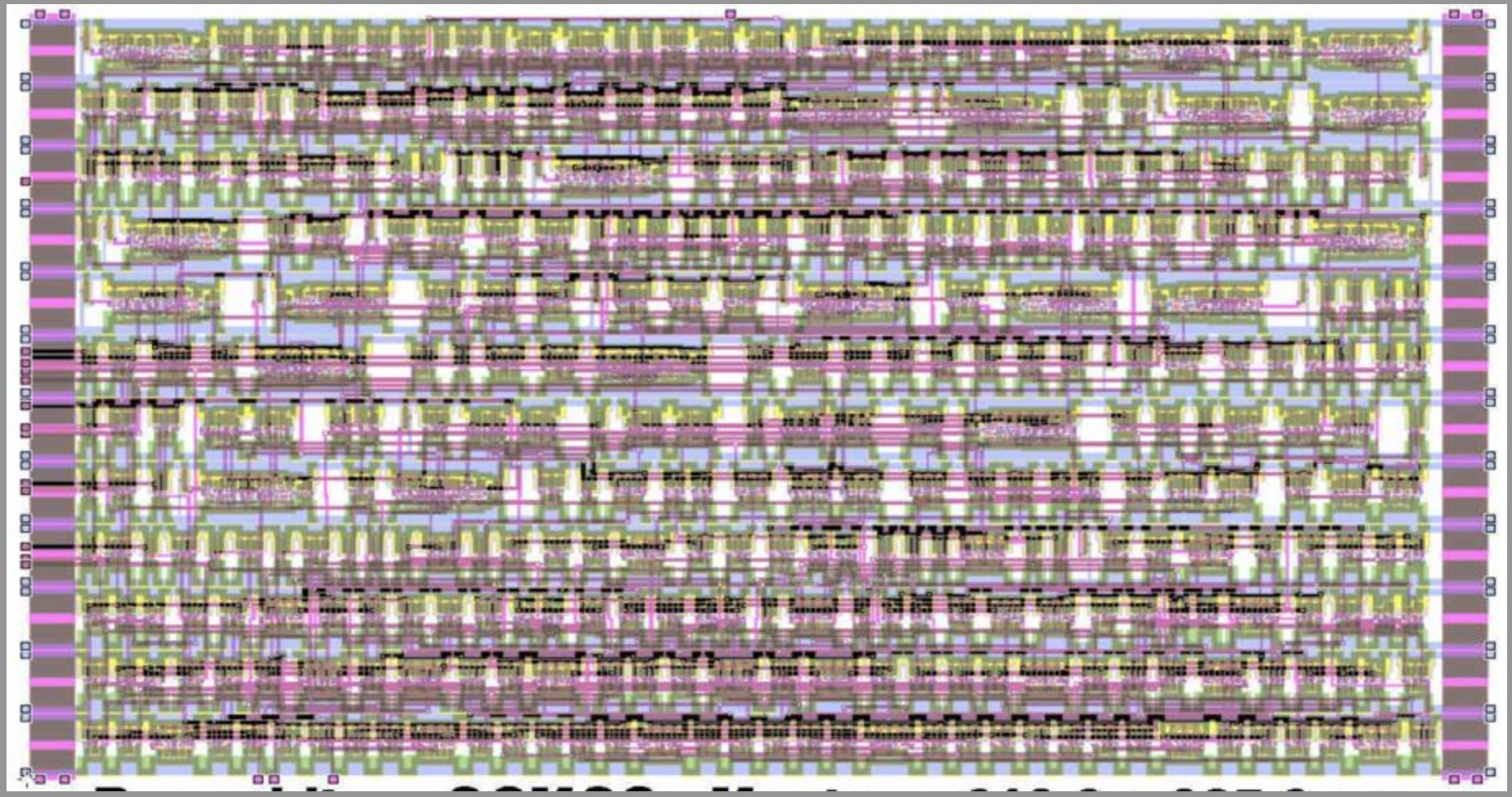
Gate Arrays (MPGAs)



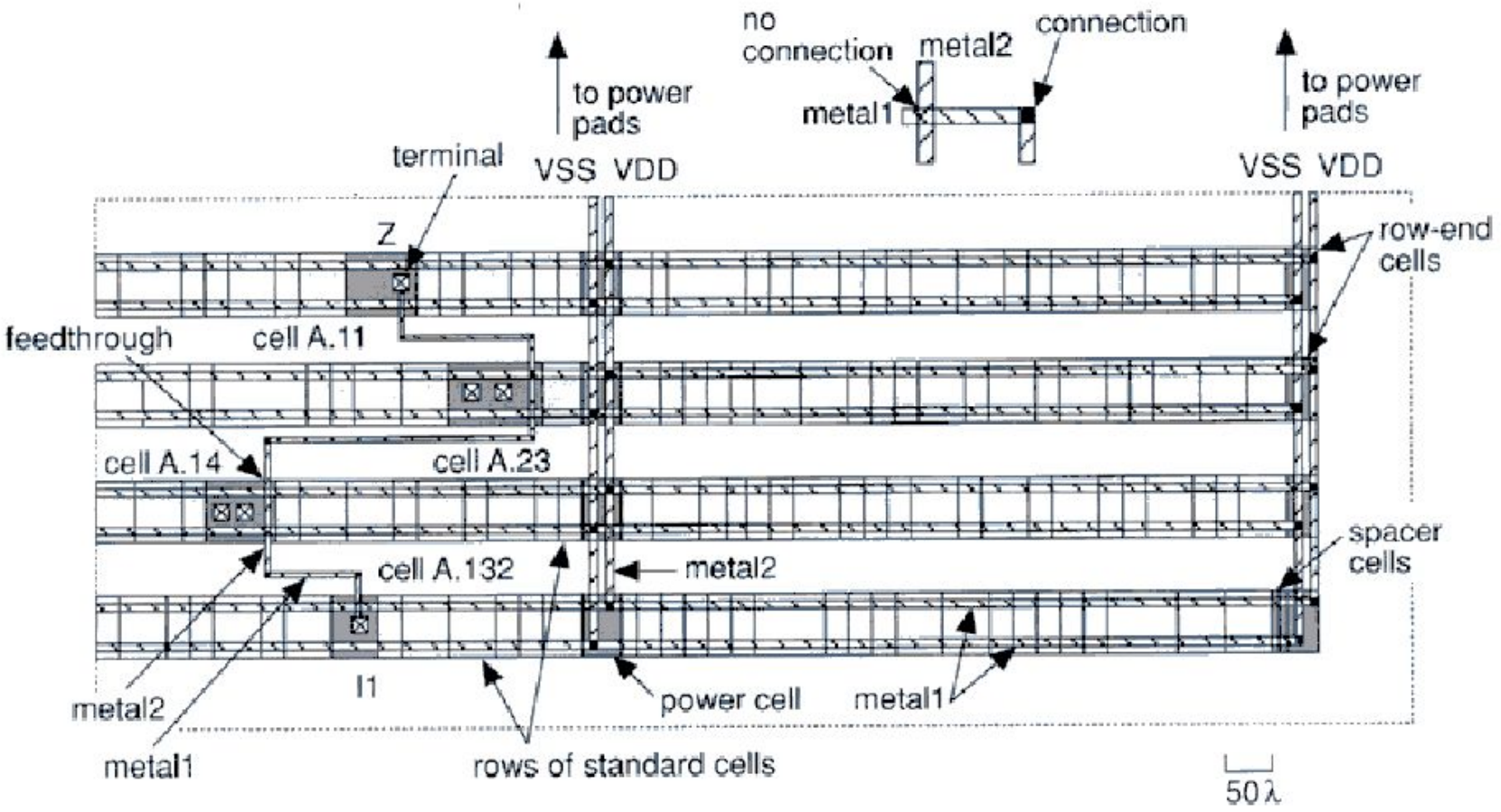
Gate Arrays (MPGAs)



Standard Cell Design



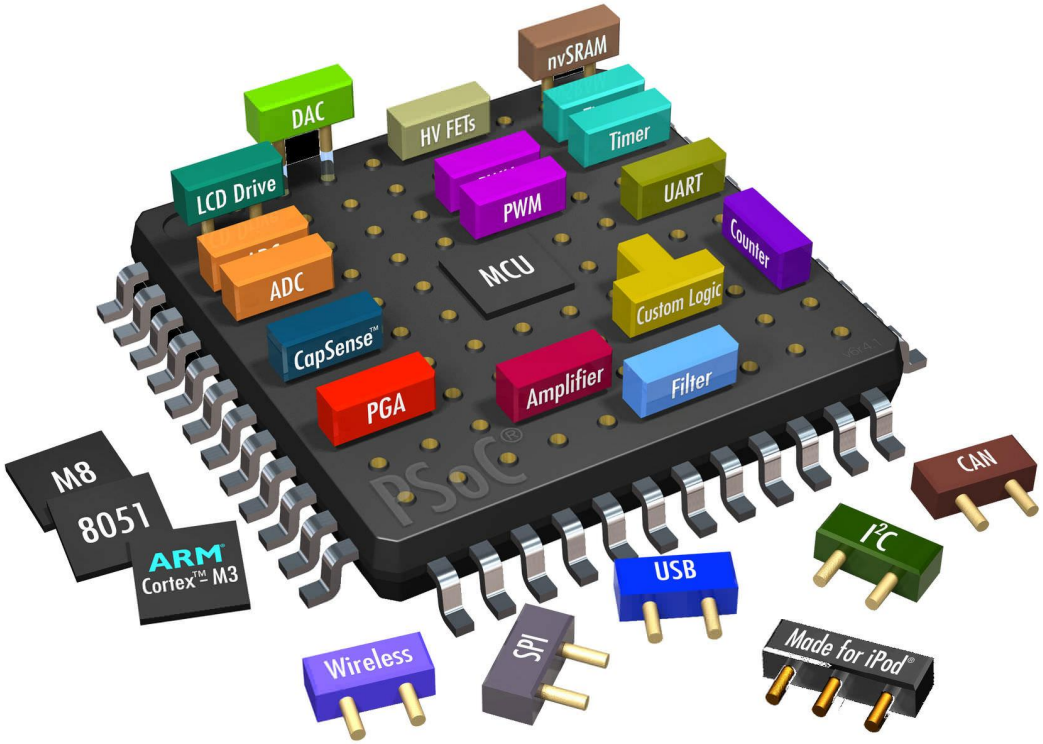
Standard Cells Interconnection Layout



Typical Standard Cell Library Components

- SSI logic: Nand, Nor, Xor, AOI, Not, Registers
- MSI logic: Decoders, Encoders, Parity trees, Adders, Comparators
- Data Path: Alus, Adders, Register files, Shifters, Busses,
- Memory: RAM, ROM, CAM
- System: Multipliers, Micro-Controllers, UARTS, RISC processors

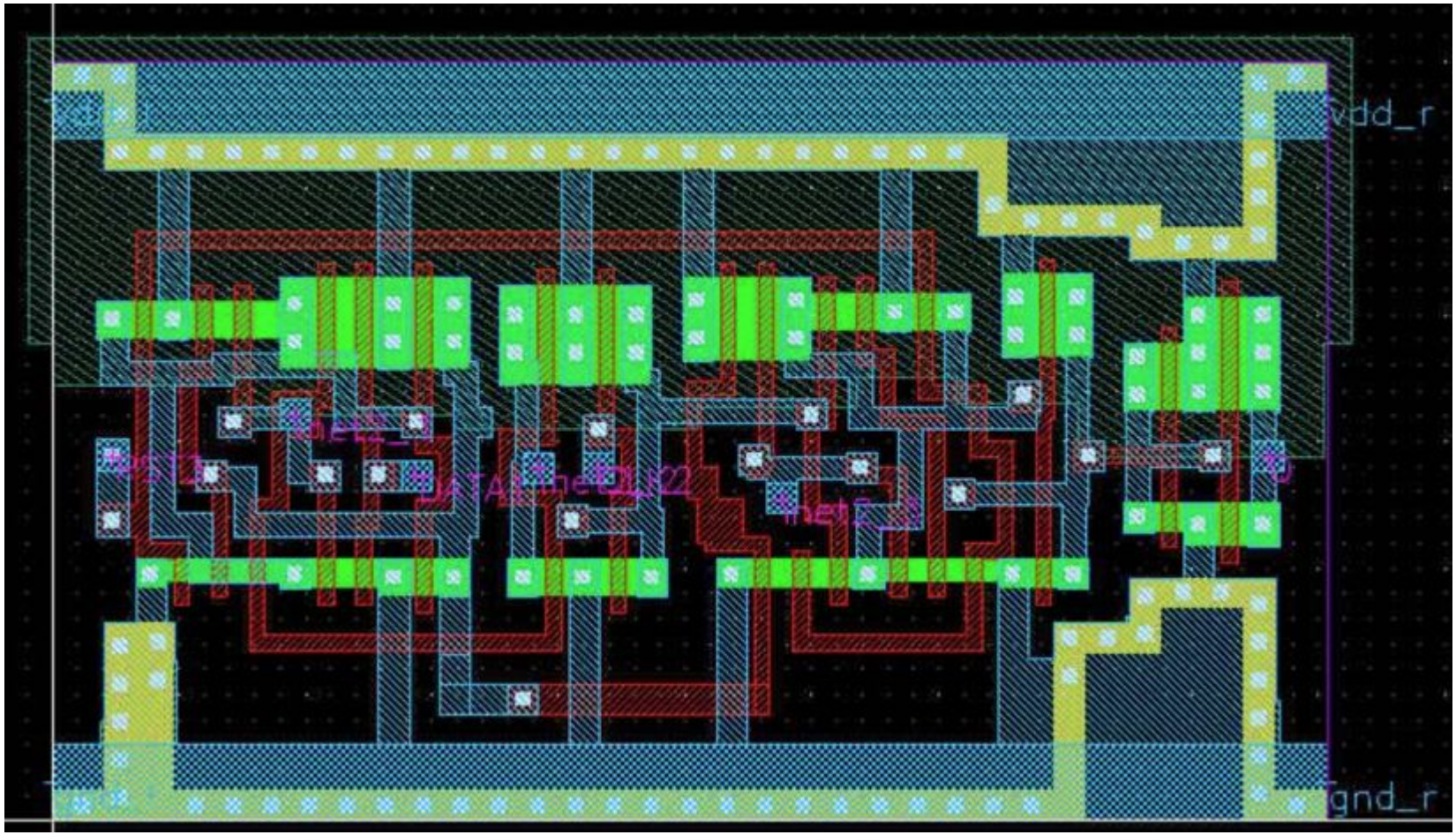
Systems-on-Chip



Full Custom ASIC

- Designer has complete control over layout within the design rules for the given technology (e.g., minimal line width and spacing)
- Each transistor can be individually sized for optimum performance
- Requires large design team and expensive resources
- Typical productivity is 6 transistors/per day/per person

Full Custom ASIC



Comparing Technologies: Density

Highest to lowest density:

1. Full Custom
2. Standard Cell
3. Gate Array
4. FPGAs
5. CPLD
6. PLD

Highest end FPGA density is equal to low-end ASIC densities

Comparing Technologies: Speed

Highest to lowest performance:

1. Full Custom
2. Standard Cell
3. Gate Array
4. PLDs / CPLDs
5. FPGAs

Again, large performance gap between ASIC technologies and programmable technologies.

Comparing Technologies: Speed

Depends heavily on volume. If only need a few hundred, then FPGAs can be cheaper. If need thousands, then ASIC technologies are cheaper.

Cost comparison

- Two components of cost:
  - Fixed design costs (NRE)
  - Cost per part
- Total cost =
  NRE + (cost per part × volume)

Cost Comparison

- Components of fixed costs:
  - Personnel (training, work time)
  - Infrastructure: Workstations, CAD tools
  - Mask production, test vector creation
  - Second sourcing (just in case…)

Cost Comparison

- Components of cost per unit:
  - Wafer size
  - Gate density (gates/area)
  - Yield (Wafer defects)
  - Profit margin of fabrication facility

Summary

- Full custom can give best density and performance
- Faster design time and ease of design are key advantages of gate array and standard cell over full custom.
- Fast fabrication time and lower cost are key advantages of gate arrays over standard cell.
- Gate arrays offer much higher density over FPGAs and are cheaper than FPGAs in volume production.

Ranking of Time-to-Market from Shortest to Longest

- FPGAs
- MPGAs
- STD CELL designs
- Custom Design