9/4/2015

Bowei Zhao HW2

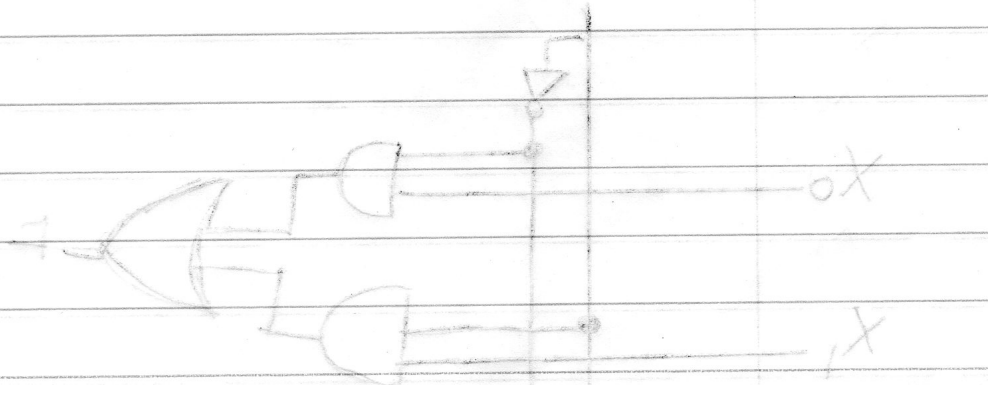
1a)

S_1	S_0	X_3	X_2	X_1	X_0	F
0	0	x	x	x	0	0
0	0	x	x	x	1	1
0	1	x	x	0	x	0
0	1	x	x	1	x	1
1	0	x	0	x	x	0
1	0	x	1	x	x	1
1	1	0	x	x	x	0
1	1	1	x	x	x	1

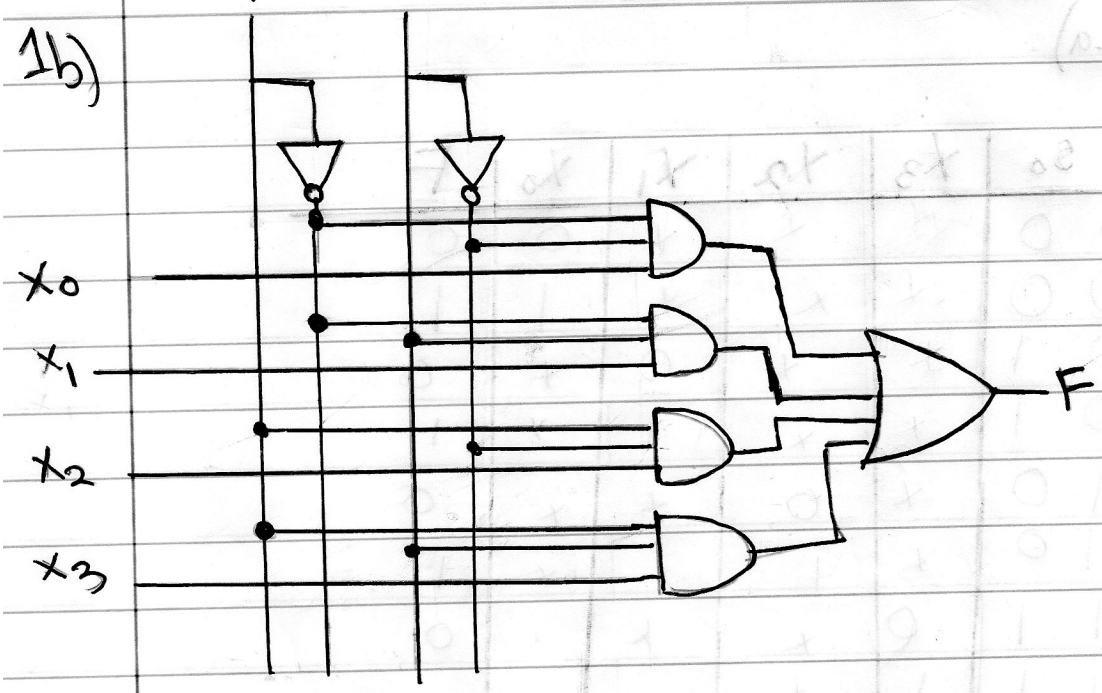
S_1S_0

F	00	01	11	10
0	$\bar{x_0}$	x_1	x_3	x_2
1	x_0	x_1	x_3	x_2

$$F = (\bar{S_1}\bar{S_0})x_0 + (\bar{S_1}S_0)x_1 + (S_1\bar{S_0})x_2 + (S_1S_0)x_3$$



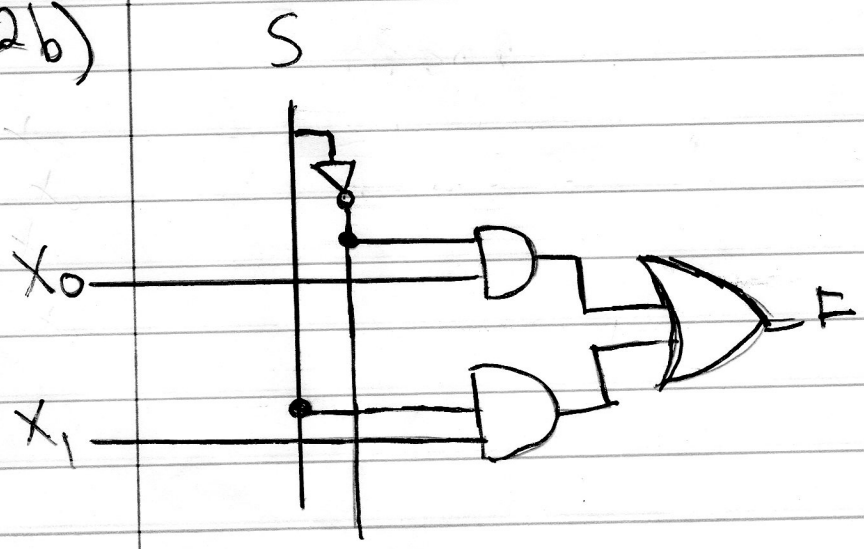
1b)



2a)

S	X_1	X_0	F
0	x	0	0
0	x	1	1
1	0	x	0
1	1	x	1

2b)



3a)

E	A	B	F
0	x	0	0
0	x	1	1
1	0	x	0
1	1	x	1

$$F = \bar{E}B + EA$$

3b) The diagram above, in a sense, is relatable to that of a mux because of its "selecting element". Wherein a Mux chooses which of its 2^n inputs by n select lines, the logic above chooses with the tri-state buffer. At any time, only either A or B will output a value but not both. This is due to the inverted E input. Where the E has one line connected directly to the active Low of one tri-state buffer and another line connected thrgh an inverter to a like buffer to A. This means only A or B can come out but not Both. Thus E is a selecting element that chooses what input to output.

#4)

```
int a=1;
int mover= a <<k;
int tester = mover & val;
  if (tester == mover)
   {
      return 1;
   }
   else
    {
       return 0;
    }
```

Problem 5. The flip-flops in the following diagram are positive-edge-triggered devices. Complete the timing diagram that is shown below. Assume that both flip-flops have been initialized to 0.