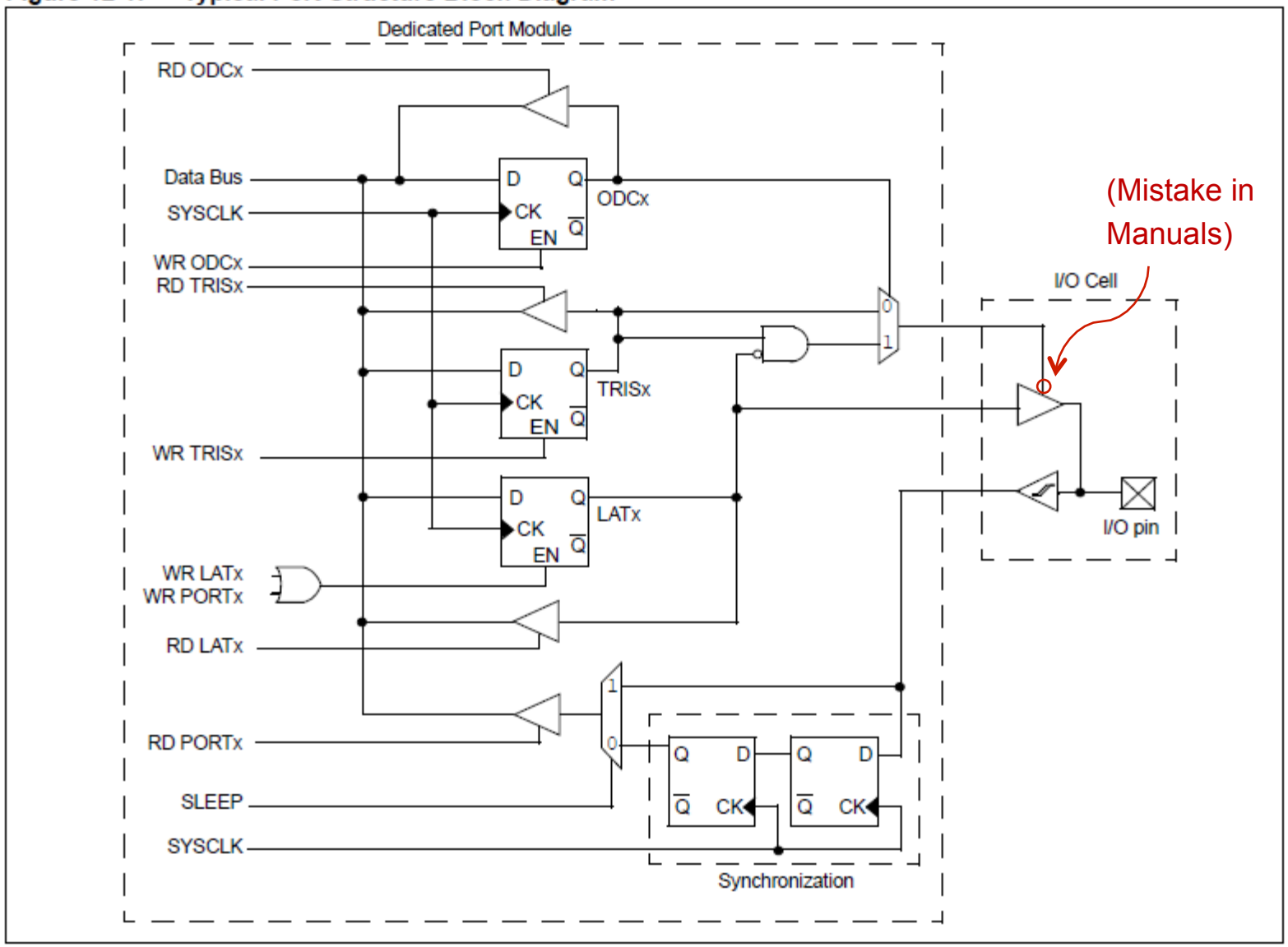
ECE 2534

More about

Input/output ports on the PIC32

One bit on a PIC32 I/O port

Figure 12-1: Typical Port Structure Block Diagram



I/O ports on the PIC32

TRISA

PORTA

LATA

ODCA

…

…

…

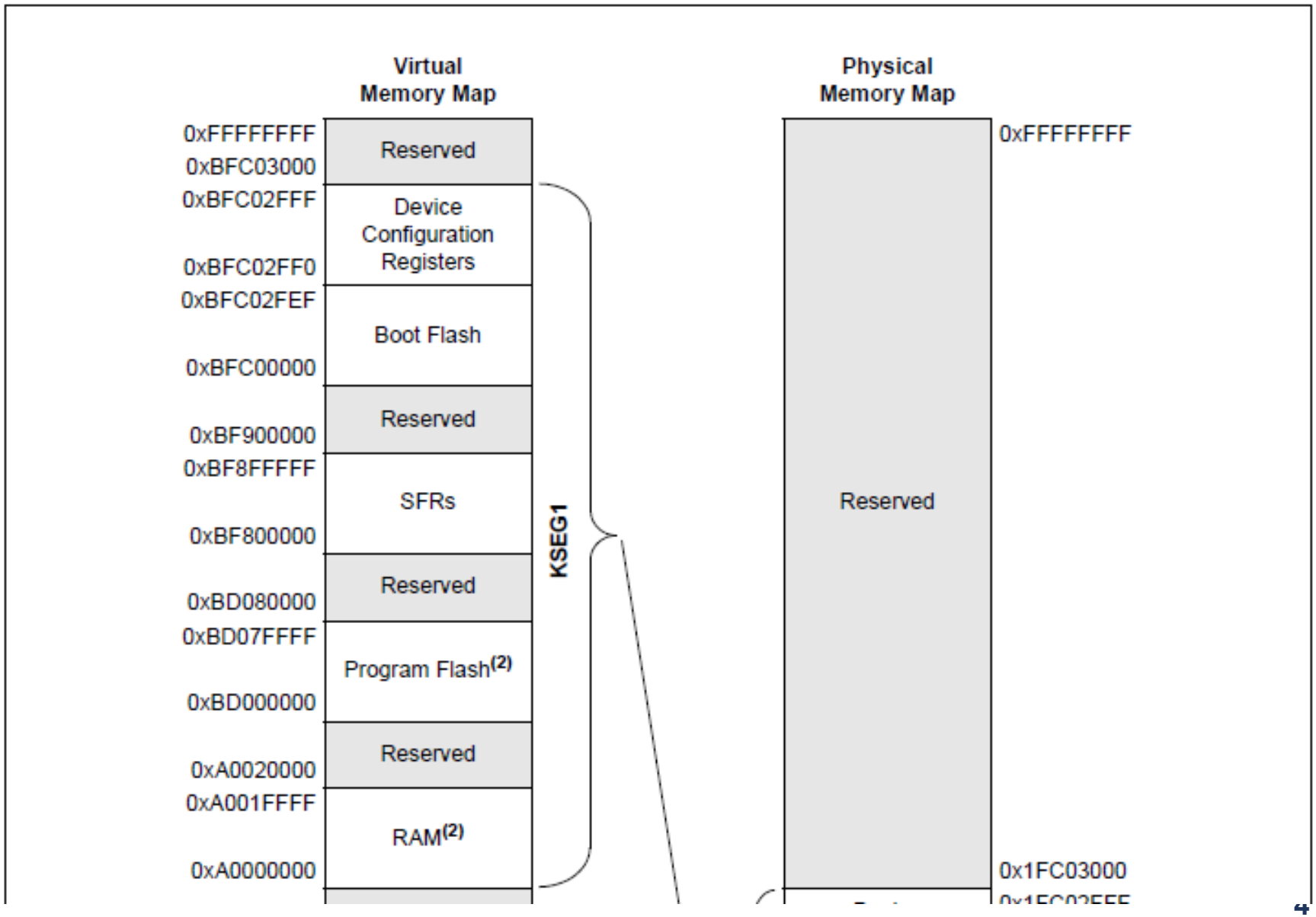
TRISG

PORTG

LATG

ODCG

FIGURE 4-6: MEMORY MAP ON RESET FOR PIC32MX695F512H, PIC32MX695F512L, PIC32MX795F512H AND PIC32MX795F512L DEVICES



From PIC32 Datasheet Table 4-24

Address 0xBF886000 TRISA

Address 0xBF886010 PORTA

Address 0xBF886020 LATA

Address 0xBF886030 ODCA

From PIC32 Datasheet Table 4-24

Address 0xBF886000 TRISA
Address 0xBF886004 TRISACLR
Address 0xBF886008 TRISASET
Address 0xBF88600C TRISAINV
Address 0xBF886010 PORTA
Address 0xBF886014 PORTACLR
Address 0xBF886018 PORTASET
Address 0xBF88601C PORTAINV
Address 0xBF886020 LATA
Address 0xBF886024 LATACLR
Address 0xBF886028 LATASET
Address 0xBF88602C LATAINV
Address 0xBF886030 ODCA
Address 0xBF886034 ODCACLR
Address 0xBF886038 ODCASET
Address 0xBF88603C ODCAINV

From PIC32 Datasheet Table 4-35

Address 0xBF886180 TRISG

Address 0xBF886190 PORTG

Address 0xBF8861A0 LATG

Address 0xBF8861B0 ODCG

From PIC32 Datasheet Table 4-35

Address 0xBF886180 TRISG
Address 0xBF886184 TRISGCLR
Address 0xBF886188 TRISGSET
Address 0xBF88618C TRISGINV
Address 0xBF886190 PORTG
Address 0xBF886194 PORTGCLR
Address 0xBF886198 PORTGSET
Address 0xBF88619C PORTGINV
Address 0xBF8861A0 LATG
Address 0xBF8861A4 LATGCLR
Address 0xBF8861A8 LATGSET
Address 0xBF8861AC LATGINV
Address 0xBF8861B0 ODCG
Address 0xBF8861B4 ODCGCLR
Address 0xBF8861B8 ODCGSET
Address 0xBF8861BC ODCGINV

GPIO OUTPUT

- Initialize bit n of Port G to perform normal output:

```
ODCGCLR = (1 << n);
TRISGCLR = (1 << n);
```

- Output a 1 on bit n of Port G:

```
LATGSET = (1 << n);
```

- Output a 0 on bit n of Port G:

```
LATGCLR = (1 << n);
```

GPIO INPUT

- Initialize bit n of Port G to perform input:

```
ODCGCLR = (1 << n);
TRISGSET = (1 << n);
```

- Read Port G:

```
int inval;
inval = PORTG;
```