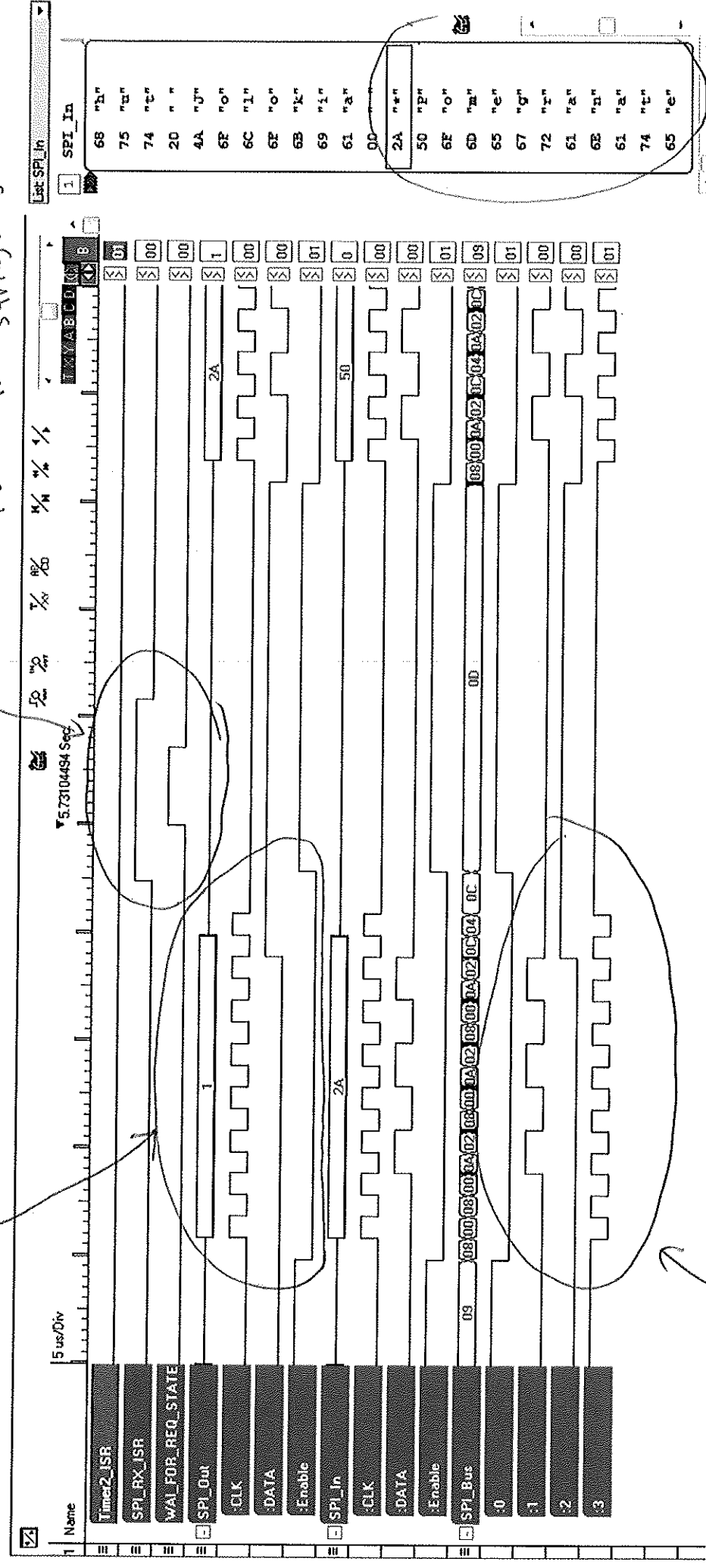5x size True Scale

SPI Example – from Logic Analyzer

Request for Fruit (from Master)

Note 1SR SPI RX Interrupt –
Also Note that 1SR is in the
"Waiting for Request" State
Takes approx. 3.5 µs to set up
strings to send.

Note how SPI is configured. Clock
is active low and data is set
on rising clock edge and read
on the falling clock edge.

String send by
SPI slave 3
"Pomegranate"

5 µs/Div

5.73104494 Seq

Name
Timer2_ISR
SPI_RX_ISR
WAL_FOR_REQ_STATE
SPI_Out
CLK
DATA
Enable
SPI_In
CLK
DATA
Enable
SPI_Bus
0
1
2
3

List: SPI_In

SPI_In
68 "h"
75 "u"
74 "t"
20 " "
4A "J"
6F "o"
6C "l"
6F "o"
6B "k"
69 "i"
61 "a"
0D
2A "*"
50 "P"
6F "o"
6D "m"
65 "e"
67 "g"
72 "r"
61 "a"
6E "n"
61 "a"
74 "t"
65 "e"

SPI Example – from Logic Analyzer – 50 µsec thru scale.
This is the complete string exchange on an SPI bus.

Note: Slave transmits a Ø to terminate the C-string.

List SPI_In

1	SPI_In
6C	"l"
6F	"o"
6B	"k"
69	"i"
61	"a"
00	""
2A	"*"
50	"P"
6F	"o"
6D	"m"
65	"e"
67	"g"
72	"r"
61	"a"
6E	"n"
61	"a"
74	"t"
65	"e"
00	" "
2A	"*"
4B	"K"
75	"u"
6D	"m"
71	"q"

▼5.73124871 Sec.

50 us/Div

Name
Timer2_ISR
SPI_RX_ISR
WAIT_FOR_REQ_STATE
SPI_Out
CLK
DATA
Enable
SPI_In
CLK
DATA
Enable
SPI_Bus
- 0
- 1
- 2
- 3