ECE 2534 - Homework 2 – Fall 2015
(Patterson section)
Due at Scholar before 5:00 pm on Sept. 8

Instructions: Work all of the problems, and submit your solutions to Scholar as a single document. Do not submit paper copies. It is okay to do the work by hand, and then scan those pages. The preferred format for submission is PDF, although MS Word is acceptable. Show your work to a reasonable extent, and clearly indicate your answers. In order to give you faster feedback, only a subset of these problems will be graded in detail.

You may use any appropriate reference materials, including things from ECE 2504 and the internet. You may share references with your classmates, but you may not share your solutions. The work that you submit must be your own.

Problem 1. The operation of a 4-to-1 multiplexer is described in the function table below:

| s_1	s_0	Mux output
0	0	x_0
0	1	x_1
1	0	x_2
1	1	x_3

The symbols $\{x_3, x_2, x_1, x_0\}$ represent the input "data" signals to the device, and symbols $\{s_1, s_0\}$ represent "select" signals that determine which one of the input signals will appear at the output. By convention, the binary pattern associated with the select signals will match the subscript of x_i. (For example, if $\{s_1, s_0\} = 10$, then x_2 is passed to the output.)

a) Write a Boolean logic equation that represents a 4-to-1 multiplexer. Use symbol F to represent the output.

b) Draw a logic diagram (using logic gates, not simply a multiplexer symbol) that matches your answer in part (a). (Neatness counts!)

Problem 2.
a) Create a function table for a 2-to-1 multiplexer. Follow the naming conventions given in the previous problem.

b) Draw a logic diagram (using logic gates, not simply a multiplexer symbol) that matches your answer in part (a).

Problem 3. The following logic diagram contains one standard logic gate (an inverter) and two 3-state gates (sometimes called tri-state gates). Each 3-state gate is indicated by the symbol "3.s." near its output, and each is enabled by an active-low signal shown at the side of the gate.
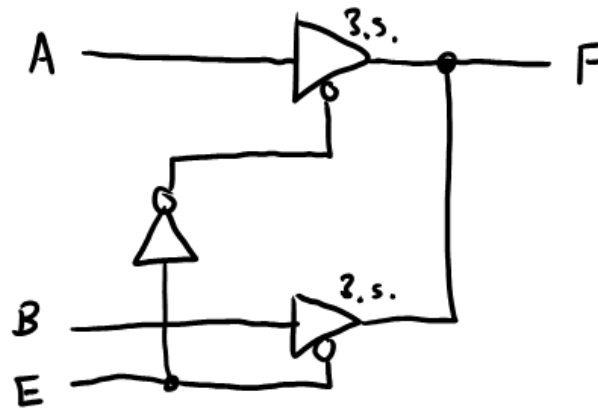
a) Write a Boolean equation that describes the output F of this logic diagram, as a function of the signals A, B, and E.

b) In what sense is the diagram shown above related to the concept of a multiplexer? Provide a brief description.

Problem 4. For this problem, assume that you are developing code in the C language for a 32-bit CPU such as the PIC32. As usual, bit position 0 refers to the least-significant bit. Write a C function that satisfies the description given in the header below. (Do not submit a separate source file for this problem; just place your code as text into the file containing your HW solutions. You are not required to compile and run your code, although that is recommended as a way for you to check your solution.)

```
/////////////////////////////////////////////
// Function name: getBitValue
// Input parameters:
//      val: an arbitrary integer
//      k:   an integer, assumed to be in the range [0, 31]
// Returns:
//      1 if val contains a 1 at bit position k; else return 0
//
int getBitValue ( int val, int k )
{
```

}

Problem 5. The flip-flops in the following diagram are positive-edge-triggered devices. Complete the timing diagram that is shown below. Assume that both flip-flops have been initialized to 0.

A

B — D Q | G0

D Q | G1 — F

CLK

CLK

A

B

Q0

Q1

F