一、4-bit synchronous binary up counter

(一)、Design Specification

Function : count from 0 to 15, and repeat.

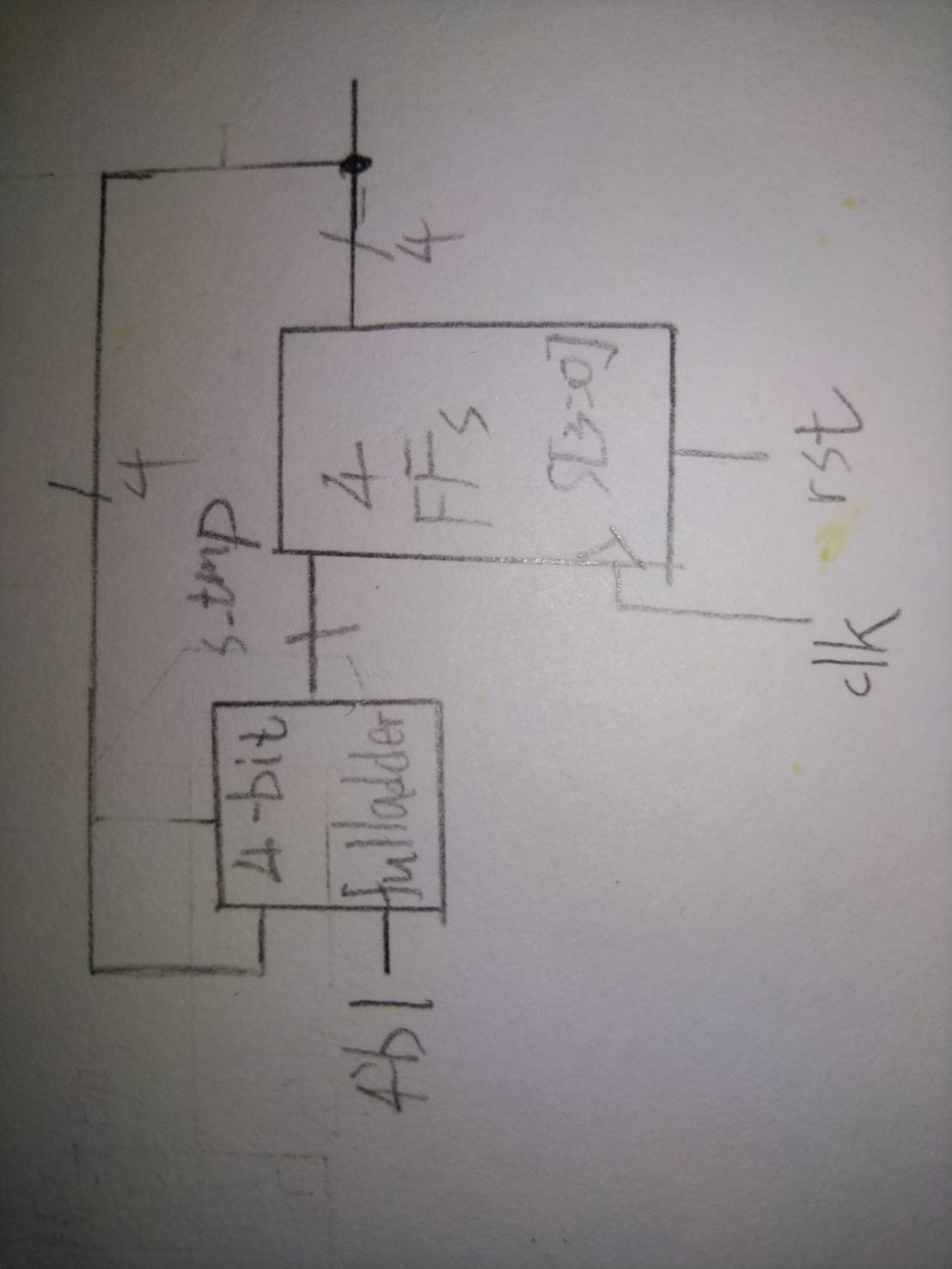
input : rst, clk

output : reg [3:0]s

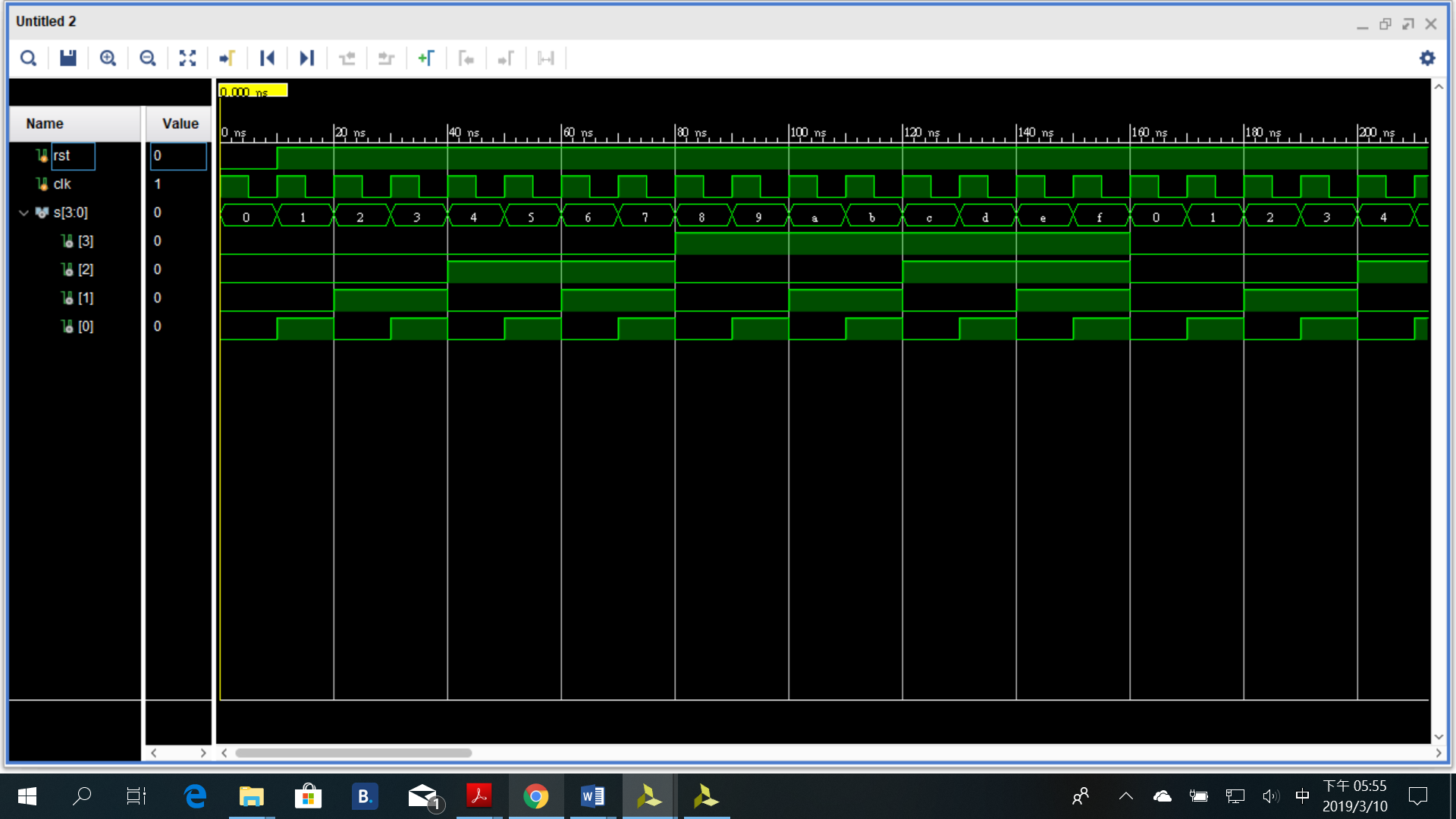
reg [3:0]s\_tmp(record number after plus 1)

(二)、Block diagram

First we need four DFFs to store the numbers, then we need a fulladder so the DFFs can be added continuously. Point s\_tmp is used to represent wire between DFFs and fulladder. Last rst was added to initial the value.



(三)、Testbench

From testbench, we can see that for every posedge clock, the DFFs will go up 1. And at 15,the value will overflow. So the value will go to zero.

二、8-bit ring register

(一)、Design Specification

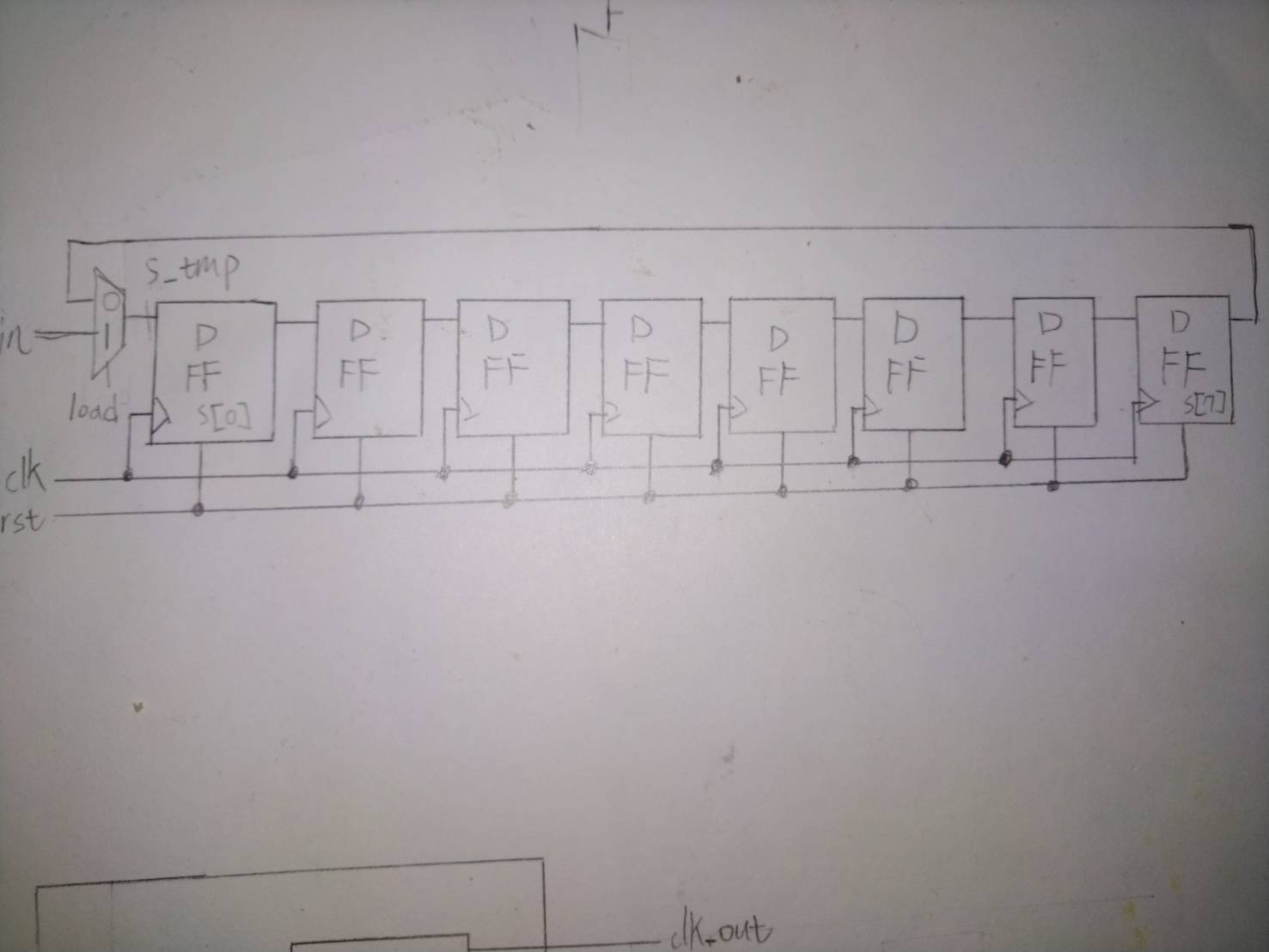
Function : shift every DFF’s number to next DFF also have ability to load number.

input : load(decide to load or not), in(load value), clk, rst

output : reg [7:0]s

reg s\_tmp (wire after selector)

(二)、Block diagram

First we need 8 DFFs to store the value, because the value will shift, so every DFF’s input value is the output of previous DFF’s value. And a selector was added to select the mode of load number or shifting. 

(三)、Testbench

From testbench we can see that the initial value is 01010101,and for every positive edge, the DFFs have shifted a bit.

三、討論

這一次的預報實驗也沒有很難做，也是都在複習上學期的基本觀念，然後實作到verilog上，基本上沒遇到太大問題。