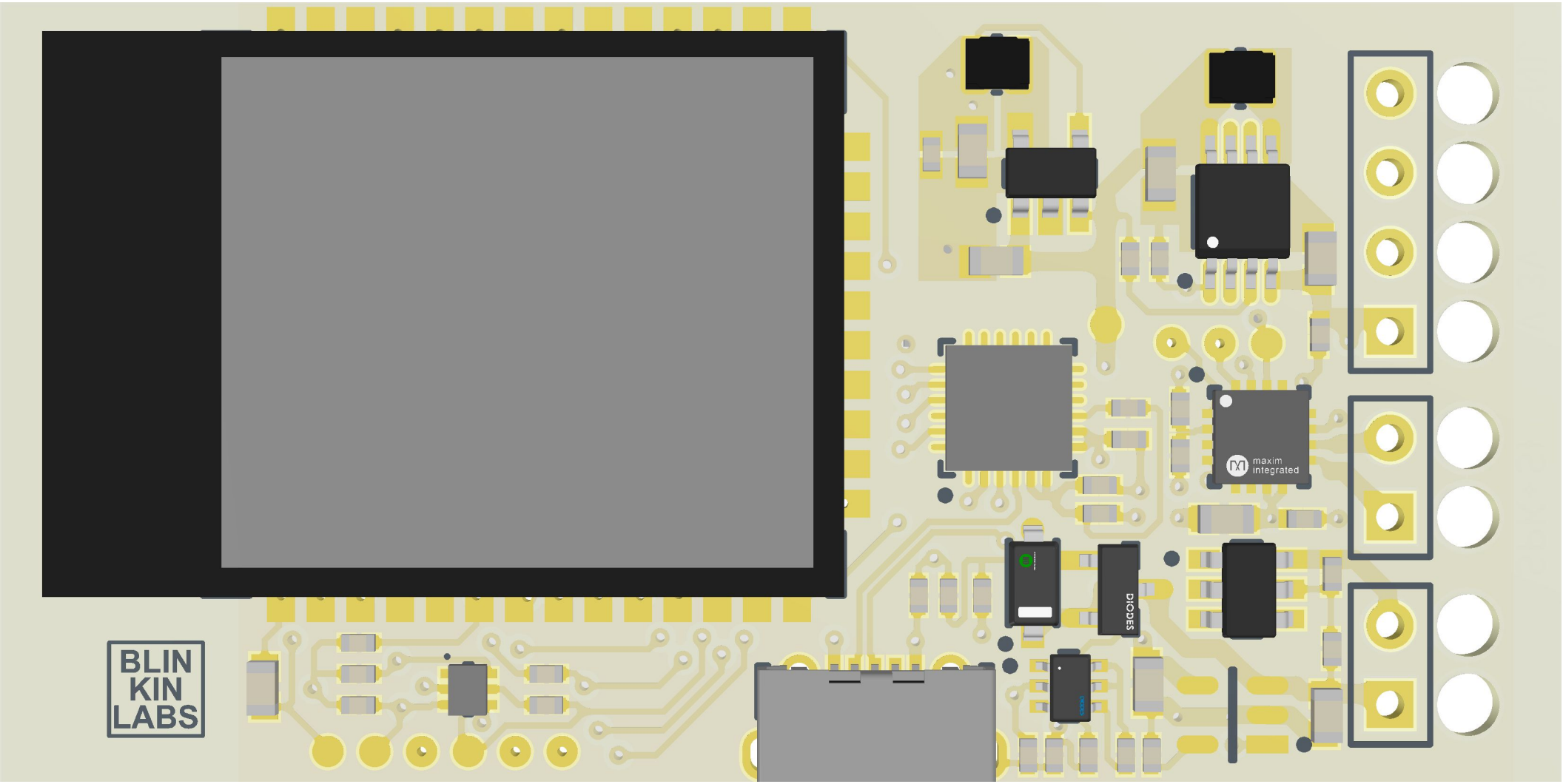
BLIN
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LABS
maxim
integrated
DIODES

Alles

3/22/2021
RevB

RELEASE

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

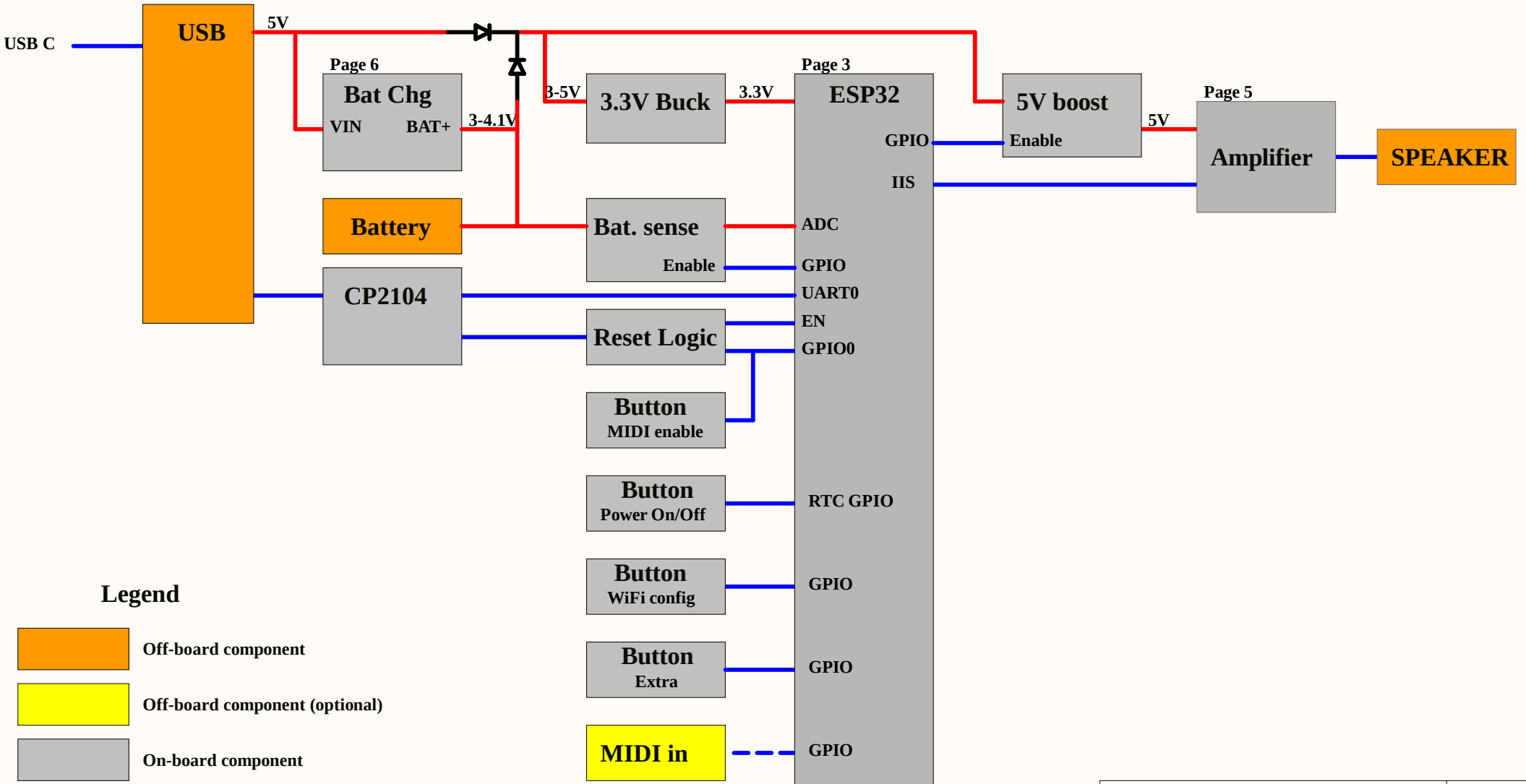
DESIGN NOTE:
Example text for critical design notes.

DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

Title: Cover Page		BLIN KIN LABS
Project: Alles	Revision: RevB	
Date: 3/22/2021 Time: 10:54:43 AM	Sheet 1 of 7	

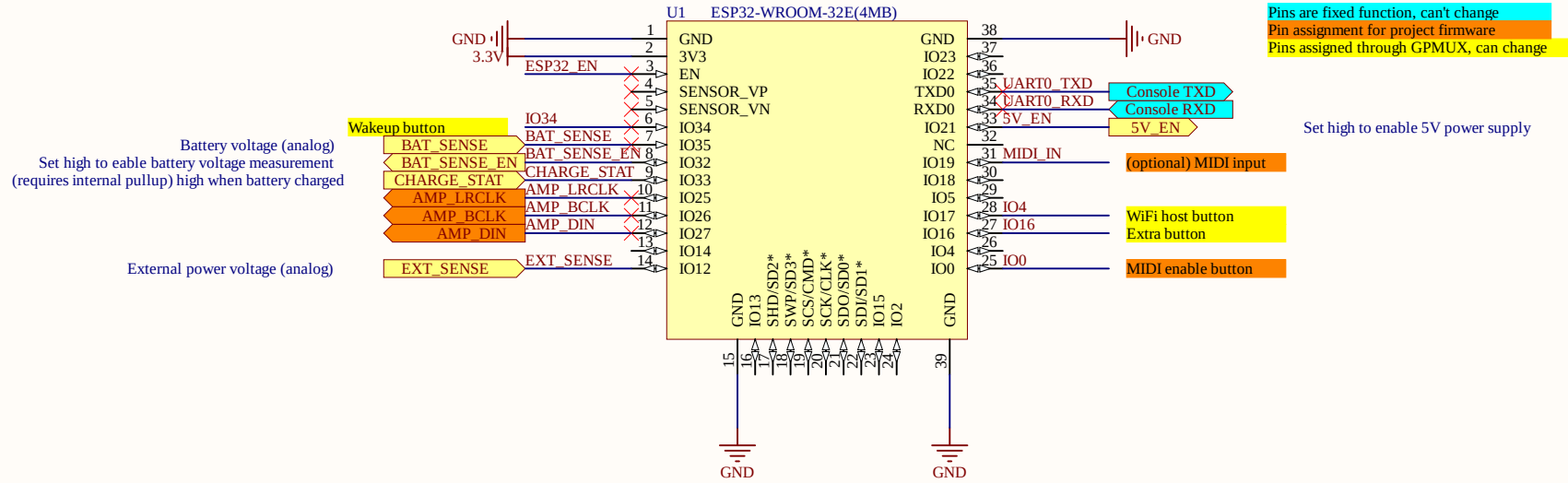
Alles



Title: Block Diagram		
Project: Alles		Revision: RevB
Date: 3/22/2021	Time: 10:54:43 AM	Sheet 2 of 7

BLIN KIN LABS

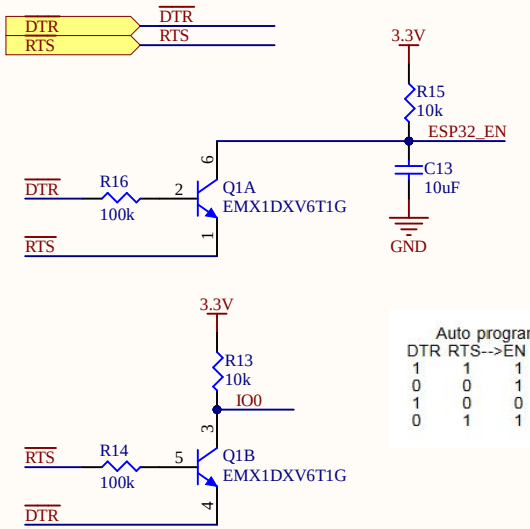
ESP32



Test points

AMP_BCLK TP4
AMP_LRCLK TP5
AMP_DIN TP3
ESP32_EN TP13
IO0 TP6
UART0_TXD TP17
UART0_RXD TP18
DTR TP19
RTS TP16

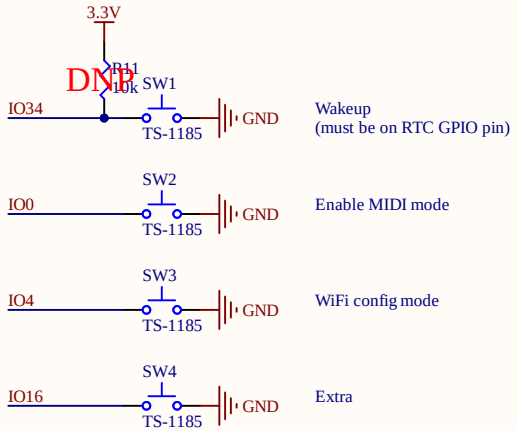
Auto-reset



Auto program

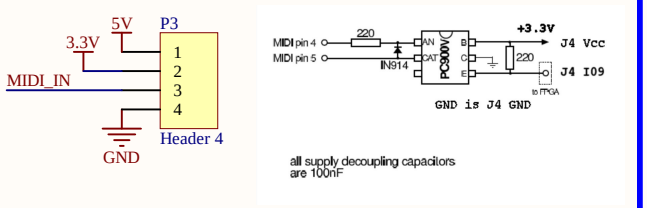
DTR	RTS-->EN	IO0	
1	1	1	1
0	0	1	1
1	0	0	1
0	1	1	0

Configuration buttons



Note: use 2.5mm tall buttons

Support for optional MIDI input

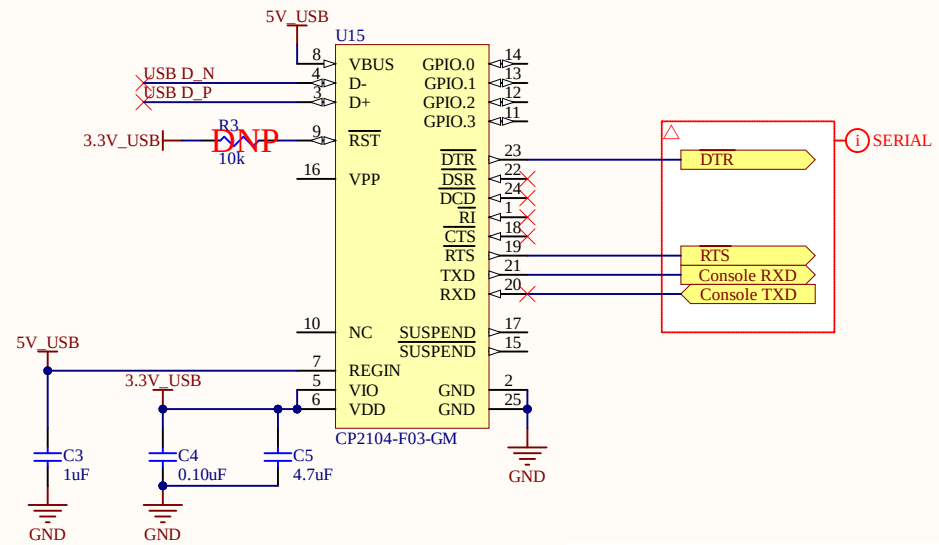


Title: ESP32			
Project: Alles		Revision: RevB	
Date: 3/22/2021	Time: 10:54:43 AM	Sheet 3 of 7	

BLIN KIN LABS

USB-to-Serial converter

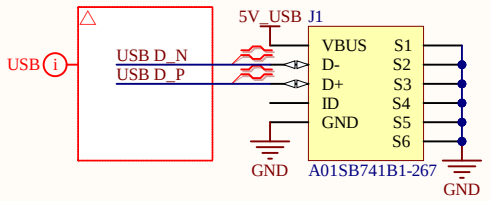
USB-to-Serial converter



Note: CP2104 configured in 'bus powered' mode

TODO: test that the ESP32 reset circuit doesn't back-power the serial converter while in battery mode

MicroUSB jack

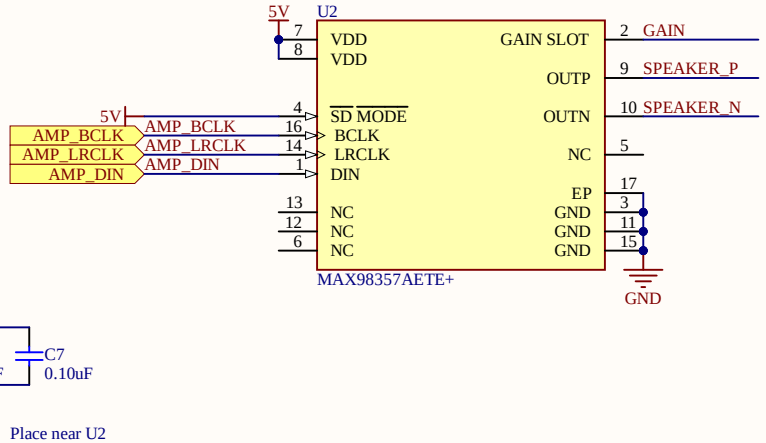


Title: USB-to-Serial converter		
Project: Alles	Revision: RevB	
Date: 3/22/2021 Time: 10:54:43 AM	Sheet 4 of 7	

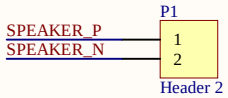
BLIN KIN LABS

Amplifier

Amplifier IC



Speaker output header



Amplifier gain

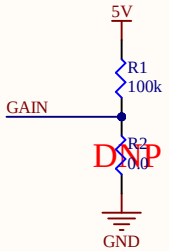


Table 8. Gain Selection

GAIN_SLOT	I²S/LJ GAIN (dB)
Connect to GND through 100kΩ ±5% resistor	15
Connect to GND	12
Unconnected	9
Connect to V_{DD}	6
Connect to V_{DD} through 100kΩ ±5% resistor	3

Note: GAIN tied high in project description, possible to change with resistor jumper

Expected power usage

Quiescent Current	I_{DD}	T_A = +25°C	2.75	3.35	mA
		T_A = +25°C, V_{DD} = 3.7V	2.4	2.85	
Shutdown Current	I_{SHDN}	SD_MODE = 0V, T_A = +25°C	0.6	2	µA
Standby Current	I_{STNDBY}	SD_MODE = 1.8V, no BCLK, T_A = +25°C	340	400	µA

Maximum power calculation:

Speaker is 4ohm
Gain is set to 6dB

According to the datasheet 'electrical characteristics' table, maximum power output with 12dB setting into 4ohm load is 3.2W. From the 'efficiency vs output power' section, the efficiency with a 4ohm speaker is roughly 80%, so the input power would need to be 4W. Finally, to derate the power output to a 6dB setting, the maximum output would be 1/4 of the 12dB setting, or 1W.

Using that number, the maximum input current to the device with a 5V power supply can be calculated as:

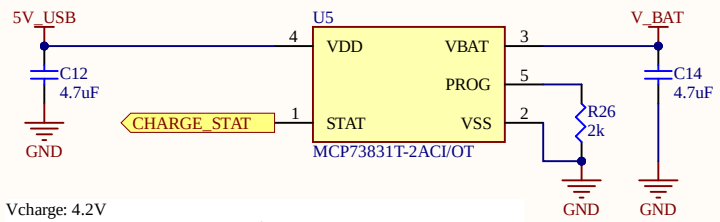
P=V*I so I = 1/5 = .2A

Title: DAC		
Project: Alles		Revision: RevB
Date: 3/22/2021	Time: 10:54:43 AM	Sheet 5 of 7

BLIN KIN LABS

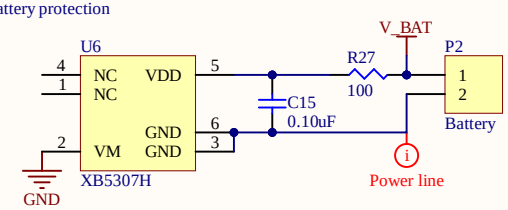
Power Supply

Battery charger



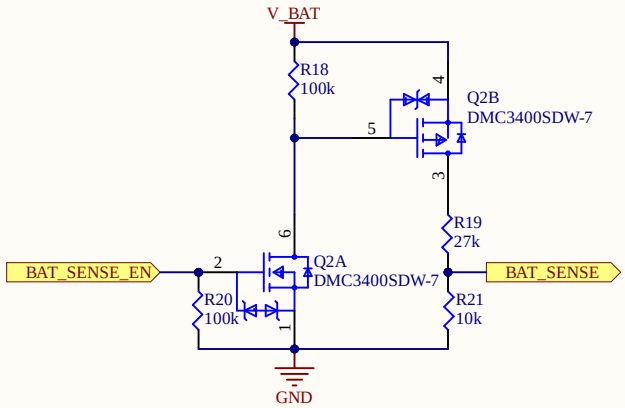
Vcharge: 4.2V
max charge current: 500mA @2K reference

Battery protection

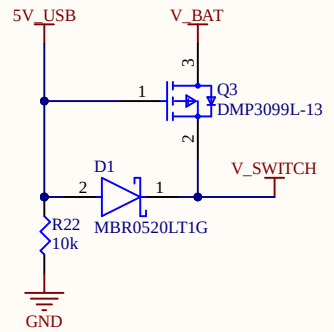


Vovercharge: 4.425V (4.25V release)
Vunderdischarge: 2.9V (3.0V release)
Overcurrent: 5A
Normal power consumption: 2.8uA

Battery sense (enable only when measuring battery)

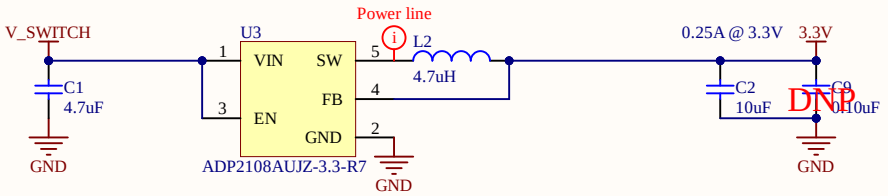


Power in with battery switchover



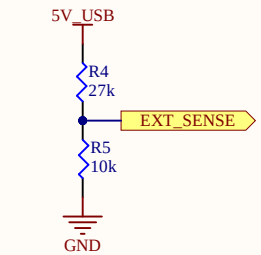
See Microchip App note AN1149

3.3V, low quiescent current supply (always on)

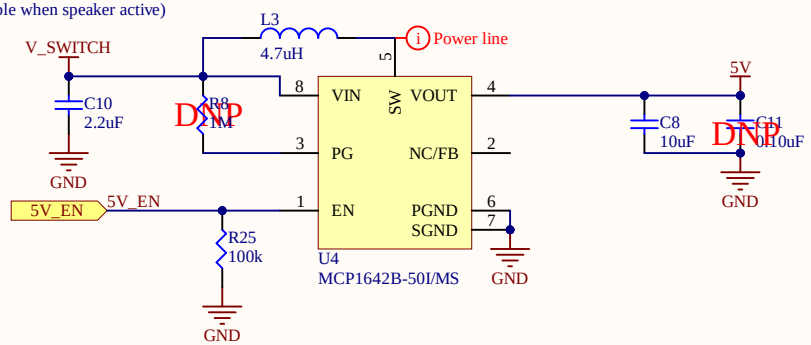


Power draw in hibernation mode:
* ADP2108 has 18uA quiecenct current
* low load efficiency = 88%, esp takes 10uA in deep sleep/hibernate
* Total <50uA @battery

External power sense



5V boost (enable when speaker active)



Power delivery requirements:

.2A @ 5V (amplifier)
.25A @ 3.3V (esp32, WiFi TX, periodic)
.1A @ 3.3V (esp32, WiFi RX)

Power line 5V_USB
Power line V_SWITCH
Power line 5V
Power line 3.3V
Power line V_BAT
Power line GND

TP1 V_SWITCH

Title: Power Supply		
Project: Alles		Revision: RevB
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BLIN KIN LABS

Designator
[01] cover page.SchDoc

Designator
[02] Block Diagram.SchDoc

Designator
[03] ESP32.SchDoc

Designator
[04] Serial Console.SchDoc

Designator
[05] Amplifier.SchDoc

Designator
[06] Power Supply.SchDoc

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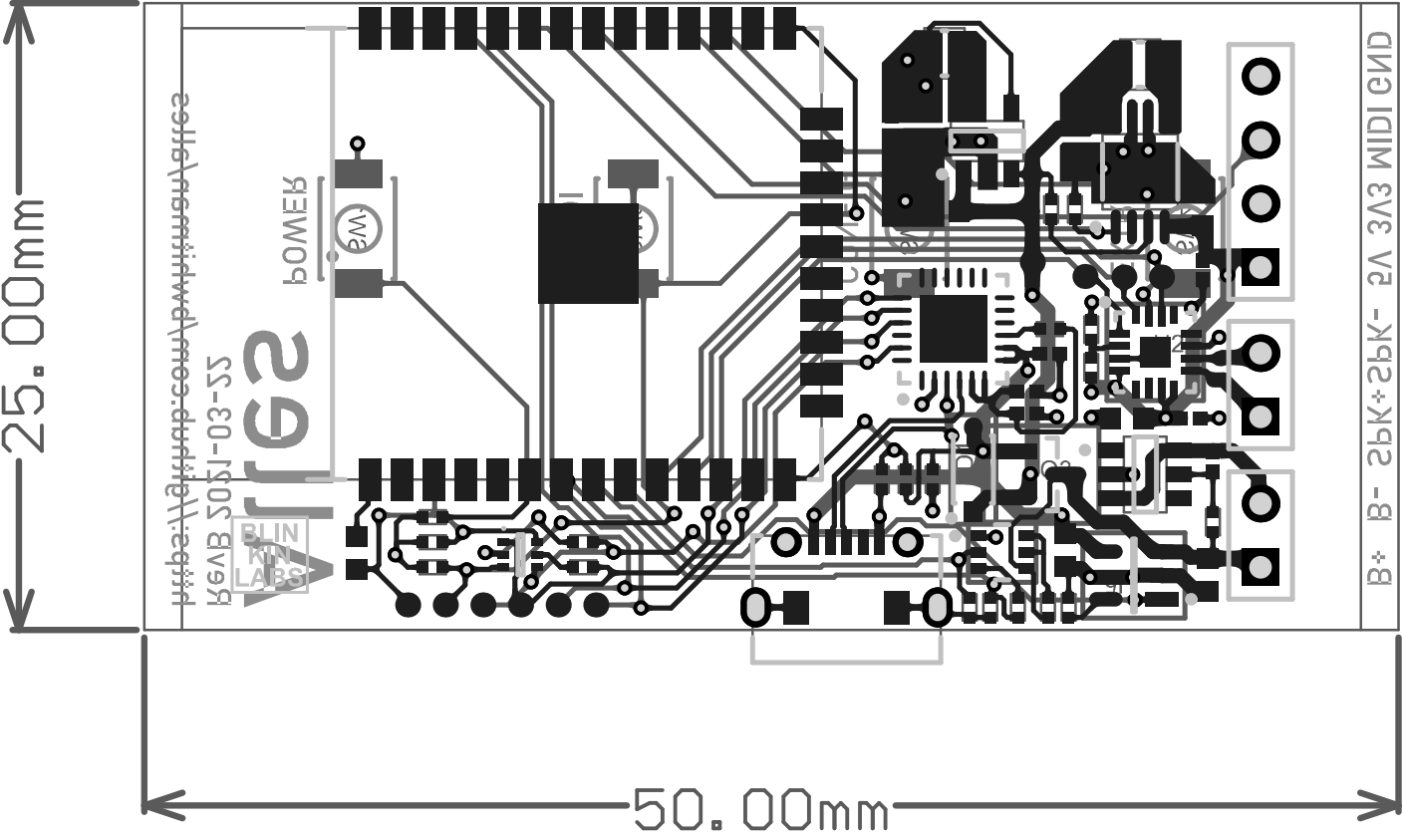
Title: *		BLIN KIN LABS
Project: Alles.PrjPcb	Revision: RevB	
Date: 3/22/2021 Time: 10:54:43 AM	Sheet 7 of 7	



Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	SM-001	0.013mm	4
1	Top Layer	Copper	0.035mm	
	Dielectric 2	PP-022	0.200mm	4.6
2	Layer 1	Copper	0.018mm	
	Dielectric 3	Core-039	0.665mm	4.8
3	Layer 2	Copper	0.018mm	
	Dielectric 4	PP-022	0.200mm	4.6
4	Bottom Layer	Copper	0.035mm	
	Bottom Solder	SM-001	0.013mm	4
	Bottom Overlay			
Total board thickness:			1.197mm	

Design Rules Verification Report

Filename : C:\Users\matt\Blinkinlabs-Repos\alles-pcb\pcb\Alles.PcbDoc

Warnings 0
Rule Violations 15

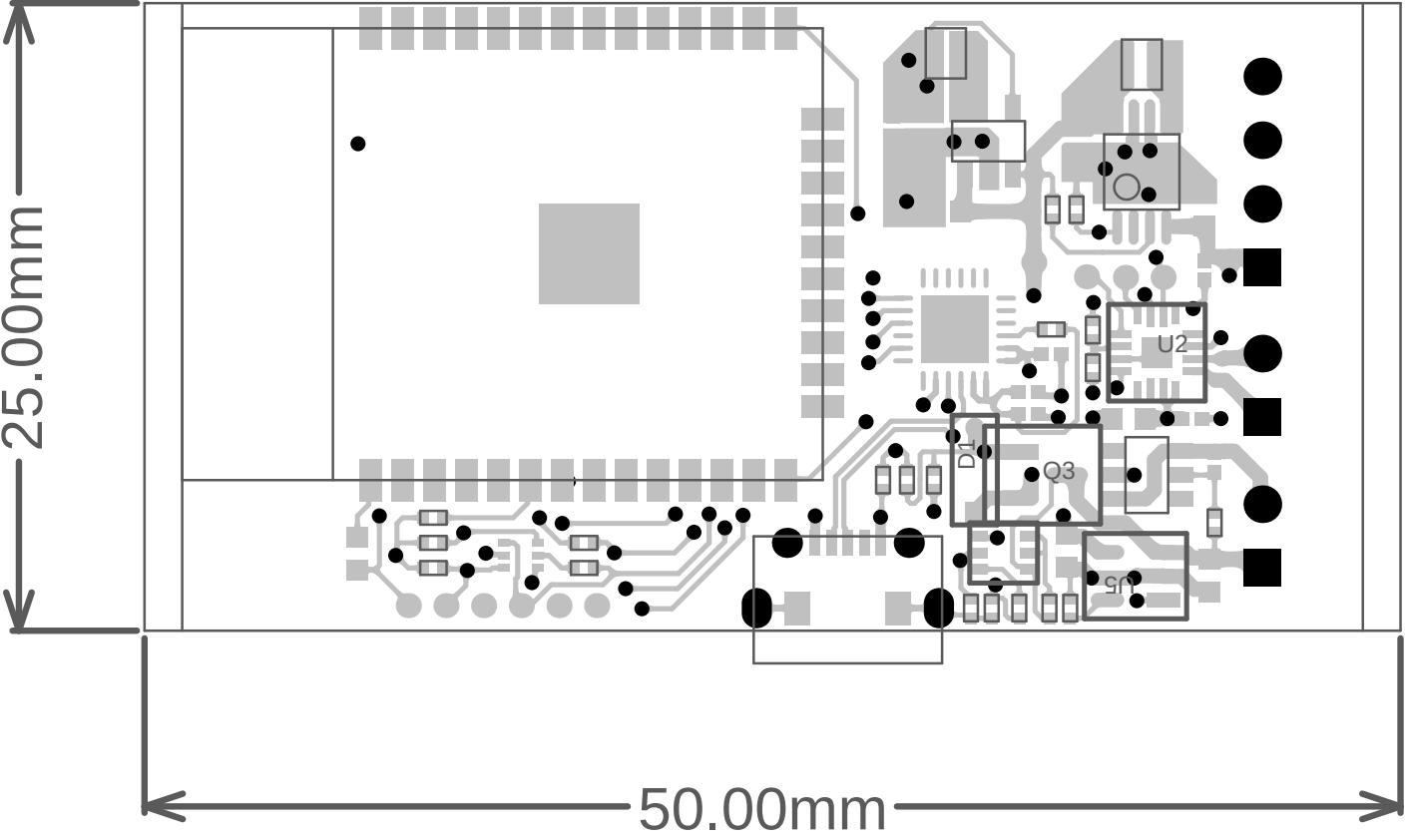
Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	15
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.2mm) (Max=0.6mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Component Clearance Constraint (Horizontal Gap = 0.254mm, Vertical Gap = 0.254mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	15

Clearance Constraint (Gap=0.2mm) (All),(All)
Clearance Constraint: (0.193mm < 0.2mm) Between Track (27.447mm,3.597mm)(27.447mm,4.075mm) on Top Layer And
Clearance Constraint: (0.193mm < 0.2mm) Between Track (27.447mm,3.597mm)(27.447mm,4.075mm) on Top Layer And
Clearance Constraint: (0.127mm < 0.2mm) Between Track (27.447mm,4.075mm)(27.509mm,4.137mm) on Top Layer And
Clearance Constraint: (0.127mm < 0.2mm) Between Track (27.447mm,4.075mm)(27.509mm,4.137mm) on Top Layer And
Clearance Constraint: (0.193mm < 0.2mm) Between Track (27.447mm,4.075mm)(27.509mm,4.137mm) on Top Layer And
Clearance Constraint: (0.127mm < 0.2mm) Between Track (27.509mm,4.137mm)(27.509mm,6.138mm) on Top Layer And
Clearance Constraint: (0.127mm < 0.2mm) Between Track (27.509mm,4.137mm)(27.509mm,6.138mm) on Top Layer And
Clearance Constraint: (0.127mm < 0.2mm) Between Track (27.509mm,4.137mm)(27.509mm,6.138mm) on Top Layer And
Clearance Constraint: (0.193mm < 0.2mm) Between Track (27.509mm,4.137mm)(27.509mm,6.138mm) on Top Layer And
Clearance Constraint: (0.127mm < 0.2mm) Between Track (27.509mm,6.138mm)(29.719mm,8.347mm) on Top Layer And
Clearance Constraint: (0.127mm < 0.2mm) Between Track (27.509mm,6.138mm)(29.719mm,8.347mm) on Top Layer And
Clearance Constraint: (0.127mm < 0.2mm) Between Track (27.509mm,6.138mm)(29.719mm,8.347mm) on Top Layer And
Clearance Constraint: (0.127mm < 0.2mm) Between Track (27.841mm,6mm)(29.856mm,8.015mm) on Top Layer And Track
Clearance Constraint: (0.127mm < 0.2mm) Between Track (29.719mm,8.347mm)(32.25mm,8.347mm) on Top Layer And
Clearance Constraint: (0.127mm < 0.2mm) Between Track (29.719mm,8.347mm)(32.25mm,8.347mm) on Top Layer And

Electrical Rules Check Report

Class	Document	Message
Warning	[03] ESP32.SchDoc	5V_EN contains IO Pin and Output Port objects (Pin U1-33, Port 5V_EN).
Warning	[03] ESP32.SchDoc	BAT_SENSE_EN contains IO Pin and Output Port objects (Pin U1-8, Port BAT_SENSE_EN).
Warning	[03] ESP32.SchDoc	CHARGE_STAT contains IO Pin and Input Port objects (Pin U1-9, Port CHARGE_STAT).
Warning	[04] Serial Console.SchDoc	Component U15 CP2104-F03-GM at 2400mil,5600mil: Component revision is Out of Date.
Warning	[03] ESP32.SchDoc	EXT_SENSE contains IO Pin and Input Port objects (Pin U1-14, Port EXT_SENSE).
Warning	[06] Power Supply.SchDoc	Floating Power Object 3.3V at (8600mil,2200mil)
Warning	[06] Power Supply.SchDoc	Floating Power Object 5V at (8600mil,2400mil)
Warning	[06] Power Supply.SchDoc	Floating Power Object 5V_USB at (8600mil,2800mil)
Warning	[06] Power Supply.SchDoc	Floating Power Object GND at (8600mil,1800mil)
Warning	[06] Power Supply.SchDoc	Floating Power Object V_BAT at (8600mil,2000mil)
Warning	[06] Power Supply.SchDoc	Floating Power Object V_SWITCH at (8600mil,2600mil)



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3	Layer 2	Copper	0.018mm	
	Dielectric 4	PP-022	0.200mm	4.6
4	Bottom Layer	Copper	0.035mm	
	Bottom Solder	SM-001	0.013mm	4
	Bottom Overlay			
Total board thickness:			1.197mm	

C13
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C11
C10
C9
C8
C7
C6
C5
C4
C3
C2
C1
R10
R9
R8
R7
R6
R5
R4
R3
R2
R1
D1
Q1
Q2
U1
U2
U3
U4
J1
J2
J3
J4
J5
J6
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