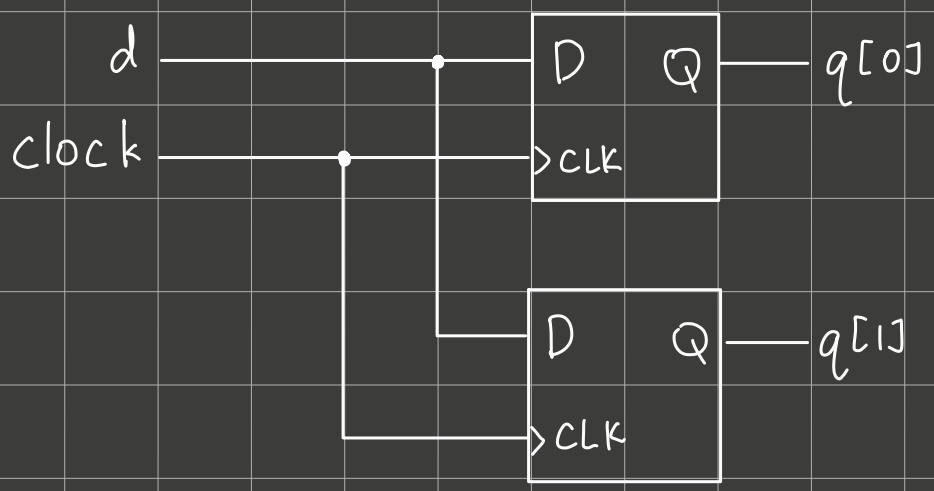
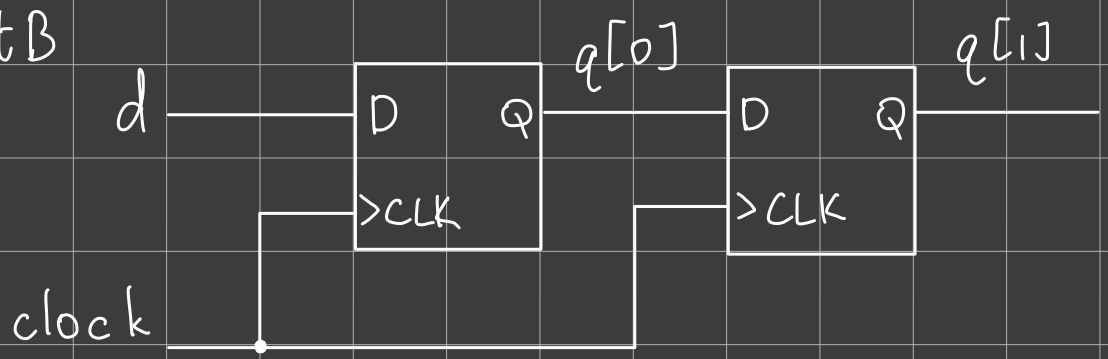
6231358221 วิภาวรรณ เต็มธีรภัจ

5.1) shift A



shift B



5.2) blocking (=) จะทำค่าสั่งตามลำดับจากบนลงล่าง

nonblocking (<=) จะทำทุกค่าสั่งพร้อมกัน

5.3) Yes, using nonblocking. For 8 bits

```
module shiftReg #(parameter MSB = 8) (
    output [MSB-1:0] q,
    input d,
    input clock);

always @(posedge clock)
begin
    q <= {q[MSB-2:0], d};
end
endmodule
```