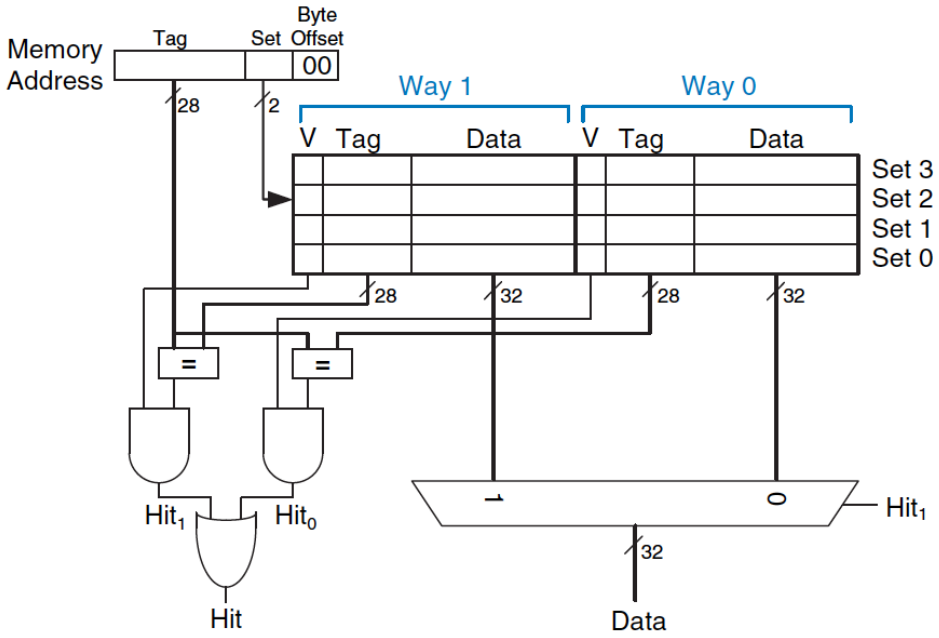

Assume we are working with the 2-way associative cache setup above.

1. Where is the address 0x0001309C mapped?

2. Give two addresses that will conflict with the address from (1).

3. Assume the cache is initially empty, but it updates after each read. Are each of the following memory lookups hits or misses? Assume the **least recently used** address is removed from the cache when there is a conflict.

Memory address	Hit/miss?
0x00001308	
0x000013C8	
0x00001308	
0x00001388	
0x00001308	
0x000013C8	
0x00001304	
0x000013C4	
0x00001304	

4. How would (3) have been different if we were working with a direct-mapped cache?

5. If a direct-mapped cache has n bits for its tag, how many does a 2-way set associative cache of the same size have?

6. Assume memory is 32-bit addressable. If a 2-way set associative cache holds one word per block and the tag field is 17 bits long, how many sets are there in the cache? How much data can be stored in the cache?