Pipelined Processor

Recall

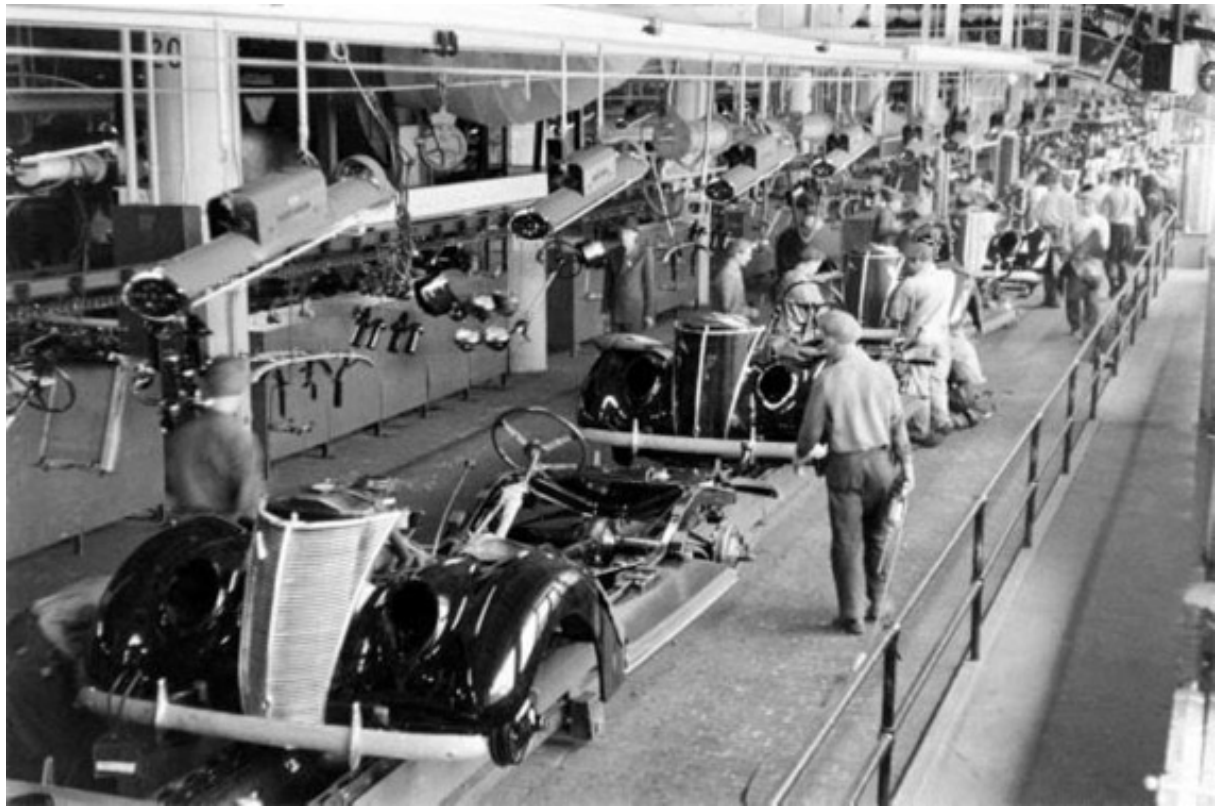
Latency: Time required for one piece of information to pass through the system from start to finish.

Inputs producing outputs.

Througput: how much information can be produced at a given time.

Parallelism

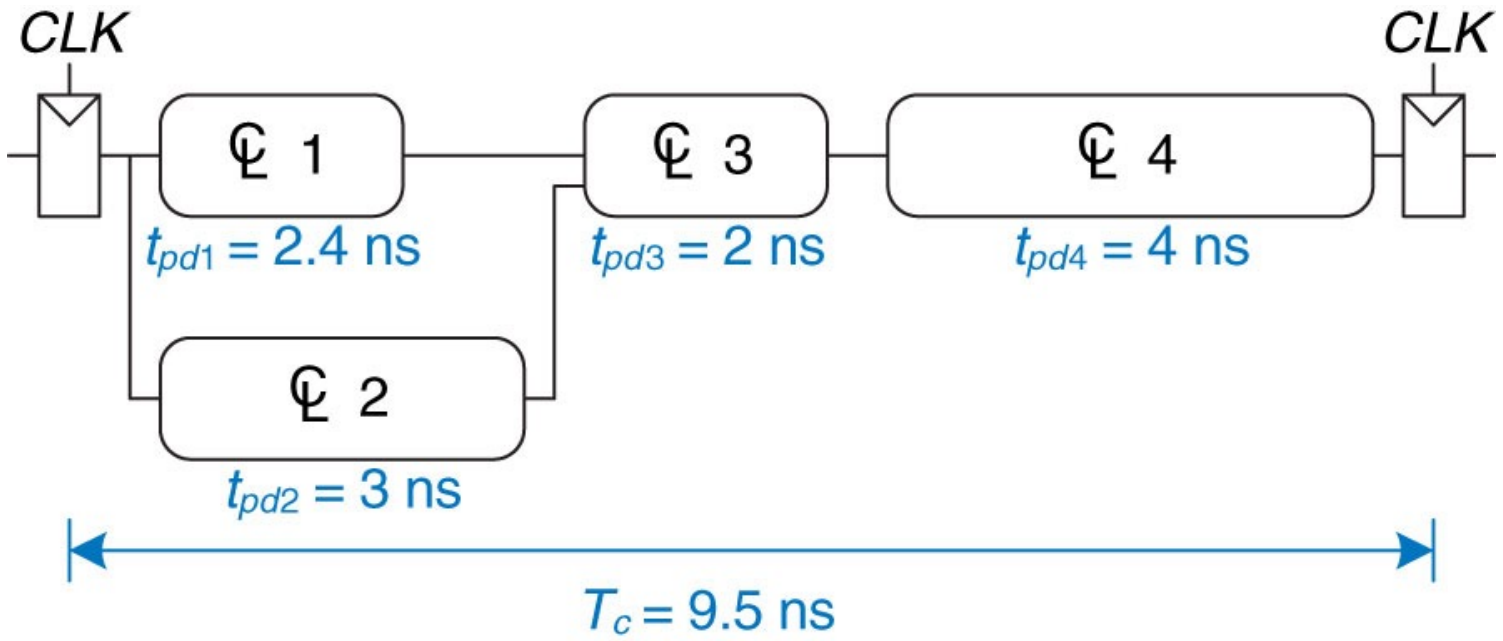
Spatial Parallelism

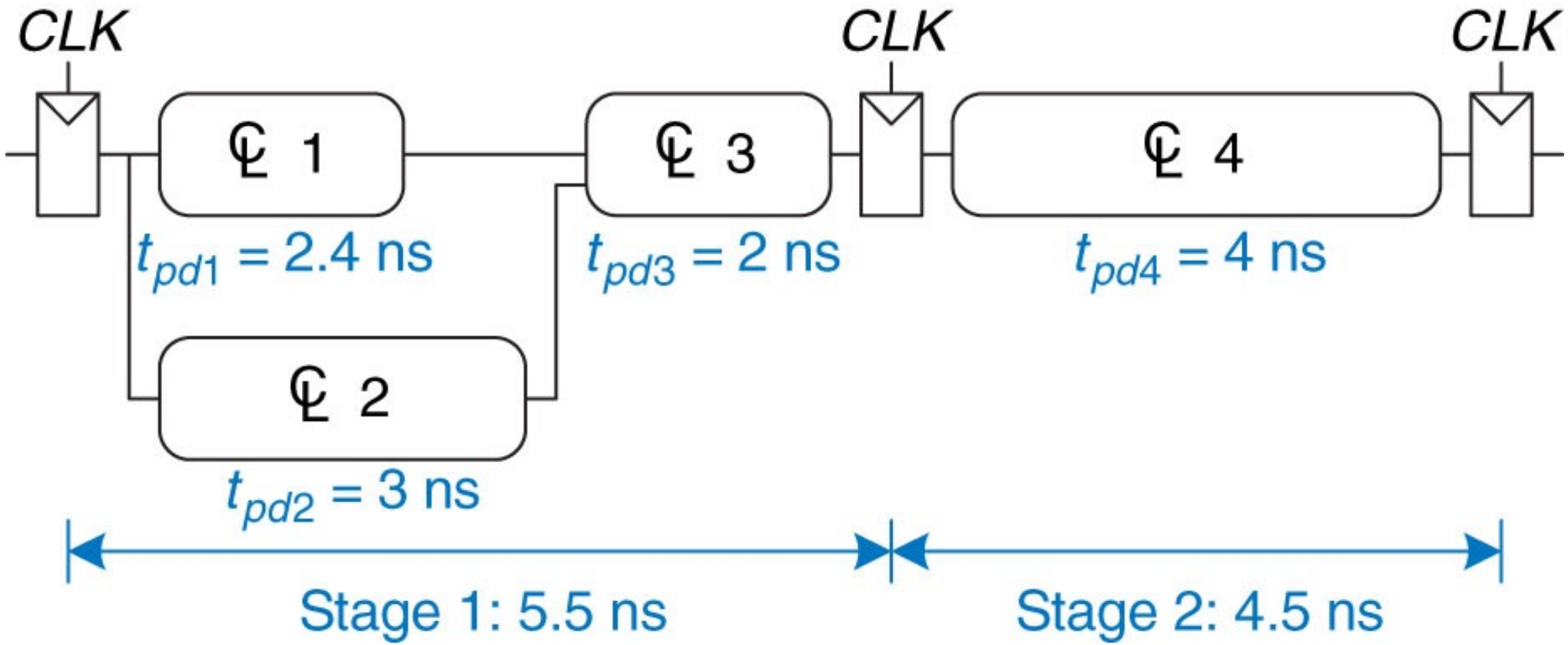


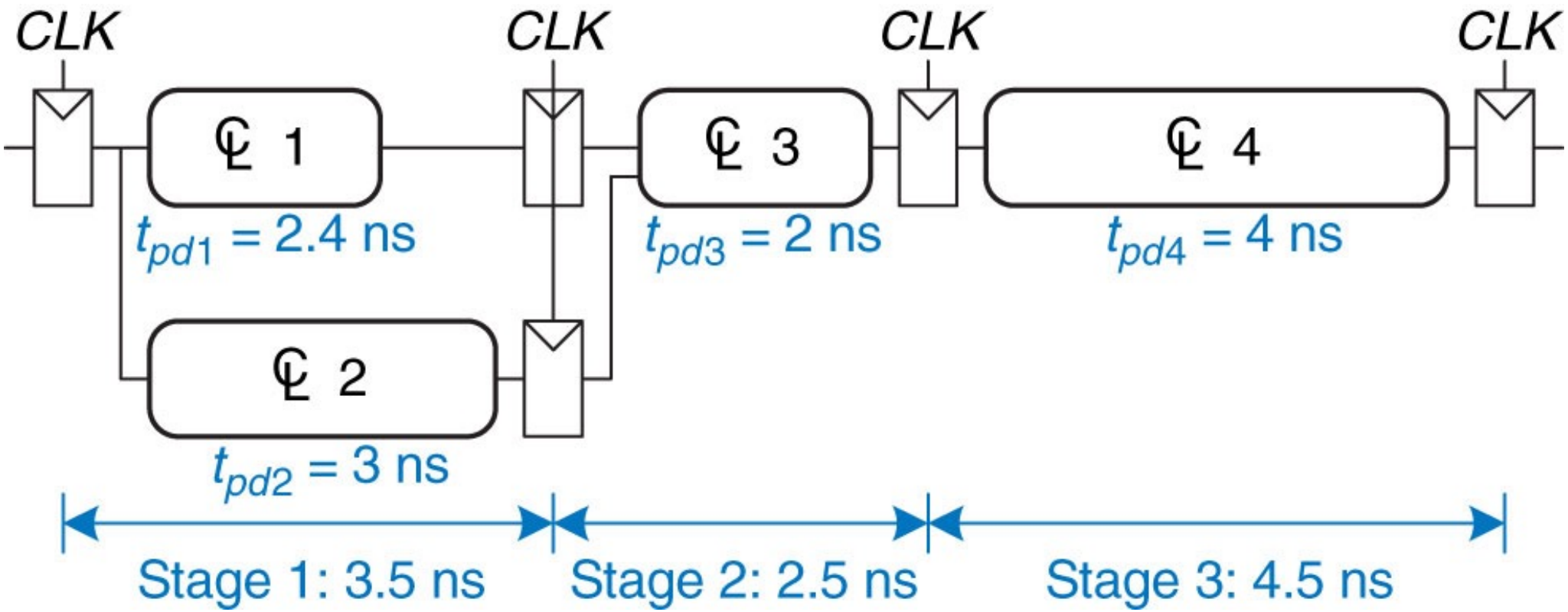
Temporal Parallelism

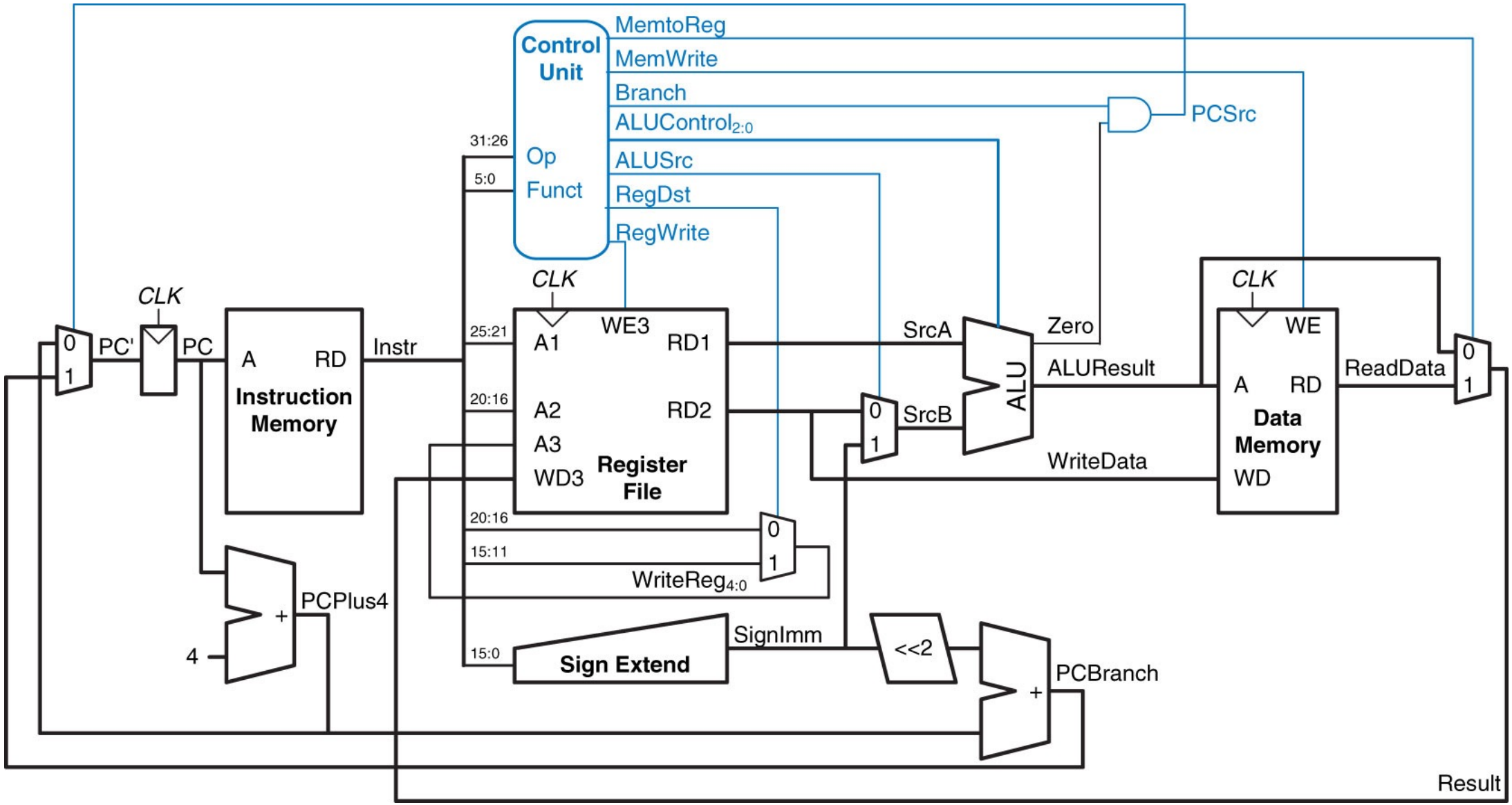
Pipelining

Temporal parallelism involves breaking the system up into chunks, with registers in between to allow multiple simultaneous operations.




CLK
CLK
CLK
1
3
4
2
t_{pd1} = 2.4 ns
t_{pd3} = 2 ns
t_{pd4} = 4 ns
t_{pd2} = 3 ns
Stage 1: 5.5 ns
Stage 2: 4.5 ns


CLK
CLK
CLK
CLK
1
2
3
4
t_{pd1} = 2.4 ns
t_{pd2} = 3 ns
t_{pd3} = 2 ns
t_{pd4} = 4 ns
Stage 1: 3.5 ns
Stage 2: 2.5 ns
Stage 3: 4.5 ns


Control Unit
MemtoReg
MemWrite
Branch
ALUControl2:0
ALUSrc
RegDst
RegWrite
Op
Funct
31:26
5:0
PCSrc
CLK
PC'
PC
A
RD
Instruction Memory
Instr
25:21
20:16
A1
A2
A3
WD3
WE3
RD1
RD2
Register File
SrcA
SrcB
ALU
Zero
ALUResult
WriteData
WE
Data Memory
WD
ReadData
0
1
20:16
15:11
WriteReg4:0
PCPlus4
4
+
15:0
Sign Extend
SignImm
<<2
PCBranch
Result

Identify Delay

Reading/writing memory, using the ALU are typically the biggest delay.

Five stages mean each stage executes one of these slow steps.

Fetch, Decode, Execute, Memory, Writeback

Fetch:

Processor reads instruction from instruction memory

Decode:

Read source operands from the register file and decode to produce instruction signals.

Execute:

ALU computation

Memory:

Read/write data memory

Writeback:

Processor writes the results to a register file.

Pipelined Datapath

Cutting the single-cycle CPU into a pipeline implementation requires adding registers to store state.

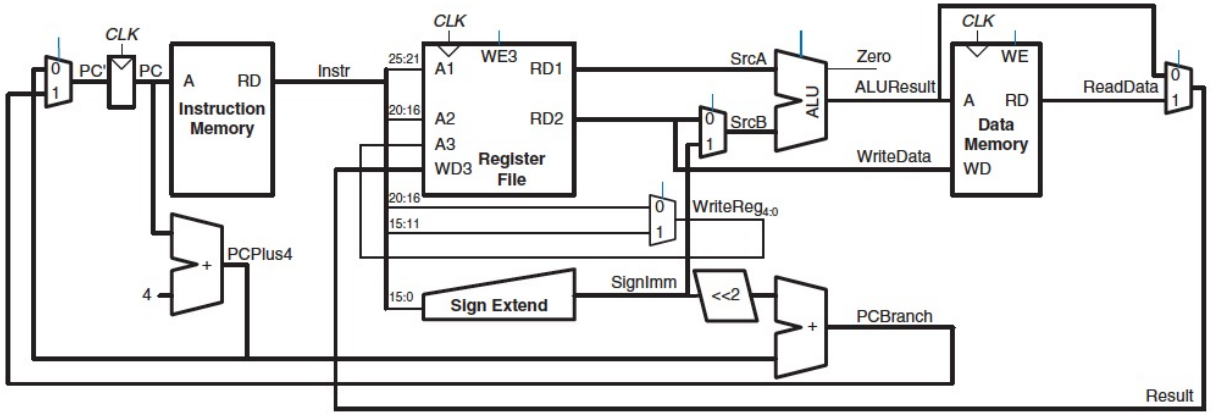
All signals associated with a particular instruction must advance in unison.

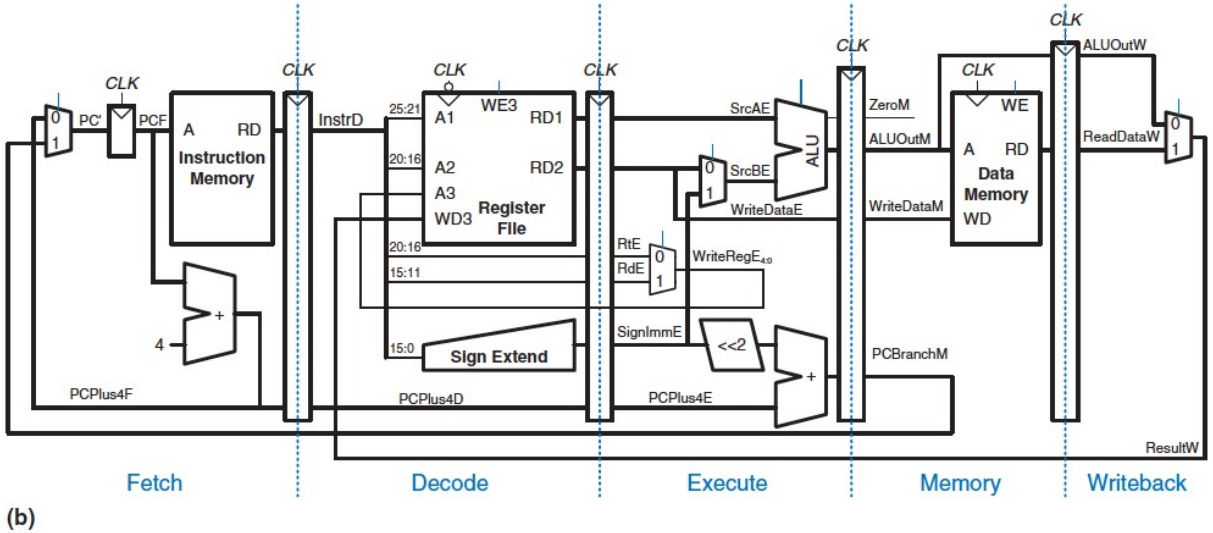
Can you find the error in the figure?

Next figure corrects the datapath.

Also an issue with PC' logic, might be updated in Fetch or Memory stages.

Fix this hazard later.





Pipelined Control

Same control signals that we've seen before.

But we must pipeline control signals along with the datapath to keep them synchronized.

RegWrite must be pipelined into Writeback stage before it feeds back to the register file.