Pipeline Performance

Why Pipeline?

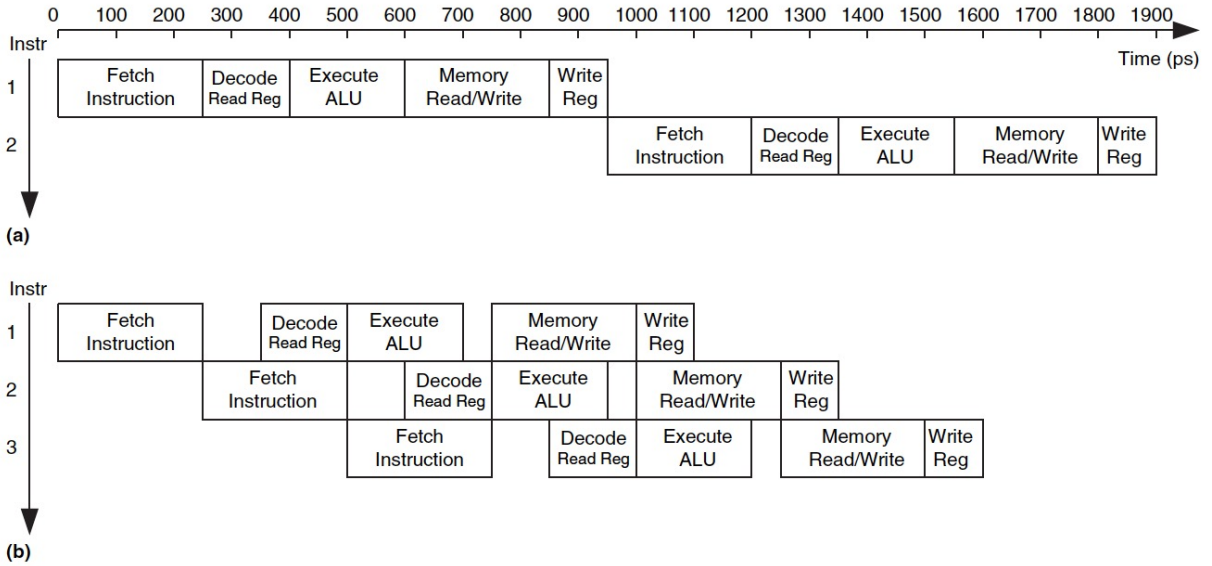
Improve throughput of a digital system.

Latency is slightly changed.

Throughput is *ideally* five times faster

Which is more important, throughput or latency for a modern processor?

Pipelining is done by all modern processors.



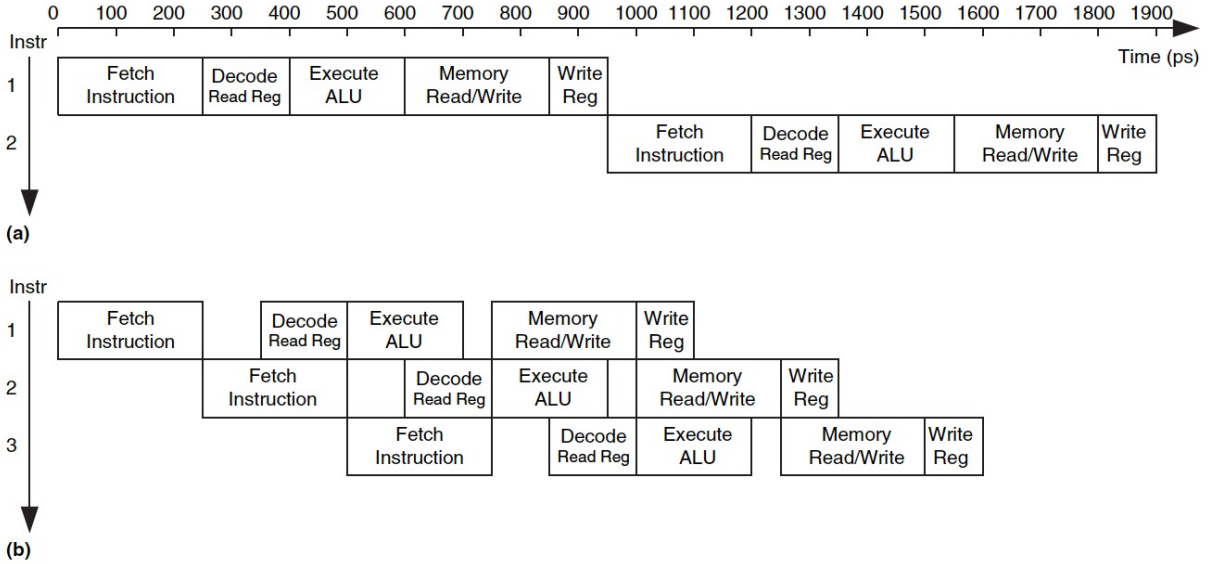
Timing Comparison

Single-Cycle Processor:

Instruction read at time 0, then executed.

950ps latency, throughput of 1 instruction/950ps (1.05 billion instructions per second)

What about pipelined processor with 250ps clock cycle?



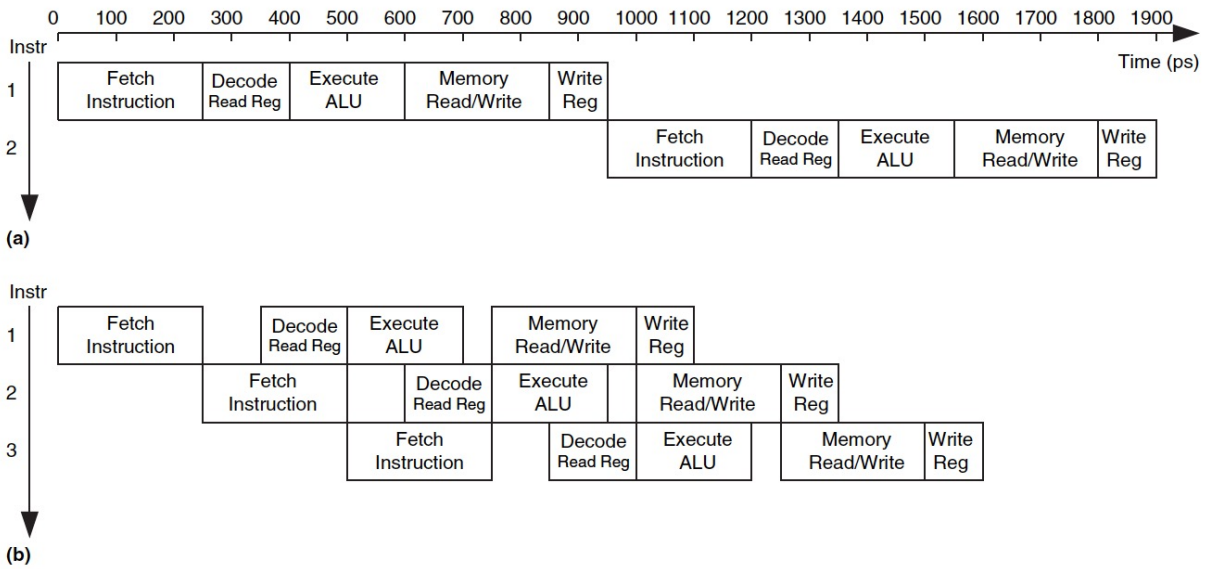
Timing Comparison

Length of the pipeline is set at 250ps by the slowest stage (memory access)

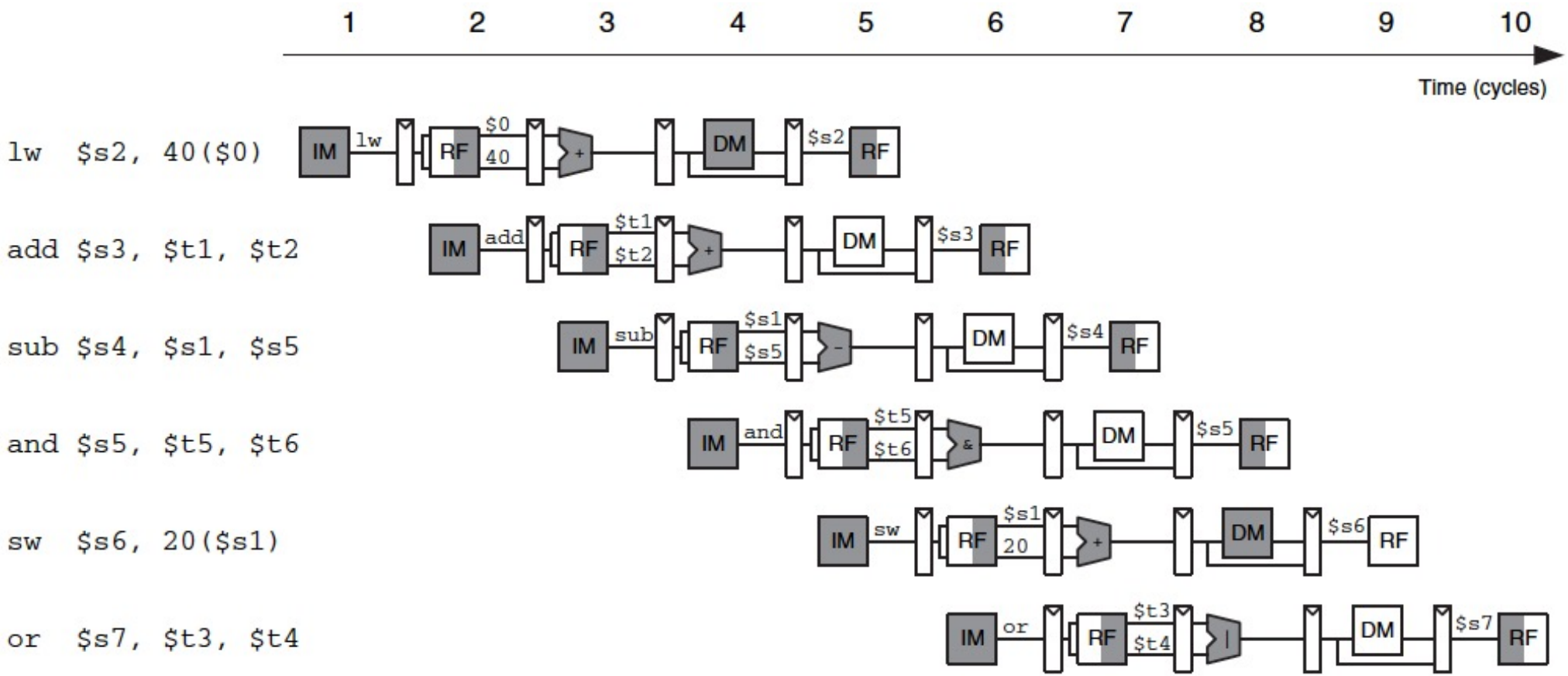
- Fetch or Memory stage.
- Latency 5x250 = 1,250ps
- Throughput 1 instruction/250ps (~4 billion instructions per second)

Latency slightly larger for pipeline versus single-cycle processor due to unequal stage lengths.

Throughput advantage makes up for this.



Pipeline Detail



Pipeline Hazards

Can be problematic if an instruction depends on the result of an unfinished instruction.

This is called a *hazard*.

We'll cover them next.