CIS 351 – Pipelining

1. Assume there is a 4-stage pipeline with 7 operations that need to be completed. Draw a diagram demonstrating how each operation moves through the pipeline over time.

Using your diagram, answer the following questions. Assume the clock period is 4ns.

2. After how many nanoseconds does the first operation finish? The second?

3. How many nanoseconds pass until all 7 operations are completed?

Assume the pipeline splits up the logic perfectly, so that each separate stage would take 4ns on its own. Disregarding register delays, answer the following about the **equivalent non-pipelined** system:

4. After how many nanoseconds does the first operation finish? The second?

5. How many nanoseconds pass until all 7 operations are completed?

6. What is the throughput of the non-pipelined system? How does this compare to the throughput of the pipelined system?

Challenge question:

Draw a system (connected blocks of combinational logic with delays assigned to each block) for which pipelining is very unhelpful. You can try playing with the number of blocks and the delay for each block. Is it possible to find a system for which pipelining *decreases* throughput over the long term?