CIS 351 Practice Test 2 Solutions

February 20, 2022

Updated February 20, 2022

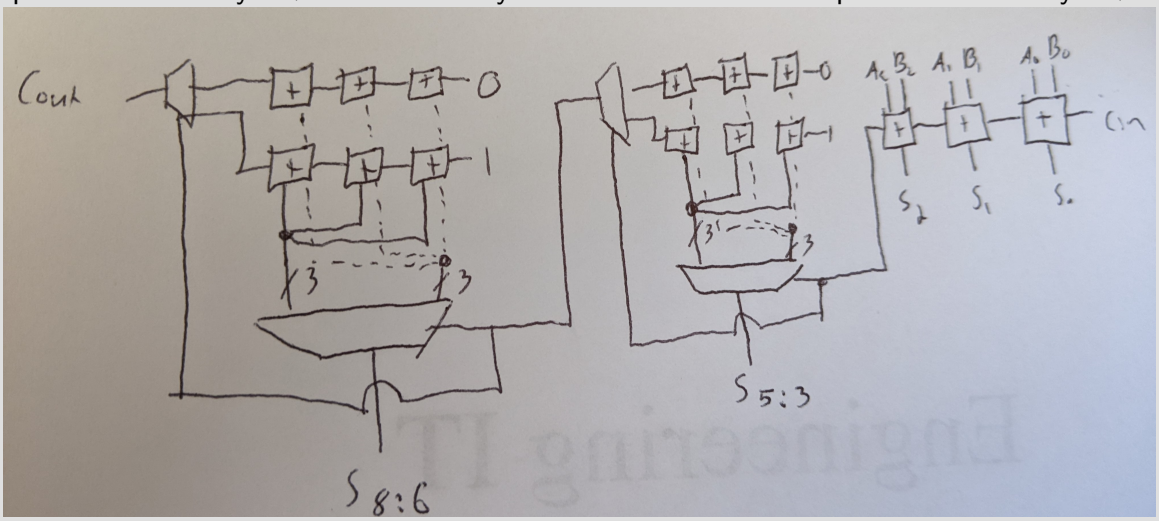
1. Explain **specifically** what makes a carry-lookahead adder faster than a ripple-carry adder of the same size.

   The block-generate and block-propagate values are computed in parallel in all of the blocks. This allows the carry to propagate quickly through the circuit. (You should understand this process in detail.)

2. Draw a nine-bit carry-select adder with 3-adder blocks. How many adders and muxes are required to build your circuit? Give the propagation delay for all of the sum bits (not just the final ones).

   A (very) rough sketch of the adder is included below. It requires 15 full adders and 4 muxes. If the muxes must be one-bit, then it would require 8 muxes.

   The first three sum bits require 1, 2, and 3 FA delays, respectively. The next three require 3 FA delays + 1 mux delay. The final three require 3 FA delays + 2 mux delays.



3. Build a 4:1 mux using logic gates.

   See the slides for an example.

4. Show how to build an `AND` gate and an `OR` gate out of a mux.

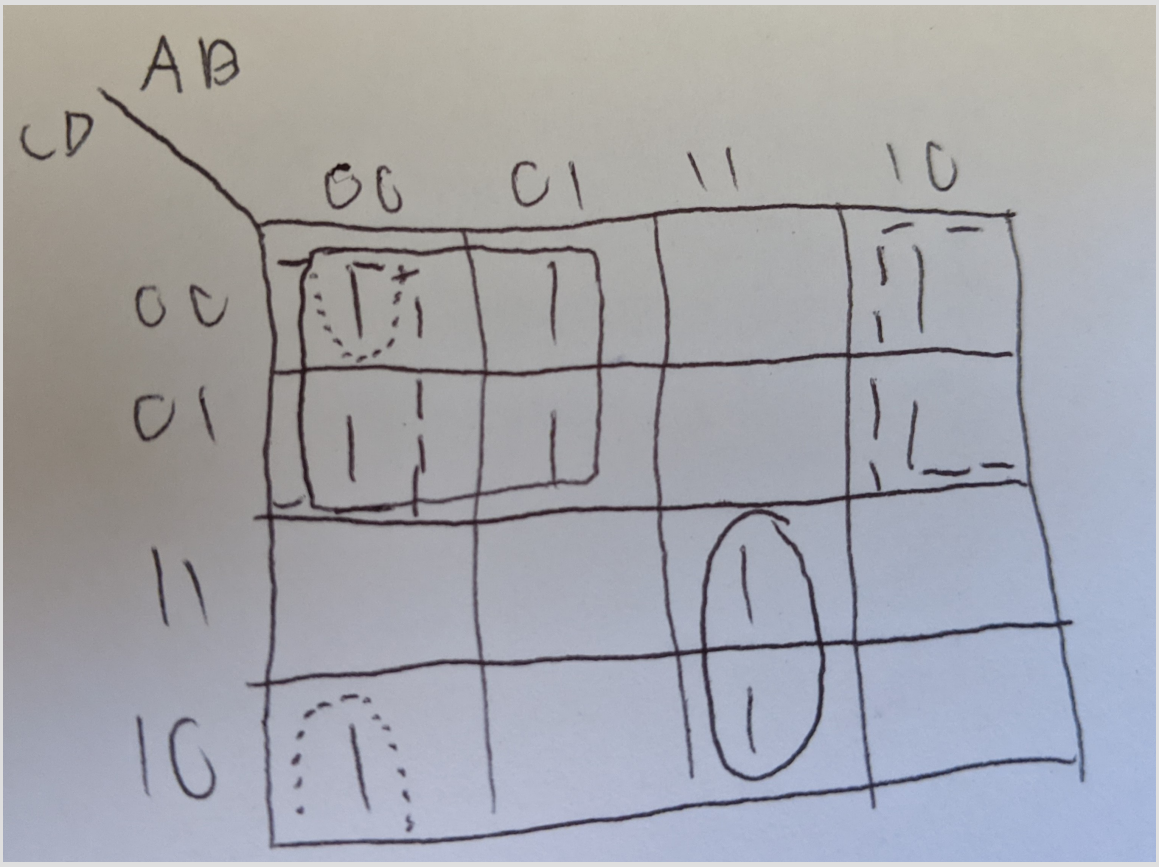
Use `A` and `B` as the selectors and wire up the inputs as `1` or `0` to match the truth table for `AND` or `OR`. See the slides for an example.

5. Use a Karnaugh map to simplify the following Boolean expression:

   `A'B'C'D' + A'B'C'D + A'B'CD' + A'BC'D' + A'BC'D + AB'C'D' + AB'C'D + ABCD' + ABCD`

   Remember: it should be easy to write out the truth table for an expression that is already in sum-of-products form.

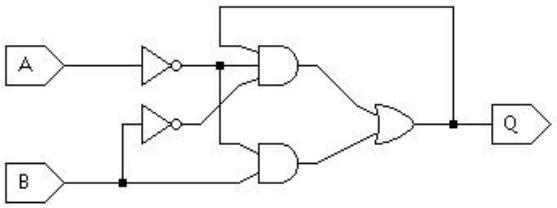
The circled K-map is given below.



The resulting expression is `A'C' + B'C' + ABC + A'B'D'`

6. Complete the characteristic table for the circuit shown below:

A_n	B_n	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



What fundamental circuit has the same characteristic table? An SR latch

7. Complete the characteristic table for the circuit shown below: Note, there is no clock pulse here. Your answers should show the states Q and $\bar{Q}$ after they have reached a steady state given R, S, and current values of Q and $\bar{Q}$. If the given inputs will produce a non-deterministic output (i.e., the output depends on which gate changes first), write "random" in the row.

R	S	Q_{now}	$\bar{Q}_{now}$	Q_{next}	$\bar{Q}_{next}$
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	random	
1	0	1	0	random	
1	0	1	1	1	1
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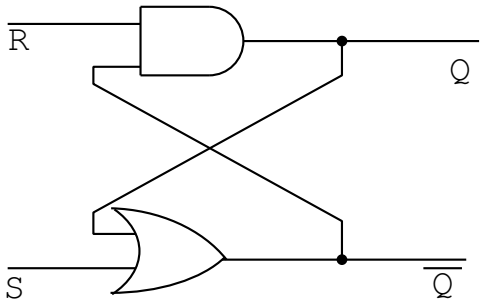
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1



To do this problem, you need to follow the process we did when you first learned about SR latches. For example, assume we are starting with state (1, 1, 1, 0). You could write these values on their respective lines in the diagram. Then, assume that both gates happen at once, and figure out what their outputs would be. In this case, the AND gate sees a 1 (R) and a 0 (Qnot), so the next (temporary) value of Q is 0. At the same time, the OR gate sees a 1 (S) and a 1 (Q) (remember, it is using the original value of Q because the gates should happen at the same time!), so the next value of Qnot is 1. We need to keep going until we reach a steady state, so we repeat the process. The AND now sees 1 (R) and 1 (Qnot) and ouputs 1 for the next Q. The OR now sees 1 (S) and 0 (Q) and ouputs 1 for the next Qnot. Since Q changed this iteration, we repeat the process. The AND now sees 1 (R) and 1 (Qnot) and ouputs 1 for the next Q. The OR now sees 1 (S) and 1 (Q) and ouputs 1 for the next Qnot. So, the steady state is Q=1, Qnot=1.

8. Choose a row labeled "random", and explain why the output is random.

Following the process from the previous answer, we will start off in the state (1, 0, 0, 1). Again, I would encourage you to draw these in the diagram as you go to make sense of what is happening. The AND

sees 1 (R) and 1 (Qnot) and ouputs 1 for the next Q. The OR sees 0 (S) and 0 (Q) and ouputs 0 for the next Qnot. Next, the AND sees 1 (R) and 0 (Qnot) and ouputs 0 for the next Q. the OR sees 0 (S) and 1 (Q) and ouputs 1 for the next Qnot. We now see that we have a problem, because our circuit is back to its initial state of (1, 0, 0, 1). If we keep going in this manner, we will see that it oscillates forever between (1, 0, 0, 1) and (1, 0, 1, 0), never reaching a steady state.

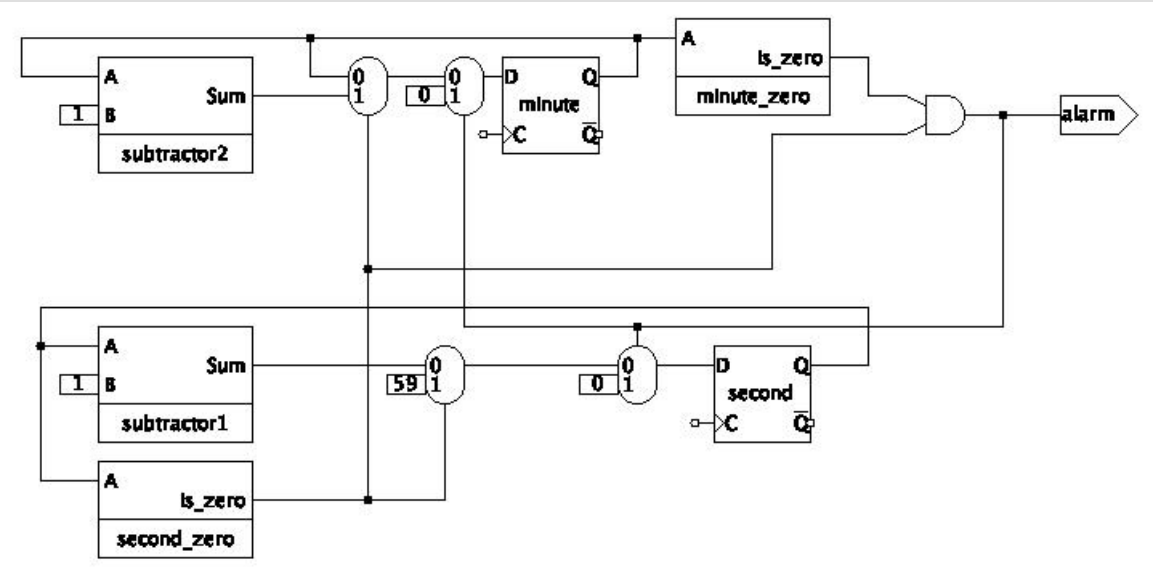
In reality, the gates will not have the exact same delay and we cannot switch the inputs at exactly the same time, so eventually they will get out of sync and converge to a steady state. So, rather than saying that it will oscillate permanently, we say that it will converge to a random state based on physical factors such as gate speed or which input was switched first.

9. Review the Sequential Circuits homework.

Now that your notes are available, this is especially important, because the kind of things I can ask on a homework would still be challenging on an open-note exam. I understand that a homework assignment is meant to be done over a week instead of a few hours, and I will take your time constraints under consideration when designing questions.

10. Review the "golfer" example from Week 5 activities – questions 20 - 22. (You should review the activities in general, but this one tests several skills you will need on the exam.)

11. Design a sequential circuit to run a countdown timer. This circuit should contain two registers: One for the minutes and one for the seconds. Decrement the seconds every time the clock ticks. Stop decrementing when the timer reaches 0. This circuit should have three outputs: `minutes`, `seconds`, and a one-bit `alarm` output that will be set to 1 when the timer reaches 0.



12. Review questions 1 - 3 from the Week 6 activities. You will not be asked about pipelined circuits on this exam (that will show up later), but you should understand circuit timing and be able to set the clock period for a non-pipelined sequential circuit.