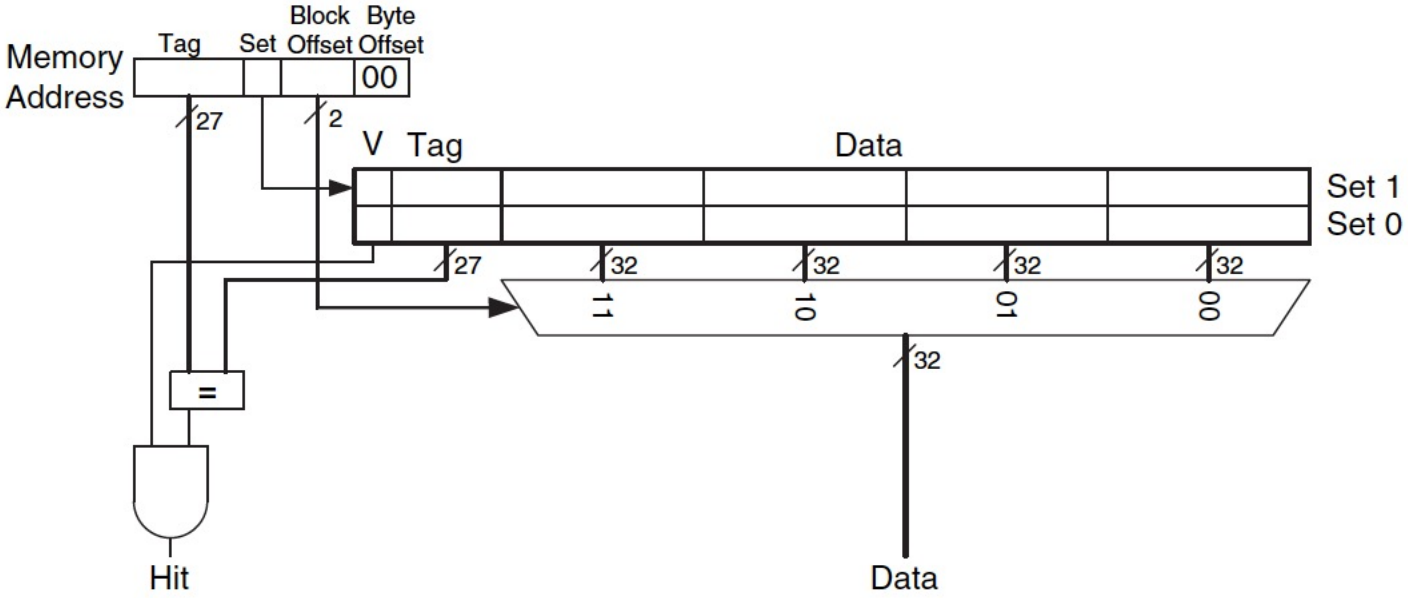
Direct Mapped Cache w/ 4-word blocks

MUX to select the word within the block.

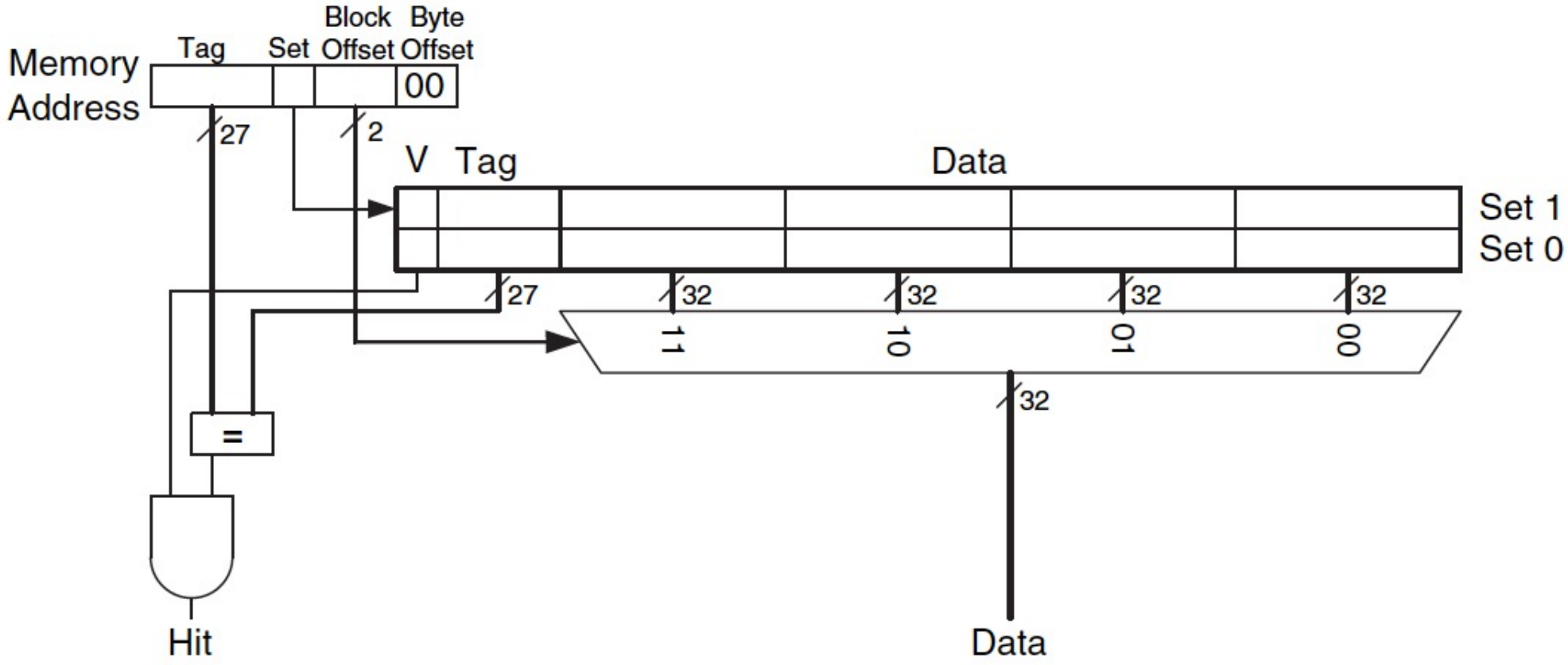
MSB 27 bits form the tag.

- Only one tag needed since the words in the block are at consecutive addresses.
- Remaining 27 bits are the tag.

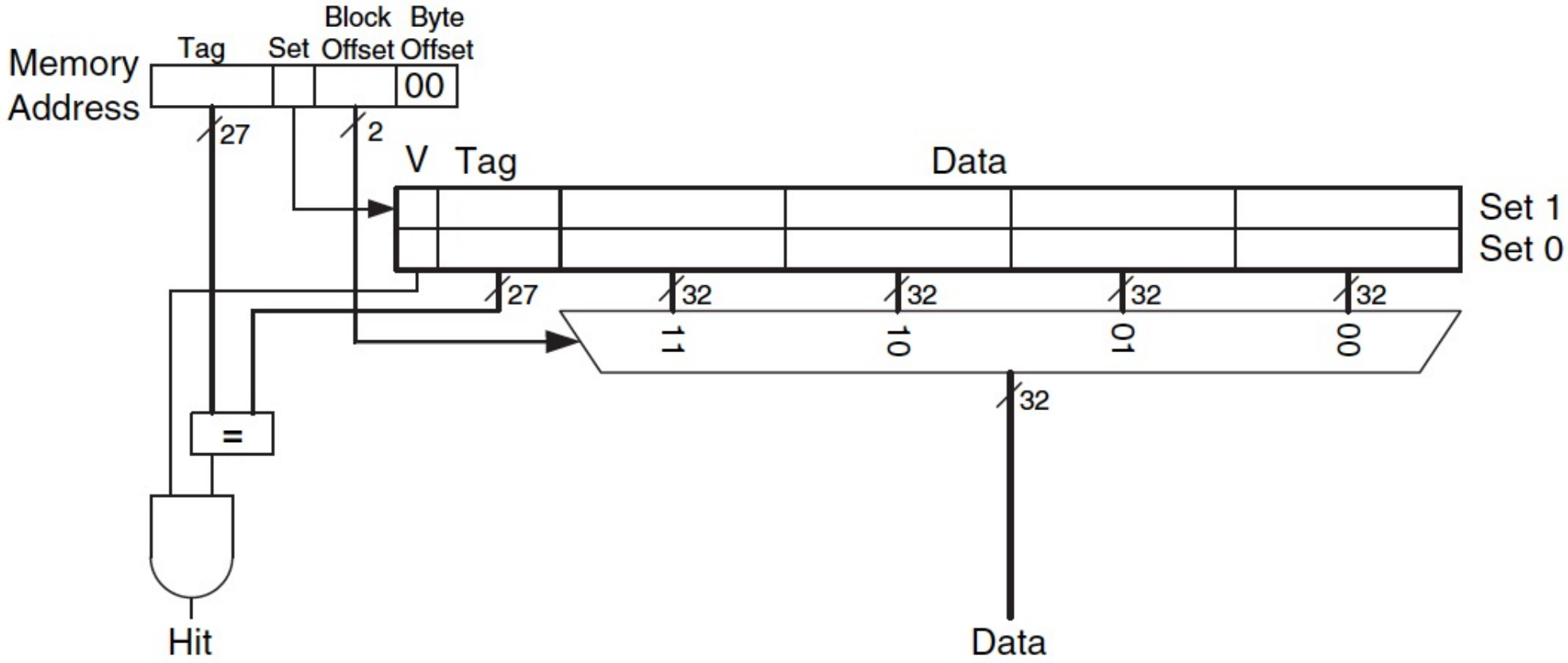
Note the order of the set bit and the block offset bits – set bit is on the left (more significant) side



```
lw $t1, 0x0($0)
lw $t1, 0x4($0)
lw $t1, 0x8($0)
lw $t1, 0xC($0)
```

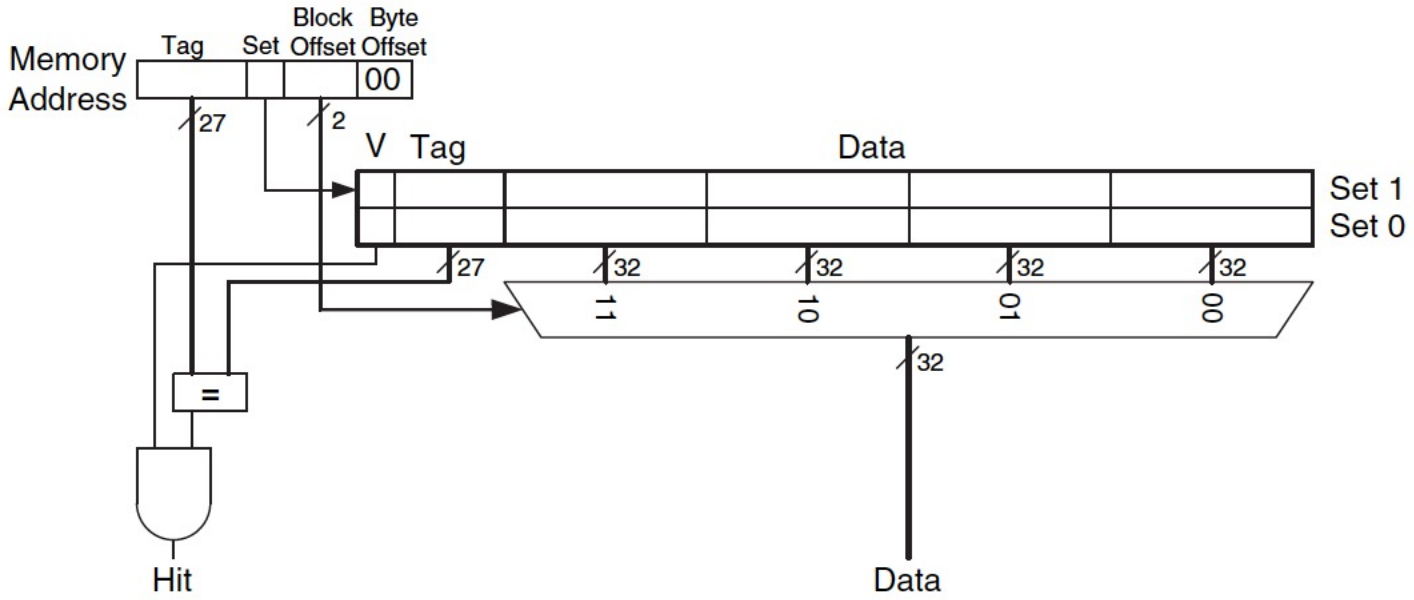


```
lw $t1, 0x0($0)
lw $t1, 0x28($0)
lw $t1, 0x4($0)
```



Grabbing a Block

The address requested is not necessarily the first address in the block!



Grabbing a Block

- Assume we have a block size of 16 bytes (4 words)

- When address 0x000000A4 is requested, what memory addresses are pulled into the cache?