Pipelining

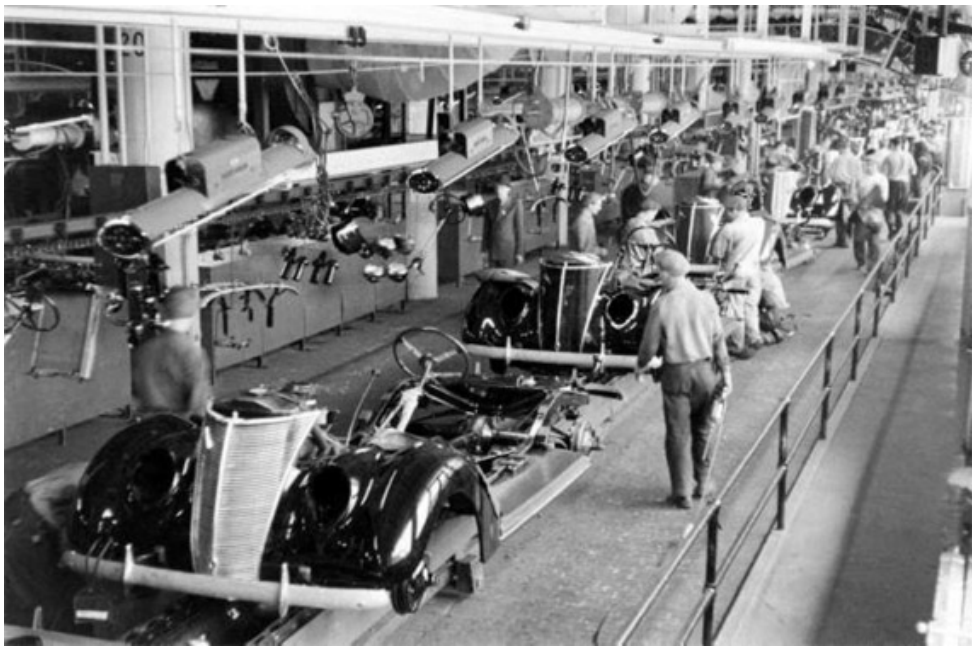
System Productivity

Circuit may be broken into smaller chunks of combinational logic residing between registers

This can have major impact on performance

Parallelism

Spatial Parallelism



Temporal Parallelism

System Productivity

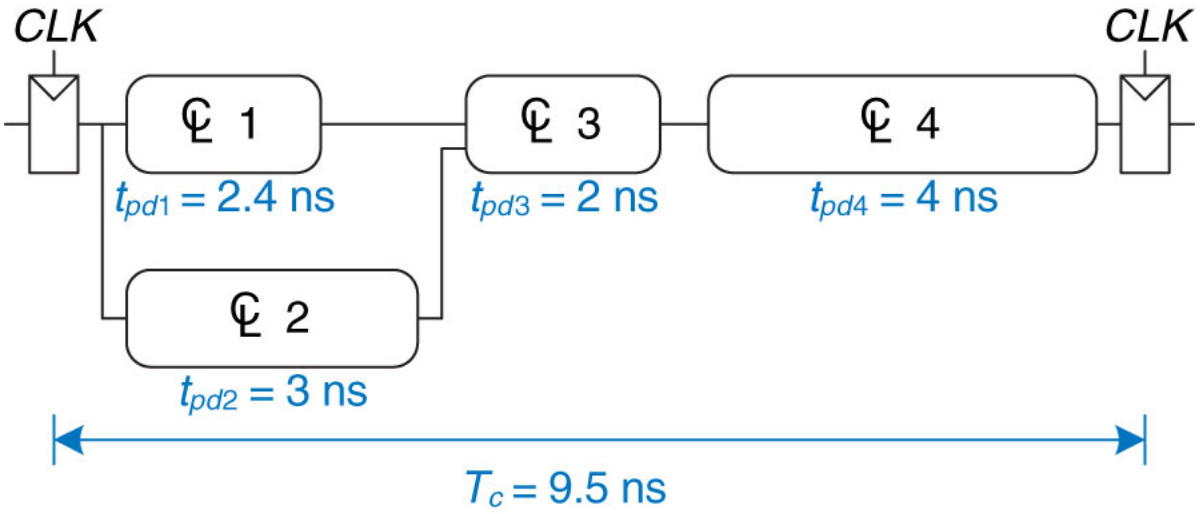
Latency: Time required for one piece of information to pass through the system from start to finish.

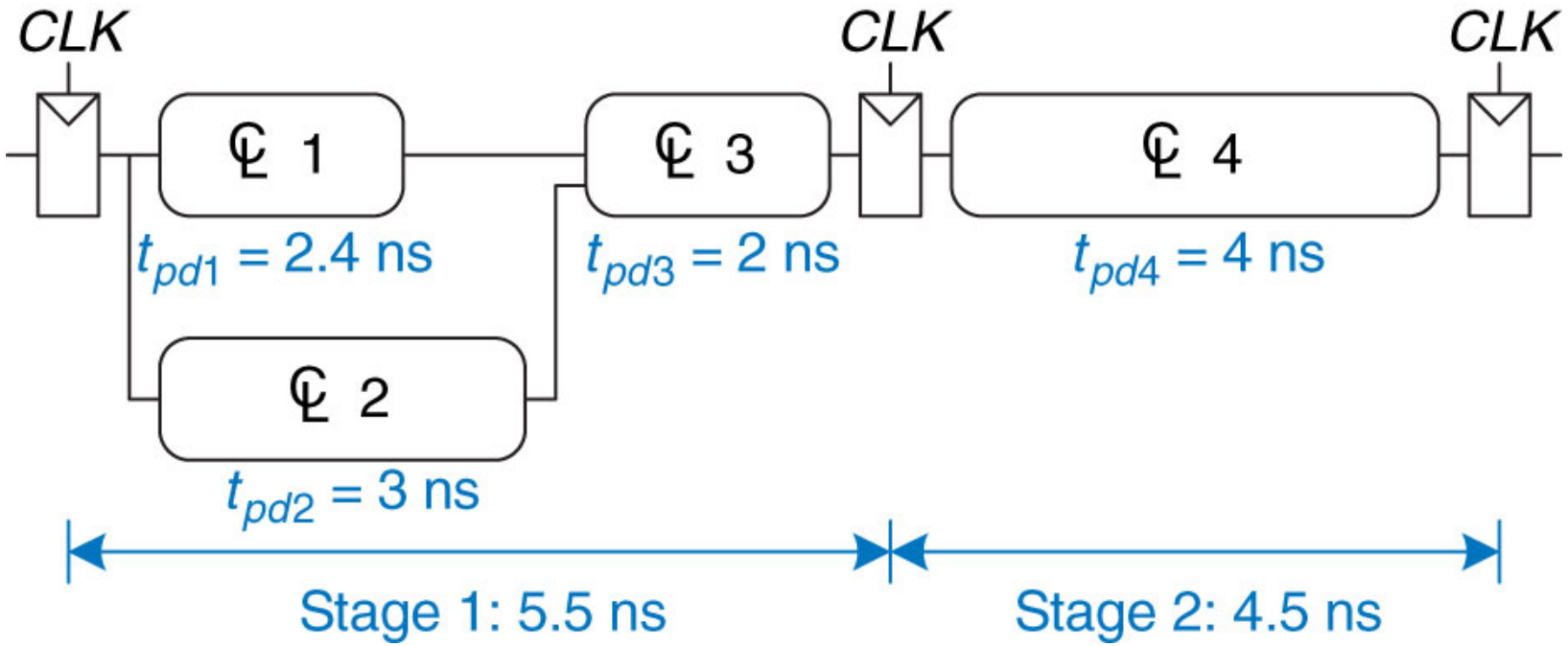
Inputs producing outputs.

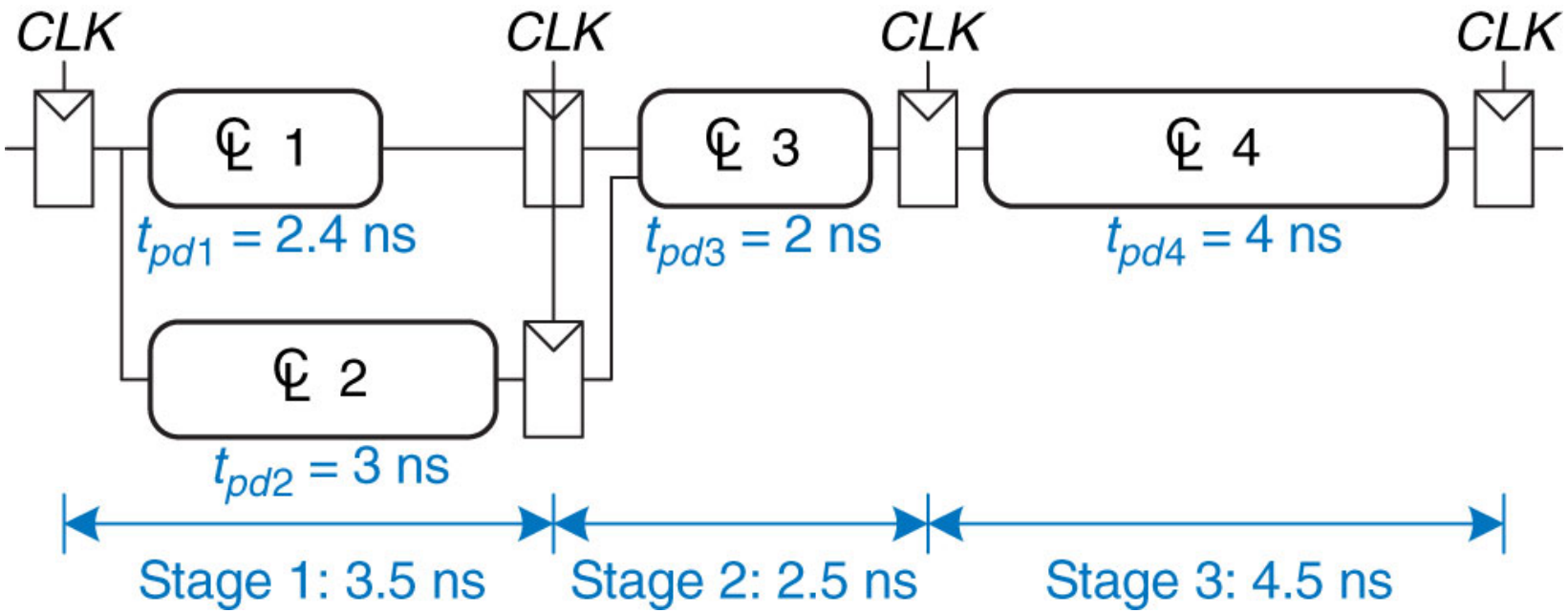
Througput: how much information can be produced at a given time.

Pipelining

Temporal parallelism involves breaking the system up into chunks, with registers in between to allow multiple simultaneous operations.




CLK
CLK
CLK
1
2
3
4
t_{pd1} = 2.4 ns
t_{pd2} = 3 ns
t_{pd3} = 2 ns
t_{pd4} = 4 ns
Stage 1: 5.5 ns
Stage 2: 4.5 ns


CLK
CLK
CLK
CLK
1
2
3
4
t_{pd1} = 2.4 ns
t_{pd2} = 3 ns
t_{pd3} = 2 ns
t_{pd4} = 4 ns
Stage 1: 3.5 ns
Stage 2: 2.5 ns
Stage 3: 4.5 ns

Latency and Throughput

Both latency and throughput depend on longest stage

Latency is (# stages)*(time of longest stage)

Long-term throughput is 1/(time of longest stage)

Pipelining

Not exactly a 2x speed up when breaking into two.

- Overhead from registers and latency