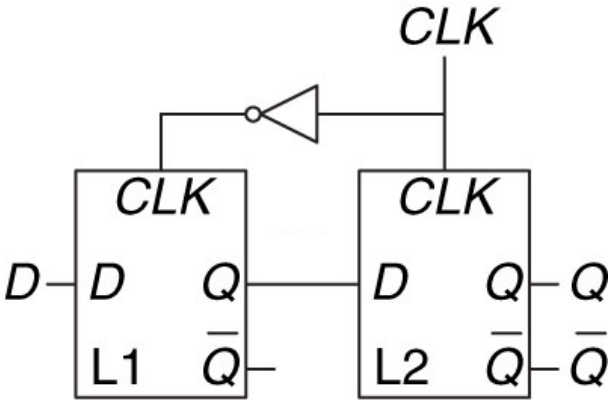
Flip-flops

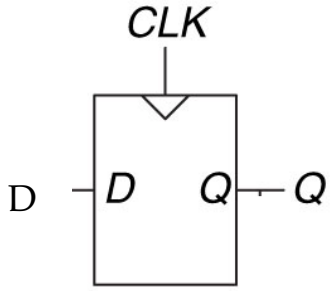
D Flip-Flop

Two D-latches connected

Note inverter on clock – impossible for outputs of both latches to change at once

How does output ever change?

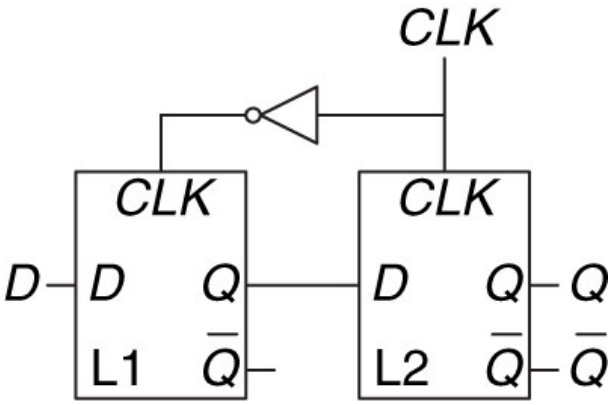




D Flip-Flop

When CLK == 0, first latch allows D through

Second latch does not allow D through



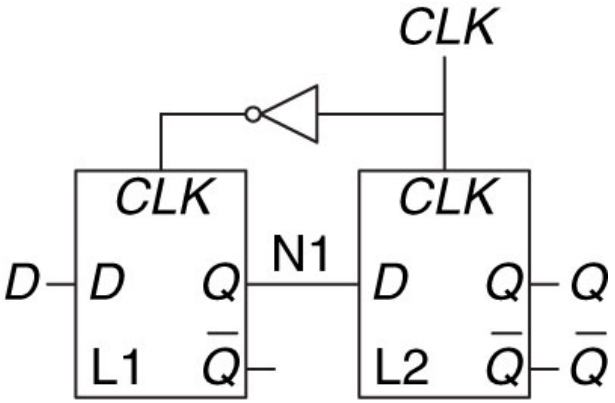
D Flip-Flop

When CLK == 0, first latch allows D through

Second latch does not allow D through

Keep track of value on wire between latches – call it N1

When CLK == 0, N1 := D



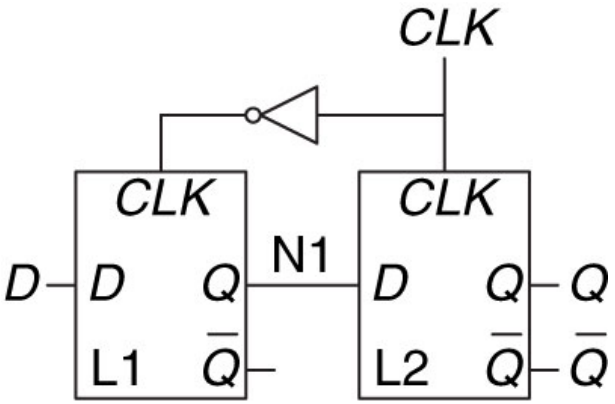
D Flip-Flop

When CLK == 1, D cannot get through first latch

N1 thus remains unchanged as long as CLK == 1

N1 can get through second latch, so

Q := N1

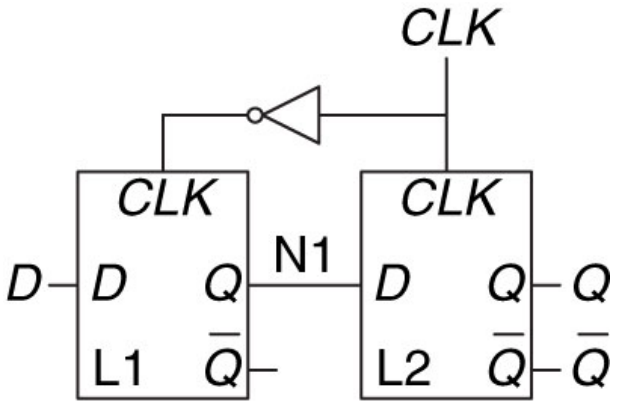


D Flip-Flop

As long as CLK is 0, D cannot get through second latch

As long as CLK is 1, D cannot get through first latch

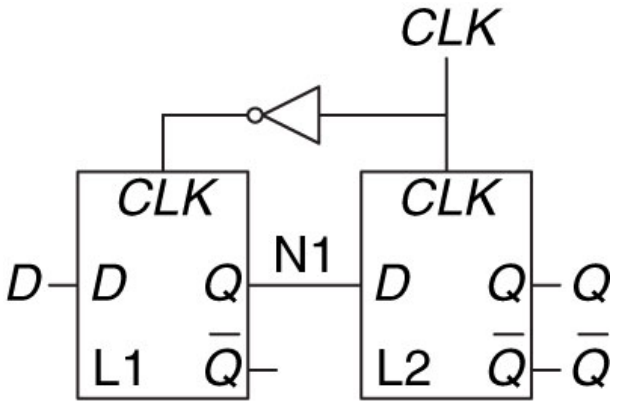
D affects Q only indirectly, through N1



D Flip-Flop

1. CLK at 0, D -> N1
2. CLK goes to 1, N1 -> Q

Q changes only on **rising edge** of clock – moment when clock goes from 0 to 1

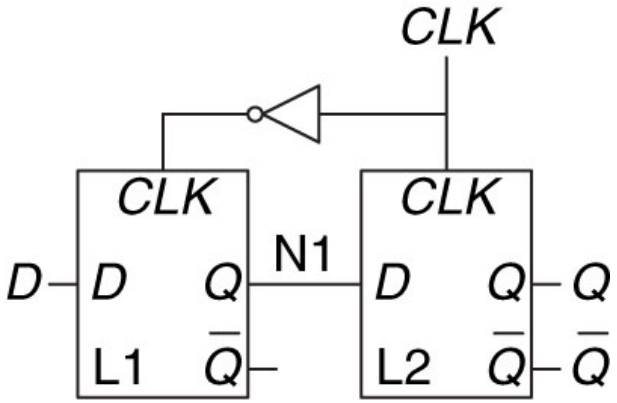


D Flip-Flop

Output Q of flip-flop changes only on rising edge of clock

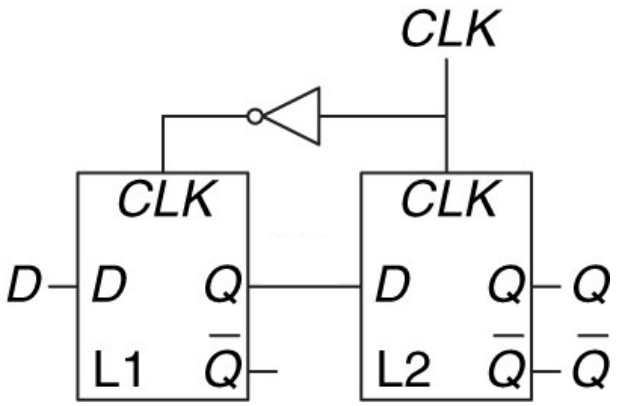
Does not change when:

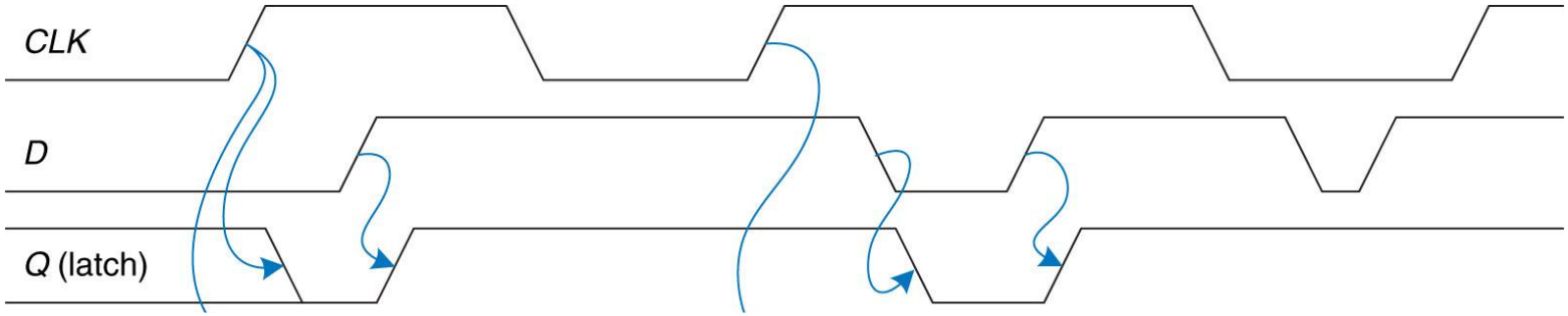
- CLK = 1
- CLK = 0
- CLK goes from 1 to 0

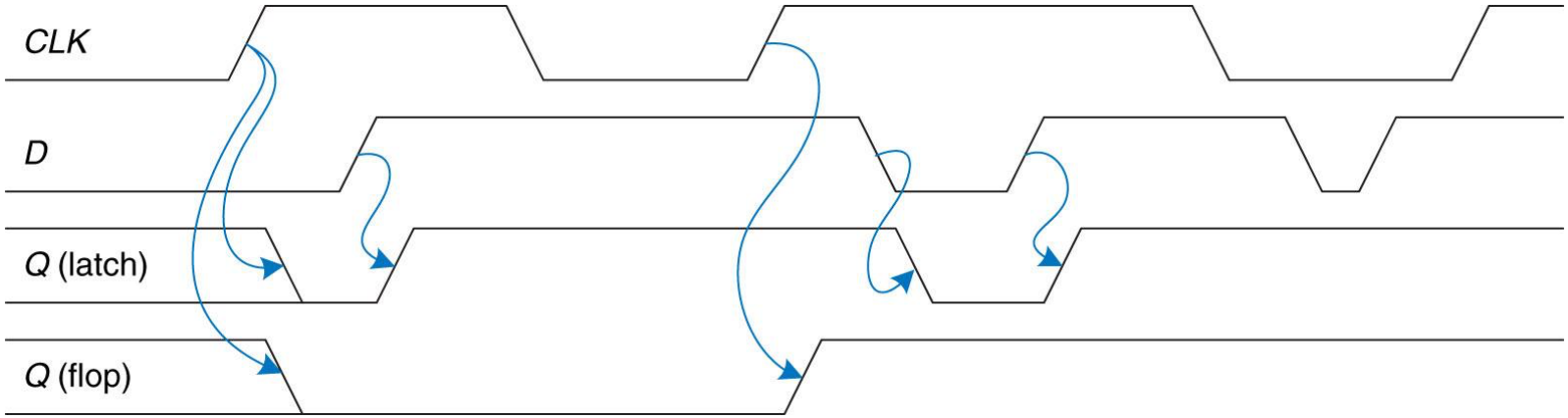


D Flip-Flop

A D flip-flop copies D to Q on the rising edge of the clock, and remembers its state at all other times.




CLK
D
Q (latch)


CLK
D
Q (latch)
Q (flop)

D Flip-Flop

As with all circuits, it is useful to distinguish *what* flip-flop does vs *how* it is implemented

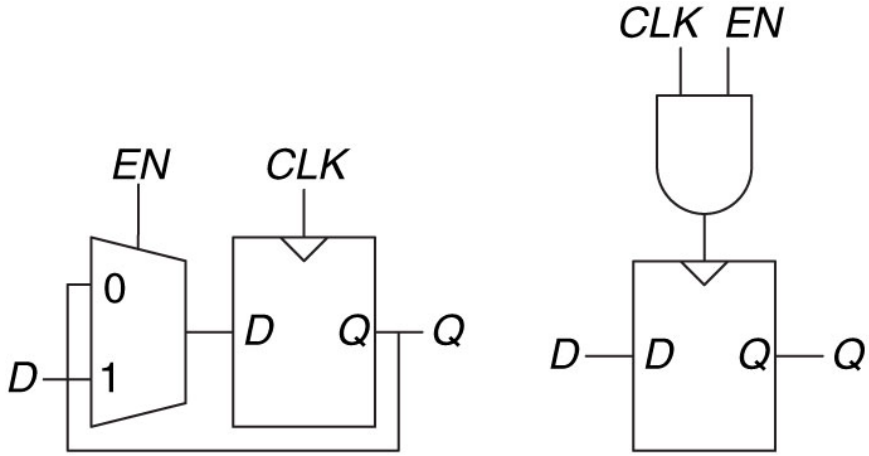
You should understand and be able to describe *how* a flip-flop works

However, even if you are still working on understanding that part, you should still have clear idea of *what* flip-flop does: changes state only on rising edge of clock

Enabled Flip-Flop

Control whether or not a flip-flop is updated on the clock pulse.

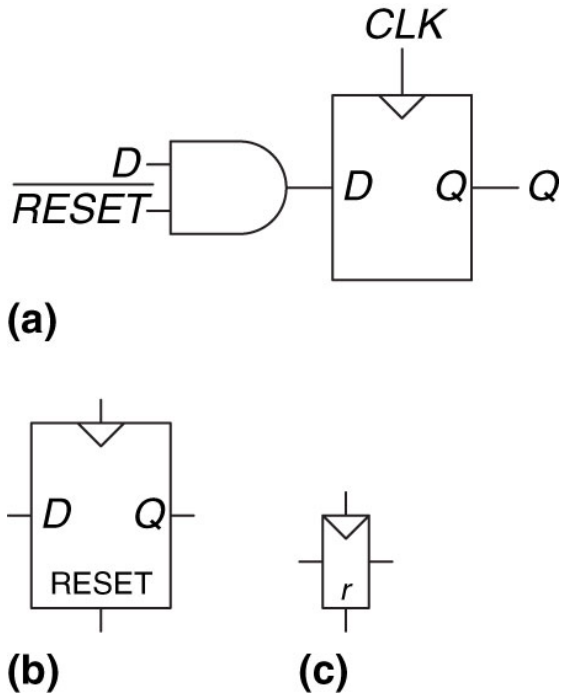
Why might we want to do this?



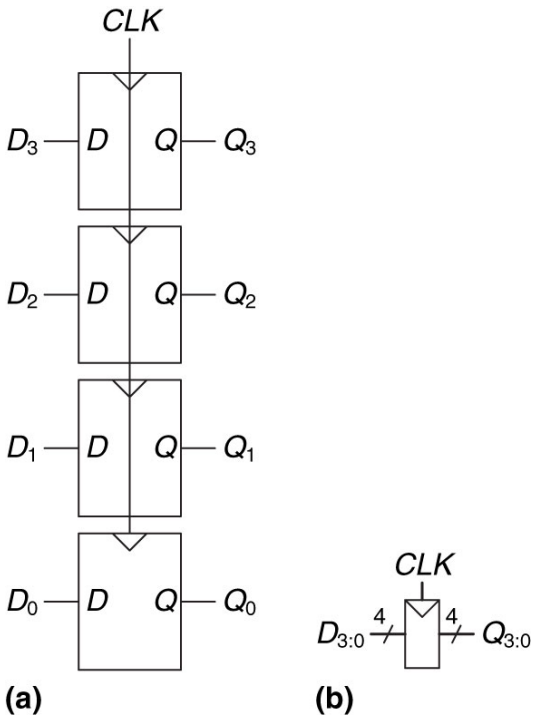
Resettable Flip-Flops

Reset the state of a flip-flop to 0.

Useful when turning on the system, or returning to a known state.



Register



Combining multiple D flip-flops together creates a basic register.

When CLK is asserted, the flip-flops are updated simultaneously.

Basic memory!