

# MOSIS Tiny Chip Padframe

Tanner Hi-ESD Pad Library  
AMI C5N ( $0.5\mu$ ) Process

Prepared By  
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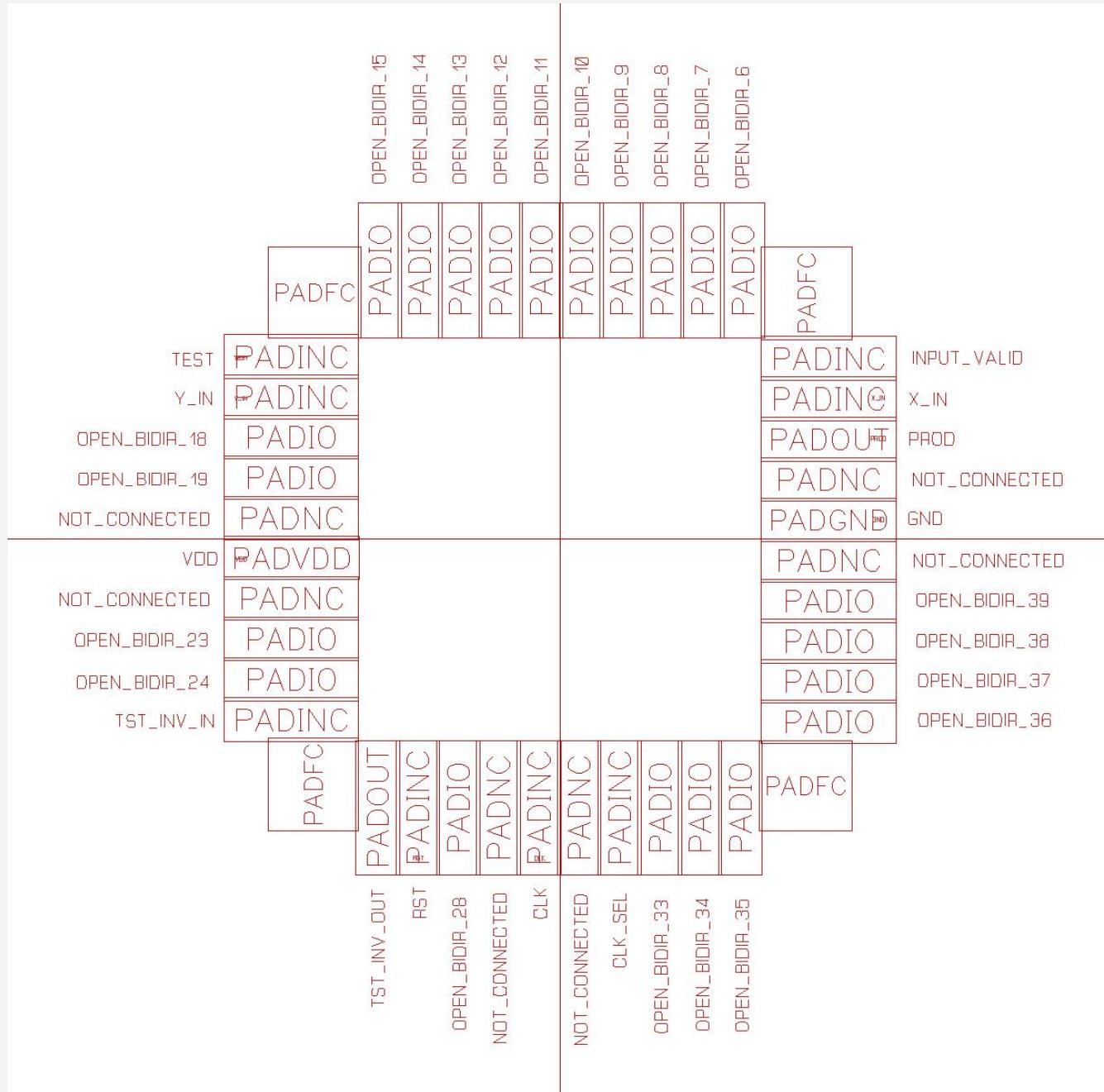
# What is Padframe

- You complete layout of the module/core, perform DRC, do netlist extraction and simulate (and it's working).

Now what?

- Use Padframe for the module/core interaction with external environment.
- Connect module I/O, sources with Padframe I/O and sources.
- Perform the DRC, PEX, and simulation after you integrate your design in the Padframe.

Padframe Internals



## **Power / Ground**

## **PAD:**

- PADVDD
  - PADGND

## **Input PAD:**

- PADINC

## **Output PAD:**

- PADOUT

## Bi-directional

## PAD:

- PADIO

# PAD Frame

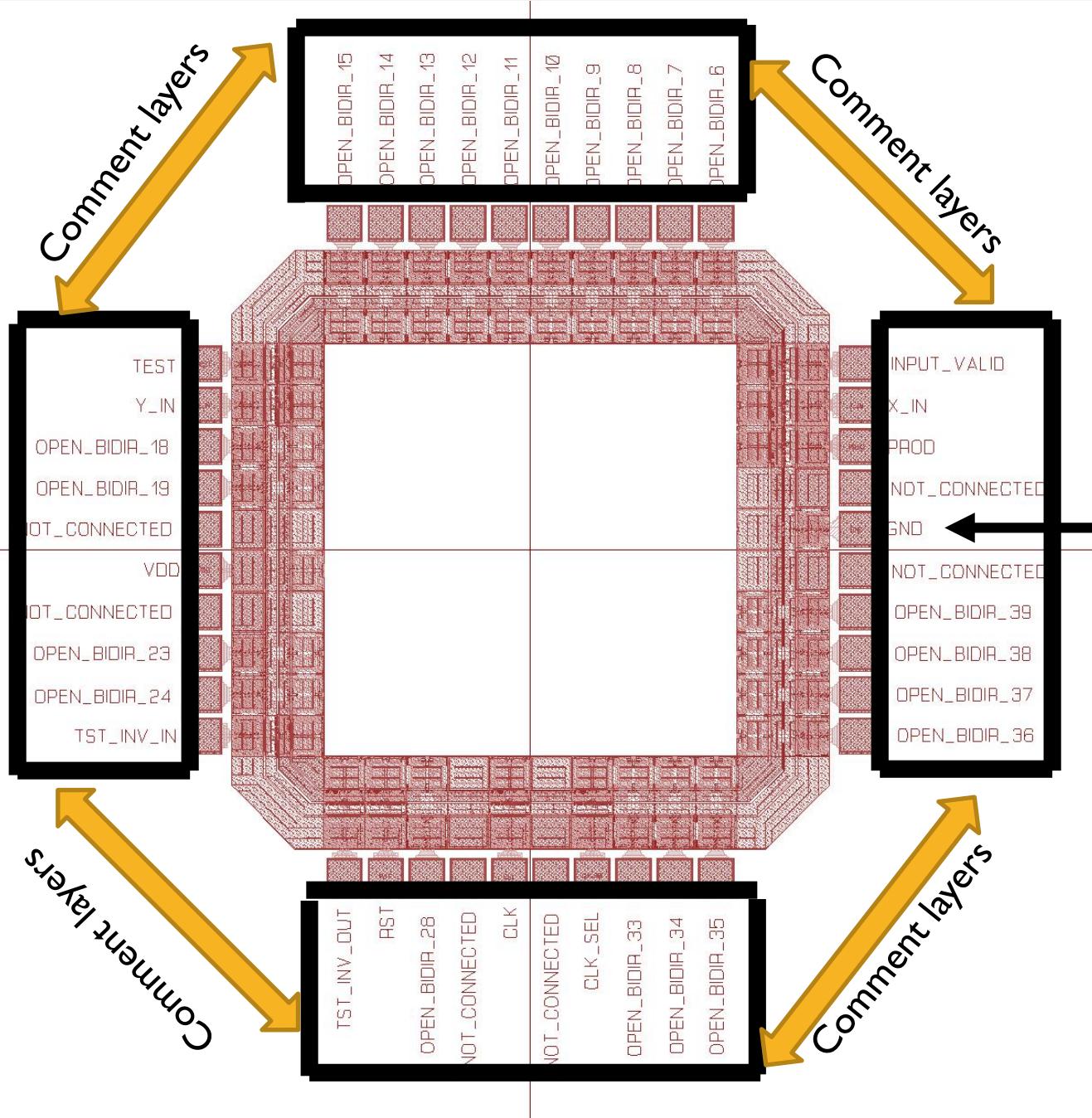
## **Corner:**

- PADFC

## **PAD Spacer (No connection):**

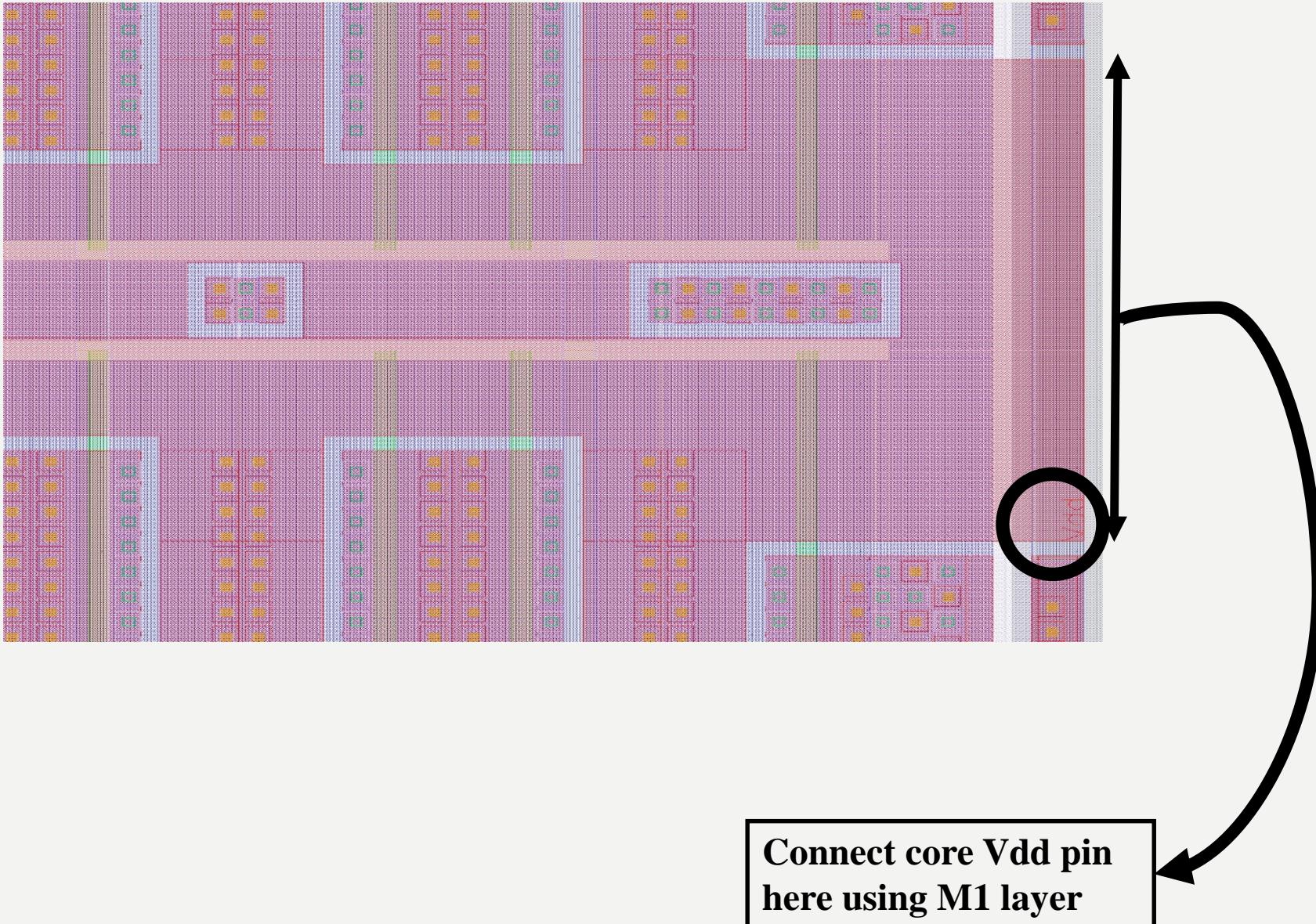
- PADNC

# Flattened Padframe

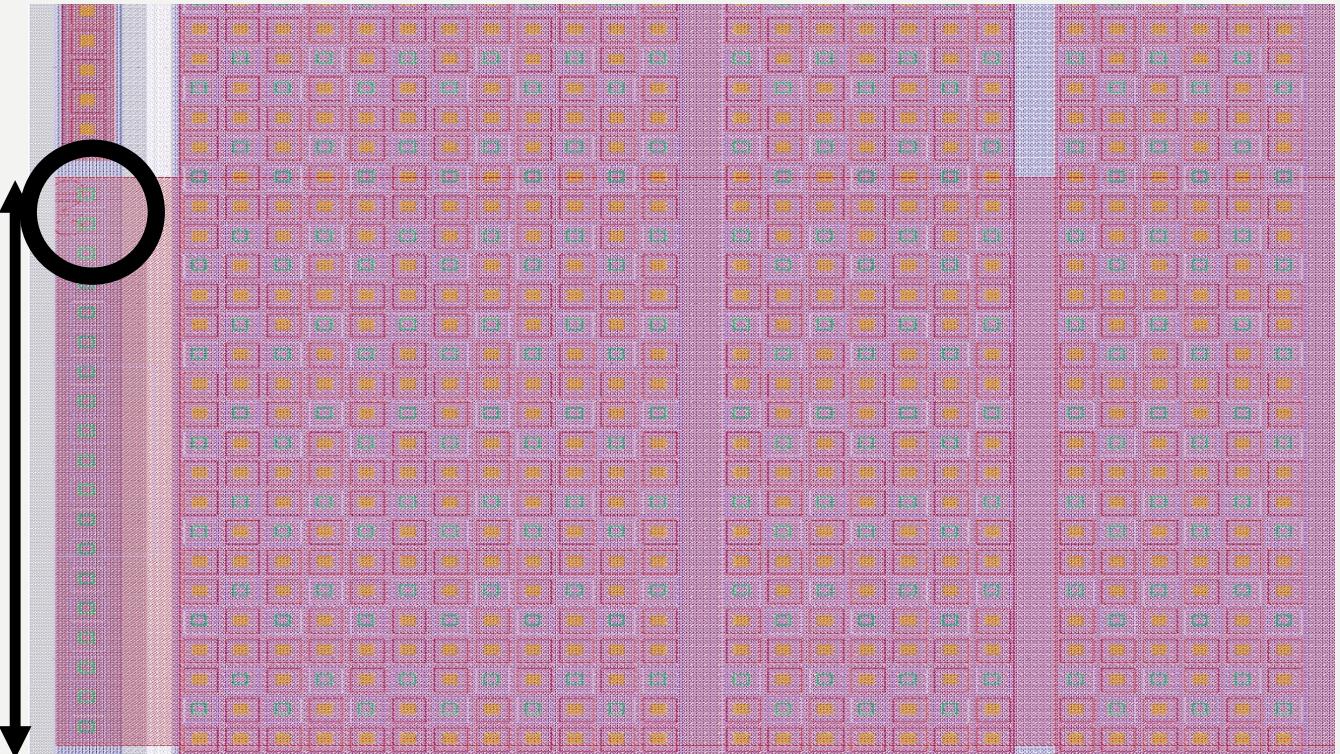


\_# : PIN Number

PAD Vdd

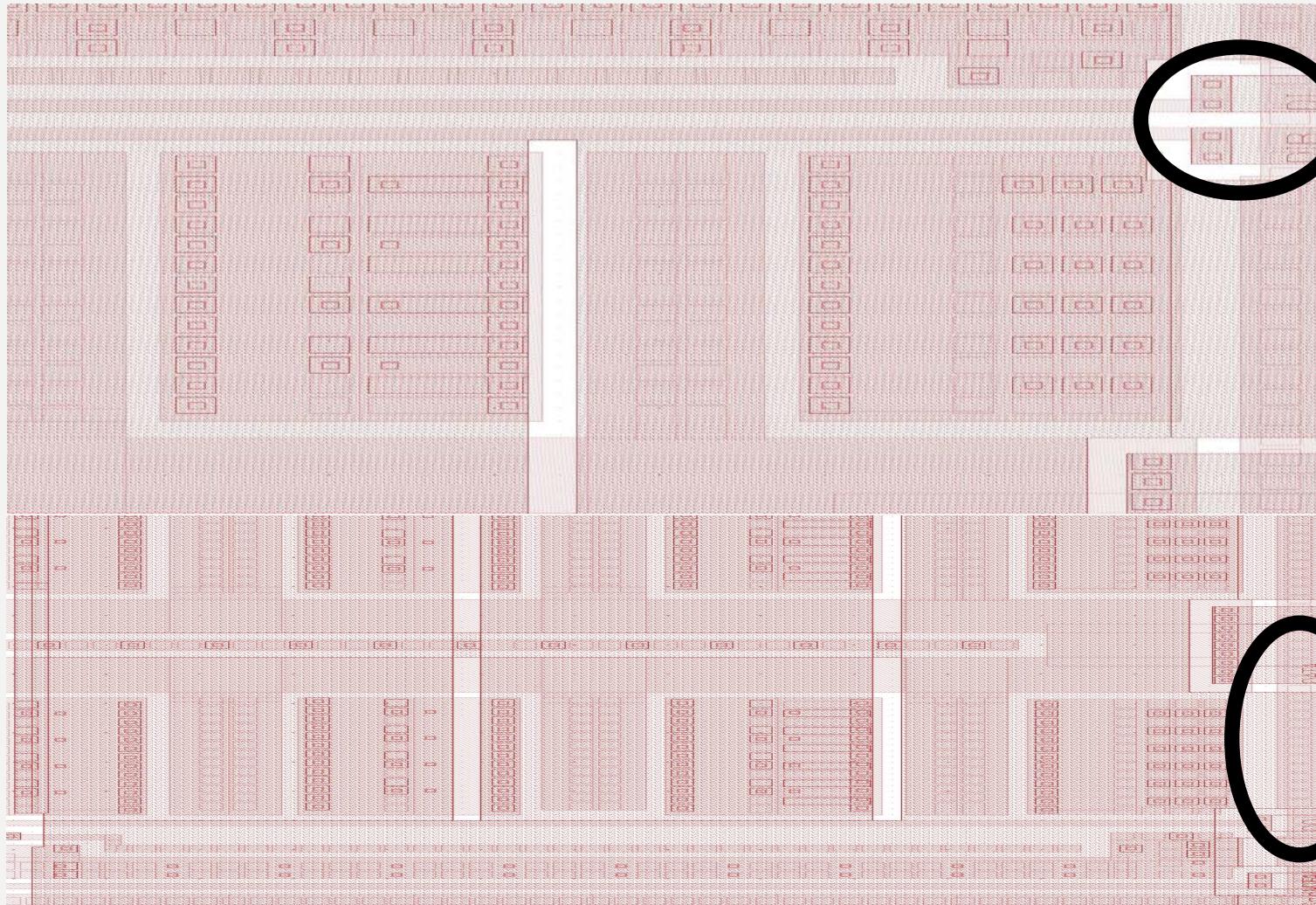


# PAD GND



**Connect core GND pin  
here using M1 layer**

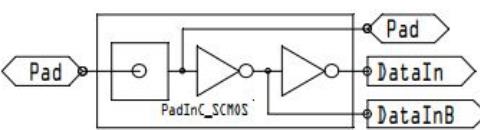
# PADINC



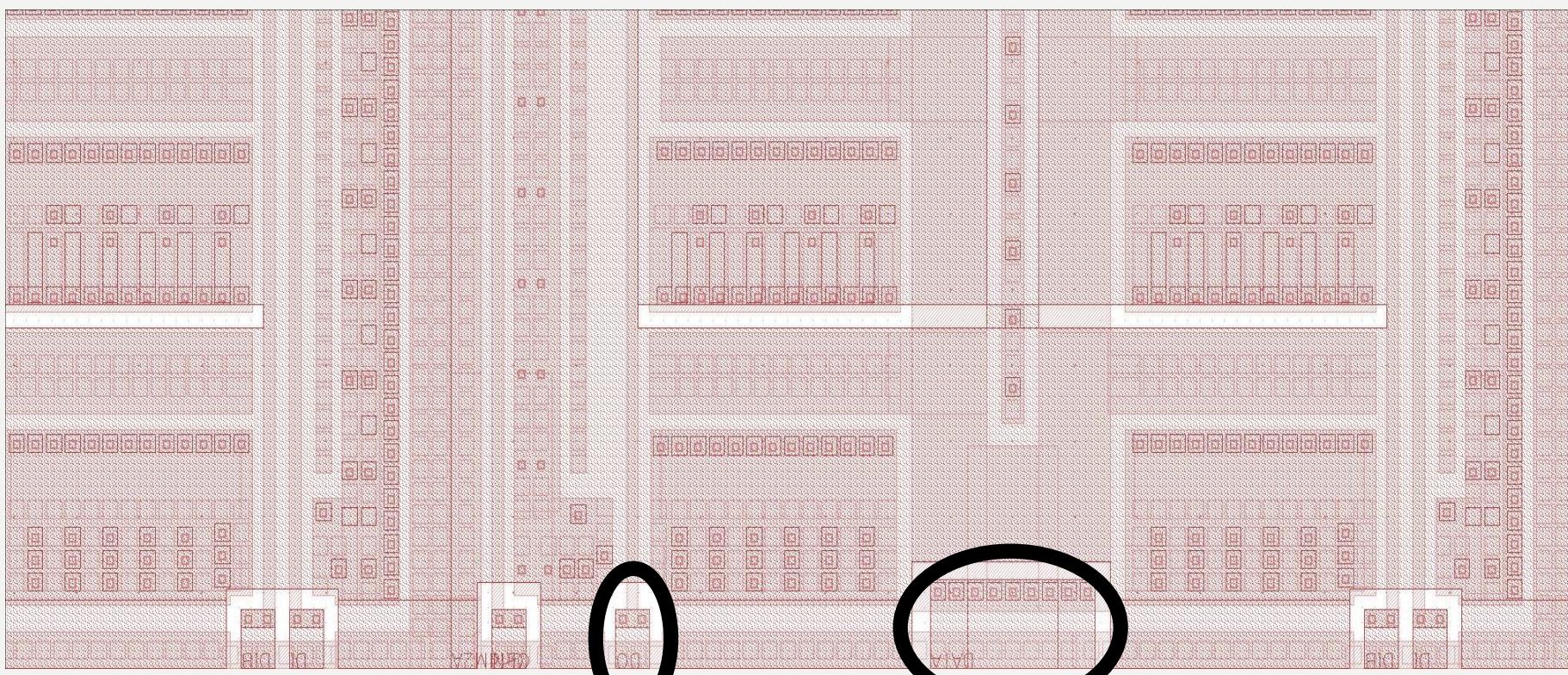
DataInBar  
DataInBar

Do not connect here

Connect your input signal here using M2

Logic Symbol			Truth Table		
			PAD	DI	DIB
0	0	1	1	1	0

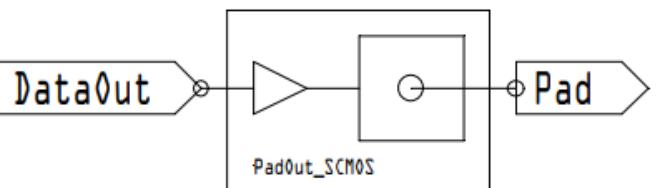
# PADOUT



DataOut

Donot connect here

(connect your signal here using M2 layer)

Logic Symbol		Truth Table							
	PadOut_SCMOS	<table border="1"><thead><tr><th>PAD</th><th>D0</th></tr></thead><tbody><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></tbody></table>	PAD	D0	0	0	1	1	
PAD	D0								
0	0								
1	1								

# Padframe Example

