CDA 4213 001L/CIS 6930 012
Fall 2019
CMOS VLSI Design

Lab 2 Report

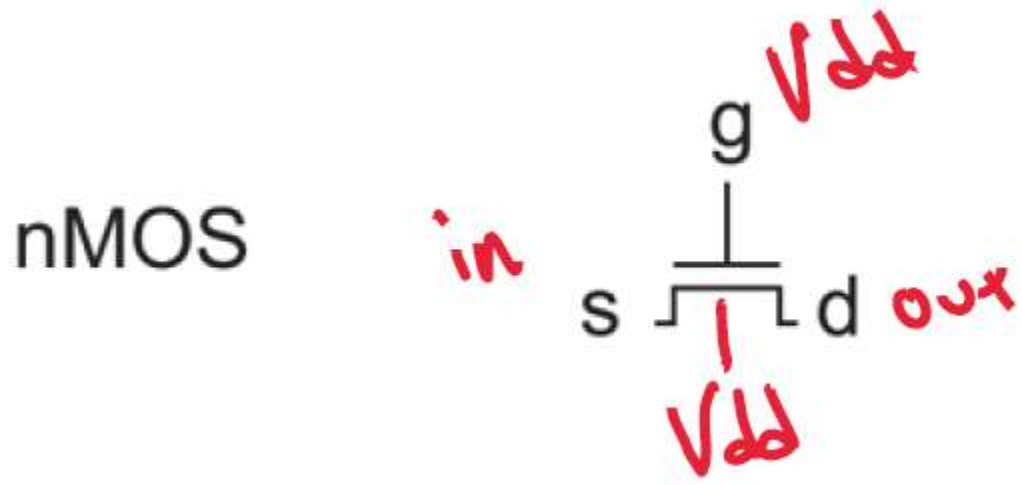
Canvas Submission
Due: 11:59 PM, 22nd Sept. 2019

Note: Upload PDF version of this report. Only PDF format is accepted.

Today's Date:	9/11/19
Your Name:	Boyang Wu
Your U Number:	U95035892
No. of Hours Spent:	4
Exercise Difficulty: (Easy, Average, Hard)	Average
Any Other Feedback:	Took a while to figure out parts 1 and 2 (which are really the easiest) but everything was fine after that.

Question 1 (5 pts): NMOS Transistor

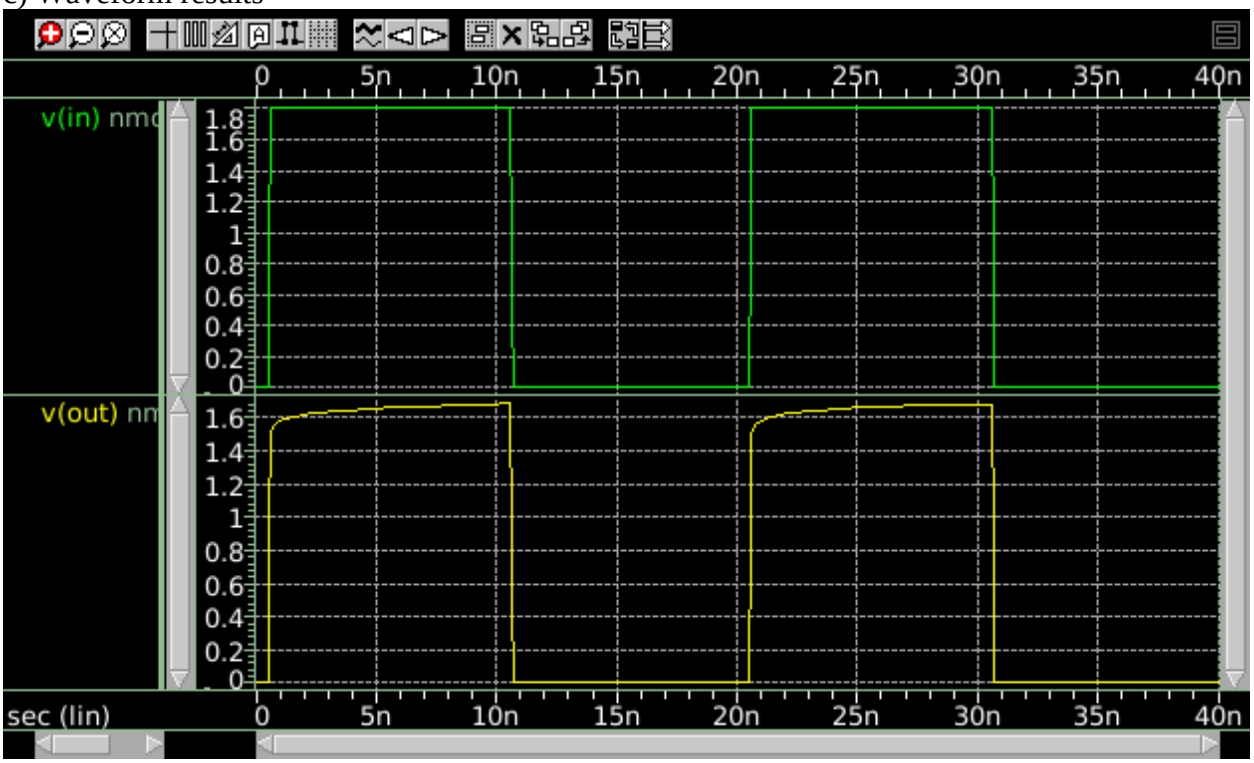
Include the following
a) Transistor level diagram



b) Spice netlist (.sp file contents)

```
  GNU nano 2.0.9                File: nmos.sp

**-------------------------------------------------------------
* Inverter SPICE deck
**-------------------------------------------------------------
* Parameters and models
**-------------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------------
Vdd Vdd 0 1.8V
*Vin in 0 PWL(0 0 10ns 0 11ns 1.8 20ns 1.8)
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns

m0 out Vdd in Vdd NMOS W=180 L=180
*m1 out  0  in  0  PMOS W=180 L=180

*Cload out 0 0.01pF

.tran 1ns 40ns
.measure tran tr TRIG v(out) val=0.36 RISE=1 TARG v(out) val=1.44 RISE=1
.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=0.36 FALL=1
.measure tran tpdr TRIG v(in) val=0.9 FALL=1 TARG v(out) val=0.9 RISE=1
.measure tran tpdf TRIG v(in) val=0.9 RISE=1 TARG v(out) val=0.9 FALL =1

***  Output Statements
.plot V(in) V(out)
.end
```

c) Waveform results



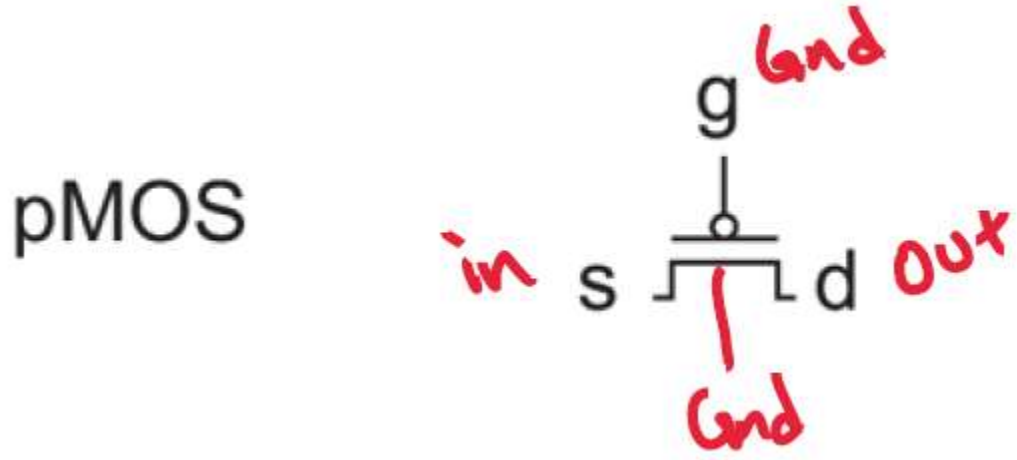
d) Explain how you demonstrate that NMOS transistor is good (poor) conductor of 0 (1).

When Vin goes to 1.8V, Vout only goes to 1.65V -> degraded 1.8V or 1

When Vin goes to 0V, Vout goes to 0V -> strong 0

Question 2 (5 pts): PMOS Transistor

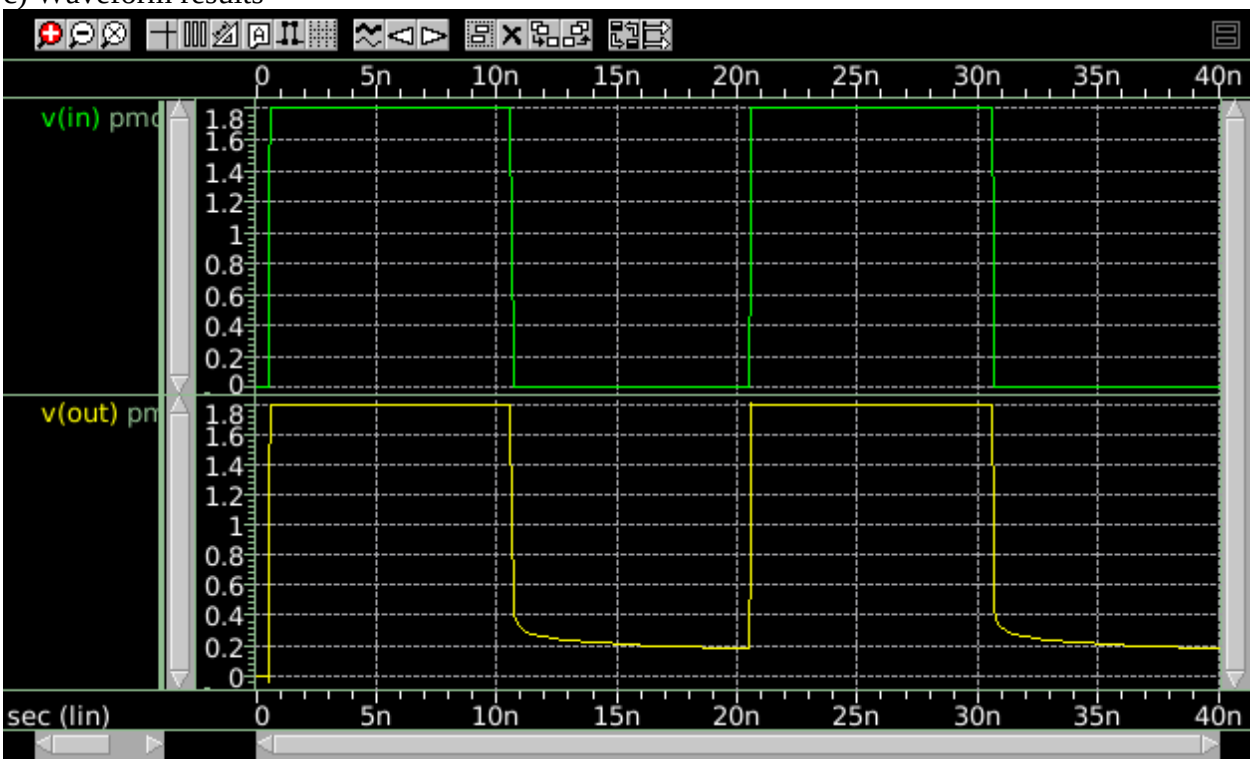
Include the following
a) Transistor level diagram



b) Spice netlist (.sp file contents)

```
  GNU nano 2.0.9                    File: pmos.sp

**-------------------------------------------------------------
* Inverter SPICE deck
**-------------------------------------------------------------
* Parameters and models
**-------------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------------
Vdd Vdd 0 1.8V
*Vin in 0 PWL(0 0 10ns 0 11ns 1.8 20ns 1.8)
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns

*m0 out Vdd in Vdd NMOS W=180 L=180
m1 out  0  in  0  PMOS W=180 L=180

*Cload out 0 0.01pF

.tran 1ns 40ns
.measure tran tr TRIG v(out) val=0.36 RISE=1 TARG v(out) val=1.44 RISE=1
.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=0.36 FALL=1
.measure tran tpdr TRIG v(in) val=0.9 FALL=1 TARG v(out) val=0.9 RISE=1
.measure tran tpdf TRIG v(in) val=0.9 RISE=1 TARG v(out) val=0.9 FALL =1

***  Output Statements
.plot V(in) V(out)
.end
```

c) Waveform results



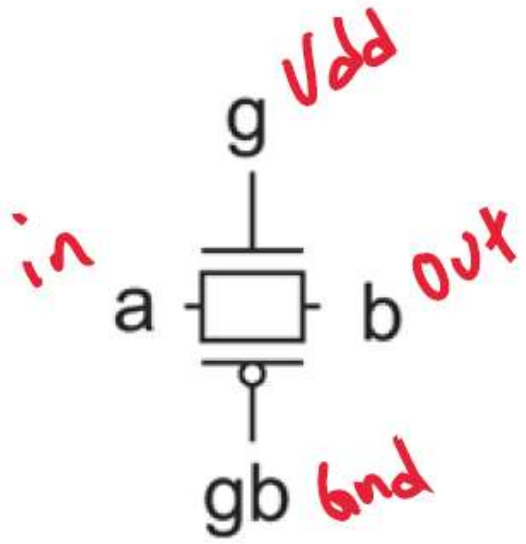
d) Explain how you demonstrate that PMOS transistor is good (poor) conductor of 0 (1).

When Vin goes to 1.8V, Vout goes to 1.8V -> strong 1.8V or 1

When Vin goes to 0V, Vout goes to 0.2V -> degraded 0

Question 3 (10 pts): Transmission Gate

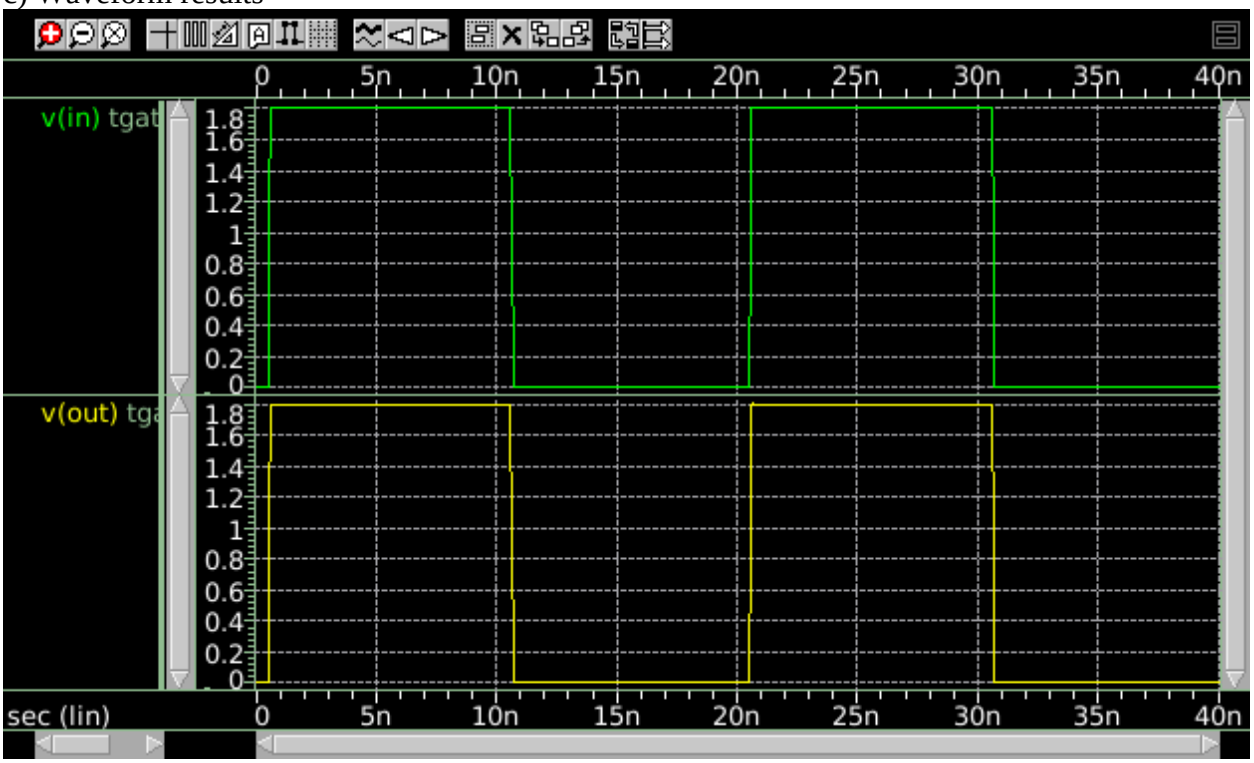
Include the following
a) Transistor level diagram



b) Spice netlist (.sp file contents)

```
  GNU nano 2.0.9                    File: tgate.sp

**-------------------------------------------------------
* Inverter SPICE deck
**-------------------------------------------------------
* Parameters and models
**-------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------
Vdd Vdd 0 1.8V
*Vin in 0 PWL(0 0 10ns 0 11ns 1.8 20ns 1.8)
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns

m0 out Vdd in Vdd NMOS W=180 L=180
m1 out  0  in  0  PMOS W=180 L=180

*Cload out 0 0.01pF

.tran 1ns 40ns
.measure tran tr TRIG v(out) val=0.36 RISE=1 TARG v(out) val=1.44 RISE=1
.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=0.36 FALL=1
.measure tran tpdr TRIG v(in) val=0.9 FALL=1 TARG v(out) val=0.9 RISE=1
.measure tran tpdf TRIG v(in) val=0.9 RISE=1 TARG v(out) val=0.9 FALL =1

***  Output Statements
.plot V(in) V(out)
.end
```

c) Waveform results



d) Explain how you demonstrate that the transmission gate is good conductor of both 1 and 0.

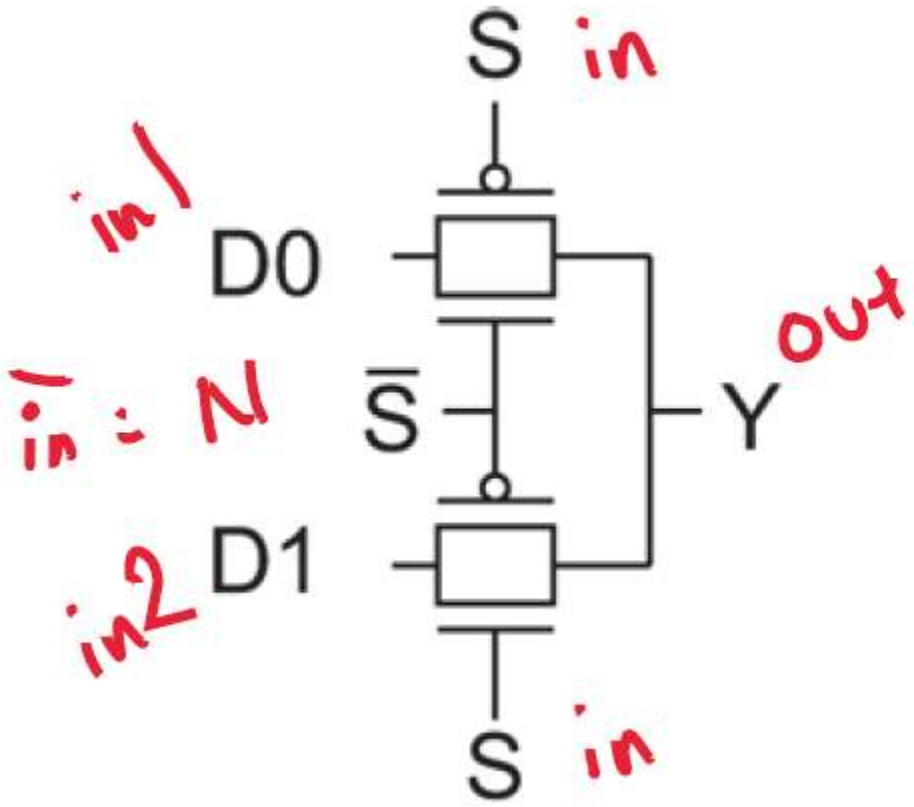
When Vin goes to 1.8V, Vout goes to 1.8V -> strong 1.8V or 1

When Vin goes to 0V, Vout goes to 0V -> strong 0

Question 4 (10 pts): 2-input Multiplexor

Include the following

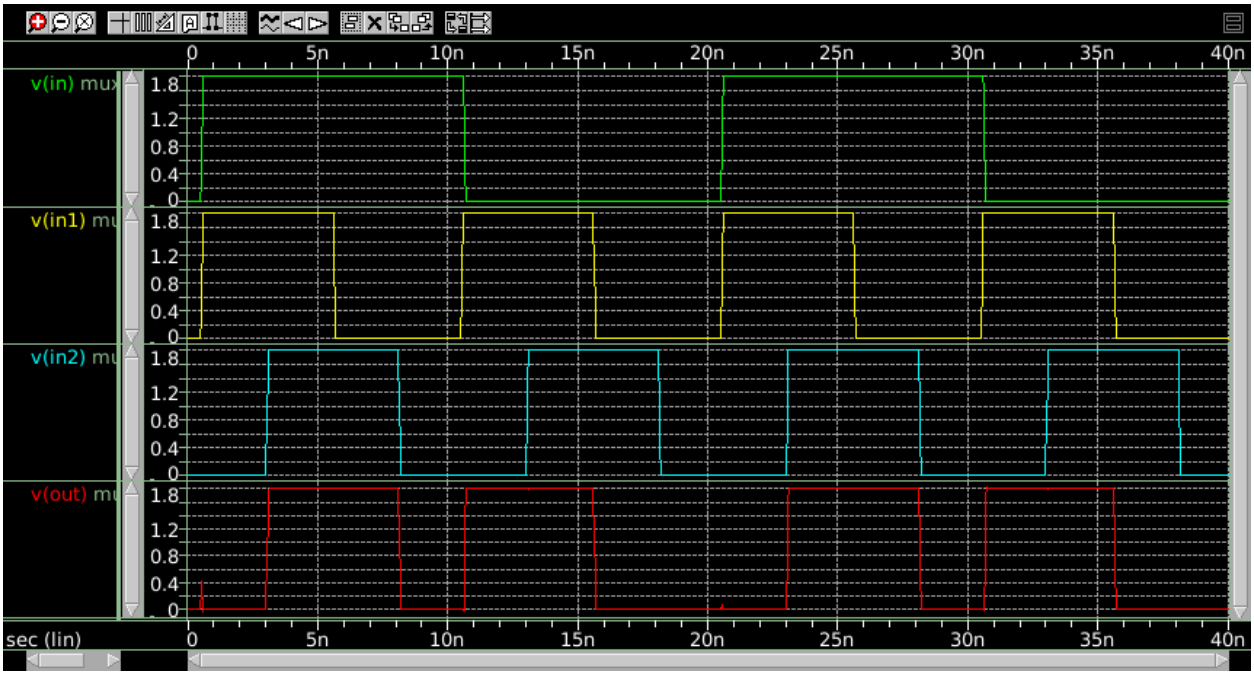
a) Transistor level diagram



b) Spice netlist (.sp file contents)

```
  GNU nano 2.0.9                    File: mux.sp

**--------------------------------------------------------
* Inverter SPICE deck
**--------------------------------------------------------
* Parameters and models
**--------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**--------------------------------------------------------
* Simulation netlist
**--------------------------------------------------------
Vdd Vdd 0 1.8V

*Vname N1 N2 PWL(T1 V1 T2 V2 T3 V3)
*Vin   in 0  PWL(0 0 10ns 0 11ns 1.8 20ns 1.8)

*Vname N1 N2 PULSE V1 V2 td tr tf pw per
Vin  in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns
Vin1 in1 0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns  5ns 10ns
Vin2 in2 0 PULSE 0 1.8V 3.0ns 0.1ns 0.1ns  5ns 10ns

*m# drain gate source body XMOS W=#nm L=#nm

*Transmission gate D0
m0 out N  in1 Vdd NMOS W=180 L=180
m1 out in in1  0  PMOS W=180 L=180

*Transmission gate D1
m2 out in in2 Vdd NMOS W=180 L=180
m3 out N  in2  0  PMOS W=180 L=180

*Inverter for input
m4  N  in Vdd Vdd PMOS W=180 L=180
m5  N  in  0   0  NMOS W=180 L=180

*Cload out 0 0.01pF

.tran 1ns 40ns
.measure tran tr TRIG v(out) val=0.36 RISE=1 TARG v(out) val=1.44 RISE=1
.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=0.36 FALL=1
.measure tran tpdr TRIG v(in) val=0.9 FALL=1 TARG v(out) val=0.9 RISE=1
.measure tran tpdf TRIG v(in) val=0.9 RISE=1 TARG v(out) val=0.9 FALL =1

***  Output Statements
.plot V(in) V(out)
.end
```

c) Waveform results



1st row – V(in) or Mux selector (S)
2nd row – V(in1) or D0
3rd row – (Vin2) or D1
4th row – (Vout) or Y

As you can see, when the selector (Vin) is high (1.8V) only V(in2) input will go to V(out). When selector is low (0V) only V(in1) input will go to V(out)