CDA 4213 001/CIS 6930 012
Fall 2019
CMOS VLSI Design

Lab 5 Report

Canvas Submission
Due: 11:59 PM, 20th Oct. 2019

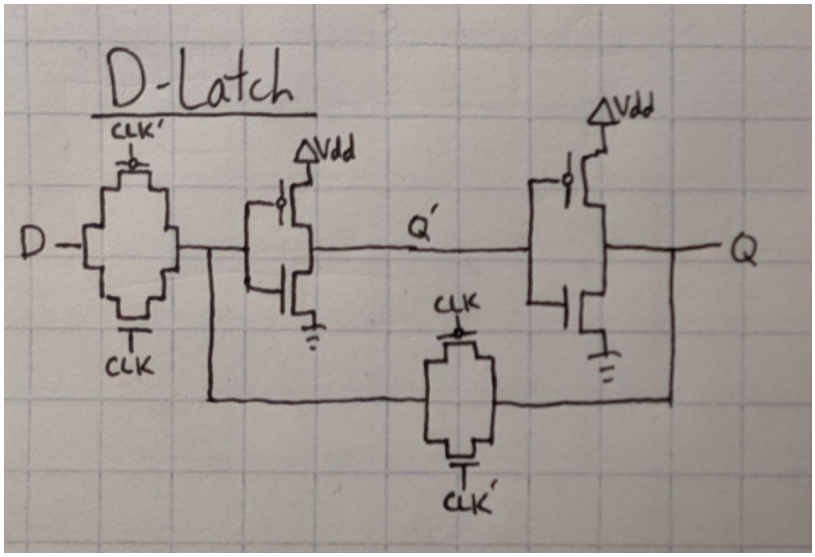
You need to submit only report for your team.

Note: Upload PDF version of this report. Only PDF format is accepted.

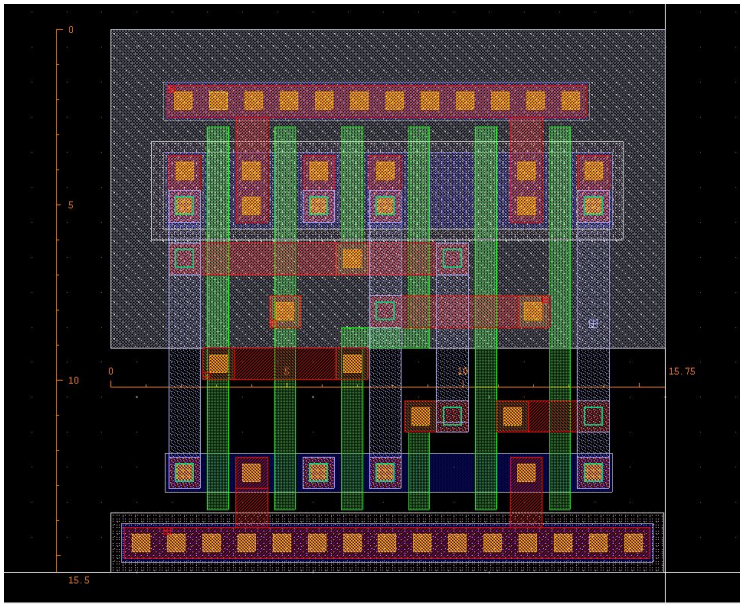
Today's Date:	10-19-19
Your Team and U Numbers:	Trent Callahan - U14228486 Denislav Tsonev - U64519666 Boyang Wu - U95035892
Your U Number:	U14228486
No. of Hours Spent:	30
Exercise Difficulty: (Easy, Average, Hard)	Hard
Work Distribution: (Identify who did what)	Boyang - D Flip-Flop and 3-Bit Shift Register design and layout Denislav - D Latch design and layout Trent - Lab report, unused NAND-based D Latch
Any Other Feedback:	

Question 1 (5 pts): Positive Level Sensitive D-latch
Include the following
a) Transistor level diagram
b) Image of your layout
c) Bounding box area (width x height)
d) Waveform results

Transistor Level Diagram -



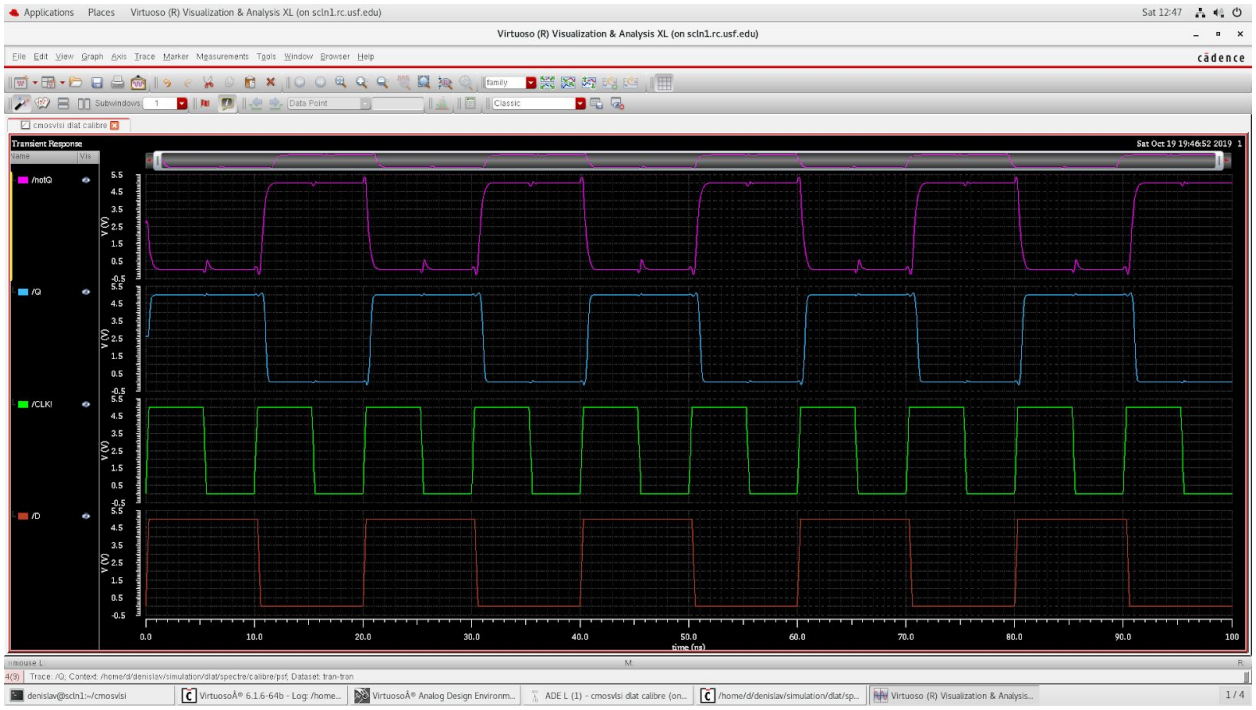
Layout image -



Bounding Box Area -

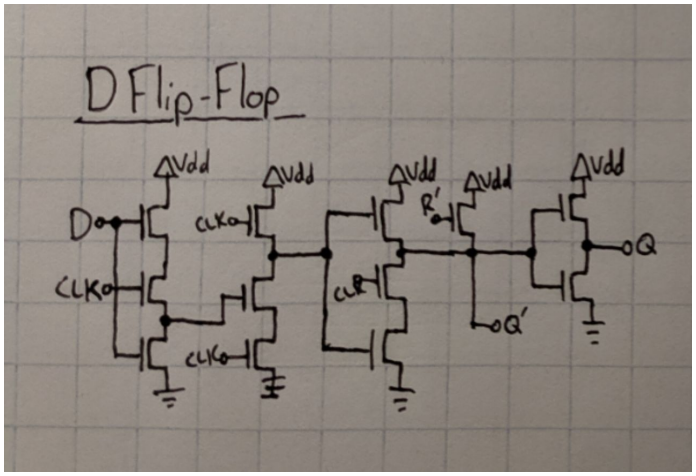
15.5 * 15.75 = **244.125**

Waveform Results -

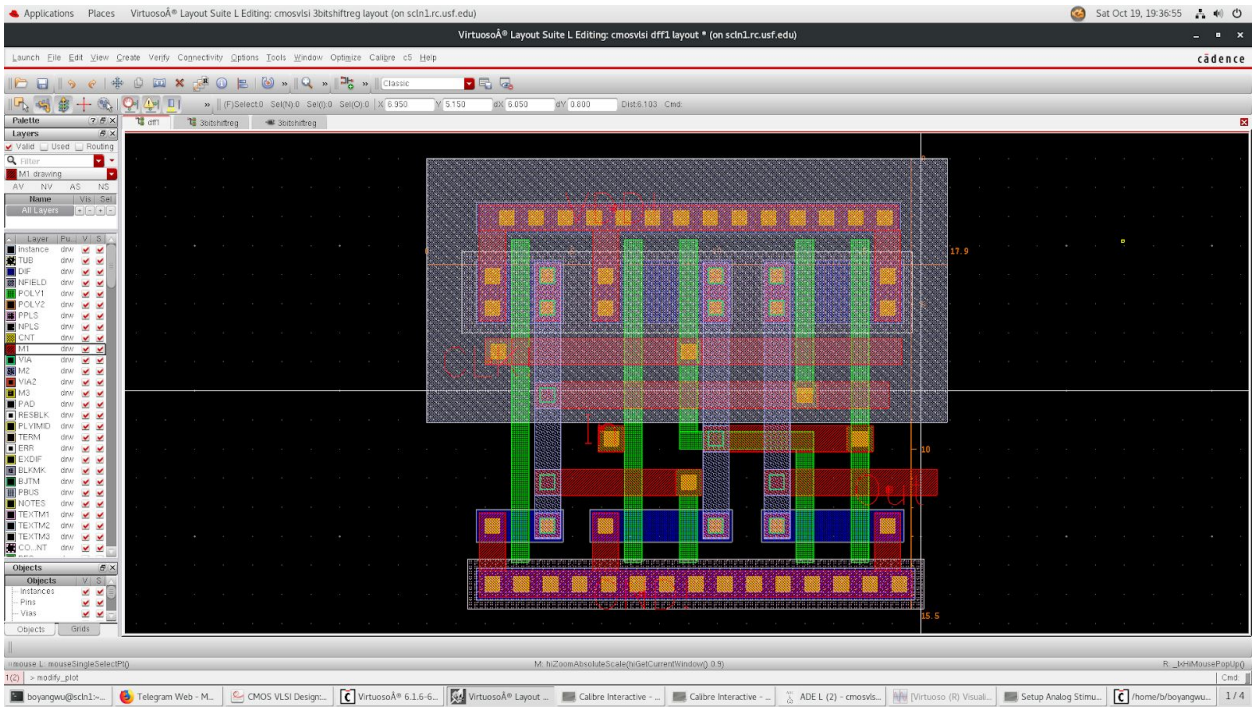


Question 2 (5 pts): Positive Edge Triggered D Flip-flop
Include the following
a) Transistor level diagram
b) Image of your layout
c) Bounding box area (width x height)
d) Waveform results

Transistor Level Diagram -



Layout Image -



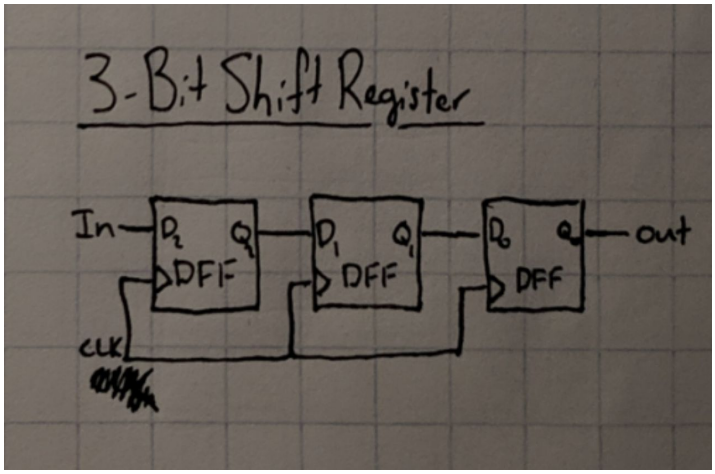
Bounding Box Area -

15.5 * 17.9 = **277.45**

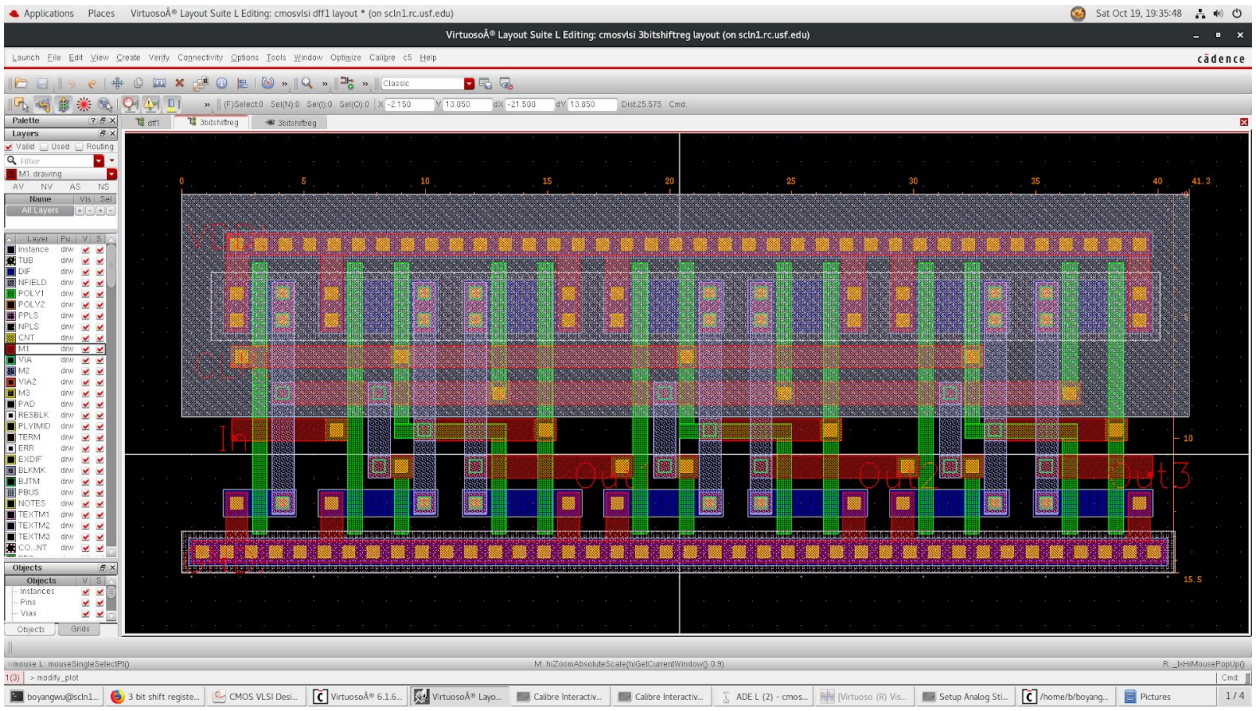
Waveform Results -

Question 3 (10 pts): 3-bit Shift Register
Include the following
a) Transistor level diagram
b) Image of your layout
c) Bounding box area (width x height)
d) Waveform results

Transistor Level Diagram -



Layout Image -



Bounding Box Area -

41.3 * 15.5 = **640.15**

Waveform Results -