Introduction to SPICE

Acknowledgement

- These slides are adapted from the lecture: Spice Simulation by Prof. David Harris of Harvey Mudd College.

Introduction to SPICE

- **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis
  - Developed in 1970's at Berkeley
  - Many commercial versions are available
  - HSPICE is a robust industry standard
    - Has many enhancements that we will use
- Written in FORTRAN for punch-card machines
  - Circuits elements are called *cards*
  - Complete description is called a SPICE *deck*

Writing Spice Decks

- Writing a SPICE deck is like writing a good program
  - Plan: sketch schematic on paper or in editor
    - Modify existing decks whenever possible
  - Code: strive for clarity
    - Start with circuit name and its functionality
    - Generously comment
  - Test:
    - Predict what results should be
    - Compare with actual
    - *Garbage In, Garbage Out!*

Voltage Sources

- Node 0 is the ground terminal
- *DC* Source

  Vname N1 N2 Type Value

  Example:

  ```
  Vdd vdd 0 5
  ```

- *Piecewise Linear* Source

  Vname N1 N2 PWL(T1 V1 T2 V2 T3 V3 ...)

  Example:

  ```
  Vin in 0 pwl 0ps 0 100ps 0 150ps 1.8 800ps 1.8
  ```

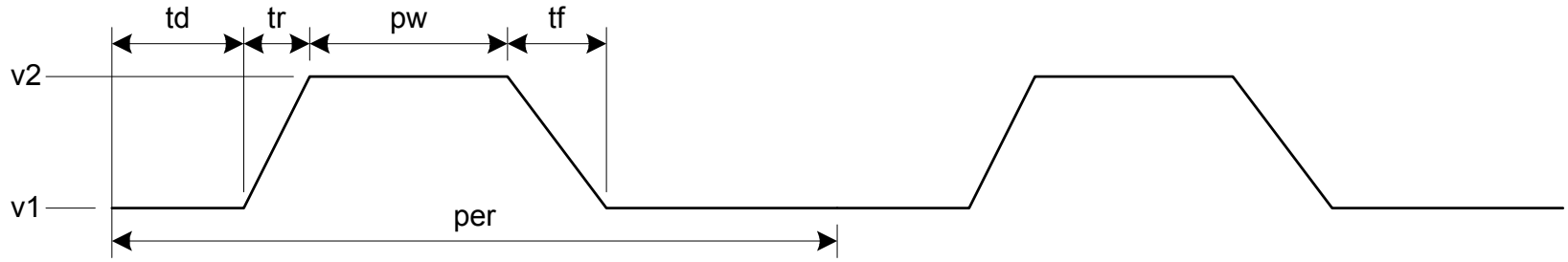
Voltage Sources…contd.

- *Pulsed* Source

V<name> N1 N2 PULSE V1 V2 td tr tf pw per

Example: Vin in gnd PULSE 0 5 0.5ns 0.1ns 0.1ns 4ns 8ns

PULSE v1 v2 td tr tf pw per



SPICE Elements

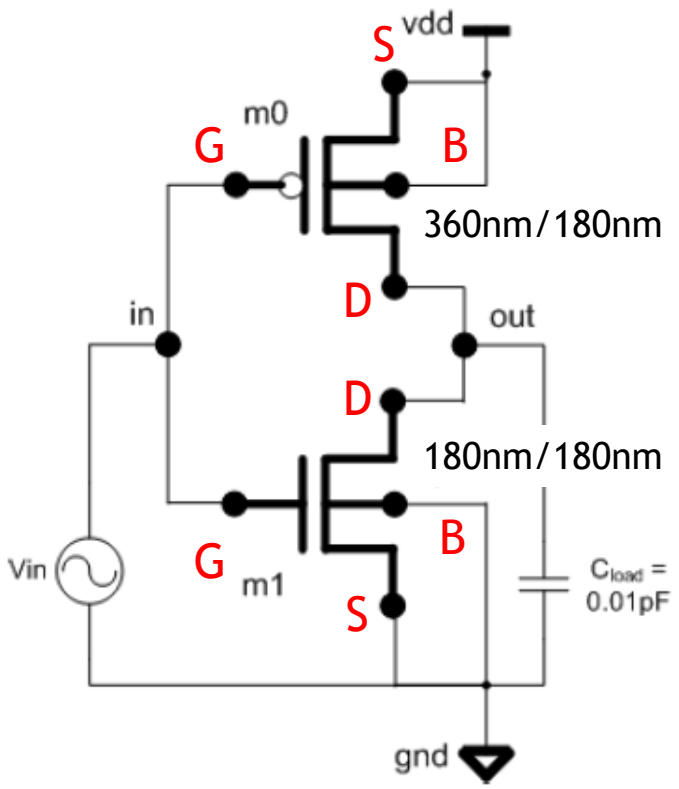
Letter	Element
R	Resistor
C	Capacitor
L	Inductor
K	Mutual Inductor
V	Independent voltage source
I	Independent current source
M	MOSFET
D	Diode
Q	Bipolar transistor
W	Lossy transmission line
X	Subcircuit
E	Voltage-controlled voltage source
G	Voltage-controlled current source
H	Current-controlled voltage source
F	Current-controlled current source

Units

Letter	Unit	Magnitude
a	atto	10^{-18}
f	fempto	10^{-15}
p	pico	10^{-12}
n	nano	10^{-9}
u	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
x	mega	10^{6}
g	giga	10^{9}

Ex: 100 femptofarad capacitor = 100fF, 100f, 100e-15

Example: INV Circuit



- Each MOSFET has four terminals:
  - D (Drain)
  - G (Gate)
  - S (Source)
  - B (Body)
- The bulk terminal of **PMOS** should be tied to **Vdd**
- The bulk terminal of **NMOS** should be tied to **Ground**
- Each MOSFET has W (Width) and L (Length)

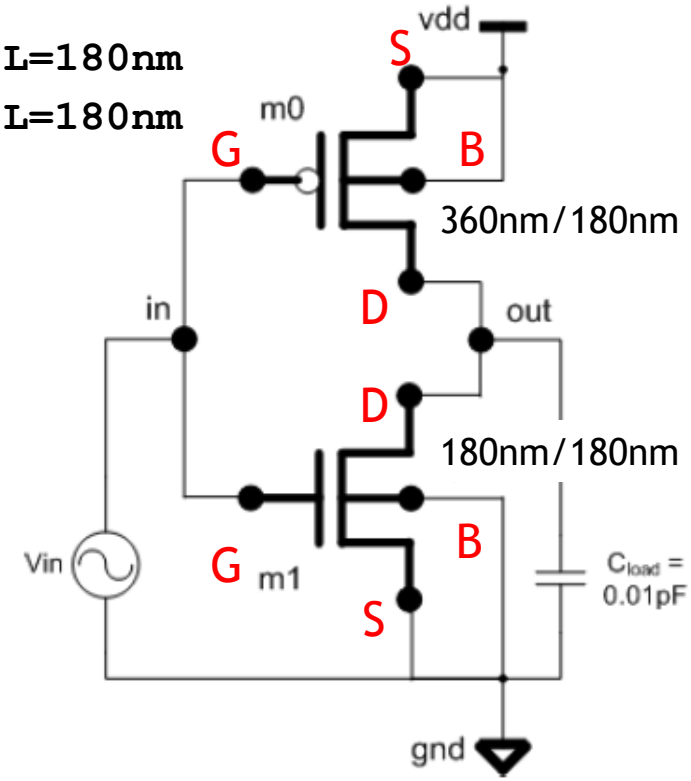
MOSFET Elements

M element for MOSFET

```
Mname drain gate source body type W=<width> L=<length>
```

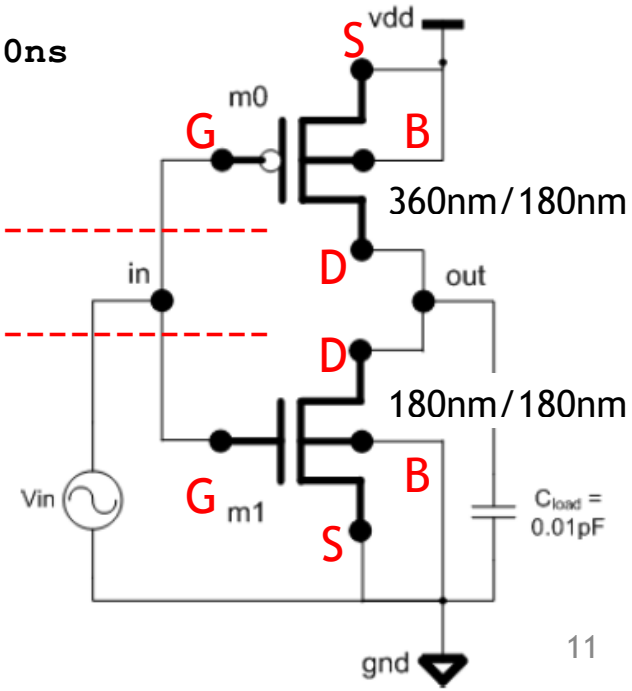
Example:

```
m0 out in vdd vdd PMOS W=360nm L=180nm
m1 out in   0   0 NMOS W=180nm L=180nm
```



INV Circuit SPICE Deck

```
**-------------------------------------------------------------
*       Inverter SPICE deck
**-------------------------------------------------------------
*       Parameters and models
**-------------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n
**-------------------------------------------------------------
*       Simulation netlist
**-------------------------------------------------------------
Vdd Vdd 0 1.8V
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns
m0  out in Vdd Vdd PMOS W=360 L=180
m1  out in  0   0  NMOS W=180 L=180
Cload out 0 0.01pF
**-------------------------------------------------------------
*       Stimulus and plot statements
**-------------------------------------------------------------
.tran   1n  40n
.plot   V(in) V(out)
.end
```



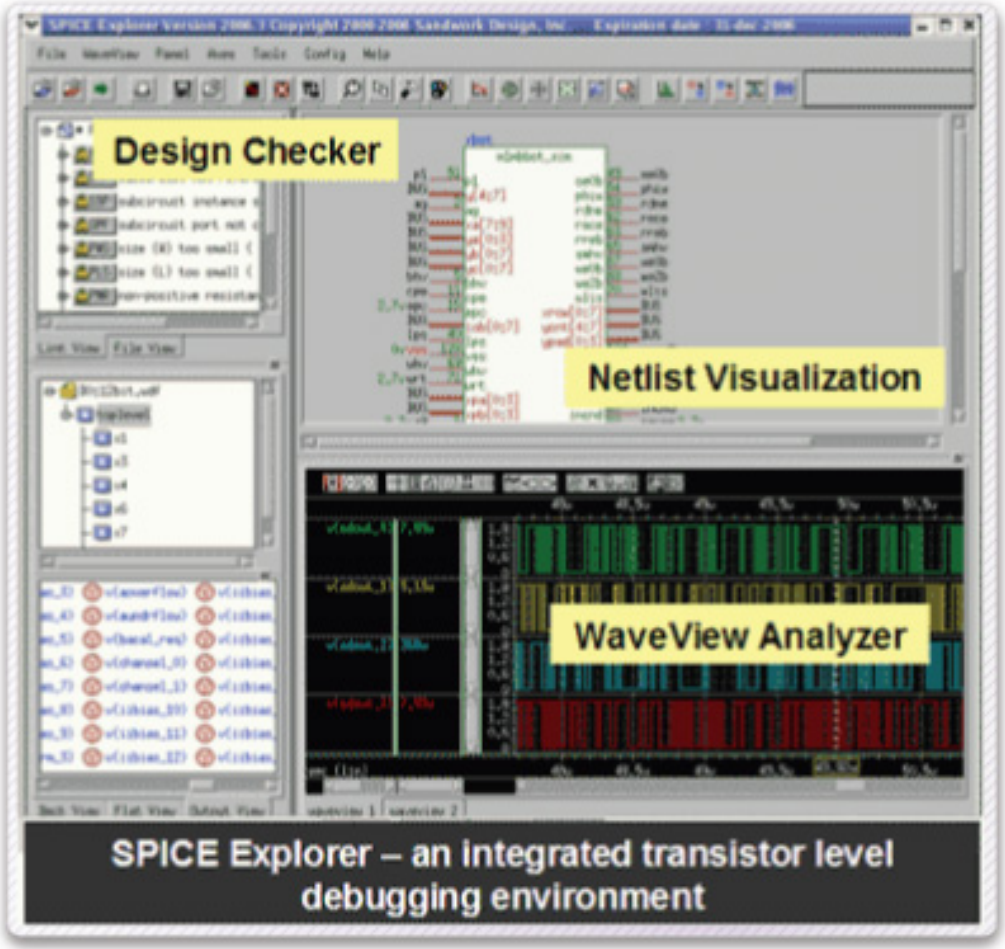
Running HSPICE

- Run from Command Line
  prompt% hspice -i inv.sp -o inv.lis

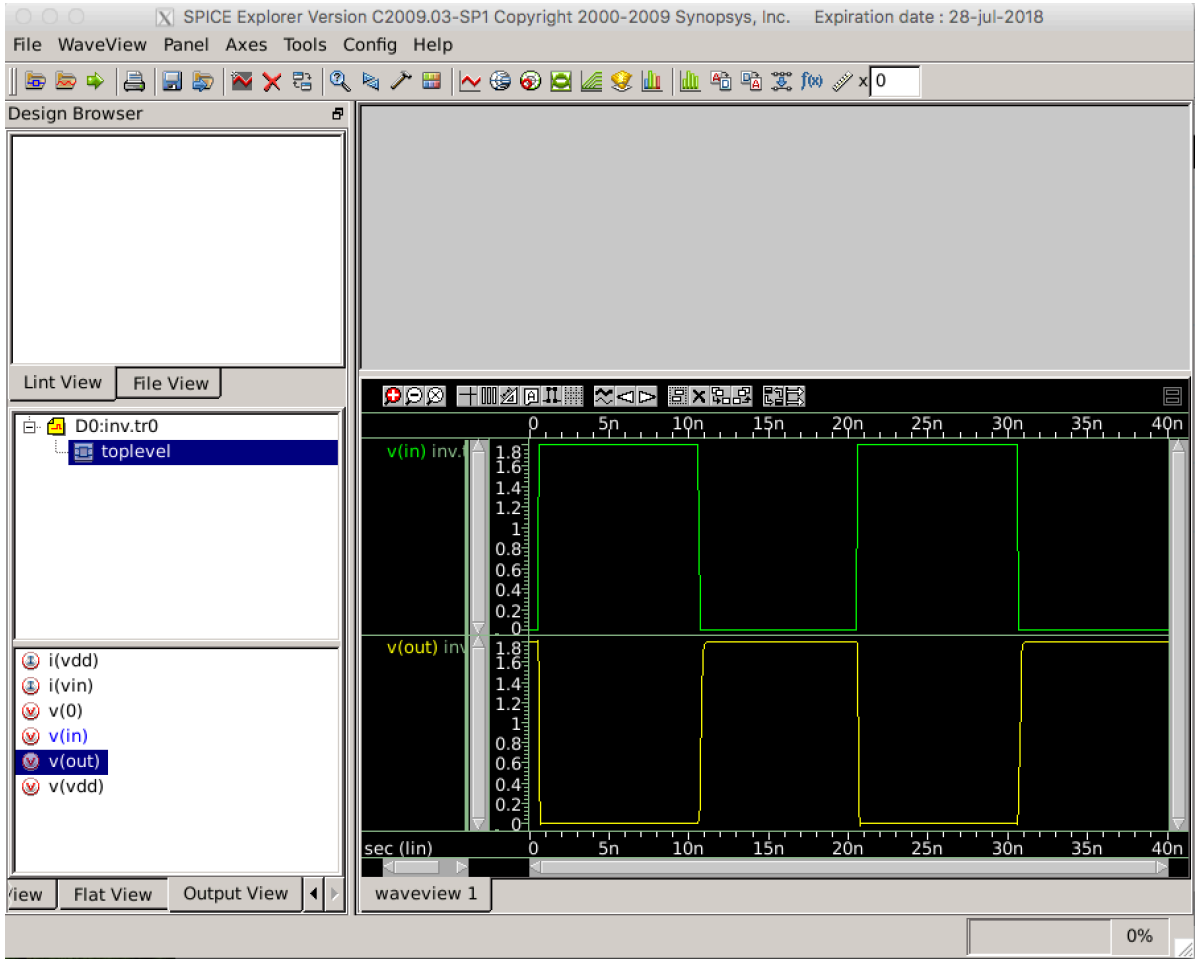
- When the job finishes, HSPICE displays:
  >info: ***** hspice job concluded

SPICE Explorer

prompt% sx



Viewing Waveforms



Getting Started

- Connect to USF RC Research Cluster
- Setup path by editing .bashrc file
- Copy inverter and model files
- Run **hspice**
- Run **sx**
- Print the waveforms to a file