CDA 4213L 001/CIS 6930 012
Fall 2019
CMOS VLSI Design

Lab 1 Report

Canvas Submission
Due: 11:59 PM, 15th Sept. 2019

Note: Upload PDF version of this report. Only PDF format is accepted.

Today's Date:	9/4
Your Name:	Boyang Wu
Your U Number:	U95035892
No. of Hours Spent:	4 hours
Exercise Difficulty: (Easy, Average, Hard)	Average
Any Other Feedback:	Needs better documentation

Question 1: Inverter

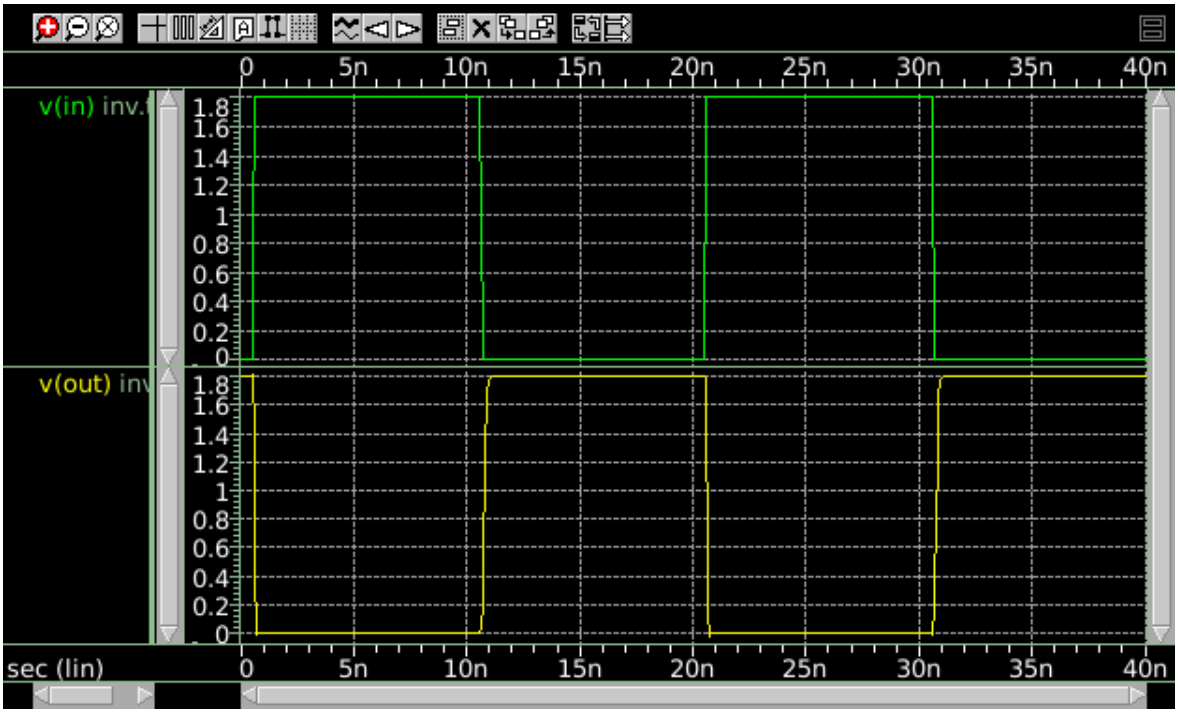
a) Complete the following table with values estimated in your simulations

Cload	tr	tf	tpdr	tpdf
0.01 pF	1.261e-10	7.594e-11	1.097e-10	7.506e-11
0.05pF	6.196e-10	4.282e-10	4.395e-10	3.113e-10
0.1pF	1.238e-09	7.968e-10	8.952e-10	5.651e-10

b) For each C_{load}, show your hspice netlist (.sp file contents) and the waveform results. Use as many pages as needed.

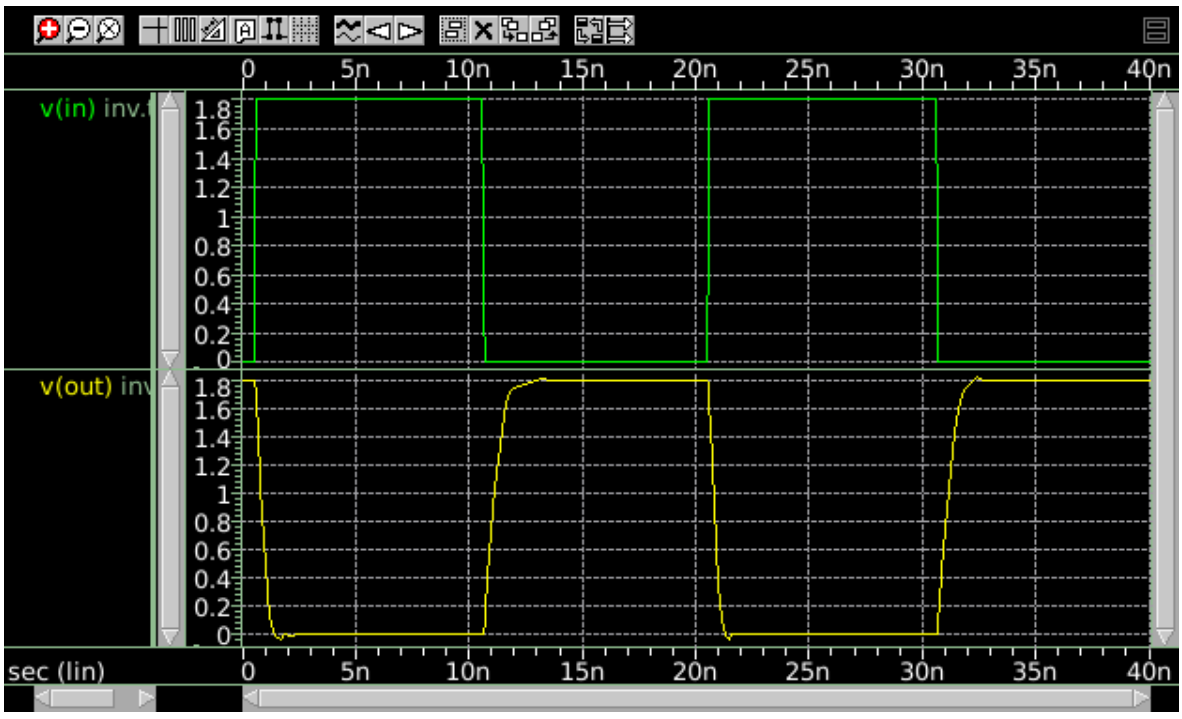
0.01pF

```
  GNU nano 2.0.9                    File: inv.sp

**-------------------------------------------------------------
* Inverter SPICE deck
**-------------------------------------------------------------
* Parameters and models
**-------------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------------
Vdd Vdd 0 1.8V
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns

m0 out in Vdd Vdd PMOS W=360 L=180
m1 out in  0   0  NMOS W=180 L=180

Cload out 0 0.01pF

.tran 1ns 40ns
.measure tran tr TRIG v(out) val=0.36 RISE=1 TARG v(out) val=1.44 RISE=1
.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=0.36 FALL=1
.measure tran tpdr TRIG v(in) val=0.9 FALL=1 TARG v(out) val=0.9 RISE=1
.measure tran tpdf TRIG v(in) val=0.9 RISE=1 TARG v(out) val=0.9 FALL =1
*.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=0.36 FALL=1

***  Output Statements
.plot V(in) V(out)
.end
```



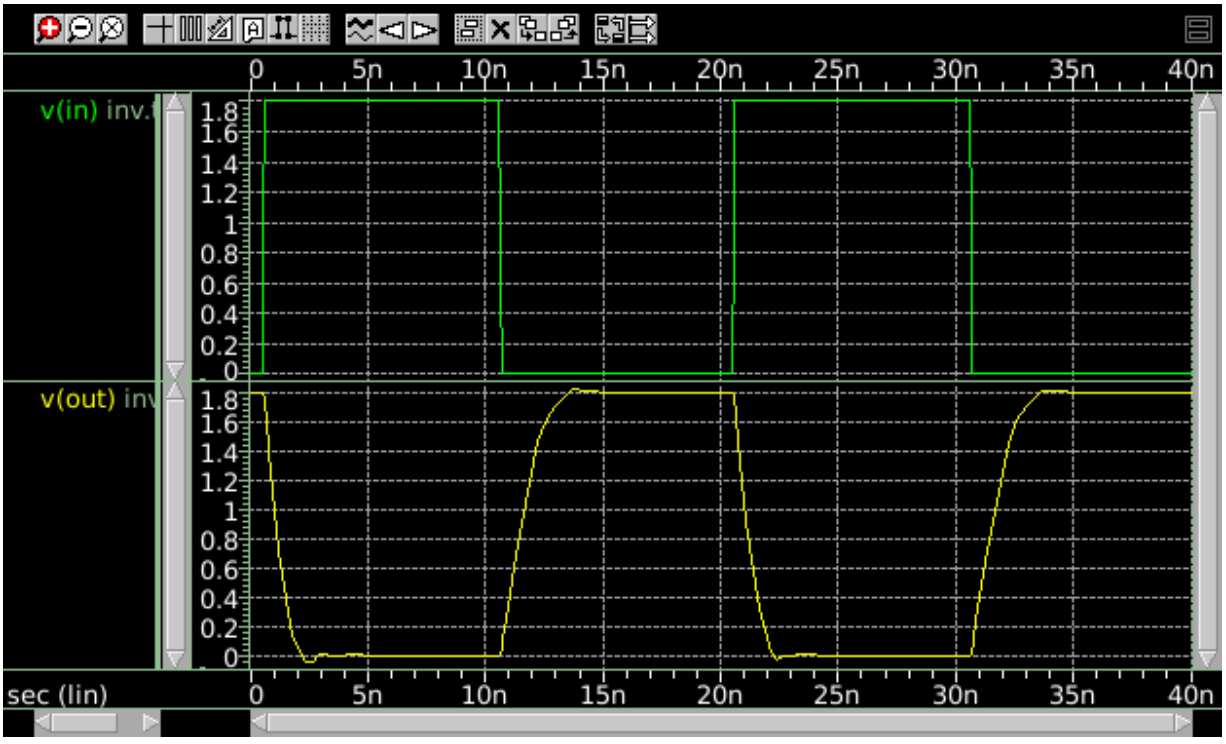
0.05pF

```
  GNU nano 2.0.9                    File: inv.sp

**------------------------------------------------------------
* Inverter SPICE deck
**------------------------------------------------------------
* Parameters and models
**------------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**------------------------------------------------------------
* Simulation netlist
**------------------------------------------------------------
Vdd Vdd 0 1.8V
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns

m0 out in Vdd Vdd PMOS W=360 L=180
m1 out in  0   0  NMOS W=180 L=180

Cload out 0 0.05pF

.tran 1ns 40ns
.measure tran tr TRIG v(out) val=0.36 RISE=1 TARG v(out) val=1.44 RISE=1
.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=0.36 FALL=1
.measure tran tpdr TRIG v(in) val=0.9 FALL=1 TARG v(out) val=0.9 RISE=1
.measure tran tpdf TRIG v(in) val=0.9 RISE=1 TARG v(out) val=0.9 FALL =1
*.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=0.36 FALL=1

***  Output Statements
.plot V(in) V(out)
.end
```



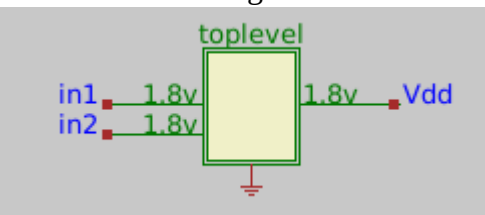
0.1pF

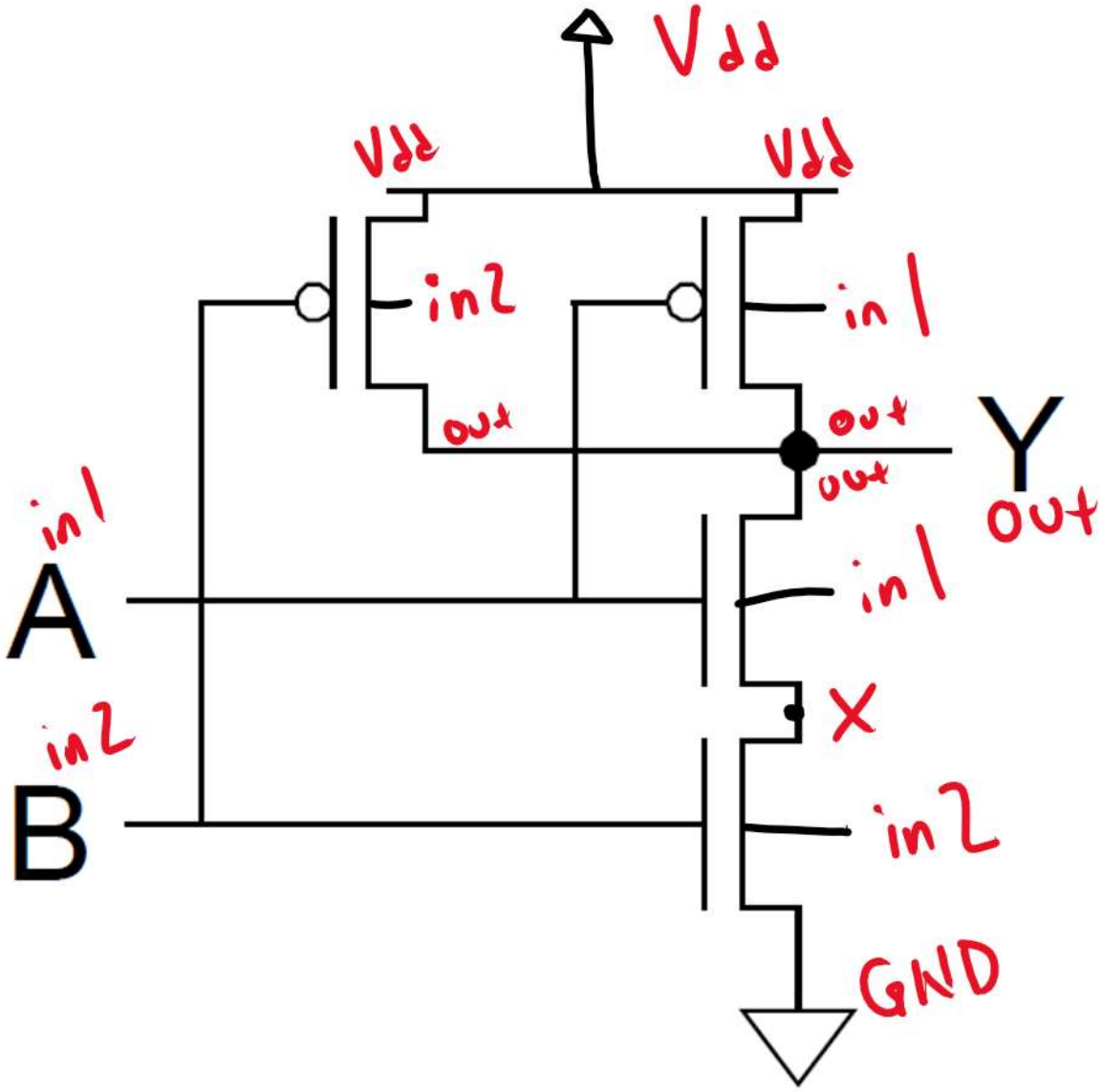
```
  GNU nano 2.0.9                    File: inv.sp

**------------------------------------------------------------
* Inverter SPICE deck
**------------------------------------------------------------
* Parameters and models
**------------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**------------------------------------------------------------
* Simulation netlist
**------------------------------------------------------------
Vdd Vdd 0 1.8V
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns

m0 out in Vdd Vdd PMOS W=360 L=180
m1 out in  0   0  NMOS W=180 L=180

Cload out 0 0.1pF

.tran 1ns 40ns
.measure tran tr TRIG v(out) val=0.36 RISE=1 TARG v(out) val=1.44 RISE=1
.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=0.36 FALL=1
.measure tran tpdr TRIG v(in) val=0.9 FALL=1 TARG v(out) val=0.9 RISE=1
.measure tran tpdf TRIG v(in) val=0.9 RISE=1 TARG v(out) val=0.9 FALL =1
*.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=0.36 FALL=1

***  Output Statements
.plot V(in) V(out)
.end
```



Question 2: 2-input NAND Gate

a) Transistor level diagram





b) Spice netlist (.sp file contents)

0-5ns is input 00

5ns-10ns is input 11

10ns-15ns is input 01

15ns-20ns is input 10

```
  GNU nano 2.0.9                    File: nand.sp

**-------------------------------------------------------------
* Inverter SPICE deck
**-------------------------------------------------------------
* Parameters and models
**-------------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------------
Vdd Vdd 0 1.8V
Vin1 in1 0 PWL(0 0 4.9ns 0 5ns 2 9.9ns 2 10ns 0 14.9ns 0 15ns 2 19.9ns 2 20ns 2 R)
Vin2 in2 0 PWL(0 0 4.9ns 0 5ns 2 9.9ns 2 10ns 2 14.9ns 2 15ns 0 19.9ns 0 20ns 0 R)

m1 out in1 Vdd Vdd PMOS W=180 L=180
m2 out in2 Vdd Vdd PMOS W=180 L=180
m3 out in1  X   0  NMOS W=180 L=180
m4  X  in2  0   0  NMOS W=180 L=180

Cload out 0 0.01pF

.tran 1n 40n
*.measure tran tr TRIG v(out) val=0.36 RISE=1 TARG v(out) val=1.44 RISE=1
*.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=0.36 FALL=1
*.measure tran tpdr TRIG v(in) val=0.9 FALL=1 TARG v(out) val=0.9 RISE=1
*.measure tran tpdf TRIG v(in) val=0.9 RISE=1 TARG v(out) val=0.9 FALL =1

***  Output Statements
.plot V(in1) V(in2) V(out)
.end
```

c) Waveform results (show waveforms for all possible input combinations)

0-5ns is input 00

5ns-10ns is input 11

10ns-15ns is input 01

15ns-20ns is input 10

The tiny spikes at 15ns and 20ns are due to the 0.1ns of inputs switching