CDA 4213 001/CIS 6930 012
Fall 2019
CMOS VLSI Design

Lab 4 Report

Canvas Submission
Due: 11:59 PM, 6th Oct. 2019

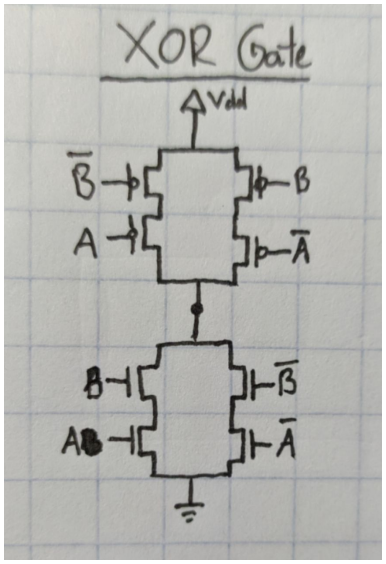
You need to submit only report for your team.

Note: Upload PDF version of this report. Only PDF format is accepted.

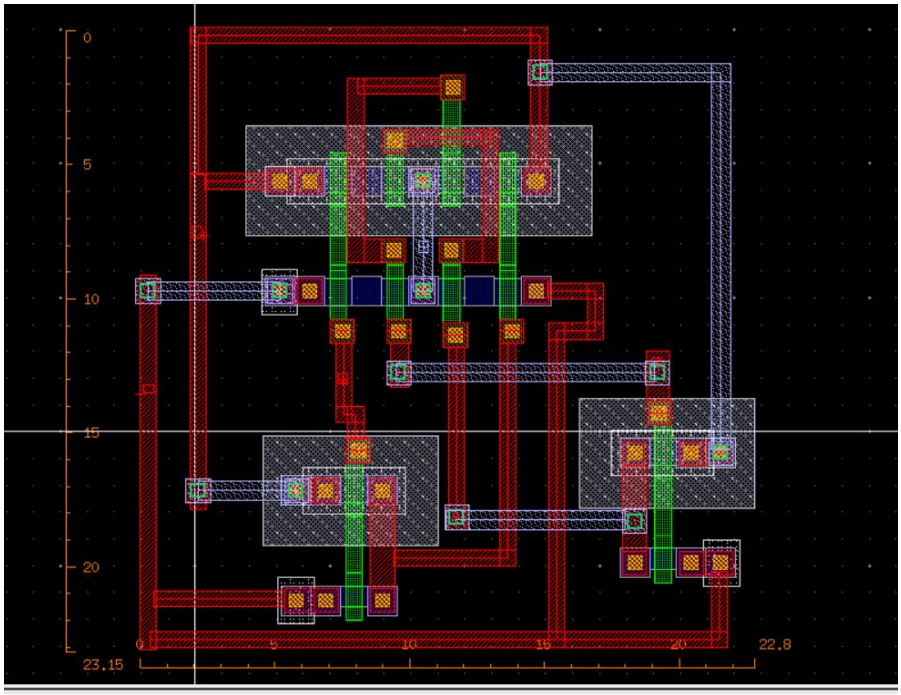
Today's Date:	10-11-19
Your Team and U Numbers:	Trent Callahan - U14228486 Denislav Tsonev - U64519666 Boyang Wu - U95035892
Your U Number:	U14228486
No. of Hours Spent:	18
Exercise Difficulty: (Easy, Average, Hard)	Average
Work Distribution: (Identify who did what)	Denislav - XOR Gate, optimization Boyang - Full Adder, fixed/optimized oscillator Trent - Initial oscillator, lab report
Any Other Feedback:	

Question 1 (5 pts): 2-input XOR
Include the following
a) Transistor level diagram
b) Image of your layout
c) Bounding box area (width x height)
d) Waveform results

Transistor Level Diagram -



Layout Image -

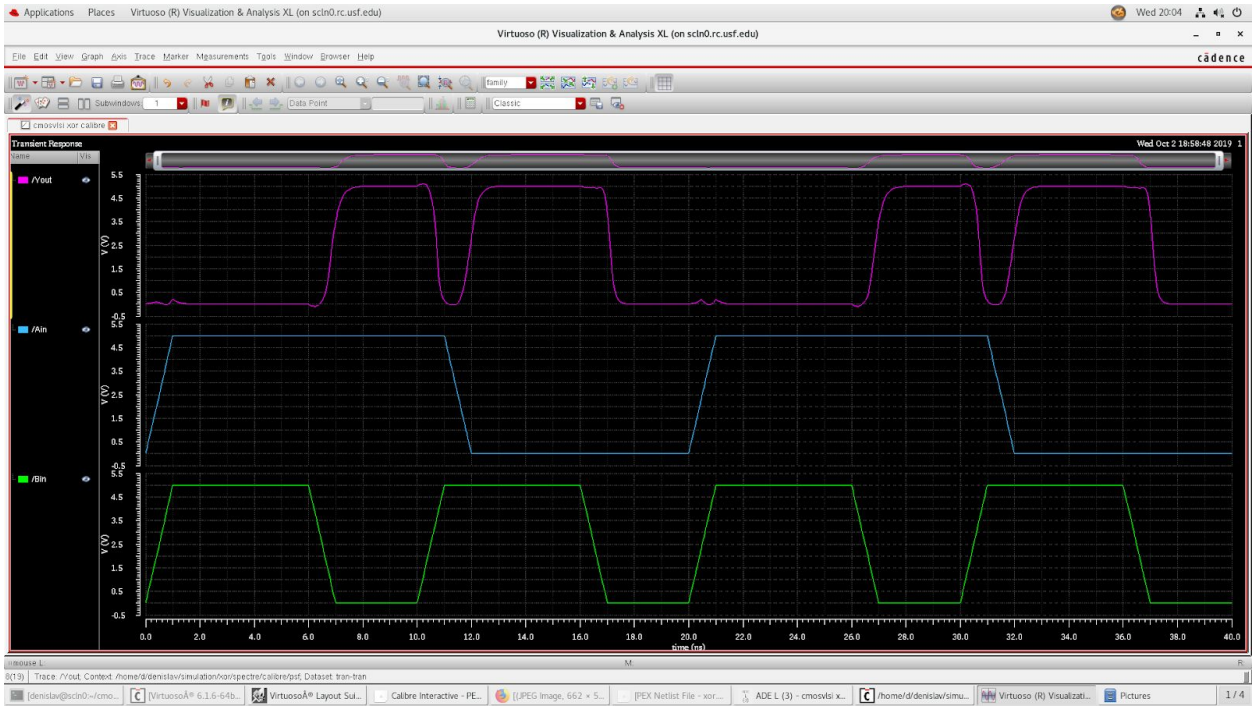


Bounding Box Area -

23.15 x 22.8 = 527.82

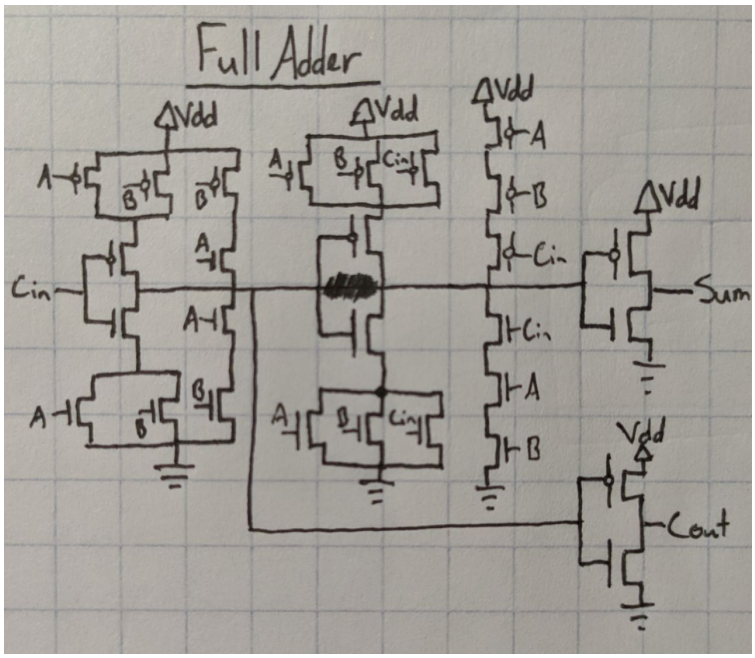
Total area is **527.82**.

Waveform Results -

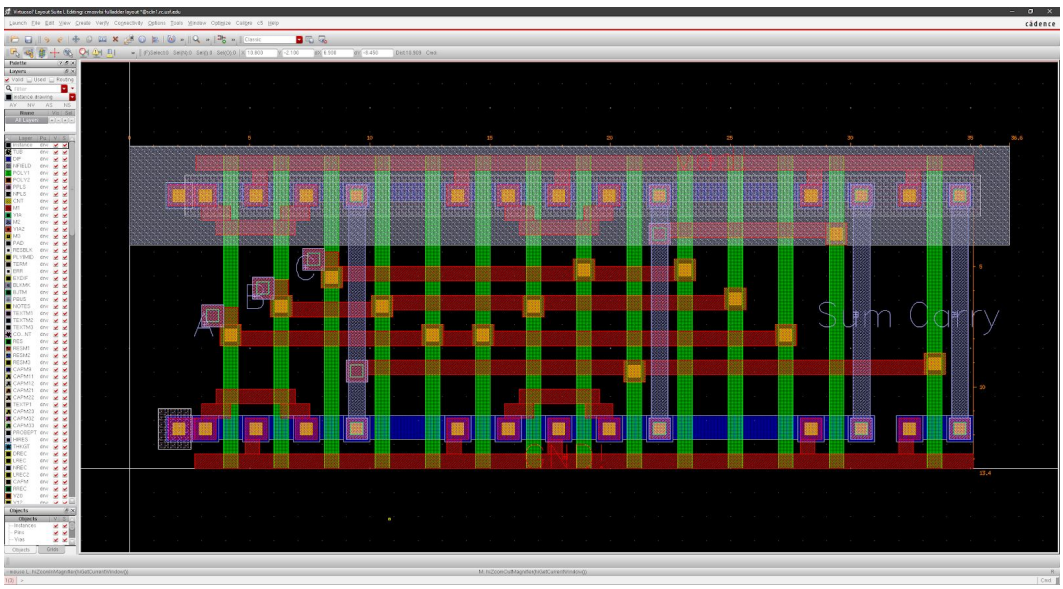


Question 2 (10 pts): Full Adder
Include the following
a) Transistor level diagram
b) Image of your layout
c) Bounding box area (width x height)
d) Waveform results

Transistor Level Diagram -



Layout Image -



Bounding Box Area -

36.6 x 13.4 = 490.44

Total area is **490.44**.

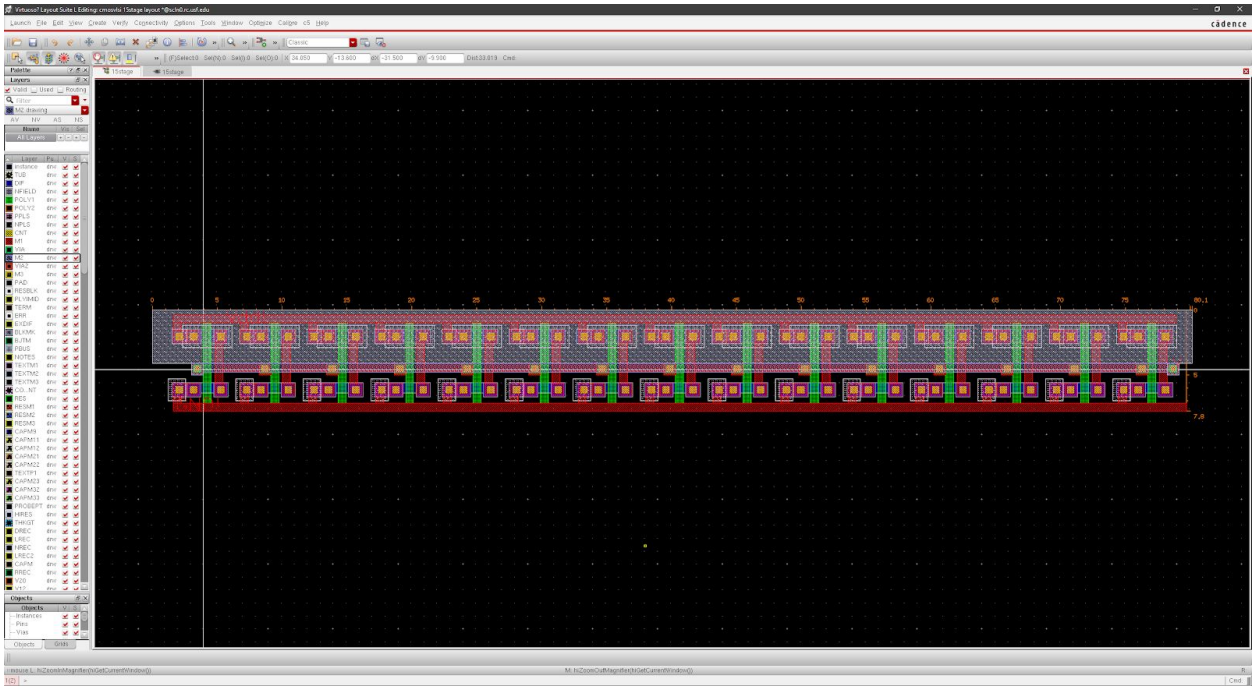
Waveform Results -

Question 3 (5 pts): 15-stage Ring Oscillator
Include the following
a) Clock frequency of the ring oscillator
b) Image of your layout
c) Bounding box area (width x height)
d) Waveform results

Clock Frequency -

Assuming roughly 7ns per cycle, the oscillator operated at a ~142MHz frequency.

Layout image -



Bounding Box Area -

80.1 x 7.8 = 624.78

Total area is **624.78**.

Waveform Results -