CDA 4213 001/CIS 6930 012
CMOS VLSI Design
Fall 2019
Lab 5

Assigned: Wednesday, 9th October 2019
Due: 11:59 PM, Sunday, 20th October 2019

Note: This lab assignment carries 7.5% of the final grade. Start early!

Teaming
Undergraduates: You can team up with up to two other Undergraduate students.
Graduates: You can team up with another Graduate student.
Objective(s) To create basic cells that will be used in your final project.

Details
For the following basic cells, draw the layout and verify the functionality by simulating the extracted netlist. You should strive to get as compact a layout as possible without violating the design rules. The *bounding box* of a layout is the smallest rectangle in which your layout can fit. In the lab report you must report the bounding box area (width x height) of each cell.

1. (5 pts.) Positive Level Sensitive D-latch. Look at page 17, fig. 1.31 in the text for ideas on optimized D-latch implementation.
2. (5 pts.) Positive Edge Triggered D Flip-flop. Design a D-latch first and then cascade two of them with appropriate clock signals. Look at page 18, fig. 1.32 in the text for ideas on optimized D flip-flop implementation.
3. (10 pts.) 3-bit Shift Register. A collection of D flip-flops sharing a common clock input can be used to create the register.

Deliverables (must be uploaded to Canvas by the deadline)

- Lab report using the template provided. PDF only.
- A compressed zip file (.tar.gz file) of the design folder of each cell in your lib directory.

Tips

- You can use the pre-drawn cells for PMOS (`epm`) and NMOS (`enm`) cells in the c5 library as the starting point for your layouts.
- You can expand/flatten epm or enm cell by first selecting the cell and then pressing **Shift-f**.
- Do not discard your designs. You will need them for your final project.
- A Word template will be provided which should be used for your report.
- Include all Layout designs, simulation waveforms. For simulation results, zoom in/out appropriately so that we can clearly see the input stimuli and the output response.

Good Luck!