CDA 4213 001/CIS 6930 012
Fall 2019
CMOS VLSI Design

Lab 3 Report

Canvas Submission
Due: 11:59 PM, Sunday, 29th Sept. 2019

You need to submit only report for your team.

Note: Upload PDF version of this report. Only PDF format is accepted.

Today's Date:	9/26/19
Your Team and U Numbers:	Trent Callahan U14228486 Denislav Tsonev U64519666 Boyang Wu U95035892
Your U Number:	U95035892
No. of Hours Spent:	20
Exercise Difficulty: (Easy, Average, Hard)	Average
Work Distribution: (Identify who did what)	Denislav - Designed NAND gate Boyang - Designed NOR gate, reduced sizes for all gates Trent - Debugging and Report
Any Other Feedback:	Tell us how to import NMOS/PMOS from C5 library earlier

Question 1 (10 pts): Inverter
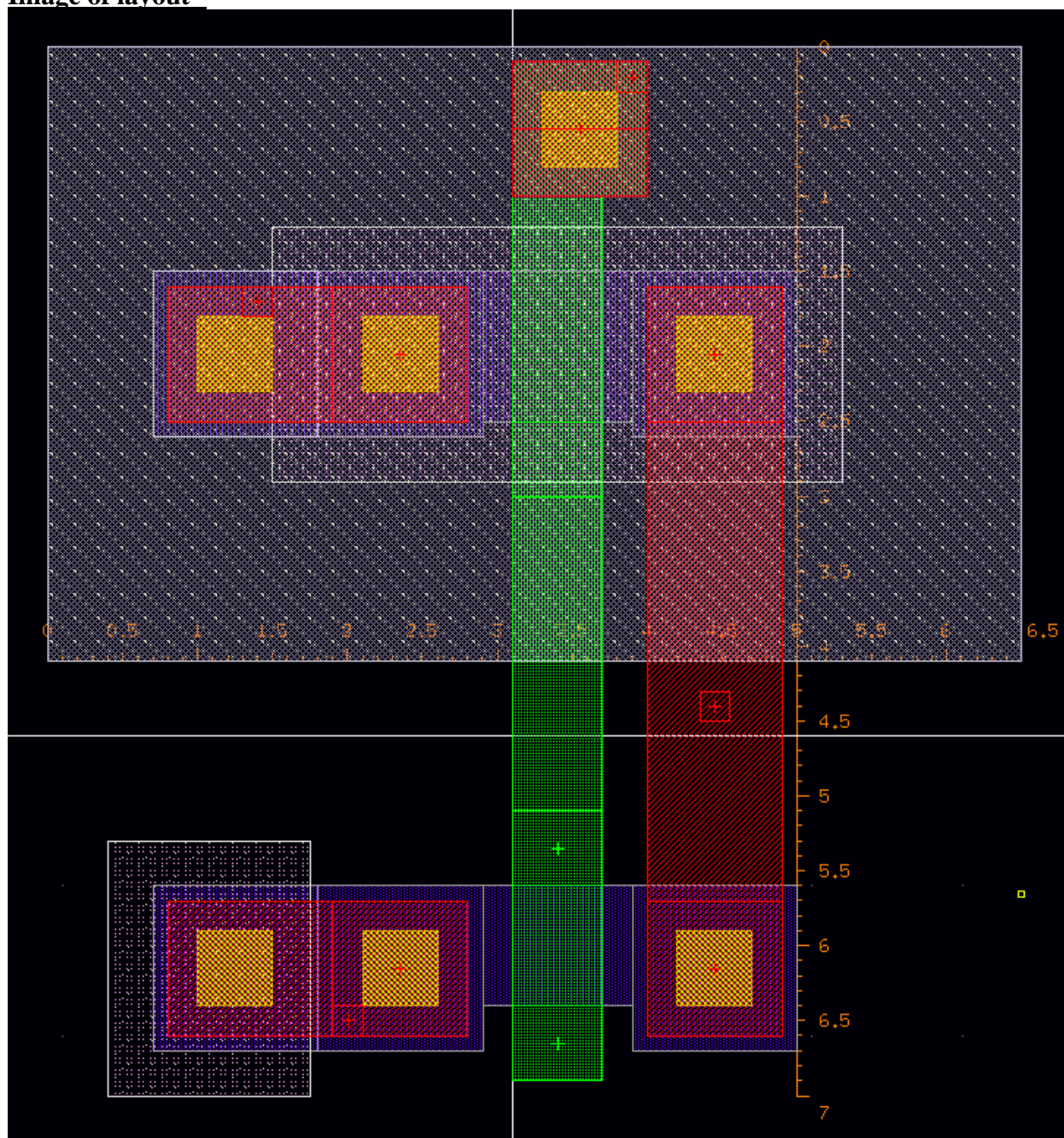Include the following

       a) Transistor level diagram
       b) Image of your layout
       c) Bounding box area (width x height)
       d) Waveform results

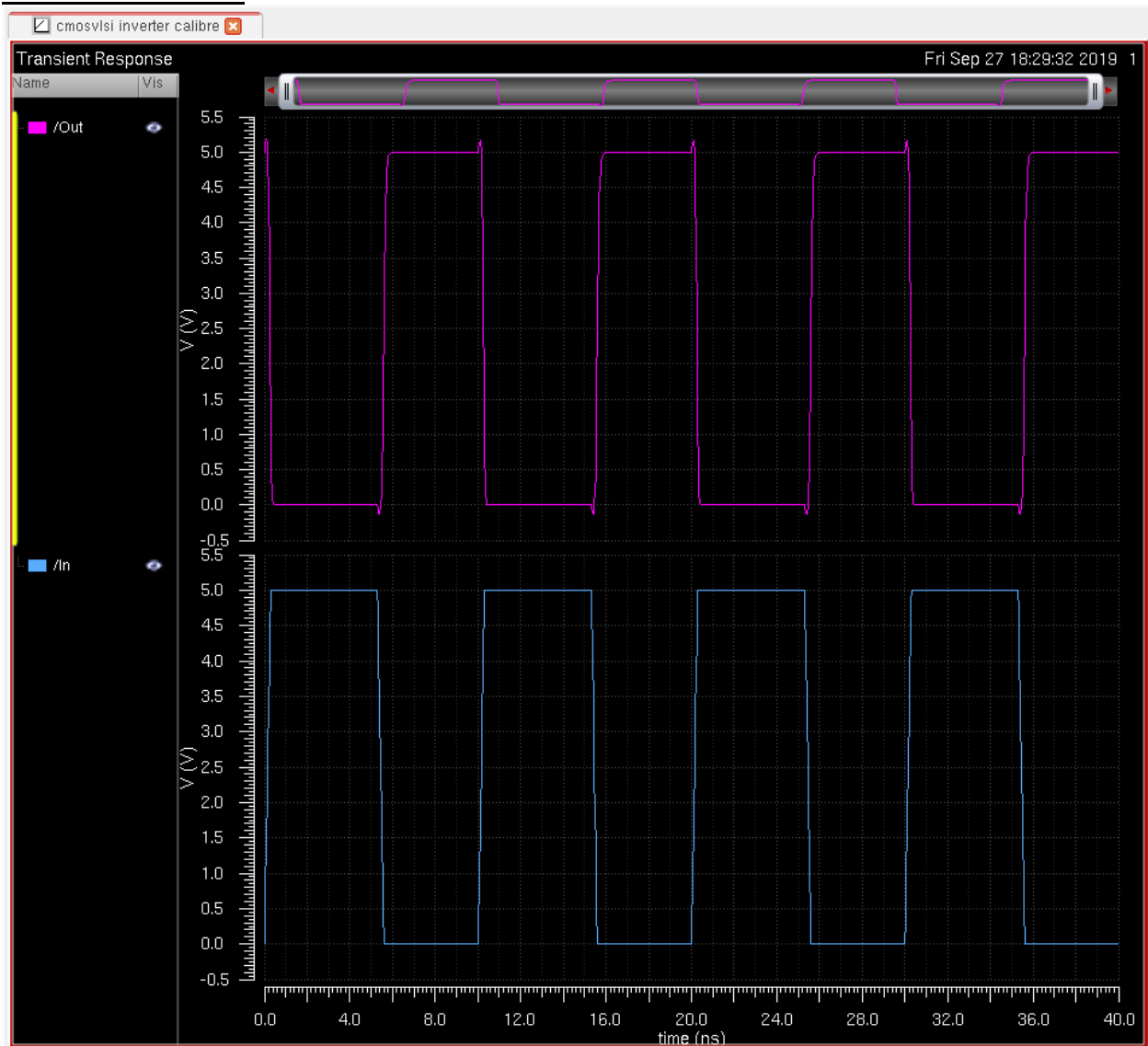## Transistor level diagram -
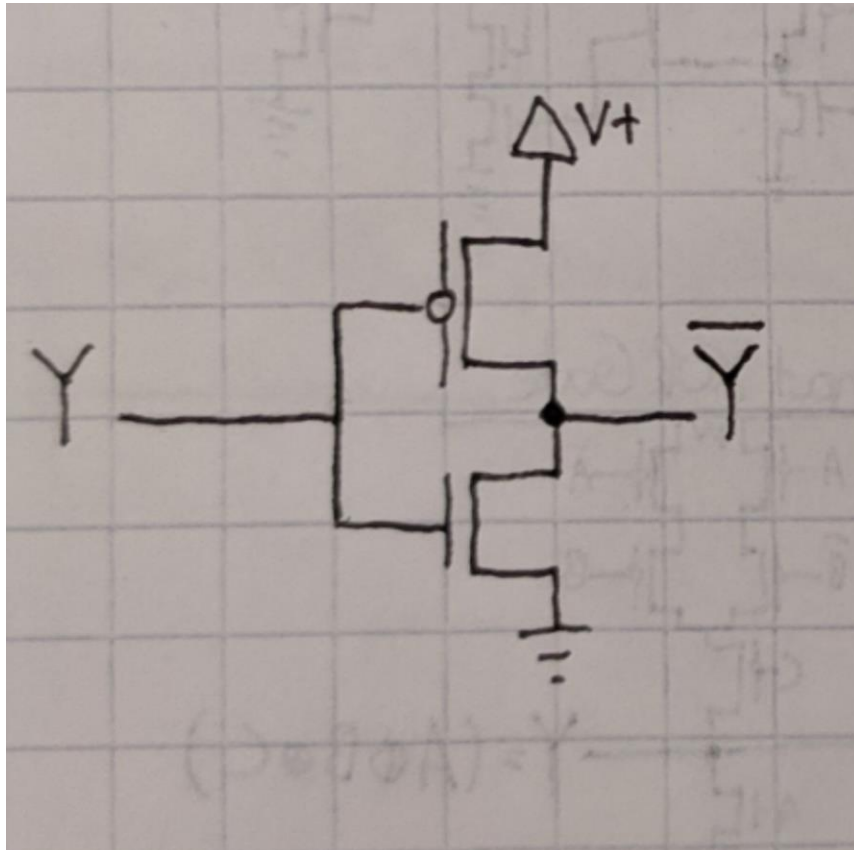
Image of layout -

Bounding box area -

7 * 6.5 = 45.5

Waveform results -

Question 2 (10 pts): 2-input NAND

Include the following

       a) Transistor level diagram

       b) Image of your layout

       c) Bounding box area (width x height)

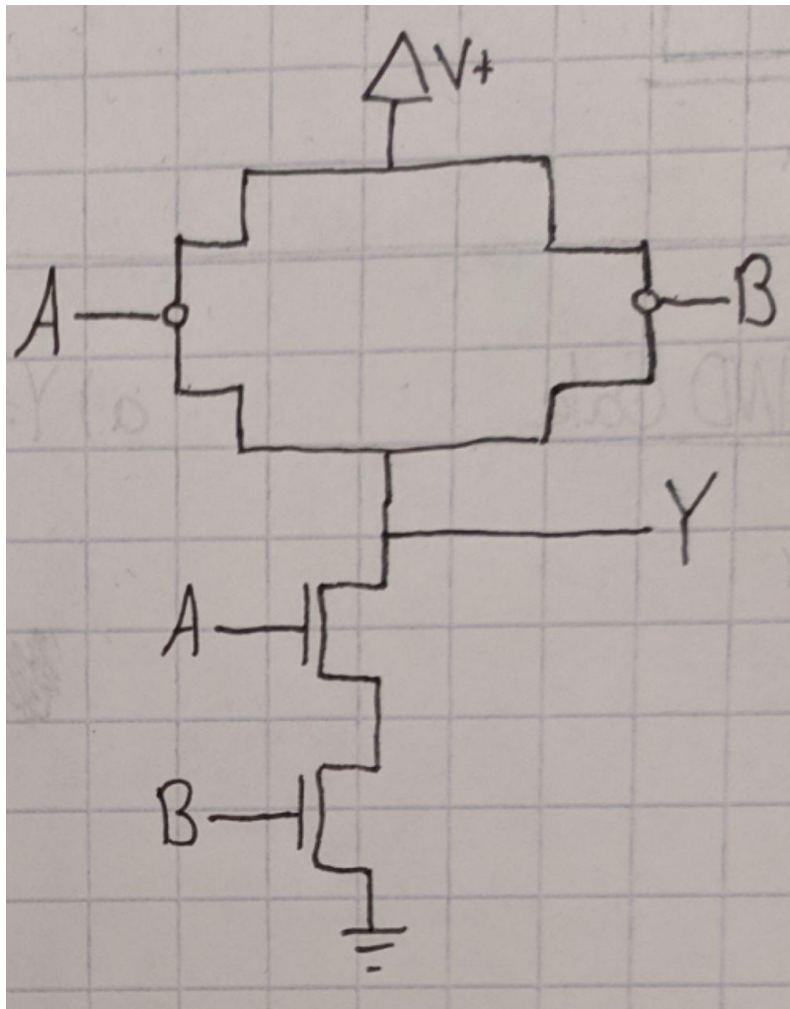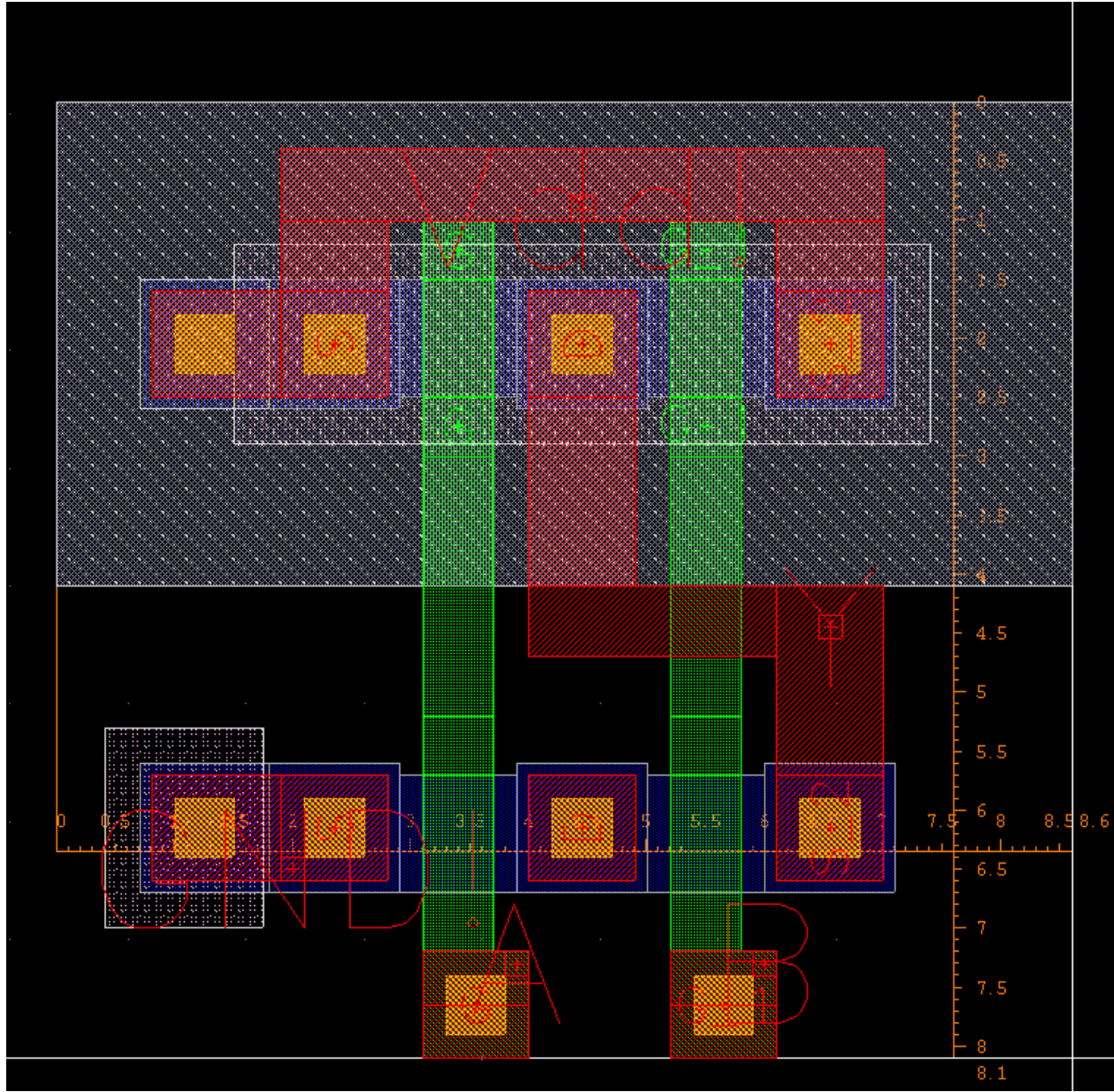   d) Waveform results

Transistor level diagram -

Image of layout -

Bounding box area -

8.1 * 8.6 = 69.66

6

Waveform results -

Question 3 (10 pts): 2-input NOR

Include the following

        a) Transistor level diagram

        b) Image of your layout

        c) Bounding box area (width x height)

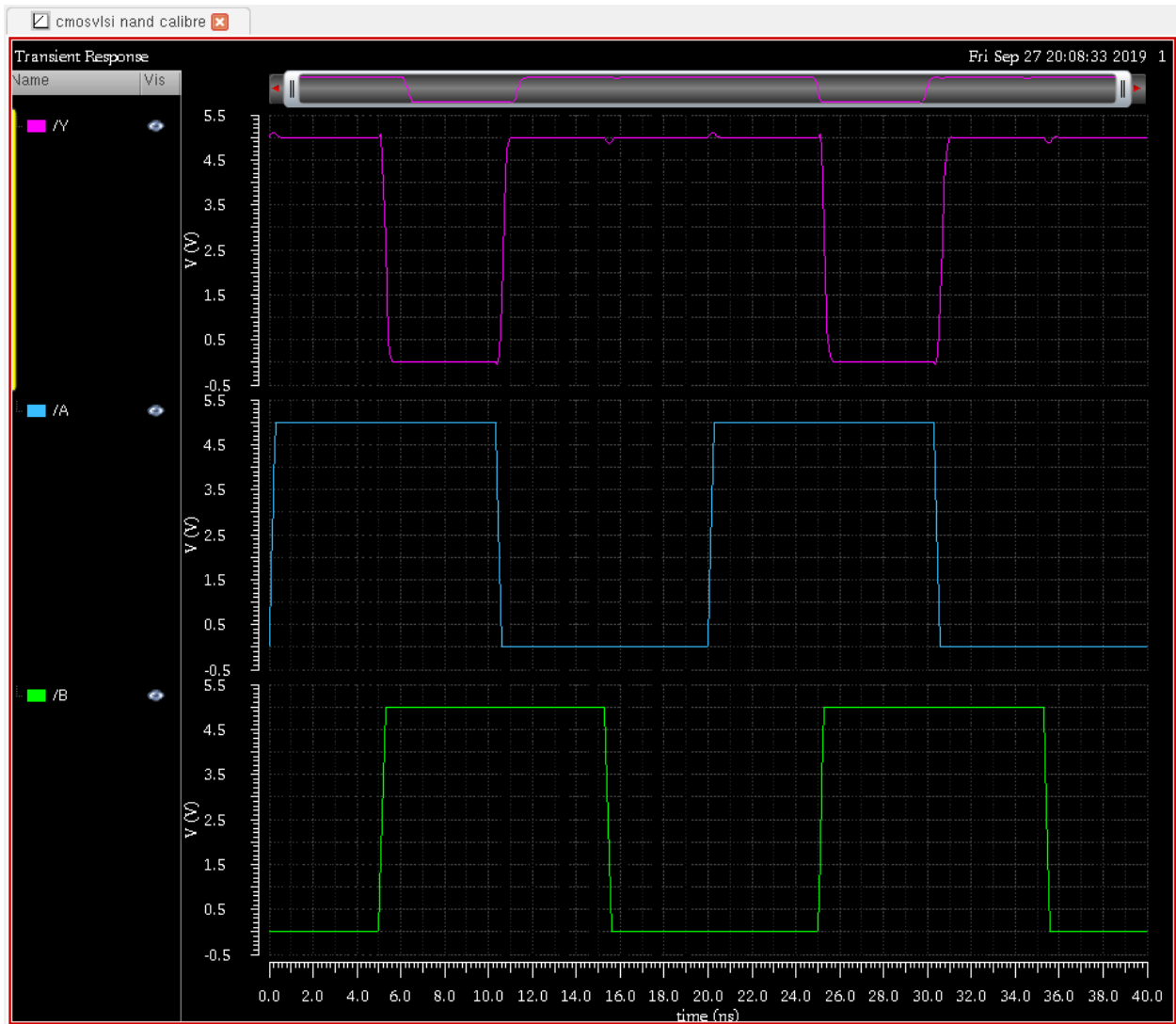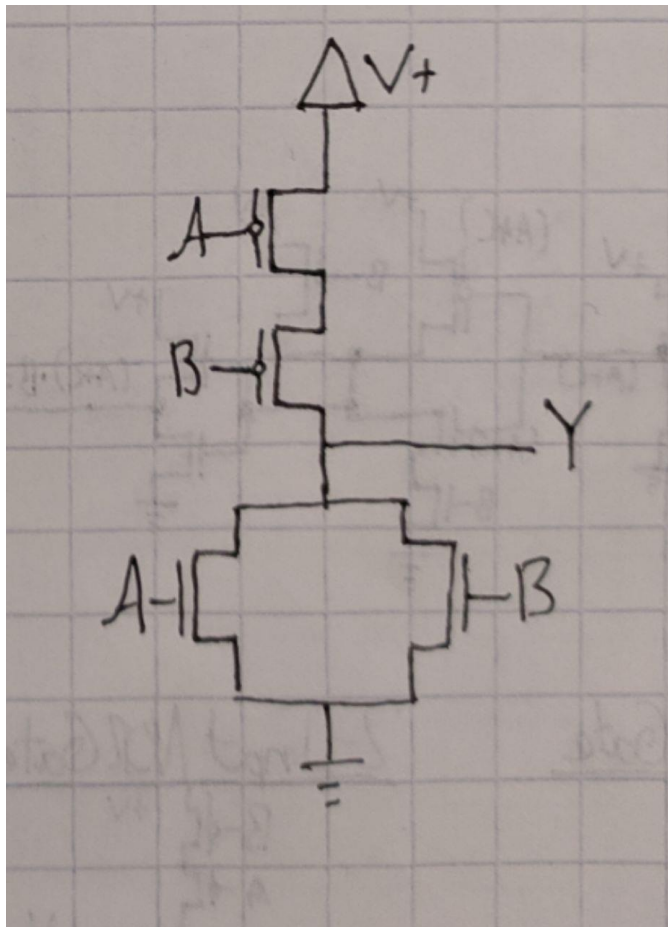   d) Waveform results

Transistor level diagram -

Image of layout -

Bounding box area -

8.1 * 8.6 = 69.23

Waveform results -