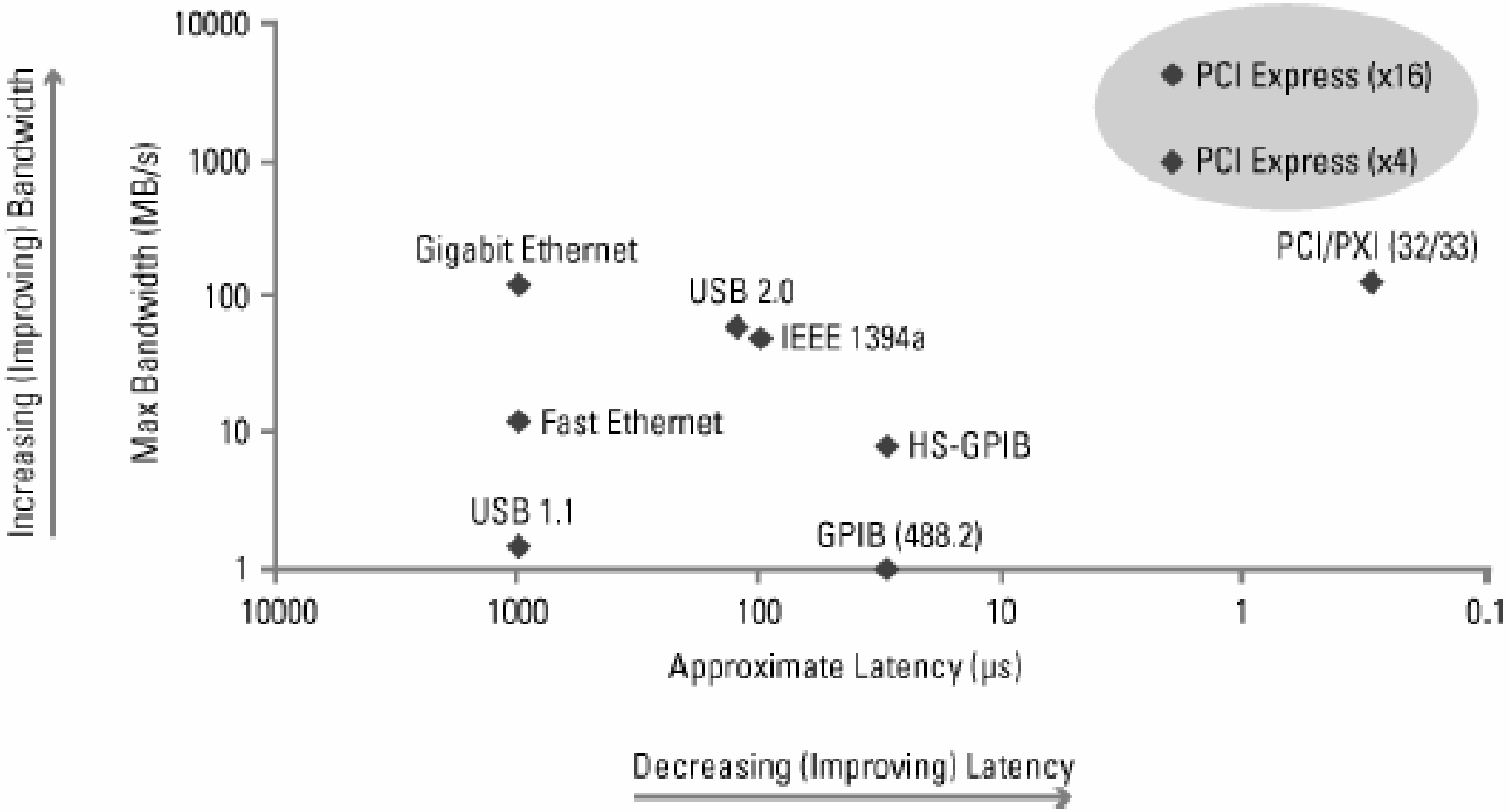
PCI Express

Advances in PC Bus Technology



PCI Express

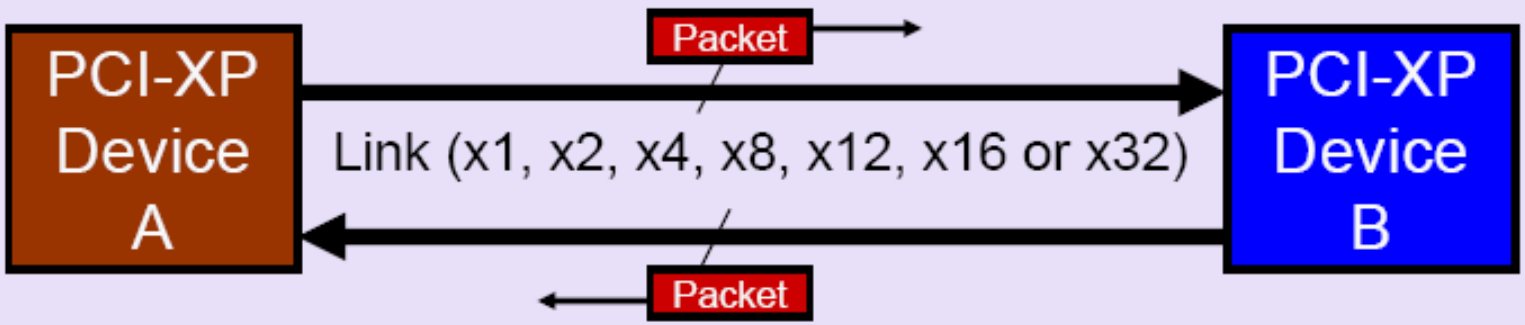
- Why do we care about PCI Express?

It's FAST

- Serial interconnect at **2.5Gb/s**
  - PCI transactions are packetized and then serialized
  - LVDS signaling, point-to-point, 8B/10B encoded
  - x1 (by 1) gives real-world performance of 200 MB/s/direction
  - x16 (by 16) gives real-world performance of 3.2 GB/s/direction
- Evolutionary version of PCI
  - Uses same software model

PCI Express Details

- Point-to-point connection
- Serial bus means fewer pins
- Scaleable: x1, x2, x4, x8, x12, x16, x32
- Gen 1 2.5Gbits/s transfer/direction/s
- Gen 1 Bandwidth: 0.5, 1, 2, 4, 6, 8, 16 GByte/s respectively
- Dual Simplex connection
- Packet based transaction protocol



PCI Express Details

- Switches used to interconnect multiple devices
- Packet based protocol
- Bandwidth and clocking
- Same memory, IO and configuration address space as PCI
  - ✓ Similar transaction types as PCI with additional message transaction
- PCI Express Transactions include:
  - ✓ memory read/write, memory read lock, IO read/write, configuration read/write, message requests
- Split transaction model for non-posted

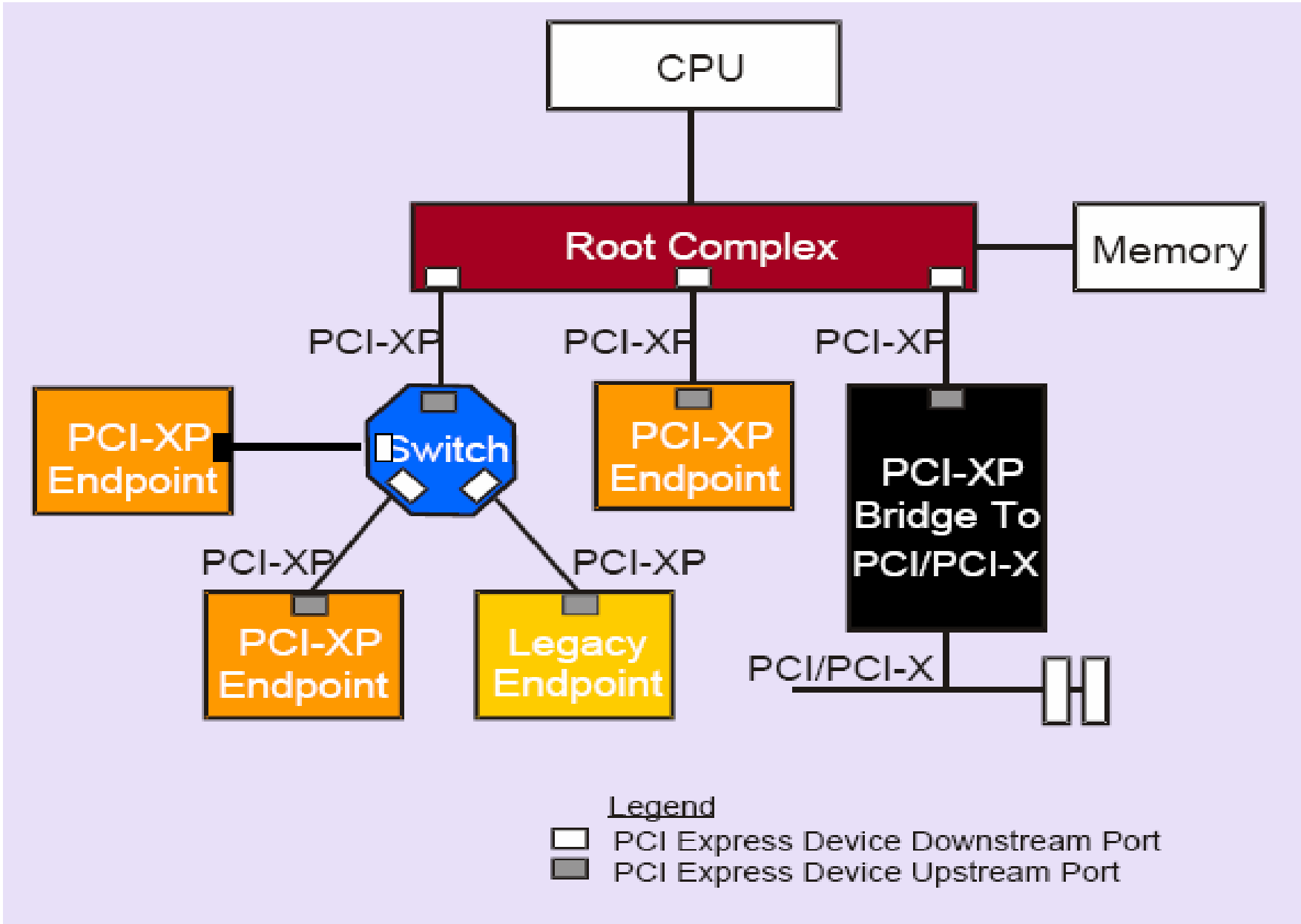
PCI Express Details

- Data Integrity and Error Handling
  - ✓ RAS capable (Reliable, Available, Serviceable)
  - ✓ Data integrity at: 1) Link level, 2) end-to-end
- Virtual channels (VCs) and traffic classes (TCs) to support differentiated traffic or Quality of Service (QoS)
  - ✓ The ability to define levels of performance for packets of different TCs
  - ✓ 8 TC's and 8 VC's available

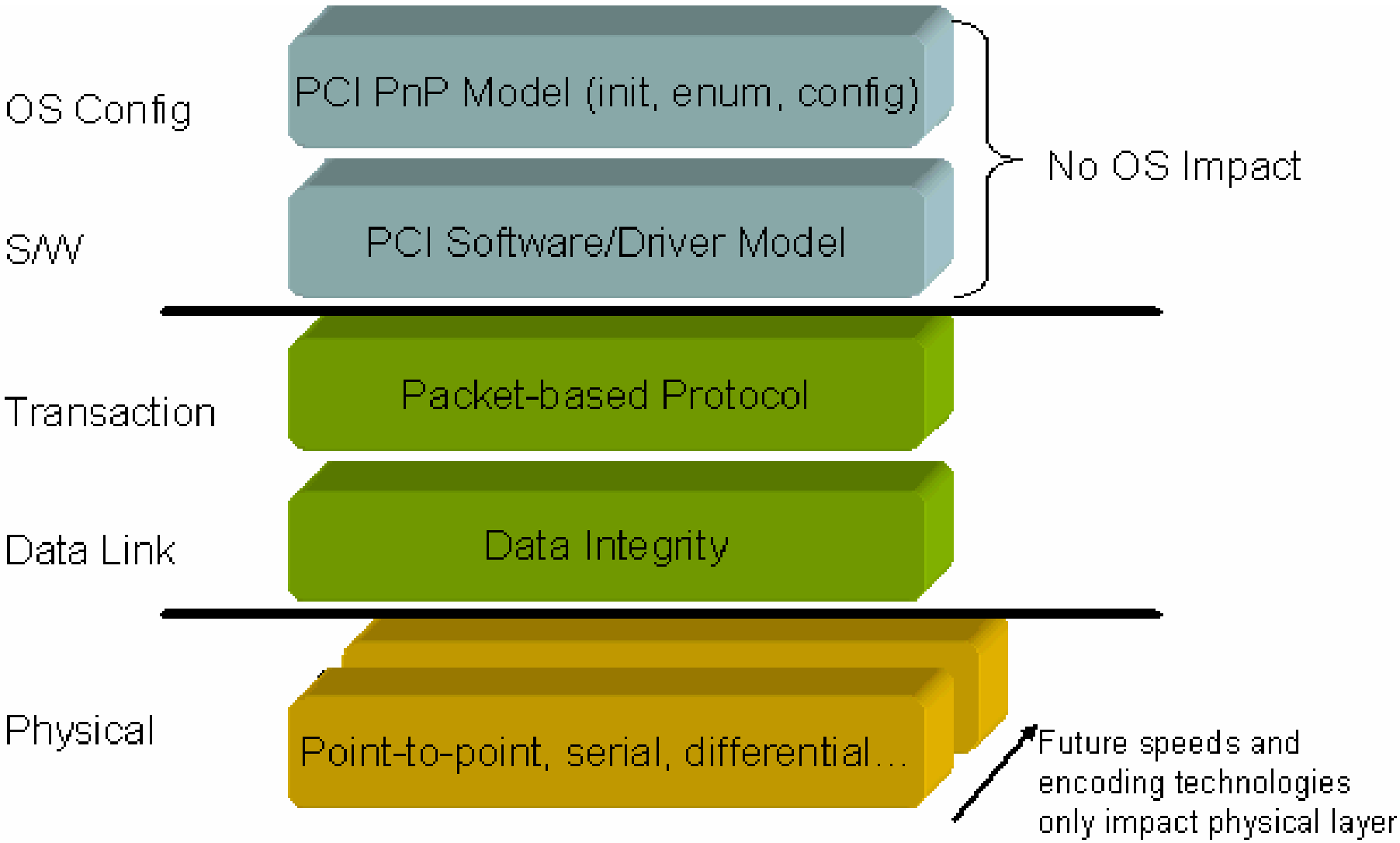
PCI Express Details

- Hot Plug and Hot Swap support
  - ✓ Native
  - ✓ No sideband signals
- PCI compatible software model
  - ✓ PCI configuration and enumeration software can be used to enumerate PCI Express hardware
  - ✓ PCI Express system will boot existing OS
  - ✓ PCI Express supports existing device drivers
  - ✓ New additional configuration address space requires OS and driver update

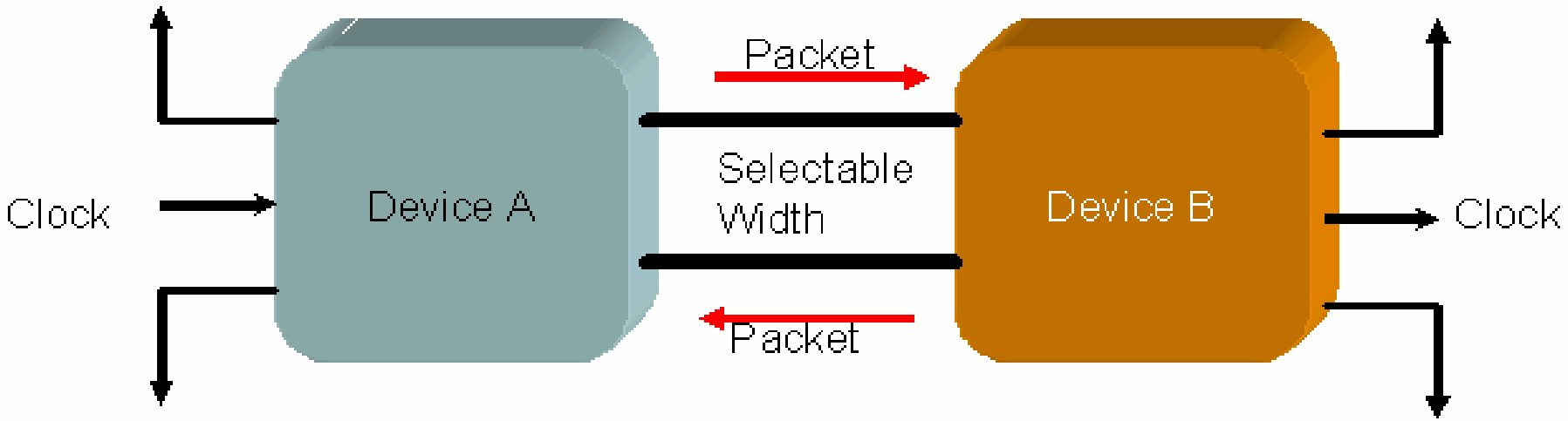
PCI Express Topology



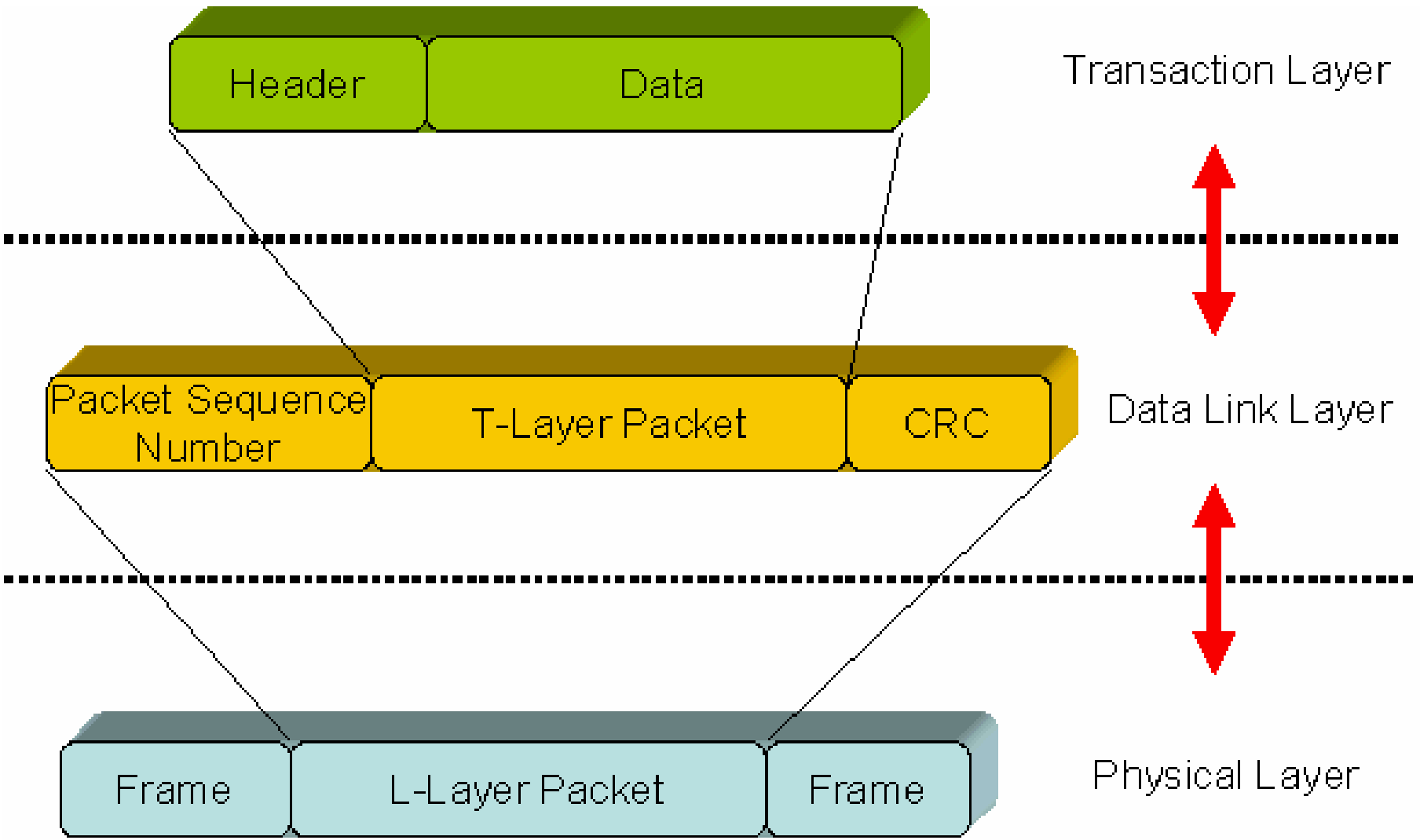
PCI Express Layers



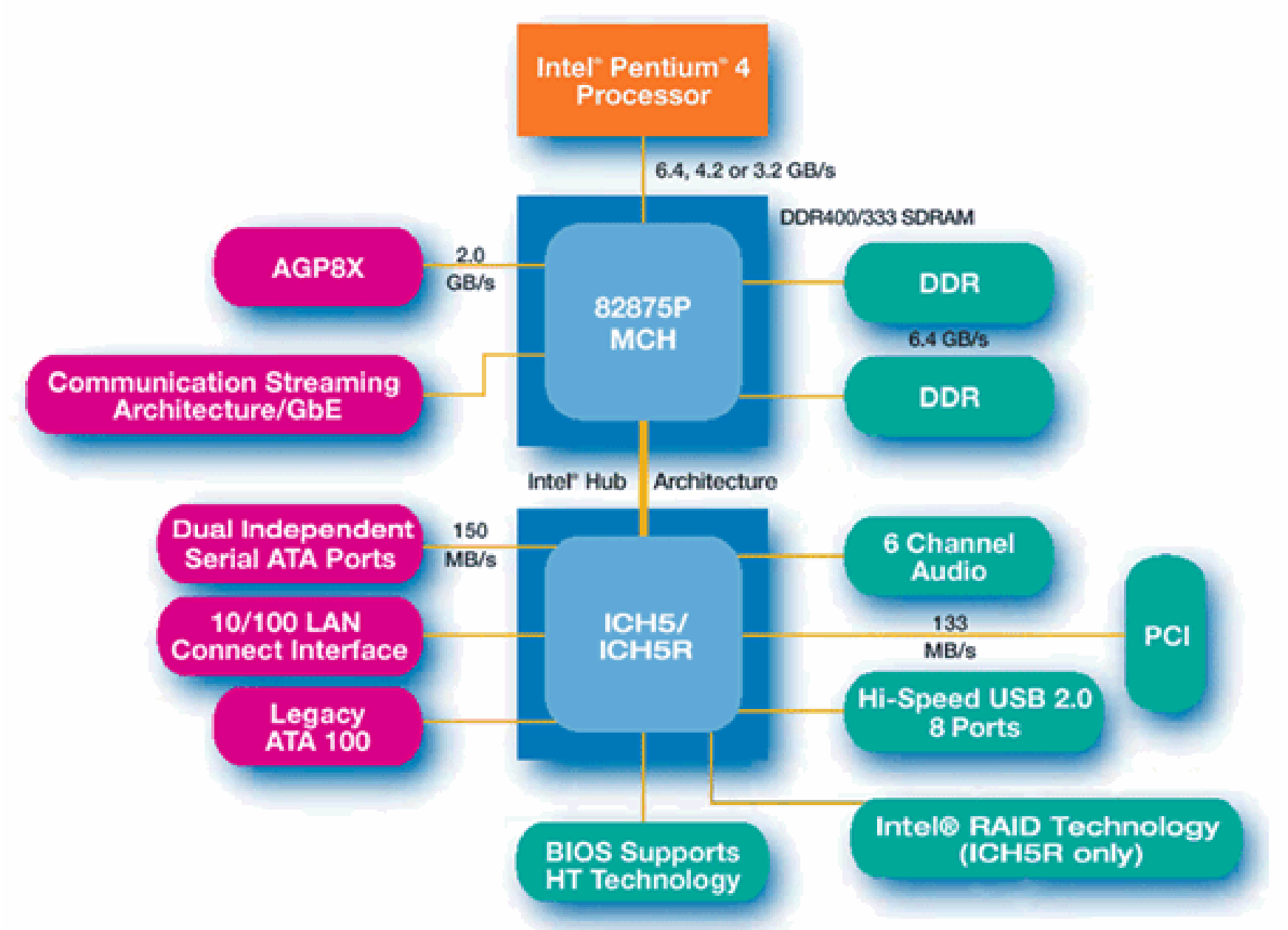
Physical Layer: 8b/10b Encoding



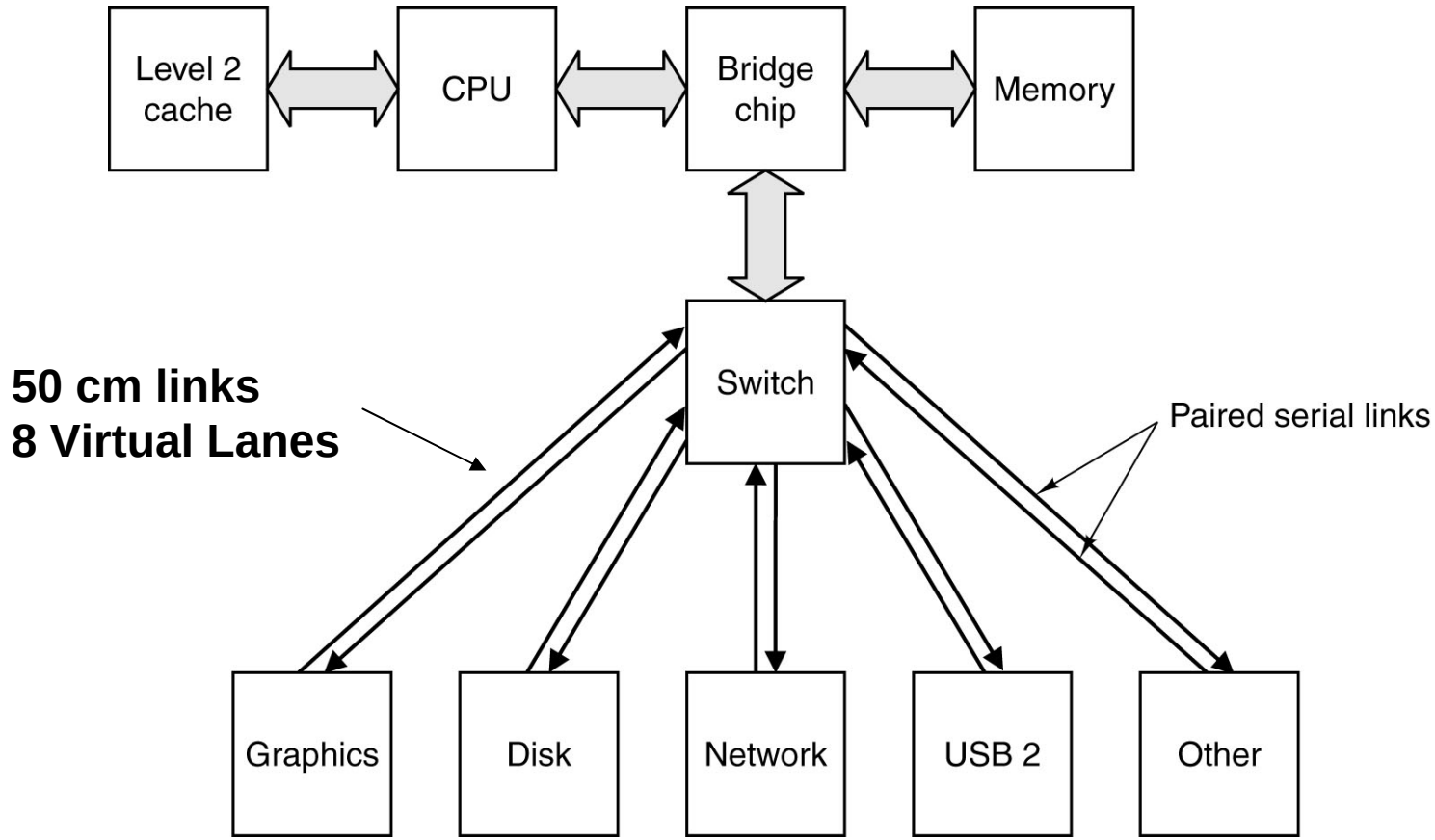
PCI Express Packet Layering



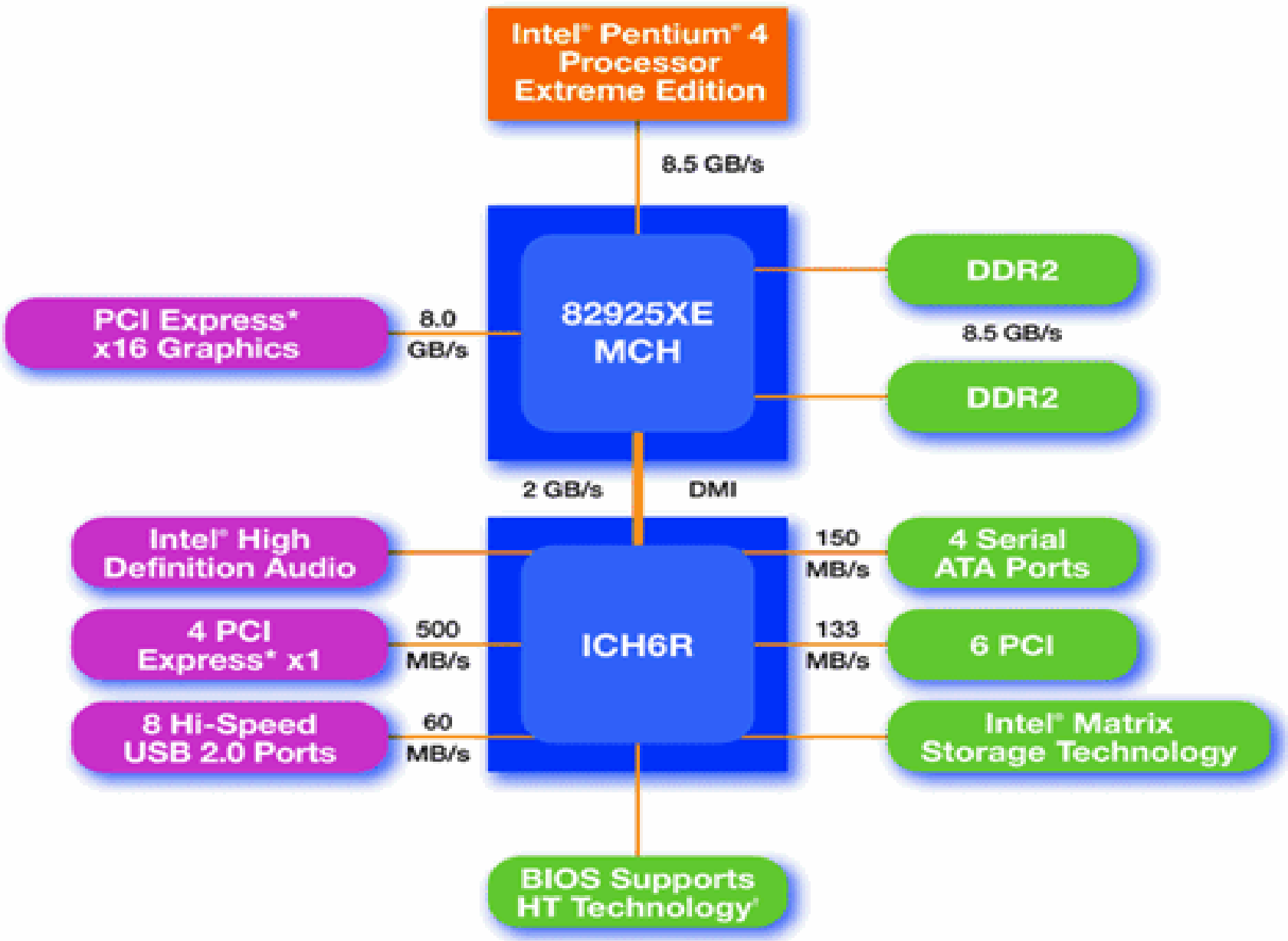
Conventional PC Type Architecture



PCI Express

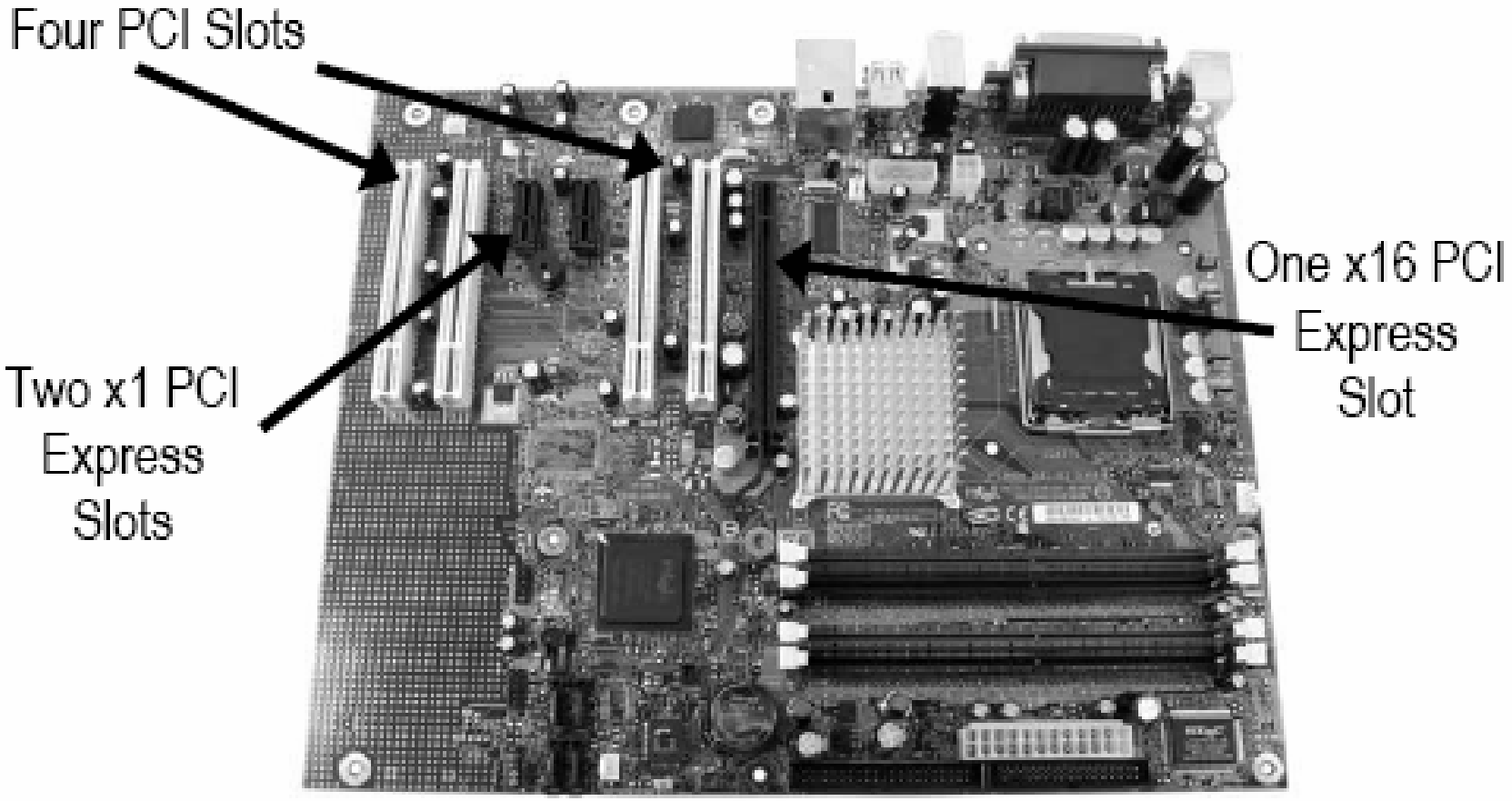

Level 2 cache
CPU
Bridge chip
Memory
Switch
50 cm links
8 Virtual Lanes
Paired serial links
Graphics
Disk
Network
USB 2
Other

PCI Express Type PC Architecture



PCI Express 8x and 16x Sockets

PCI and PCIe Slots on a Motherboard

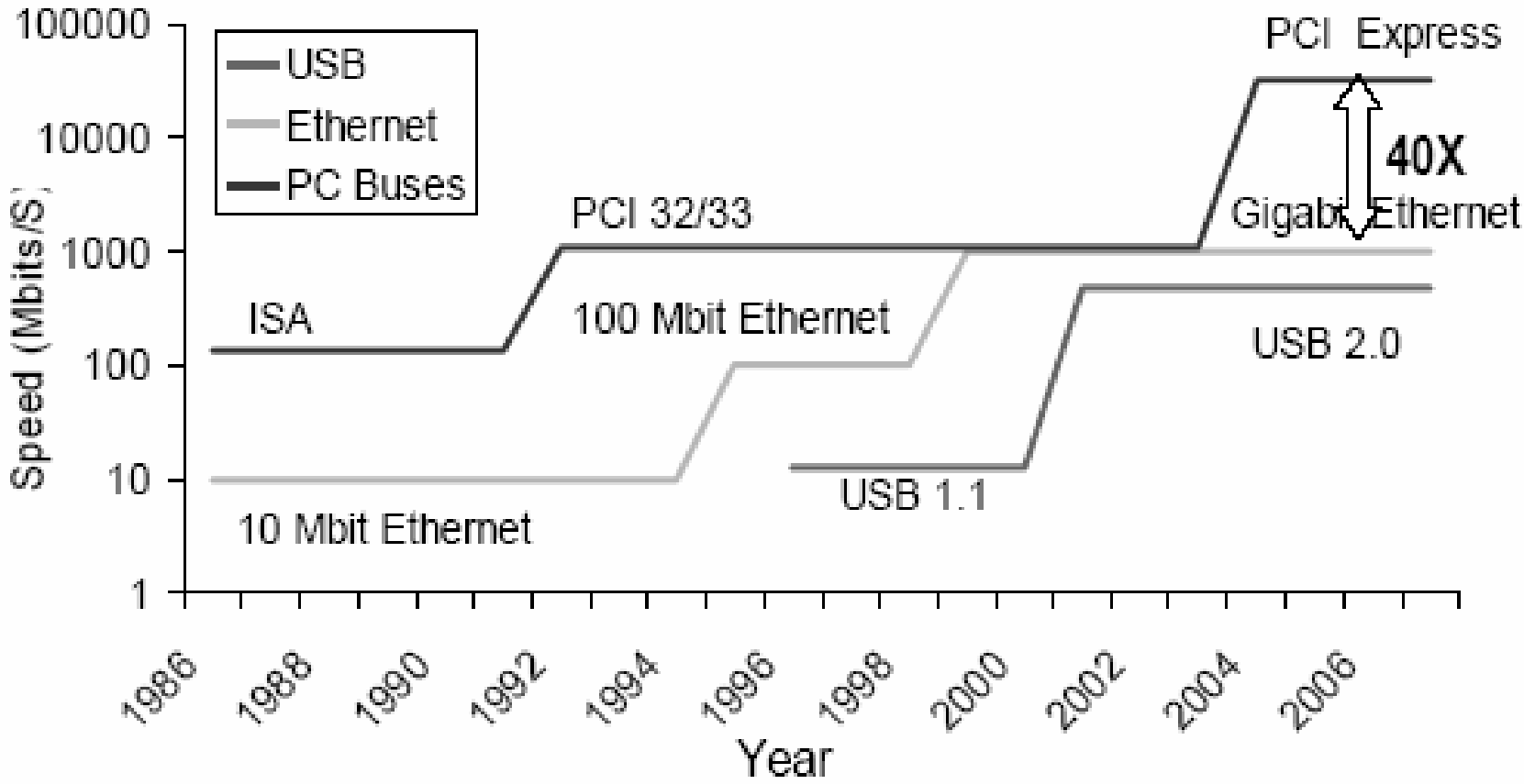


What is the PCI Express Bandwidth?

Bus	Bandwidth (MB/s)
PCI (32-bit, 33 MHz)	132 (shared)
x1 PCI Express	250 (per slot)
x4 PCI Express	1000 (per slot)
x16 PCI Express	4000 (per slot)

- Some report both directions versus single directions
- Example: x1 PCI Express
  - 500 MB/s (Both Directions)
  - 250 MB/s (Single Direction)
  - 200 MB/s (Single Direction, packet overhead correction)

Evolution of Industry Standard Buses



PCI Express Industry Adoption

- First PCI Express desktops shipped mid 2004
- First ExpressCard laptops shipped January 2005
- PCI and PCI Express are side-by-side in all Intel/Dell roadmaps
- Primary consumer drive is graphics processing (gamers, video editing)
  - PCIe x16 slot replacing AGP

Summary

- PCI and PCI Express will be offered side-by-side in Desktop PCs
- Mainstream acceptance of PCI indicates PCI availability for decades
  - ISA still available today, remains popular in industrial segments
  - PCI market size drove software compatibility for PCI Express
- PCI Express will enable new applications for Virtual Instrumentation
- Work to integrate PCI Express and PXI is underway
  - Specifications in 2005, products in 2006
  - Compatibility will preserve investment, while increasing system performance