University of Newcastle
School of Electrical Engineering and Computer Science

COMP2240 - Operating Systems
Workshop 1
Topics: Hardware Review & Operating System Overview

1. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields (Figure 1). The first byte contains the opcode and the remainder an immediate operand or an operand address.

a) What is the maximum directly addressable memory capacity (in bytes)?
b) Discuss the impact on the system speed if the microprocessor bus has
   I. 32-bit local address bus and a 16-bit local data bus, or
   II. 16-bit local address bus and a 16-bit local data bus.
c) How many bits are needed for the program counter and the instruction register?

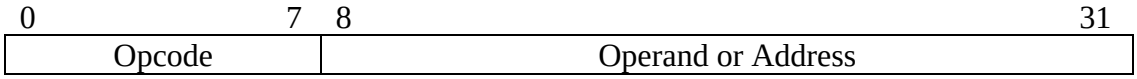

Figure 1: Instruction Format of the 32-bit Hypothetical Machine

2. A DMA module is transferring characters to main memory from an external device transmitting at 9600 bits per second (bps). The processor can fetch instructions at the rate of 1 million instructions per second.
By how much will the processor be slowed down due to the DMA activity? (You can ignore the data read/write operations and assume that the processor only fetches instructions.)

3. A computer has a cache, main memory, and a disk used for virtual memory.
If a referenced word is in the cache, 20 ns are required to access it. If it is in main memory but not in the cache, 60 ns are needed to load it into the cache (this includes the time to originally check the cache), and then the reference is started again.
If the word is not in main memory, 12 ms are required to fetch the word from disk, followed by 60 ns to copy it to the cache, and then the reference is started again. The cache hit ratio is 0.9 and the main-memory hit ratio is 0.6.

What is the average time in ns required to access a referenced word on this system?

4. How are iOS and Android similar? How are they different?

5. In a batch operating system, three jobs J1,J2, and J3 are submitted for execution. Each job involves and I/O activity, a CPU time, and another I/O activity.
Job J1 requires a total of 20 ms, with 2 ms CPU time.
J2 requires 30 ms total time with 6 ms CPU time.
J3 requires 15 ms total time with 3 ms CPU time.
What will be the CPU utilization for **uniprogramming** and **multiprogramming**?

Supplementary problems:

S1. Direct memory access (DMA) is used for high-speed I/O devices in order to avoid increasing the CPU's execution load.

a) How does the CPU interface with the device to coordinate the transfer?
b) How does the CPU know when the memory operations are complete?
c) The CPU is allowed to execute other programs while the DMA controller is transferring data. Does this process interfere with the execution of the user programs? If so, describe what forms of interference are caused.

S2. Suppose a stack is to be used by the processor to manage procedure calls and returns. Can the program counter be eliminated by using the top of the stack as a program counter?

S3. Consider a hypothetical microprocessor generating a 16-bit address (e.g., assume that the program counter and the address registers are 16 bits wide) and having a 16-bit data bus.

a) What is the maximum memory address space that the processor can access directly if it is connected to a "16-bit memory"?
b) What is the maximum memory address space that the processor can access directly if it is connected to an "8-bit memory"?
c) What architectural features will allow this microprocessor to access a separate "I/O space"?
d) If an input and an output instruction can specify an 8-bit I/O port number, how many 8-bit I/O ports can the microprocessor support? How many 16-bit I/O ports?

Explain.

S4. Suppose that we have a multiprogrammed computer in which each job has identical characteristics. In one computation period, T, for a job, half the time is spent in I/O and the other half in processor activity. Each job runs for a total of N periods. Assume that a simple round-robin scheduling is used, and that I/O operations can overlap with processor operation. Define the following quantities:

- Turnaround time = actual time to complete a job
- Throughput = average number of jobs completed per time period T
- Processor utilization = percentage of time that the processor is active (not waiting)

Compute these quantities for one, two, and four simultaneous jobs, assuming that the period T is distributed in each of the following ways:

a) I/O first half, processor second half

I/O first and fourth quarters, processor second and third quarter