Computer Architecture Homework 4

Spring 2022, April

1 Boolean Algebra and Logic Gates

Question 1.1

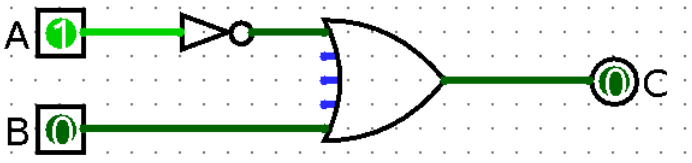
For the following function:
bool fun(bool A, bool B) return (A == B) ? true : B;
a. Write the Truth Table of it.(5 pts)
b. Write the Boolean Expression of it and simplify it (as simple as possible).(10 pts)
c. Draw the gate diagram that implements the boolean expression in b.(5 pts)

a. Take C as the return value of boolean function.

Input		Output
A	B	C
0	0	1
0	1	1
1	0	0
1	1	1

b. $C = \overline{A\bar{B}} = \bar{A}+B$

c.



Question 1.2

a. Simplify the following Boolean Expressions (as simple as possible and show enough steps please).(15 pts)

$B(AB + A\overline{B})(\overline{AC} + C) + \overline{CC} + (A + \overline{B})(\overline{CD})$

$= AB(\overline{A}+\overline{C}+C) + \overline{C} + A\overline{CD} + \overline{B}\overline{CD}$

$= AB + \overline{C} + A\overline{C} + A\overline{D} + \overline{B}\overline{C} + \overline{B}\overline{D}$

$= AB + \overline{C} + A\overline{D} + \overline{B}\overline{C} + \overline{B}\overline{D}$

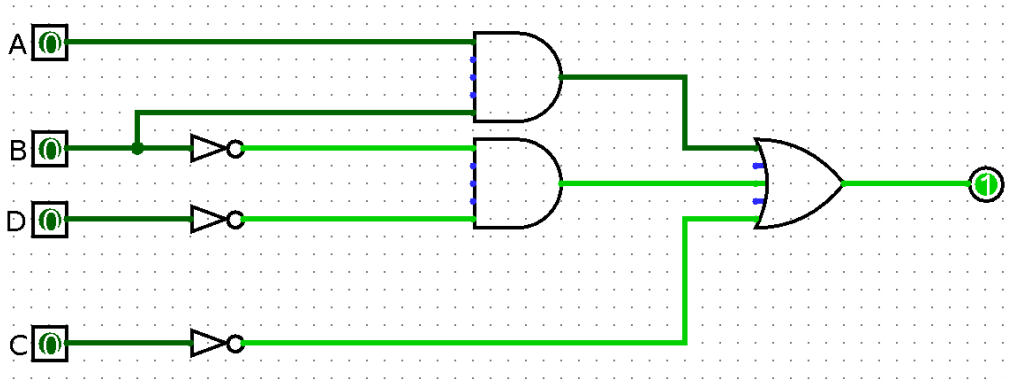
$= AB + \overline{C} + A\overline{D} + \overline{B}\overline{D}$

$= \overline{C} + AB + A(B+\overline{B})\overline{D} + \overline{B}\overline{D}$

$= \overline{C} + AB + AB\overline{D} + A\overline{B}\overline{D} + \overline{B}\overline{D}$

$= \overline{C} + AB + \overline{B}\overline{D}$

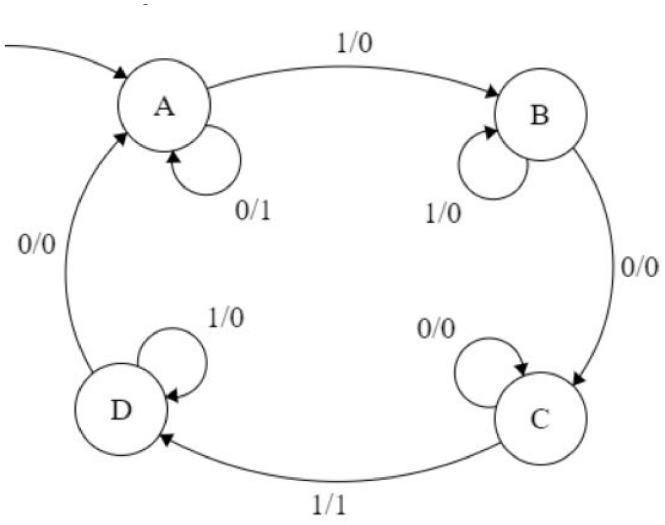
b. Draw the circuit according to the simplified boolean expression in (a) . (10 pts)



2 FSM

Question 2

For the following Finite State Machine, fill out the remainder of the table. (15 pts)



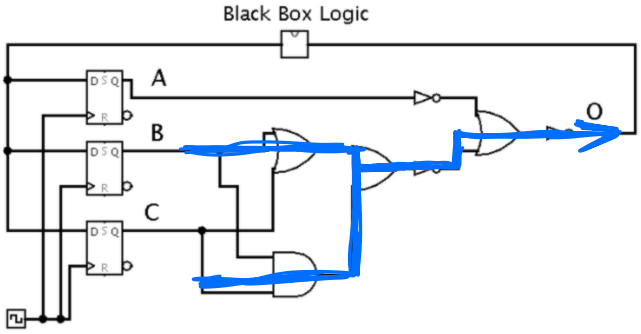
Input	-	1	0	0	1	1	0	0	0
Next State	A	B	C	C	D	D	A	A	A
Output	-	0	0	0	1	0	0	1	1

Table 1: Write Answer Here

3 SDS

Question 3

In the following circuit, NOT gates have a delay of 3ns, AND and OR gates have a delay of 7ns, and the "Black Box" logic component has a delay of 9ns. The registers have a clk-to-q delay of 6ns and setup times of 5ns.



a. What is the maximum allowable hold time of the registers? (please include enough explanation) (20 pts)

Maximum hold time

= Minimum CL delay + clk-to-q delay

= (3ns + 7ns + 3ns) + 9ns + 6ns = 28ns

b. What is the minimum acceptable clock period for this circuit? (please include enough explanation) (20 pts)

Minimum clock period

= clk-to-q delay + setup time + longest CL delay

= 6ns + 5ns + Longest Gate delay (marked by blue line) + Black Box delay

= 11ns + (7ns + 7ns + 3ns + 7ns + 3ns) + 9ns

= 47ns