S3R STABILITY MARGINS AND DESIGN GUIDELINES

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ABSTRACT

Since its introduction in the seventies, the S3R (Sequential Switching Shunt Regulator) concept for regulated bus has been successfully applied on many spacecraft. While a number of publications have been dedicated to its implementation, a detailed dynamic analysis is however still missing. The present paper is dedicated to this issue. It is shown that the sizing of the S3R commutation thresholds as originally proposed carefully balances the electrical and thermal performances. The dynamic analysis also encompasses the possible resonance between the SA parasitic capacitance and the harness inductance, and highlights the sizing provision to be made to make it fully sustainable. Accordingly, exhaustive guidelines for S3R design are provided.

1. INTRODUCTION

The S3R was introduced by ESA in the seventies as a technique to regulate spacecraft power bus by means of convenient SA (Solar Array) interface. The simplicity of the concept has motivated its selection in many missions and aroused a number of publications.

According to [4] and [9], the S3R is based on the division of the SA in a number of sections being sequentially connected to the bus or shunted to ensure bus voltage regulation. The connection and shunt operation of any one section may be operated up to a maximum ripple frequency so as to match the mean value of the payload power demand. A convenient impedance at the regulated point is ensured by a bus capacitance.

The control loop feedback includes a proportional gain and an integrator, the effect of which on the discrete commutation of the sections is studied in [7]. In [6] and [8], the effect of the parameters on the S3R operation is investigated by way of simulations. [1] concentrates on possible provisions to cope with the SA parasitic capacitance discharge when a section is shorted. Finally, [5] proposes variant circuitries for the implementation of a S3R and discusses its application for battery busses.

Although these papers give a deeper insight into the S3R ins and outs, a detailed study of the S3R dynamics has strikingly never been provided. This is likely to be explained by the discrete feature of the SA current under sequential section control and by the non symmetric time delays of the associated switching operation, making linear control theory not readily applicable. On the other hand, the impact on the S3R of the possible resonance between the SA section parasitic capacitance and the inductance of its harness has neither been analysed, leaving designers puzzled as to which extent they should worry about that.

The present paper is dedicated to these open issues. A dynamic analysis is performed based on a block diagram model of the S3R. Because of its nonlinearities, the stability margins are not investigated in terms of gain and phase, which issues make sense only for linear systems, but directly in terms of electrical performances, as well as in terms of thermal dissipation.

The study shows that the commutation thresholds design as originally proposed constitutes a careful balance between the S3R electrical and thermal features. The dynamic analysis also deals with the resonance between the SA section and its harness, and highlights the sizing provision to be made to make it fully sustainable. The paper finally provides exhaustive guidelines for S3R design.

2. S3R BLOCK DIAGRAM

A synthetic view of the S3R operation principles is given on Fig. 1.

For the sake of the regulation, the bus voltage is measured through a resistor divider and compared to a voltage reference. The voltage difference, or regulation error, is amplified according to proportional and integral gains of the MEA (Main Error Amplifier) which delivers a control voltage. That voltage operates the sequential commutation of the SA sections, thereby providing a stepwise current to the power bus. The load current is subtracted from that current and the difference is absorbed by the bus capacitance on which the bus voltage develops.

Proc. of the '8th European Space Power Conference', Constance, Germany, 14–19 September 2008 (ESA SP-661, September 2008)

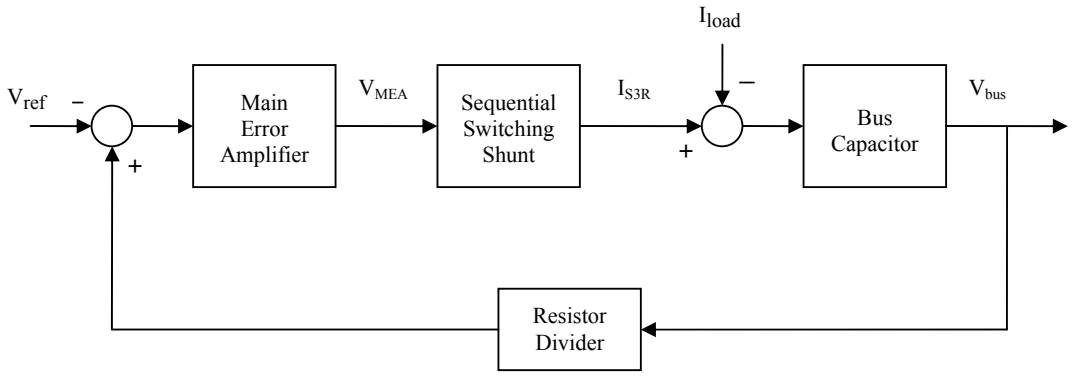

Fig. 1 : S3R principle block diagram

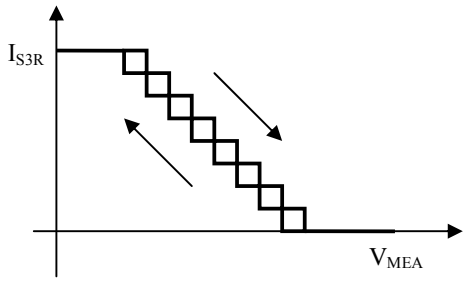

Fig. 2 : S3R stepwise current profile

The S3R stepwise current profile with respect to the MEA voltage is illustrated on Fig. 2, featuring some hysteresis. This hysteresis is drawn with an amplitude equal to the distance between thresholds of successive SA sections ; it may however be larger or smaller. Each section commutation is affected by a time delay. The delay at shunt operation (i.e. at MOSFET switch ON) is mainly due to the electronics ; the delay at bus connection (i.e. at MOSFET switch OFF) is driven by the SA parasitic capacitance charge, hence is larger than the turn ON delay.

Now, assume that the section current is divided by two. This means that the section number is doubled and that the distance between thresholds of successive SA sections is divided by two. And let divide by two the hysteresis as well. In so doing, we have a S3R current profile with respect to the MEA voltage which is unchanged from a large signal point of view. Another feature that is unchanged is the commutation delays. Indeed, the electronics switch ON delay does not depend on the section current, and the switch OFF delay depends on the ratio of the SA section capacitance by its current, i.e. does neither depend on the section current (as the capacitance is proportional to the section current). If we further let the section current tend to zero by successive division and the section number tend to infinity, we then come up with a S3R model that leaves aside the discrete feature of the S3R while keeping the remaining dynamic properties.

The S3R current response of such a model to a sine MEA voltage is shown on Fig. 3. It is illustrated that the S3R current is proportional to the minimum value taken on all MEA voltages delayed by any time lapse in between the turn ON delay and the turn OFF delay.

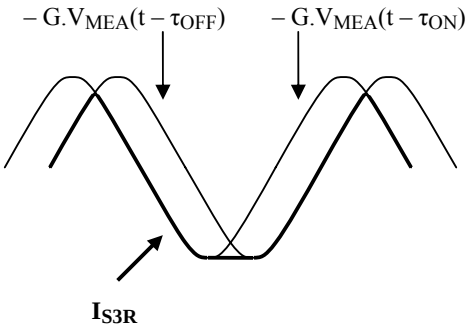

Fig. 3 : V_{MEA} to continuous I_{S3R} time response

The block diagram associated to this model is called S3R equivalent current continuous block diagram. It is displayed on Fig. 4. The factor K stands for the bus voltage resistor divider, A is the MEA gain and G the MEA voltage to S3R current transconductance. The S3R section turn ON and turn OFF delays (associated respectively to the shunt MOSFET switch ON and switch OFF operation) are represented by τ_{ON} and τ_{OFF} while C_{bus} stands for the bus capacitance.

This closed loop shall provide convenient dynamic performances, which will now be studied.

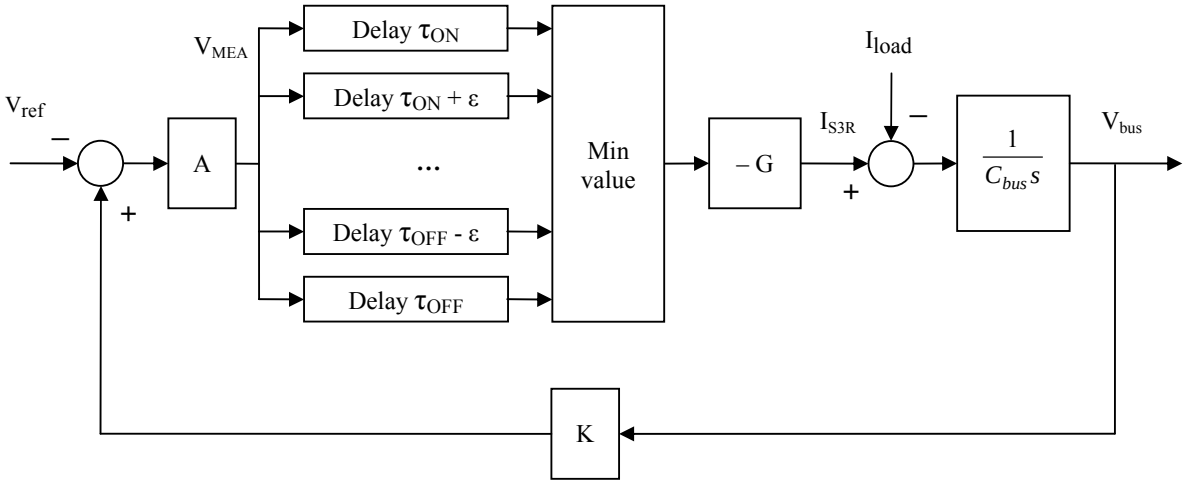

Fig. 4 : S3R equivalent current continuous block diagram

3. CURRENT OVERSHOOT

A load current step results in a current response of the S3R which depends on its switching delays. A rising S3R current profile is driven by its turn OFF delay, while a falling one is driven by its turn ON delay. Accordingly, the amplitude of the S3R current response overshoot (if any) is only driven by the turn OFF delay for positive load current steps or only driven by the turn ON delay for negative load current step.

For this reason, we now concentrate on a S3R model according to Fig. 4 where no difference is made between the turn ON and turn OFF delays. Coming up with a linear system, the size of the current response overshoot (if any) to the load current step may be analysed as a function of this symmetric switching delay.

For the sake of this study, it is assumed that the MEA gain contains no integrator. This means that A is scalar (as K and G). The purpose of this provision is to make the analysis simple. It is motivated by the fact that the MEA integral gain is dominated by the proportional gain down to a low frequency and has no significant impact on the S3R current step response amplitude.

Furthermore, let approximate the delay transfer function by its first order component as follows :

$$e^{-s\tau} = \frac{1}{e^{s\tau}} = \frac{1}{1+s\tau}$$

The associated block diagram is displayed on Fig. 5.

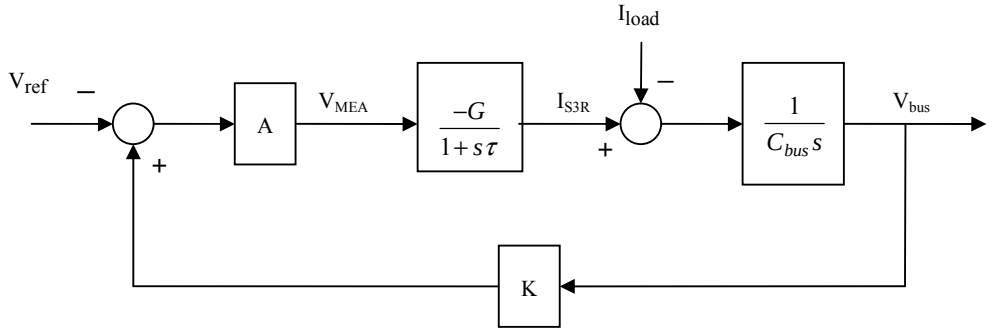

Fig. 5 : S3R equivalent linear block diagram

The load current to S3R current transfer function is then given by :

$$\frac{I_{S3R}}{I_{load}} = \frac{KAG}{\tau C_{bus} s^2 + C_{bus} s + KAG}$$

The step response associated to this transfer function will display no overshoot on the condition that its poles are not complex conjugate [3, § 5.3.2, p. 183] :

$$C_{bus}^2 - 4KAG\tau C_{bus} \geq 0$$

The zero overshoot condition becomes :

$$KAG \leq \frac{C_{bus}}{4\tau} \quad (3.1)$$

In the S3R original paper [4, p. 131], the sizing of the voltage difference between the positive (or negative) thresholds of two successive SA sections is proposed as follows :

$$\Delta V_{th} = \frac{I_{SA}}{C_{bus}} KA\tau_{OFF} \quad (3.2)$$

Reminding that the S3R transconductance is given by :

$$G = \frac{I_{SA}}{\Delta V_{th}}$$

the S3R sizing condition becomes :

$$KAG = \frac{C_{bus}}{\tau_{OFF}} \quad (3.3)$$

Hence, with reference to condition (3.1), the current step response of a S3R in accordance with (3.2) will display some overshoot. The size of this overshoot is 50 % of the step current, as this will be illustrated later by simulation. At the same time, knowing that the turn ON delay is typically an order of magnitude smaller than the turn OFF delay, we may also state that the S3R current response to a negative load current step will display no overshoot.

Note that any current overshoot is associated to a voltage overshoot, as voltage and current transients are proportional to each other according to Fig. 5 (disregarding the time delay transfer function).

Remark also that when both terms of the zero overshoot condition (3.1) are identical to each other, the open loop gain of Fig. 5 is unity under the following phase condition :

$$\left|\frac{KAG}{(1+s)C_{bus}s}\right| = 1 \iff s\tau = j\sqrt{\frac{-1+\frac{\sqrt{5}}{2}}{2}} = j\sin 14°$$

This means that the closed loop step response features no current overshoot on the condition that the phase margin be (at least) 76°. In other words, the 60° phase margin is not a sufficient condition for a linear voltage loop not to display an overshoot.

4. OUTPUT IMPEDANCE

Coming back to Fig. 4 and assuming again that the gain A is scalar, a load current step applied on a power bus under S3R control generates a voltage in accordance with :

$$\Delta V_{bus} KAG = \Delta I_{load}$$

In absence of any overshoot, the bus impedance may then be given by :

$$Z_{S3R} = \frac{\Delta V_{bus}}{\Delta I_{load}} = \frac{1}{KAG} \quad (4.1)$$

With reference to equation (3.3), one obtains :

$$Z_{S3R} = \frac{\tau_{OFF}}{C_{bus}}$$

Now, because of the associated overshoot, the bus impedance under positive load current step will be higher than the one under negative load current transient. Hence, with reference to the 50 % overshoot previously discussed for positive load current step, the bus impedance are given by :

$$\begin{aligned} Z_{S3R}^{-} &= \frac{\tau_{OFF}}{C_{bus}} \\ Z_{S3R}^{+} &= 1{,}5\frac{\tau_{OFF}}{C_{bus}} \end{aligned} \quad (4.2)$$

where Z_{S3R}^{-} and Z_{S3R}^{+} are the bus impedance under respectively negative and positive load current steps.

5. DYNAMICS OVERVIEW

The overshoot and impedance features of a S3R loop are now synthesized in Tab. 6 as a function of the KAG gain.

KAG	Section Rippling	$\Delta I_{bus} = +50\% \frac{P_{bus}}{V_{bus}}$ (positive load current step)				$\Delta I_{bus} = -50\% \frac{P_{bus}}{V_{bus}}$ (negative load current step)				Remark
		S3R Current Transient Amplitude	S3R Current Overshoot Amplitude	Bus Voltage Transient Amplitude	Z_{S3R}^{+}	S3R Current Transient Amplitude	S3R Current Overshoot Amplitude	Bus Voltage Transient Amplitude	Z_{S3R}^{-}	
$\rightarrow +\infty$	All	-	-	-	-	-	-	-	-	Instability
:	Multiple	:	:	:	:	:	:	:	:	Higher Dissipation
$\frac{C_{bus}}{\tau_{OFF}}$	Single	$1{,}5\Delta I_{bus}$	50 %	$1{,}5\frac{\tau_{OFF}}{C_{bus}}\Delta I_{bus}$	$1{,}5\frac{\tau_{OFF}}{C_{bus}}$	ΔI_{bus}	0 %	$\frac{\tau_{OFF}}{C_{bus}}\Delta I_{bus}$	$\frac{\tau_{OFF}}{C_{bus}}$	According to [4]
:	Single	$> \Delta I_{bus}$	> 0 %	$> \frac{1}{KAG}\Delta I_{bus}$	$> \frac{1}{KAG}$	ΔI_{bus}	0 %	$\frac{1}{KAG}\Delta I_{bus}$	$\frac{1}{KAG}$	Overshoot
$\frac{C_{bus}}{4\tau_{OFF}}$	Single	ΔI_{bus}	0 %	$4\frac{\tau_{OFF}}{C_{bus}}\Delta I_{bus}$	$4\frac{\tau_{OFF}}{C_{bus}}$	ΔI_{bus}	0 %	$4\frac{\tau_{OFF}}{C_{bus}}\Delta I_{bus}$	$4\frac{\tau_{OFF}}{C_{bus}}$	Zero Overshoot
:	Single	ΔI_{bus}	0 %	$\frac{1}{KAG}\Delta I_{bus}$	$\frac{1}{KAG}$	ΔI_{bus}	0 %	$\frac{1}{KAG}\Delta I_{bus}$	$\frac{1}{KAG}$	Zero Overshoot
$\rightarrow 0$	Single	ΔI_{bus}	0 %	↗↗	↗↗	ΔI_{bus}	0 %	↗↗	↗↗	Zero Overshoot

Tab. 6 : S3R dynamics overview

The original sizing condition (3.2) constitutes the reference case of the table and is identified by the thick lined rectangle.

Note that this sizing condition has been set up to prevent any steady-state double section rippling under any DC load condition. For KAG gain sized above this condition, steady-state double (or multiple) section rippling may occur associated to higher rippling frequency (not featured). This means in turn higher power dissipation because of the SA section parasitic capacitance discharges.

As a second remark, the S3R current overshoot under positive load current step may prove to be critical as well. This means indeed that the S3R current response to a TDMA (Time Domain Modulation Amplitude) load will call on a number of sections which is up to 50 % larger than the number of section corresponding to the peak to peak amplitude of the TDMA load. This must be taken into account for the thermal dissipation budget evaluation.

Thirdly, any increase of the KAG gain above the reference case with the purpose of improving the bus impedance will partially be compensated by an increase of the overshoot applicable under positive load current step.

Hence, for all these three reasons, the sizing of the S3R KAG gain as originally proposed constitutes a maximum value that has to be met under all operating conditions.

On the other hand, note that a decrease of the KAG gain below the reference case will increase the bus impedance and deteriorate its electrical performances. Such a gain decrease is not desirable ; it might however be needed as a result of TDMA operation to reduce the current overshoot i.e. the power dissipation level.

Finally, Tab. 6 suggests how to investigate the dynamic performance of a S3R closed loop by looking to its time behaviour rather than by resorting to the usual frequency sweep.

It is indeed difficult to plot a Bode diagram of a S3R for two main reasons. First, the large voltage modulation that should be used to overcome the section rippling amplitude would imply a large power modulation which would make the measurement uneasy to do. Secondly, the free running frequency feature of the rippling section generates a signal that would perturb the measurement of the spectrometer.

Hence, it is relevant to measure the time response of the S3R current to a square load current with a peak to peak amplitude of several sections : the overshoot of the S3R current with respect to the square load current shall never be larger than 50 % under all operating (worst case) conditions.

6. TURN OFF DELAY

Consider the SA section S3R interface as drawn on Fig. 7.

The SA section current source is featured along with its parasitic capacitance and harness inductance. The first serial diode stands for the string summation diodes. The second diode (possibly serial redundant) connects the section to the bus.

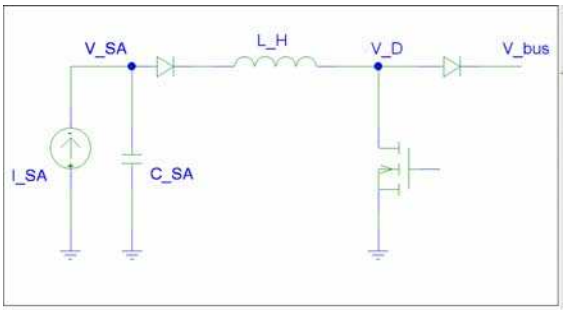

Fig. 7 : SA section S3R interface

Before to quantify the turn OFF delay, it is first underlined that the dipole constituted by the SA capacitance and the harness inductance is likely to be resonant. Indeed the resistance ensuring critical damping is given by :

$$R > 2\sqrt{\frac{L_H}{C_{SA}}}$$

Typical values for the harness inductance and SA capacitance are respectively a few µH and less than 1 µF. Hence, the order of magnitude of this resistance is a few Ohms, which is in conflict with the requirement for low conduction losses within the SA harness.

Now, the turn OFF delay is the time needed for the section to bus current to reach the section current DC value, once the MOSFET has been switched OFF. This delay mainly results from the SA parasitic capacitance, but the harness inductance is a driving parameter as well.

Consider indeed the S3R operation. As a worst case, a section may be asked to switch OFF at a time where the SA section voltage is negative because of the resonance, as suggested on Fig. 6. Considering that the

peak amplitude of the resonant current is limited to the section DC current because of the serial diode at section level preventing the current to be negative, the initial reverse SA voltage is given by :

$$V_{SA}\big|_{\min} = -\sqrt{\frac{L_H}{C_{SA}}} I_{SA}$$

Then, the very first moments of the turn OFF commutation are dedicated to the discharge of the inductance. This consists into a transfer of charges from the SA to the power bus and is therefore neutral in terms of turn OFF delays.

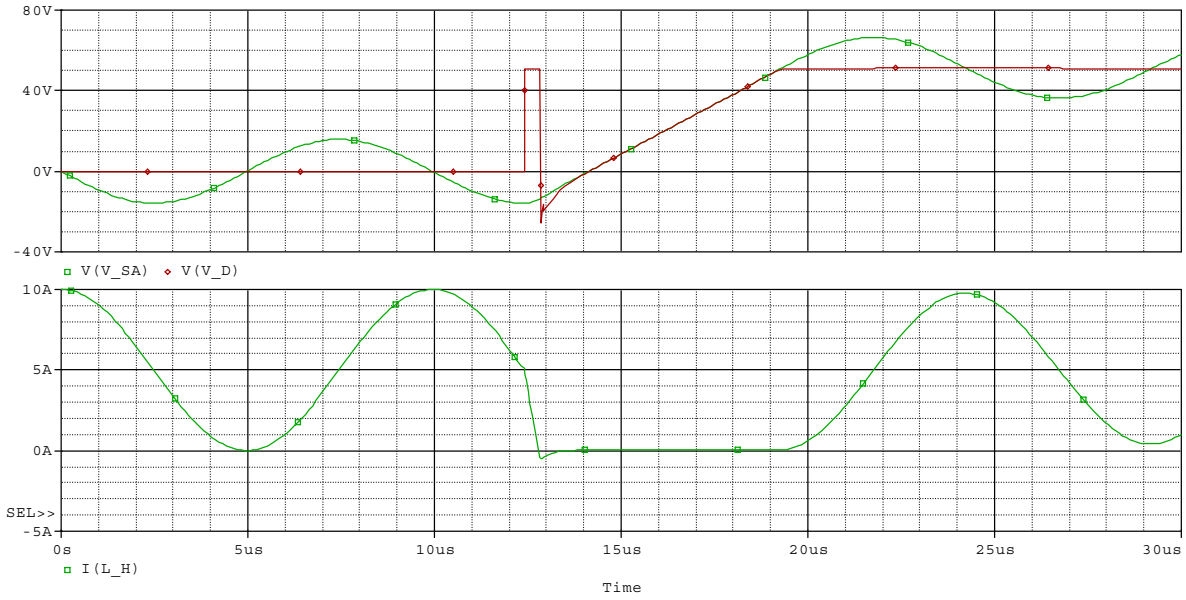

Fig. 8 : SA section to bus voltage and current waveforms

Now, the SA has not only to recover from that negative condition up to the bus voltage. It has also to go through the harness impedance before to deliver to the bus a instantaneous current reaching the DC current value of the section. The equivalent time delay for this second contributor is given by the following average value :

$$\tau_{LC} = \frac{1}{I_{SA}} \int_{O}^{\frac{\pi}{2}\sqrt{L_H C_{SA}}} I_{SA} \cos \frac{t}{\sqrt{L_H C_{SA}}} dt = \sqrt{L_H C_{SA}} \quad (6.1)$$

Hence, the overall turn OFF delay, including the control electronics reaction time, is given by :

$$\tau_{OFF} = \tau_{e^-} + \frac{C_{SA}(V_{bus} - V_{SA}\big|_{\min})}{I_{SA}} + \tau_{LC}$$

that is :

$$\tau_{OFF} = \tau_{e^-} + \frac{C_{SA} V_{bus}}{I_{SA}} + 2\sqrt{L_H C_{SA}} \quad (6.2)$$

The attention is drawn on the fact that this formula contains an additional term with respect to the one proposed in the original S3R paper [4, p. 131], which term is proportional to the period of the resonance between the SA capacitance and the harness inductance. One might argue that this term is conservative e.g. because of the damping that the current oscillation anyhow undergoes or because of the possible clamping of negative SA voltage by the IBF (Integrated Bypass Function) diodes. It is however stressed that it might also be underestimated as the time delay for the SA section to push the current through the harness impedance assumes that the SA is able to develop a voltage equal to :

$$V_{SA}\big|_{\max} = V_{bus} + I_{SA}\sqrt{\frac{L_H}{C_{SA}}}$$

which value might not be fully sustained at high SA temperature because of the lower I to V curve elbow.

As another remark, the time delay provision (6.1) is tantamount to a voltage drop provision for the S3R section rippling whose maximum value is :

$$\Delta V_{bus} = \frac{I_{SA}}{C_{bus}} \sqrt{L_H C_{SA}}$$

This value is worth to be compared to the peak voltage developed on the power bus by the SA section resonant current, that is :

$$V_{bus}\big|_{pk} = \frac{I_{SA}}{C_{bus} \frac{1}{\sqrt{L_H C_{SA}}}}$$

Both values are identical, which means that the time delay provision (6.1) covers the S3R operation with respect to the SA section resonance both in terms of amplitude and delay impacts.

As a final comment, it is noted also that the resort to an inductor to limit the SA section peak current at turn ON will have some negative impact on the S3R impedance.

7. DESIGN GUIDELINES

Before to illustrate the S3R closed loop behaviour by a sizing case and some simulations, the different formula that have been presented are now gathered, providing synthetic S3R design guidelines.

Let the following parameters be :

V_{bus} the bus voltage reference,

N_{sect} the number of SA sections,

I_{SA} the SA section current,

C_{SA} the SA section parasitic capacitance,

L_H the SA section harness inductance,

C_{bus} the bus capacitance,

$V_{th+}\big|_{SectN}$ the upper threshold of the upper section on the MEA voltage range (i.e. the Nth section),

$V_{th-}\big|_{Sect1}$ the lower threshold of the lower section on the MEA voltage range (i.e. the 1st section),

V_{ref} the low level voltage reference,

F_{ripple} the maximum section ripple frequency (driven e.g. by power dissipation or driver consumption of the MOSFET),

τ_{e-} the S3R section switching electronic delay (applicable at both turn ON and turn OFF).

The S3R closed loop may then be sized according to the following steps.

Note that a WCA (Worst case Analysis) approach shall be performed, e.g. with respect to the maximum and minimum values of the SA capacitance, the harness inductance or the distance between positive (or negative) thresholds of successive sections.

Step 1 – Turn ON and turn OFF delays according to formula (6.2).

$$\tau_{ON} = \tau_{e-}$$

$$\tau_{OFF} = \tau_{e-} + \frac{C_{SA} V_{bus}}{I_{SA}} + 2\sqrt{L_H C_{SA}}$$

Step 2 – Bus voltage ripple at maximum frequency, which ripple is met with a load current of 50 % of the SA section.

$$\Delta V_{ripple} = \frac{I_{SA}}{4 C_{bus} F_{ripple}}$$

Step 3 – Bus voltage ripple at zero turn ON and turn OFF delays.

$$\Delta V_{ripple}\big|_0 = \Delta V_{ripple} - \frac{I_{SA}}{2C_{bus}} (\tau_{OFF} + \tau_{ON})$$

Step 4 – Gain K given by the ratio between the low level voltage and the bus voltage references.

$$K = \frac{V_{ref}}{V_{bus}}$$

Step 5 – Gain A according to the maximum bus and MEA voltage ranges.

$$A \le \frac{V_{th+}\big|_{SectN} - V_{th-}\big|_{Sect1}}{K(\Delta V_{ripple}\big|_0 + (N_{sect} - 1)\frac{I_{SA}}{C_{bus}} \tau_{OFF})}$$

Step 6 – Hysteresis voltage on the MEA voltage range, i.e. the distance between the positive and negative thresholds of any one section.

$$V_{hyst} = KA.\Delta V_{ripple}\Big|_0$$

Step 7 – Distance on the MEA voltage range between two positive (or negative) thresholds of successive sections.

$$\Delta V_{th} = \frac{(V_{th+}\big|_{SectN} - V_{th-}\big|_{Sect1}) - V_{hyst}}{N_{sect} - 1}$$

The steps 6 and 7 allows any threshold on the MEA voltage range to be defined.

Step 8 – Gain G as the transconductance from MEA voltage to S3R current.

$$G = \frac{I_{SA}}{\Delta V_{th}}$$

Step 9 - Bus impedance according to formula (4.1).

$$Z^{-}_{S3R} = \frac{1}{KAG}$$
$$Z^{+}_{S3R} = \frac{1{,}5}{KAG}$$

Step 10 – MEA zero frequency (associated to the integrator gain), well below the cut off frequency given by (4.2).

$$\omega_{zero} << \frac{1}{\tau_{OFF}}$$

Note that the phase shift at the cut off frequency associated to the integrator is limited to 2° for a 30 dB ratio between the zero position and this cut off frequency.

8. ILLUSTRATION

8.1. S3R Sizing

To illustrate a S3R sizing case, let consider a 50 V power bus with the following input parameters.

V_{bus} = 50 V

N_{sect} = 8

I_{SA} = 5 A

C_{SA} = 1 µF

L_H = 0 µH

C_{bus} = 1 mF

$V_{th+}\big|_{SectN}$ = 15 V

$V_{th-}\big|_{Sect1}$ = 2 V

V_{ref} = 6,4 V

F_{ripple} = 3,5 kHz

τ_{e^-} = 1 µsec

The harness inductance has intentionally been selected to zero, hence avoiding any ringing with the parasitic capacitance, with the sole purpose to make the simulation waveforms more legible. The sizing steps may now be followed.

Step 1 – Turn ON and turn OFF delays

$$\tau_{ON} = \tau_{e^-} = 1\ \mu\text{sec}$$

$$\tau_{OFF} = \tau_{e^-} + \frac{C_{SA}V_{bus}}{I_{SA}} + 2\sqrt{L_H C_{SA}} = 11\ \mu\text{sec}$$

Step 2 – Bus voltage ripple at maximum frequency

$$\Delta V_{ripple} = \frac{I_{SA}}{4C_{bus}F_{ripple}} = 0{,}357\ \text{V}$$

Step 3 – Bus voltage ripple at zero turn ON and turn OFF delays

$$\Delta V_{ripple}\Big|_0 = \Delta V_{ripple} - \frac{I_{SA}}{2C_{bus}}(\tau_{OFF} + \tau_{ON}) = 0{,}327\ \text{V}$$

Step 4 – Gain K

$$K = \frac{V_{ref}}{V_{bus}} = 0{,}128$$

Step 5 – Gain A

$$A = \frac{V_{th+}\big|_{SectN} - V_{th-}\big|_{Sect1}}{K(\Delta V_{ripple}\big|_0 + (N_{sect} - 1)\frac{I_{SA}}{C_{bus}}\tau_{OFF})} = 143$$

Step 6 – Hysteresis voltage on the MEA voltage range

$$V_{hyst} = KA\Delta V_{ripple}\big|_0 = 6{,}0 \text{ V}$$

Step 7 – Distance on the MEA voltage range between two positive (or negative) thresholds of successive sections

$$\Delta V_{th} = \frac{(V_{th+}\big|_{SectN} - V_{th-}\big|_{Sect1}) - V_{hyst}}{N_{sect} - 1} = 1{,}0 \text{ V}$$

Step 8 – Gain G

$$G = \frac{I_{SA}}{\Delta V_{th}} = 5{,}0 \text{ A/V}$$

Step 9 - Bus impedance

$$Z_{S3R}^{-} = \frac{1}{KAG} = 11 \text{ m}\Omega$$

$$Z_{S3R}^{+} = \frac{1{,}5}{KAG} = 16{,}5 \text{ m}\Omega$$

Step 10 – MEA zero frequency

$$\frac{1}{\tau_{OFF}} = 14{,}5 \text{ kHz } 2\pi \text{ rad}$$

$$\omega_{zero} = 300 \text{ Hz } 2\pi \text{ rad} << \frac{1}{\tau_{OFF}} \text{ by 33 dB}$$

8.2. Block Diagram Simulation

We first perform some simulations of the S3R equivalent current continuous block diagram, with reference to Fig. 4.

The associated schematics in line with the previous sizing are displayed on Fig. 9. For nominal behaviour simulations, it is sufficient to consider two delay blocks, namely one for the turn ON delay and a second one for the turn OFF delay. Note also that the MEA integrator is not implemented, with the purpose of easing the interpretation of the simulated waveforms as there will be no need to sort the integrator effect from the remaining dynamics.

The time behaviour of the block diagram is shown on Fig. 10. A square load current is applied with a 3 msec period and an initial value of 6 A. We are concerned by the step response of the bus voltage to the load current.

After 1 msec, the load current is increased by 18 A up to 24 A, yielding an equivalent S3R turn OFF operation. Because of the turn OFF delay, the output current reaches the load current after an overshoot of 8,37 A or 47 % of the load step amplitude. The current step generates a bus voltage step of 198 mV, well in line with the bus impedance of 11 mΩ. The current overshoot coincides with a negative bus voltage overshoot of 111 mV or 56 % of the voltage step amplitude. Note that the difference between the relative values of the current and voltage overshoots is due to the nonlinear V_{MEA} to I_{S3R} relation (see Fig. 3).

After 2,5 msec, the load current subsides down to the initial value of 6 A. It corresponds to an equivalent S3R turn ON operation. Because the turn ON delay is significantly lower than the turn OFF delay, there is neither a current overshoot nor a voltage one.

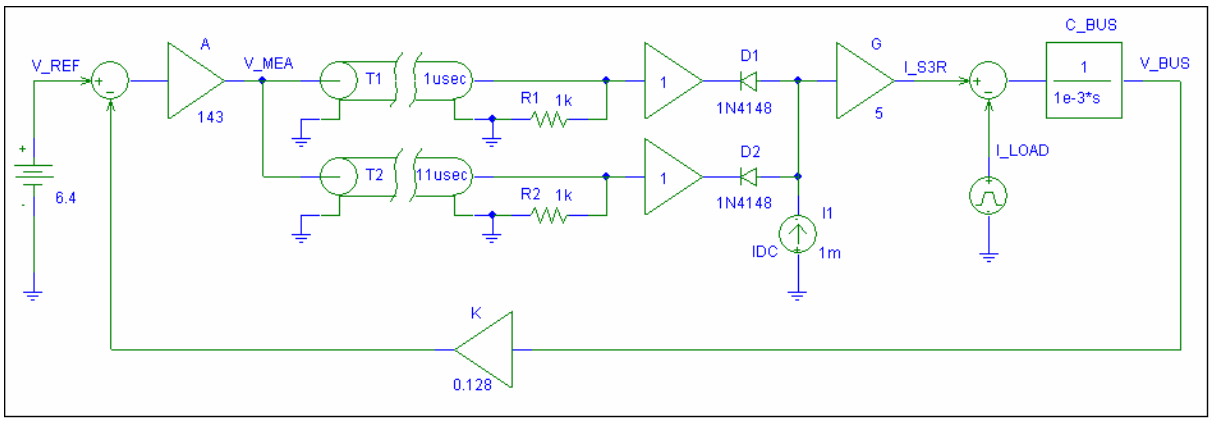

Fig. 9 : S3R equivalent current continuous schematics

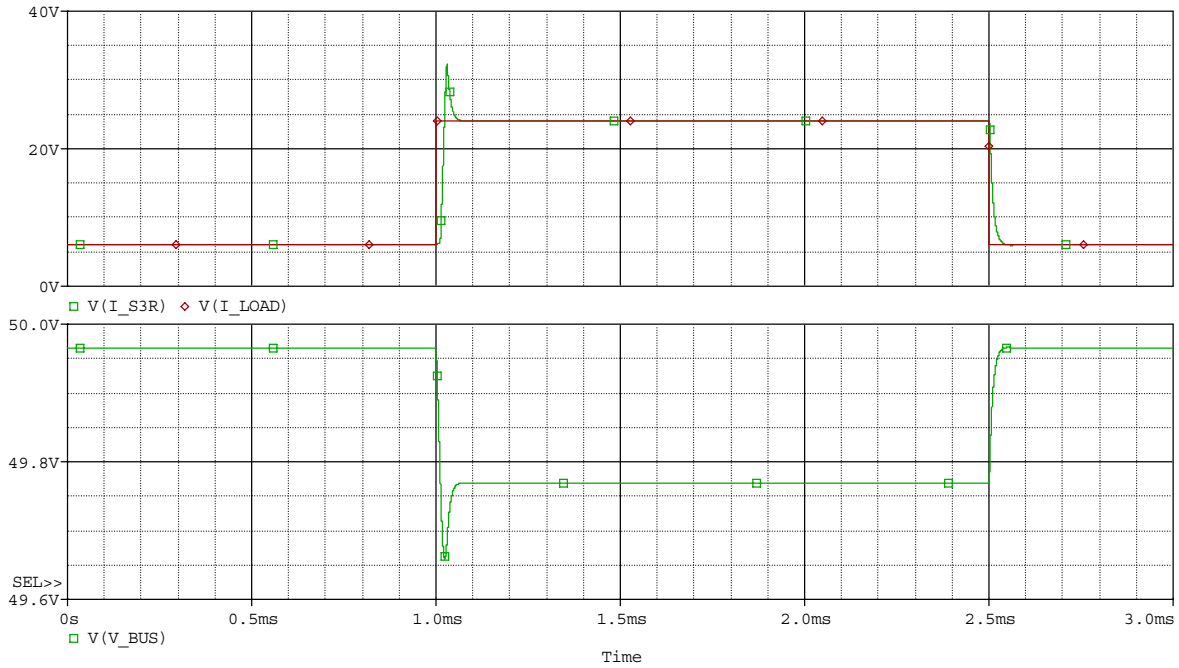

Fig. 10 : S3R equivalent continuous current and bus voltage waveforms

8.3. S3R Simulation

We now perform some simulations of an actual S3R in line with the sizing case presented above. The associated schematics is given on Fig. 11. As stated earlier, no harness inductance and no MEA integrator are considered, the purpose being to allow an easy examination of the waveforms. The attention of the reader is also drawn on the VT and VH values of the switches which correspond to positive and negative commutation thresholds of respectively (VT + VH) and (VT – VH). This means that the hysteresis voltage is equal to 2 x VH.

The time behaviour simulation is shown on Fig. 12. We are again concerned by the step response of the bus voltage to the load current. A square signal is applied with a 3 msec period and a initial value of 6 A. This simulation is to be compared to the one of Fig. 10.

When the load current increases from 6 A to 24 A, the fourth section is put in rippling mode to match the new current demand in mean value while the three first sections are connected to the bus. It is however observed that two additional sections on top of the switching one are called one transiently. This constitutes a current overshoot of 2 times 5 A. This is well consistent with the 8,4 A overshoot of Fig. 10 knowing that the S3R can only switch entire SA sections. The current overshoot coincides with a negative bus voltage overshoot that is visible in the voltage ripple associated to the section switching.

Conversely, when the load current subsides down to the initial value of 6 A, there is no section overshoot, as on Fig. 10.

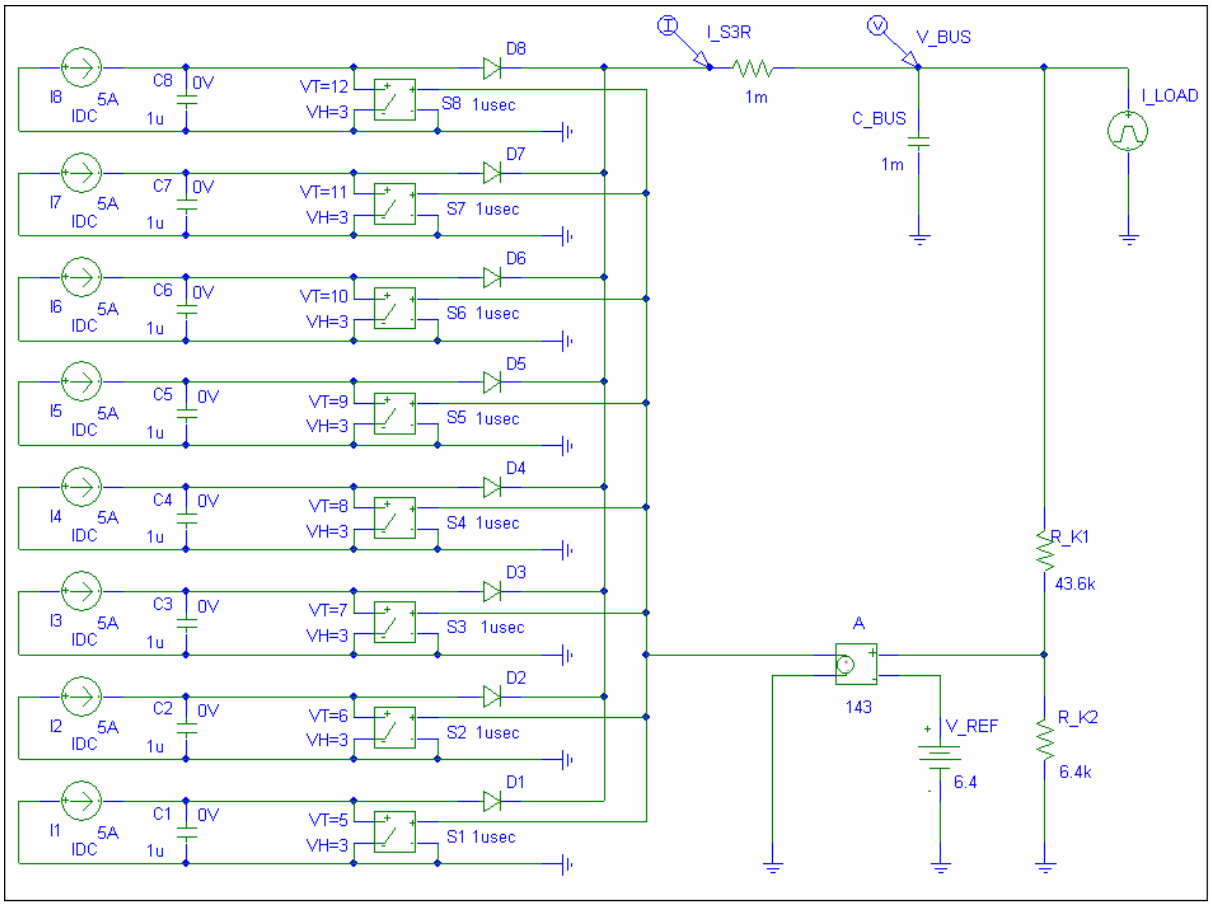

Fig. 11 : S3R schematics (no MEA integrator)

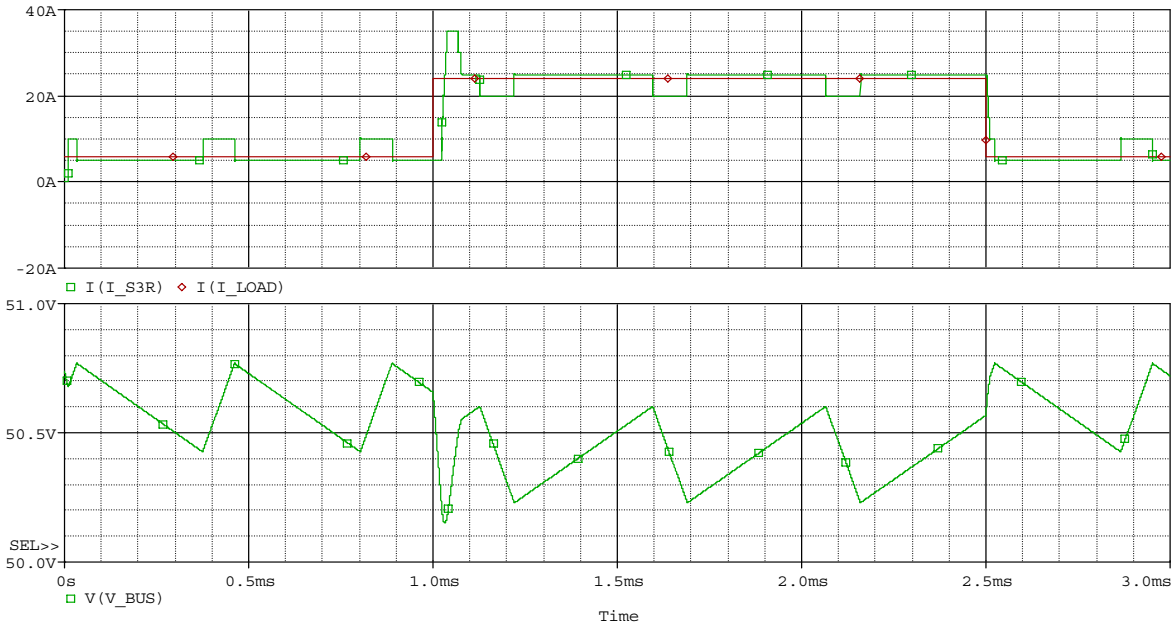

Fig. 12 : S3R current and bus voltage waveforms

9. CONCLUSIONS

A dynamic analysis of the S3R has been performed.

Considering the nonlinearities of the regulator, the stability issues have not been investigated in terms of gain and phase margins but directly in terms of electrical and thermal performances. The study has shown that the commutation thresholds design as originally proposed constitute a careful balance between the S3R electrical and thermal features. The analysis has also dealt with the resonance between the SA section and its harness, and highlighted the sizing provision to be made to make it fully sustainable.

Besides, the study has come up with a S3R equivalent current continuous block diagram giving a better insight into the S3R dynamics. Simulations have been performed of this current continuous model and of S3R schematics, showing the consistency of the analysis.

It has in particular been illustrated that the step response to a load current of a S3R, considering the parametric sizing as originally proposed, features an output current overshoot of 50 % of the step amplitude. Although a design performed with a WCA analysis will demonstrate typical performance better than that one, the attention is drawn with respect to TDMA load. In such a situation, the number of SA sections called on by the TDMA load may be significantly larger than the one corresponding to the peak to peak load amplitude. This must namely be taken into account when active control is used to limit the SA peak current at turn ON, as this provision is associated to larger dissipation level within each section in switching.

As another feature, it has been underlined that the harness inductance has some impact on the SA section turn OFF delay, and thereby on the bus impedance. This must in particular be taken into account when the SA peak current limitation at turn ON is based on a serial inductor.

Concerning the experimental validation of the S3R dynamics, rather than attempting to draw a Bode plot, it has been recommended to perform a time domain measurement by recording the S3R current response to a TDMA like load of sufficiently large amplitude and measuring the S3R current overshoot amplitude, both by simulation and on the hardware.

Finally, all the formula linking the S3R parameters have been gathered in a self contained rationale, thereby providing exhaustive guidelines for S3R sizing.

REFERENCES

[1] C. Delepaut and M. Martin, “Current Limitation techniques in a S3R Cell”, Proceedings of the 3th European Space Power Conference, Graz, Austria, 23-27 August 1993, ESA WPP-054, pp. 61-66.

[2] European Cooperation for Space Standardisation, “Space Engineering, Electrical and Electronic”, ECSS-E-20A, 4 October 1999, ISSN 1028-396X.

[3] T. E. Fortmann and K. L. Hitz, “An Introduction to Linear Control Systems”, Control and Systems Theory Volume 5, Marcel Dekker Edition, 1977, ISBN 0-8247-8016-7.

[4] D. O’Sullivan and A. Weinberg, “The Sequential Switching Shunt Regulator S3R”, Proceedings of the 3rd ESTEC Spacecraft Power Conditioning Seminar, Noordwijk, The Nederlands, 21-23 September 1977, ESA SP-126, pp. 123-131.

[5] P. Perol, “Another Look at the Sequential Switching Shunt Regulator”, Proceedings of the 5th European Space Power Conference, Tarragona, Spain, 21-25 September 1998, ESA SP-416, pp. 79-84.

[6] G. Picart, “Optimisation of S3R Parameters”, Proceedings of the 3th European Space Power Conference, Graz, Austria, 23-27 August 1993, ESA WPP-054, pp. 195-200.

[7] C. Rouzies and P. Tastet, “Analysis of a particular working mode of S3R Type Regulator”, Proceedings of the ESA sessions at the 16th IEEE Power Electronics Specialists Conference, Toulouse, France, 24-28 June 1985, ESA SP-230, pp. 73-81.

[8] L. G. Van Den Berghe, “Time Domain Analysis of a S3R System”, Proceedings of the ESA sessions at the 16th IEEE Power Electronics Specialists Conference, Toulouse, France, 24-28 June 1985, ESA SP-230, pp. 271-278.

[9] I. R. White, “Design and Development of a Sequential Switching Shunt Regulator”, Proceedings of the 3rd ESTEC Spacecraft Power Conditioning Seminar, Noordwijk, The Nederlands, 21-23 September 1977, ESA SP-126, pp. 133-136.