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IITGN

Digital Systems
LAB 6

Question -1

Design a 4-bit combined BCD/Binary Up/Down counter using the behavioral style of coding.
Implement it on FPGA and show the counter outputs. (The counter can be assumed to
switch between the mode's invalid states. For instance, the counter will not switch to BCD if
the count is non-BCD).

Counter

```
`timescale 1ns / 1ps
module counter(clk,m,reset ,Mode, Q[3:0]);
input clk,Mode,m,reset;
output reg [3:0]Q;
wire slow_clk;
Clock_divider inst1(clk, slow_clk);

always @(posedge slow_clk, reset)
//    if(reset) begin
//        if(Mode)
//    end
    if(m==0) begin
        if(Mode==0) begin
            if(reset)
                Q=0;
            else if(Q==15) begin
                Q=0;
                end
            else
                Q=Q+1;
        end
        else begin
            if(reset)
                Q=15;
            else if(Q==0)
                Q=15;
            else
                Q=Q-1;
        end
       end
```

```
  else begin
      if(Mode==0) begin
          if(reset)
              Q=0;
          else if(Q==9) begin
              Q=0;
              end
          else
              Q=Q+1;
       end
       else begin
          if(reset)
              Q=9;
          else if(Q==0)
              Q=9;
          else
              Q=Q-1;
       end
       end
endmodule
```

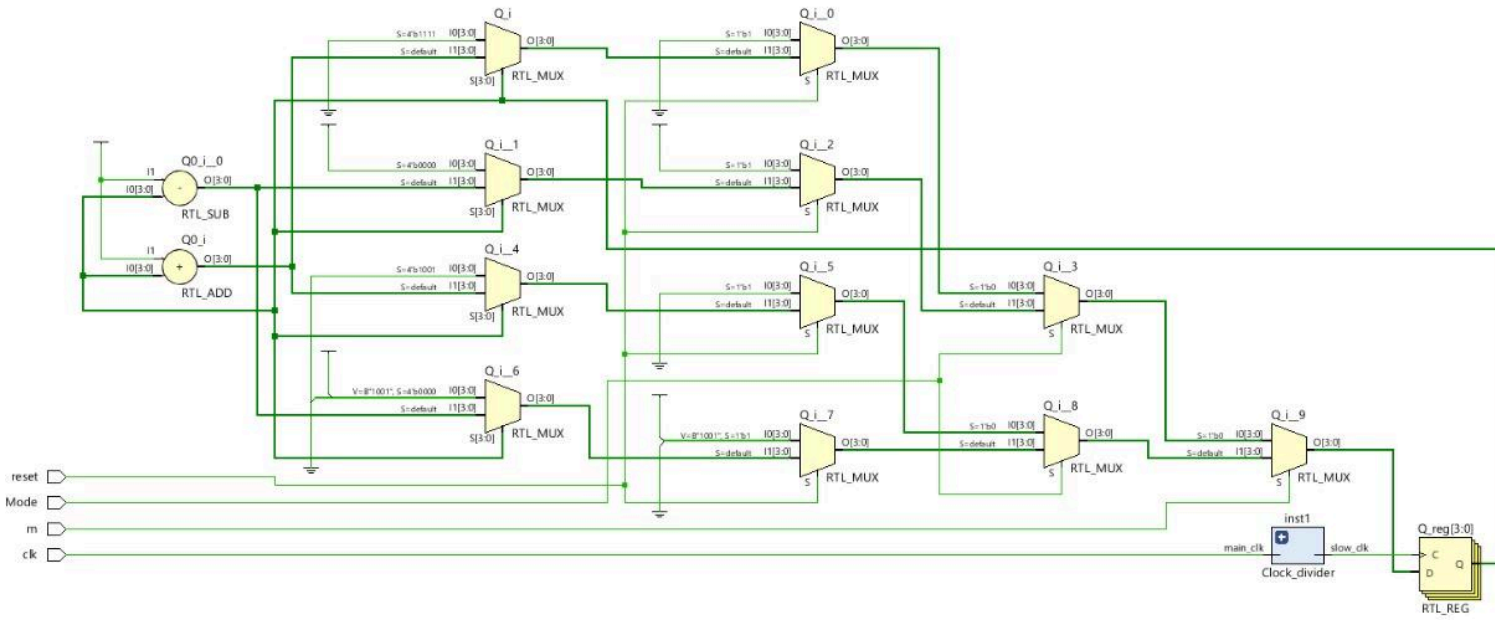
Clock Divider

```
`timescale 1ns / 1ps

module Clock_divider(
input main_clk,
output slow_clk
    );

reg [31:0] counter;

always @(posedge main_clk)
begin
    counter  <= counter + 1;
end
assign slow_clk = counter[27];
endmodule
```

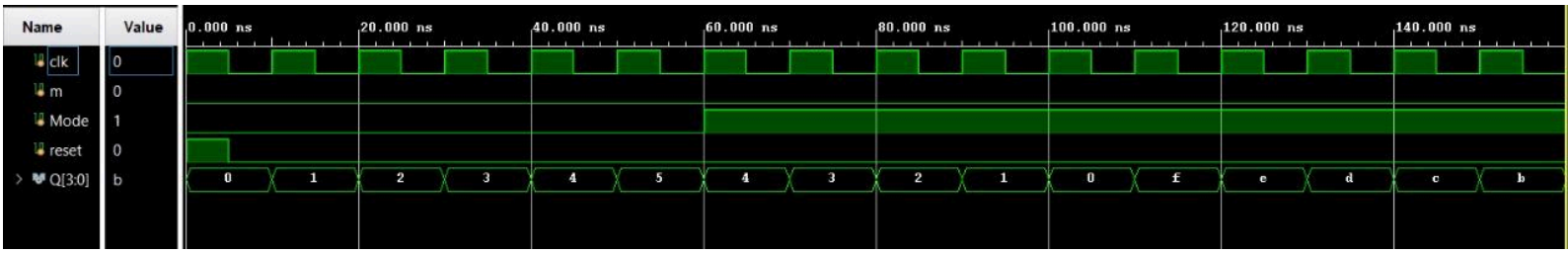
Test Bench

```
`timescale 1ns / 1ps
module test_bench();
reg clk,m,Mode,reset,slow_clk;
wire [3:0]Q;
counter uut(clk,m,reset ,Mode, Q, slow_clk);

initial
begin
clk = 1;
    forever #5 clk = ~clk;
end

initial
begin
    reset=1;
    m=0;Mode=0;
    #5;
    reset=0;
    #55;
//    m=1;
    Mode=1;
    #100;
$finish();
end
endmodule
```

Schematic



Simulation

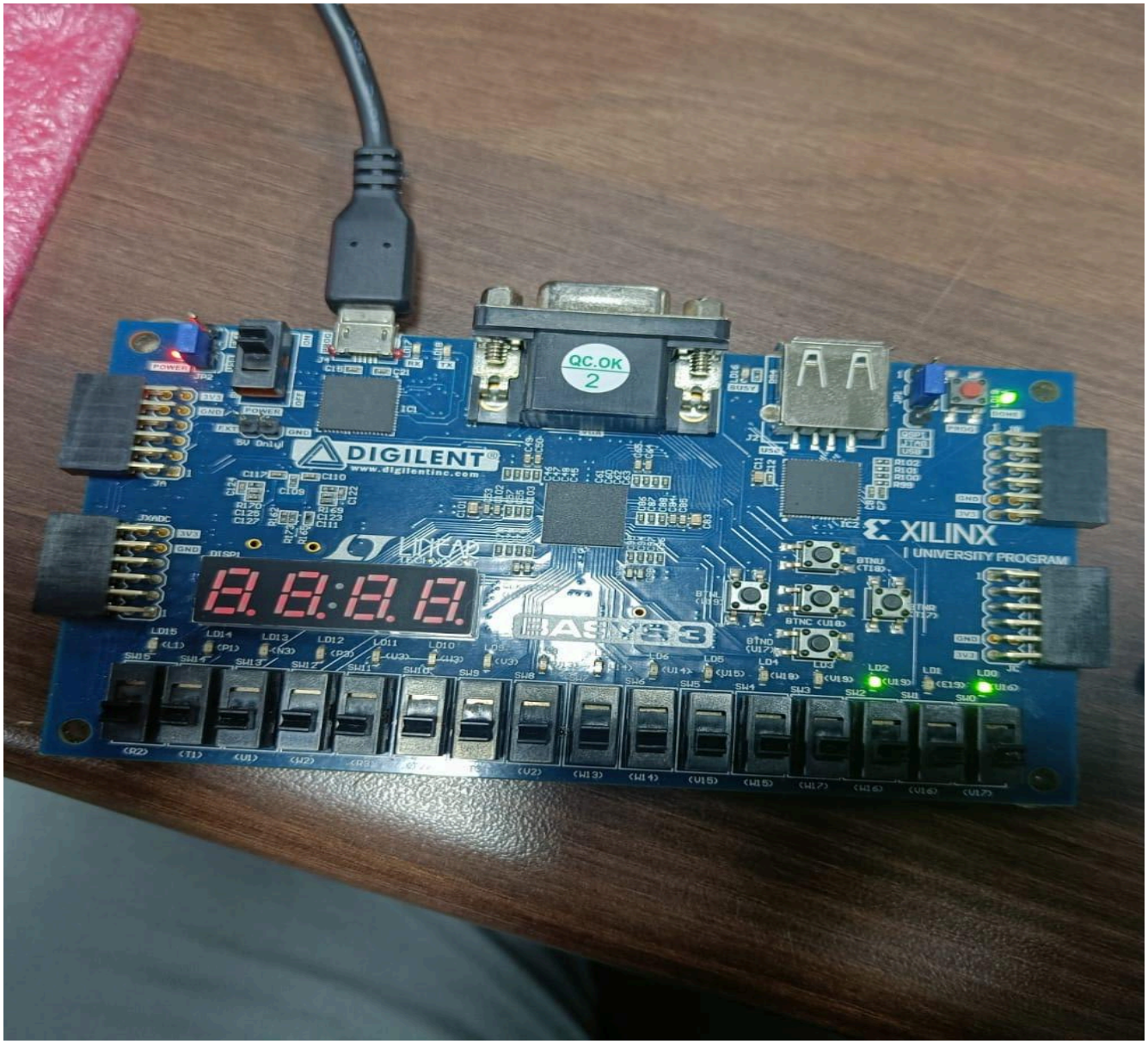


I/O Planning

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type
Q[3]	OUT				V19	✓	14	LVCMOS33*	3.300		12	SLOW
Q[2]	OUT				U19	✓	14	LVCMOS33*	3.300		12	SLOW
Q[1]	OUT				E19	✓	14	LVCMOS33*	3.300		12	SLOW
Q[0]	OUT				U16	✓	14	LVCMOS33*	3.300		12	SLOW
Scalar ports (4)												
clk	IN				W5	✓	34	LVCMOS33*	3.300			
m	IN				R2	✓	34	LVCMOS33*	3.300			
Moc	IN				T1	✓	34	LVCMOS33*	3.300			
rese	IN				U1	✓	34	LVCMOS33*	3.300			

Constraints File

```
1  set_property IOSTANDARD LVCMOS33 [get_ports {Q[3]}]
2  set_property IOSTANDARD LVCMOS33 [get_ports {Q[2]}]
3  set_property IOSTANDARD LVCMOS33 [get_ports {Q[1]}]
4  set_property IOSTANDARD LVCMOS33 [get_ports {Q[0]}]
5  set_property IOSTANDARD LVCMOS33 [get_ports clk]
6  set_property IOSTANDARD LVCMOS33 [get_ports m]
7  set_property IOSTANDARD LVCMOS33 [get_ports Mode]
8  set_property IOSTANDARD LVCMOS33 [get_ports reset]
9  set_property PACKAGE_PIN U16 [get_ports {Q[0]}]
10 set_property PACKAGE_PIN E19 [get_ports {Q[1]}]
11 set_property PACKAGE_PIN U19 [get_ports {Q[2]}]
12 set_property PACKAGE_PIN V19 [get_ports {Q[3]}]
13 set_property PACKAGE_PIN W5 [get_ports clk]
14 set_property PACKAGE_PIN R2 [get_ports m]
15 set_property PACKAGE_PIN T1 [get_ports Mode]
16 set_property PACKAGE_PIN U1 [get_ports reset]
17
```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Utilization Design Information

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1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs	7	0	20800	0.03
LUT as Logic	7	0	20800	0.03
LUT as Memory	0	0	9600	0.00
Slice Registers	4	0	41600	<0.01
Register as Flip Flop	4	0	41600	<0.01
Register as Latch	0	0	41600	0.00
F7 Muxes	3	0	16300	0.02
F8 Muxes	0	0	8150	0.00

Timing Summary Report

| Timer Settings

| ---

Enable Multi Corner Analysis : Yes
Enable Pessimism Removal : Yes
Pessimism Removal Resolution : Nearest Common Node
Enable Input Delay Default Clock : No
Enable Preset / Clear Arcs : No
Disable Flight Delays : No
Ignore I/O Paths : No
Timing Early Launch at Borrowing Latches : No
Borrow Time for Max Delay Exceptions : Yes
Merge Timing Exceptions : Yes

Corner Name	Analyze Max Paths	Analyze Min Paths
Slow	Yes	Yes
Fast	Yes	Yes

Power Report TODAY

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1. Summary

Total On-Chip Power (W)	9.187
Design Power Budget (W)	Unspecified*
Power Budget Margin (W)	NA
Dynamic (W)	9.059
Device Static (W)	0.128
Effective TJA (C/W)	5.0
Max Ambient (C)	39.1
Junction Temperature (C)	70.9
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

- Specify Design Power Budget using, set_operating_conditions -design_power_budget <value in Watts>