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IITGN

# Digital Systems
# LAB Assignment-4

**Question: Write a code for 8-bit x 8-bit (a) Array multiplier (b) Binary multiplier, and compare them. When an M-bit number is multiplied with N-bit number, the product has M+N bits.**

## Array Multiplier

```
`timescale 1ns / 1ps

module ArrayMult(a,b,y);
    parameter n=8,m=8;
    input [n-1:0]a;
    input [m-1:0]b;
    output reg [n+m-1:0] y;

    reg [n+m-1:0] product [m-1:0];
    integer i,j;

    always @(*) begin
        for (i = 0; i < m; i = i + 1) begin
            product[i]=0;
            for(j = 0; j < n; j = j + 1) begin
                if(a[j]==1 && b[i]==1)
                    product[i][i+j]=1;
                else
                    product[i][i+j]=0;
            end
        end
        y=0;
        for(i = 0; i < m; i = i + 1) begin
            y= y+ product[i];
        end
    end

endmodule
```

# Binary Multiplier

```
`timescale 1ns / 1ps

module BinaryMult(a,b,y);

    parameter n=8,m=8;
    input [n-1:0]a;
    input [m-1:0]b;
    output reg [n+m-1:0] y;
    reg [n+m-1:0] product;
    integer i;

    // size of a is n bits and size of b is m bits
    always @(*) begin
        product = 0;
        for (i = m-1; i >= 0; i = i - 1) begin
            if (b[i]==1) begin
                product = product + a; end
            if(i>0) begin
                 product = product<<1; end
        end
        y = product;
    end

endmodule
```

# Test Bench

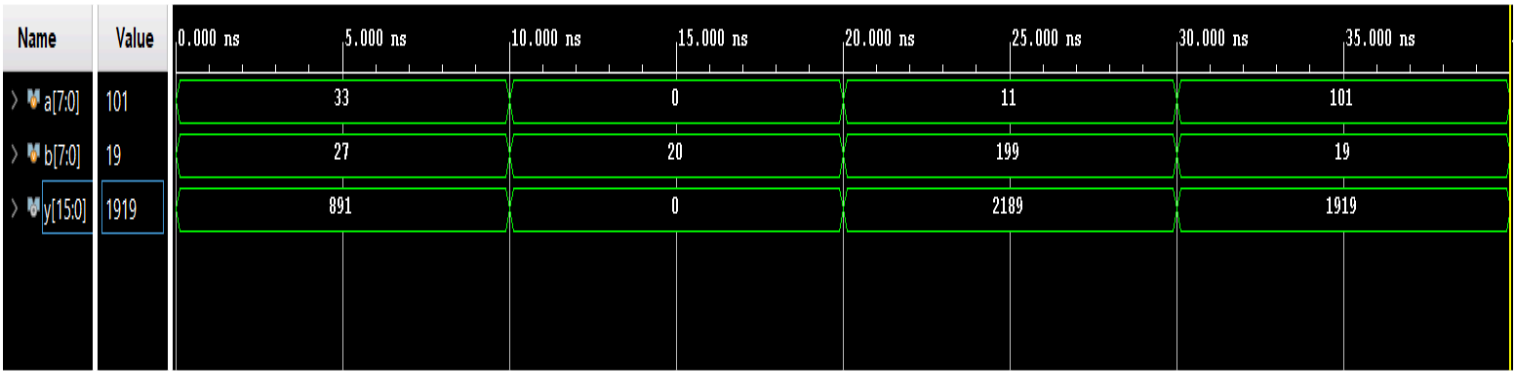
```
`timescale 1ns / 1ps

module test_bench();
reg [7:0]a,b;
wire [15:0]y;

BinaryMult uut(a,b,y);

initial begin
    a=33;b=27;
    #10;
    a=0; b=20;#10
    a=11; b=199;#10
    a=101; b=19;#10
$finish();
end;
endmodule
```

# Simulation




# I/O Planning

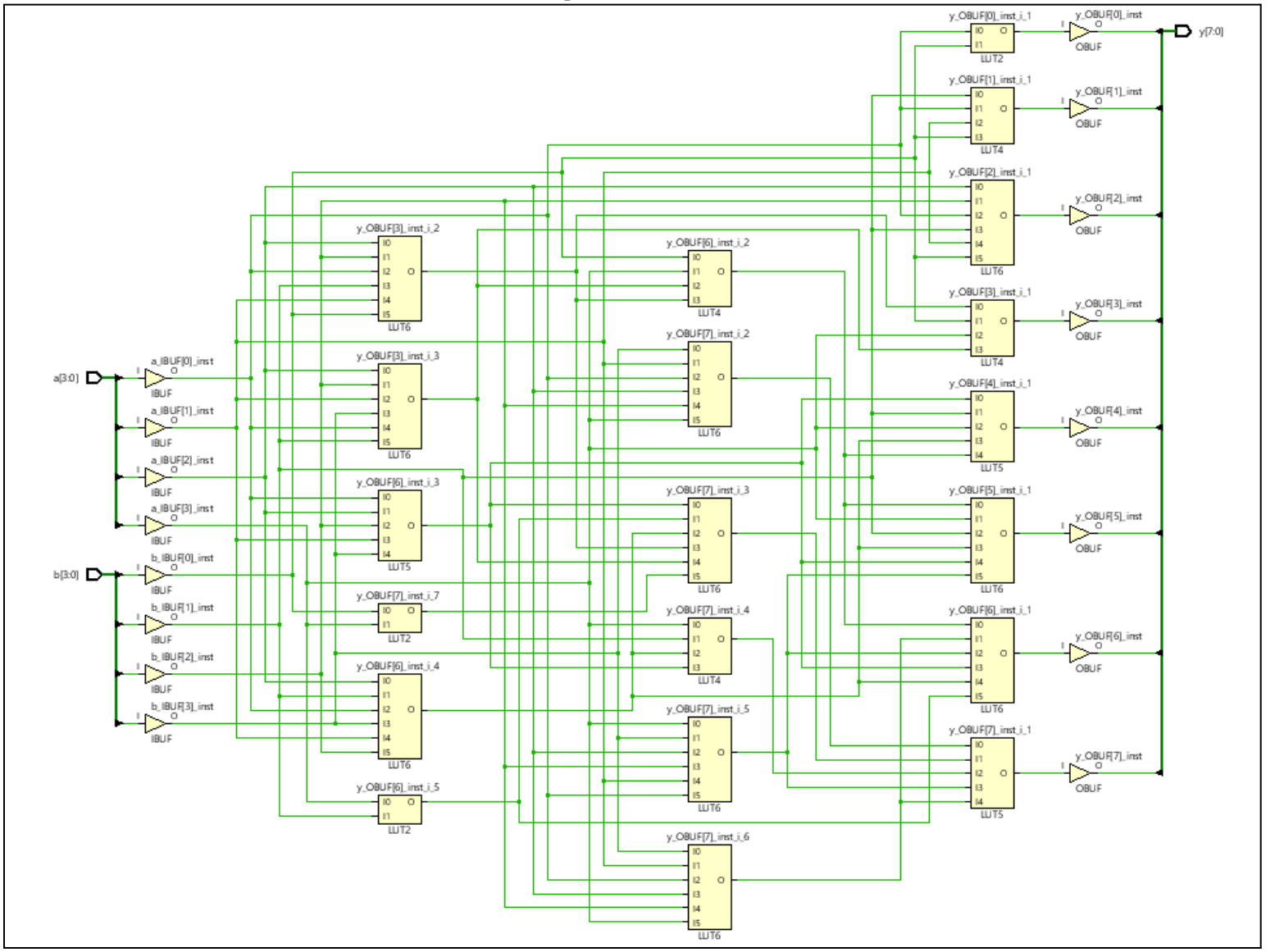
| Name | Direction | Board Part Pin | Board Part Interface | Neg Diff Pair | Package Pin | Fixed | Bank | I/O Std |
|---|---|---|---|---|---|---|---|---|
| All ports (16) | | | | | | | | |
| a (4) | IN | | | | | ☑ | 34 | LVCMOS33* |
| b (4) | IN | | | | | ☑ | 14 | LVCMOS33* |
| b[3] | IN | | | | W17 | ☑ | 14 | LVCMOS33* |
| b[2] | IN | | | | W16 | ☑ | 14 | LVCMOS33* |
| b[1] | IN | | | | V16 | ☑ | 14 | LVCMOS33* |
| b[0] | IN | | | | V17 | ☑ | 14 | LVCMOS33* |
| y (8) | OUT | | | | | ☑ | (Multip | LVCMOS33* |
| y[7] | OUT | | | | U3 | ☑ | 34 | LVCMOS33* |
| y[6] | OUT | | | | W3 | ☑ | 34 | LVCMOS33* |
| y[5] | OUT | | | | V3 | ☑ | 34 | LVCMOS33* |
| y[4] | OUT | | | | V13 | ☑ | 14 | LVCMOS33* |
| y[3] | OUT | | | | V14 | ☑ | 14 | LVCMOS33* |
| y[2] | OUT | | | | U14 | ☑ | 14 | LVCMOS33* |
| y[1] | OUT | | | | U15 | ☑ | 14 | LVCMOS33* |
| y[0] | OUT | | | | W18 | ☑ | 14 | LVCMOS33* |
| Scalar ports (0) | | | | | | | | |

# Constrain.xdc

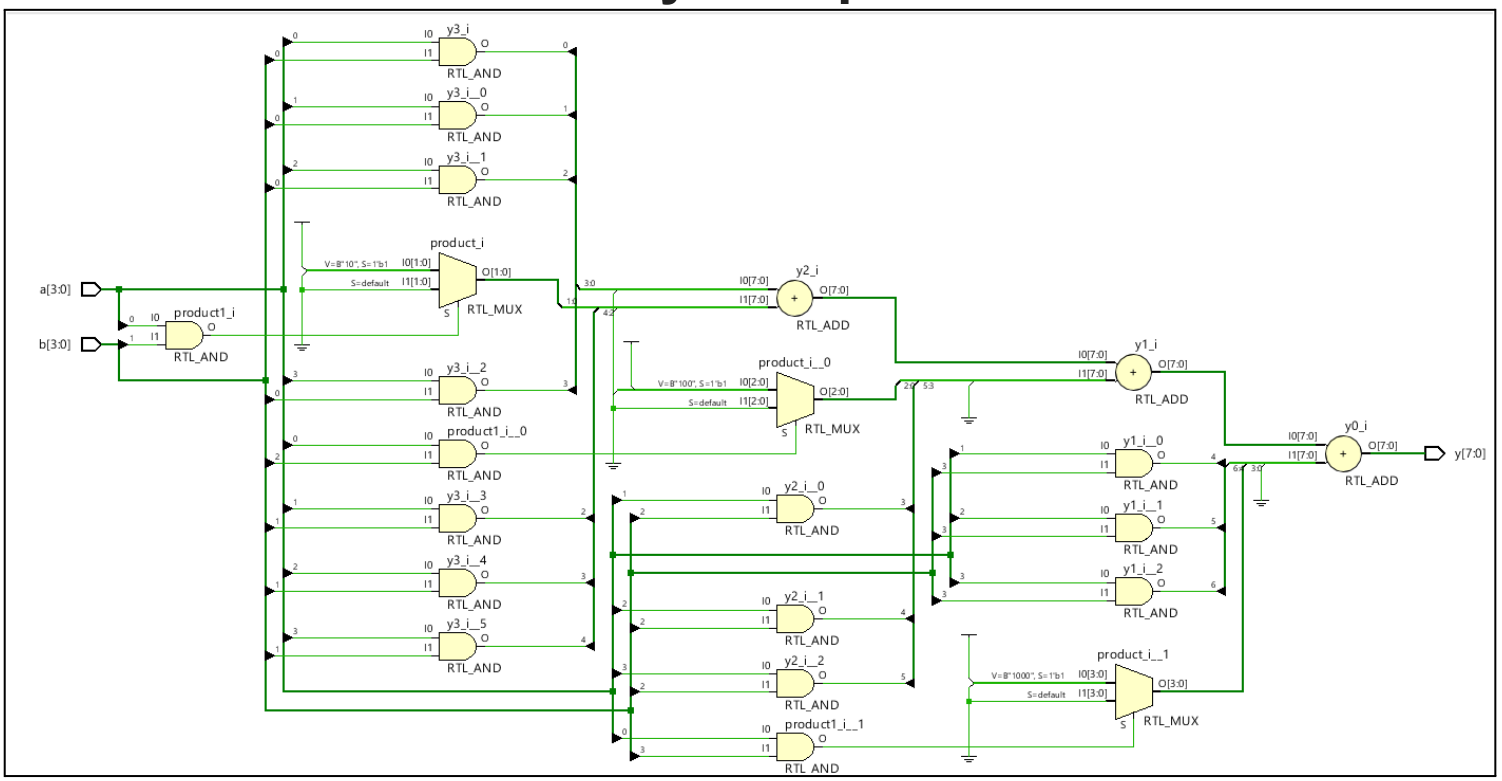
C:/Users/patel/Lab_Ass 4/Lab_Ass 4.srcs/constrs_1/new/Constrain.xdc

```
1  set_property IOSTANDARD LVCMOS33 [get_ports {a[3]}]
2  set_property IOSTANDARD LVCMOS33 [get_ports {a[2]}]
3  set_property IOSTANDARD LVCMOS33 [get_ports {a[1]}]
4  set_property IOSTANDARD LVCMOS33 [get_ports {a[0]}]
5  set_property IOSTANDARD LVCMOS33 [get_ports {b[3]}]
6  set_property IOSTANDARD LVCMOS33 [get_ports {b[2]}]
7  set_property IOSTANDARD LVCMOS33 [get_ports {b[1]}]
8  set_property IOSTANDARD LVCMOS33 [get_ports {y[8]}]
9  set_property IOSTANDARD LVCMOS33 [get_ports {y[7]}]
10 set_property IOSTANDARD LVCMOS33 [get_ports {y[6]}]
11 set_property IOSTANDARD LVCMOS33 [get_ports {y[5]}]
12 set_property IOSTANDARD LVCMOS33 [get_ports {y[4]}]
13 set_property IOSTANDARD LVCMOS33 [get_ports {y[3]}]
14 set_property IOSTANDARD LVCMOS33 [get_ports {y[2]}]
15 set_property IOSTANDARD LVCMOS33 [get_ports {y[1]}]
16 set_property IOSTANDARD LVCMOS33 [get_ports {y[0]}]
17 set_property PACKAGE_PIN R2 [get_ports {a[3]}]
18 set_property PACKAGE_PIN T1 [get_ports {a[2]}]
19 set_property PACKAGE_PIN U1 [get_ports {a[1]}]
20 set_property PACKAGE_PIN W2 [get_ports {a[0]}]
21 set_property PACKAGE_PIN W17 [get_ports {b[3]}]
22 set_property PACKAGE_PIN W16 [get_ports {b[2]}]
23 set_property PACKAGE_PIN V16 [get_ports {b[1]}]
24 set_property PACKAGE_PIN V17 [get_ports {b[0]}]
25 set_property PACKAGE_PIN U3 [get_ports {y[7]}]
26 set_property PACKAGE_PIN W3 [get_ports {y[6]}]
27 set_property PACKAGE_PIN V3 [get_ports {y[5]}]
28 set_property PACKAGE_PIN V13 [get_ports {y[4]}]
29 set_property PACKAGE_PIN V14 [get_ports {y[3]}]
30 set_property PACKAGE_PIN U14 [get_ports {y[2]}]
```

# Schematics
# Binary Multipiler



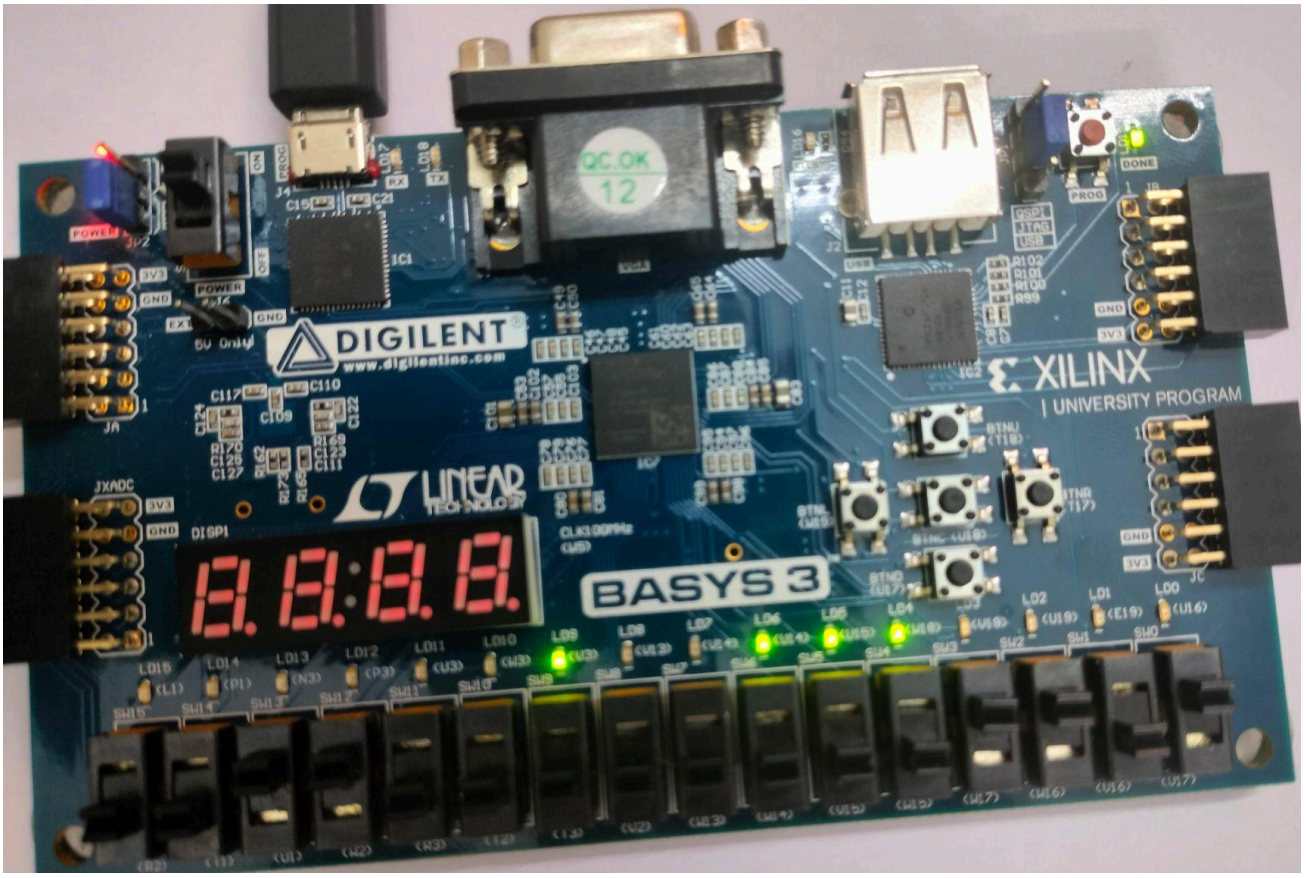
# Array Multiplier



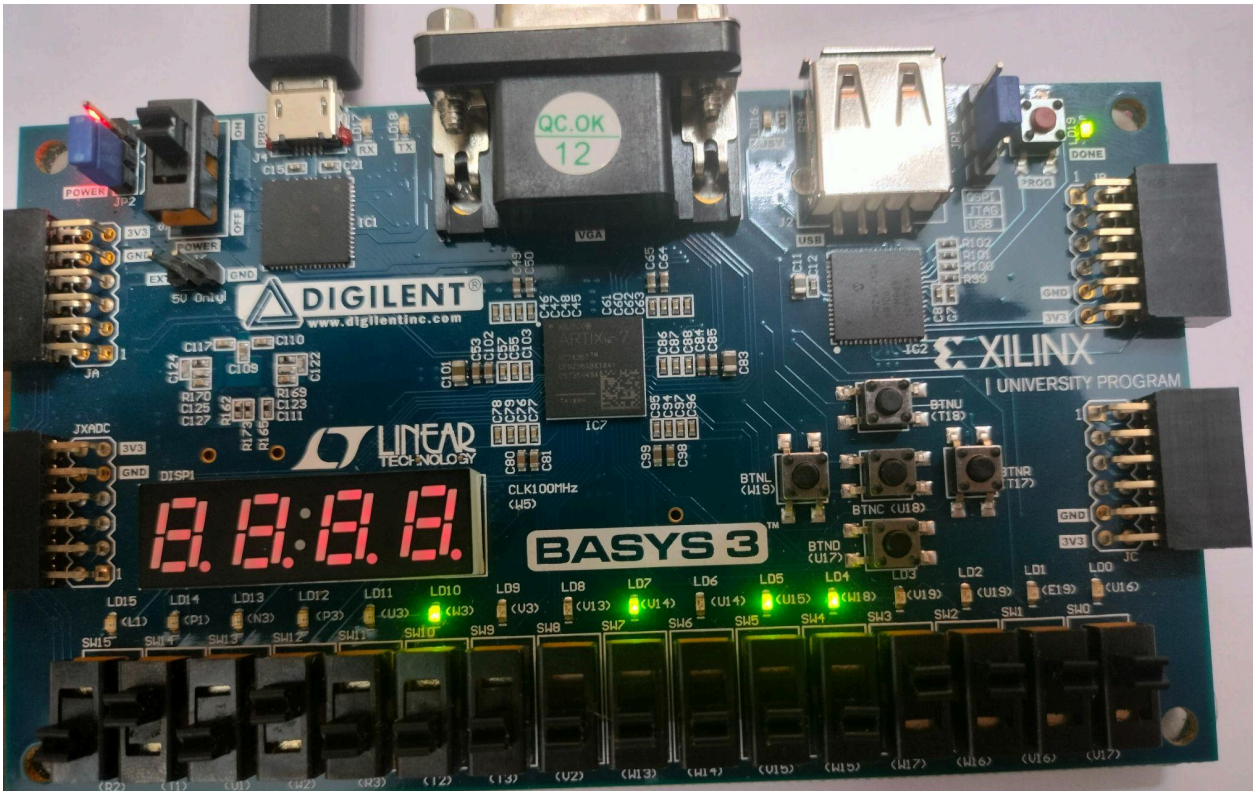
# FPGMA Implementation

a[3]=R2  a[2]=T1  a[1]=U1  a[0]=R2
b[3]=W17  b[2]=W16  b[1]=V17  b[0]=V16
Output y are middle 8 LED's with MSB at left and LSB at right


a=0111=7
b=1001=9
y=00111111=63




a=0011=3
b=1101=13
y=00100111=39




a=0101 = 5
b=1111 = 15
y=01001011=75