INDIAN INSTITUTE OF TECHNOLOGY GANDHINAGAR

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Digital Systems LAB Assignment-5

Question 1) Design a 4-bit comparator that gives a 1 when both the values are equal, 0 if they are unequal. The 4-bit comparator has A[3:0] and B[4:0] inputs, and a single output f. If A=B, f=1, otherwise f=0. You have to synthesize and show the implementation on FPGA.

4 Bit Comparator

```
`timescale 1ns / 1ps

module comparator(A, B, f);
input [3:0]A;
input [3:0]B;
output f;

assign f= (A==B) ? 1:0;
endmodule
```

Test Bench

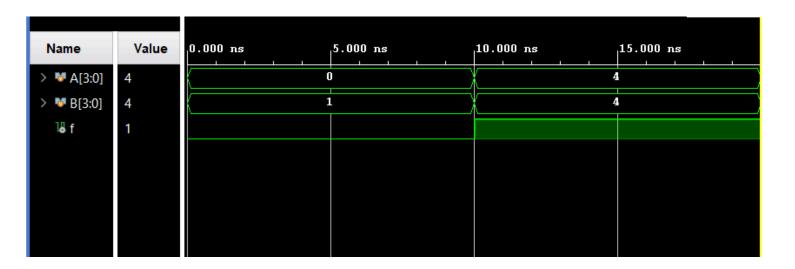
```
`timescale 1ns / 1ps

module test_bench();
reg [3:0]A;
reg [3:0]B;
wire f;

comparator uut(A,B,f);

initial
begin
A= 4'b0000; B=4'b0001;#10
A= 4'b0100; B=4'b0100;#10
```

Simulation



Constrain.xdc

× test_bench.v × Constrain.xdc comparator.v Hardware | Properues C:/Users/patel/Lab5/Lab5.srcs/constrs_1/new/Constrain.xdc set property IOSTANDARD LVCMOS33 [get ports f] set property IOSTANDARD LVCMOS33 [get_ports {A[3]}] set property IOSTANDARD LVCMOS33 [get_ports {A[2]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}] set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}] set property IOSTANDARD LVCMOS33 [get_ports {B[3]}] set property IOSTANDARD LVCMOS33 [get ports {B[2]}] set property IOSTANDARD LVCMOS33 [get_ports {B[1]}] set property IOSTANDARD LVCMOS33 [get ports {B[0]}] set_property PACKAGE_PIN R2 [get_ports {A[3]}] 10 11 set property PACKAGE_PIN T1 [get ports {A[2]}] 12 set_property PACKAGE_PIN U1 [get_ports {A[1]}] set property PACKAGE PIN W2 [get ports {A[0]}] 13 14 set_property PACKAGE_PIN R3 [get_ports {B[3]}] 15 set property PACKAGE_PIN T2 [get ports {B[2]}] 16 set_property PACKAGE_PIN T3 [get_ports {B[1]}] 17 set property PACKAGE_PIN V2 [get ports {B[0]}] 18 set_property PACKAGE_PIN U16 [get_ports f] 19

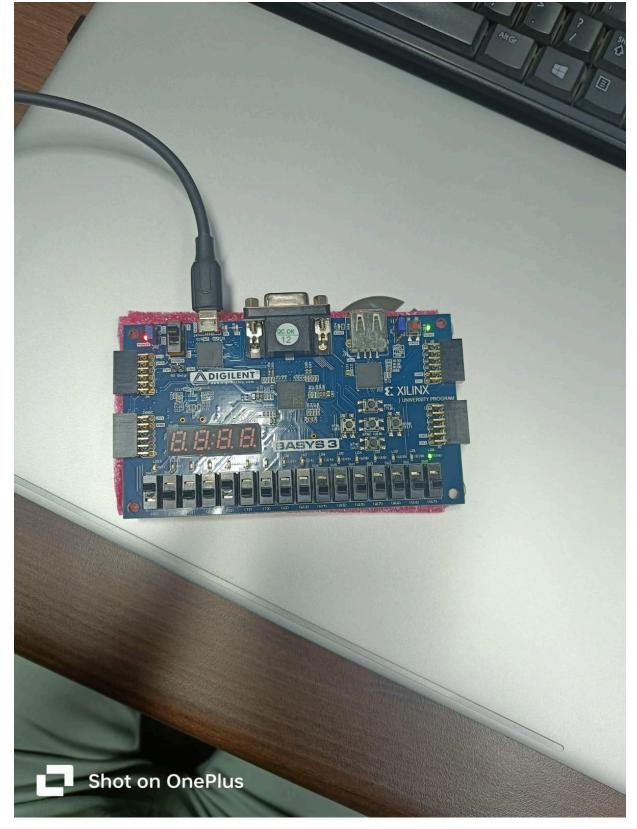
A[3]=R[2] A[2]=T[1] A[1]=U[1] A[0]=W[2] B[3]=R[3] B[2]=T[2] B[1]=T[3] B[0]=V[2] f=Led=U[16]



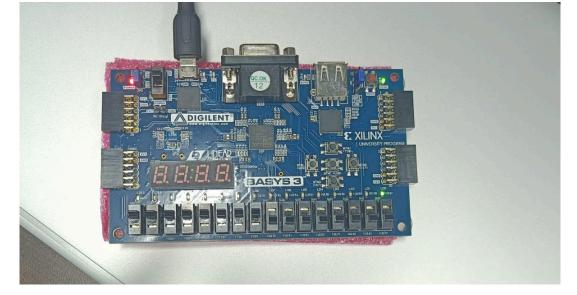
A=0000 B=0000 Led is Blinking



A=1000 B=0000 Led is Not Blinking



A=1000 B=1000 Led is Blinking



A=1111 B=1111 Led is Blinking