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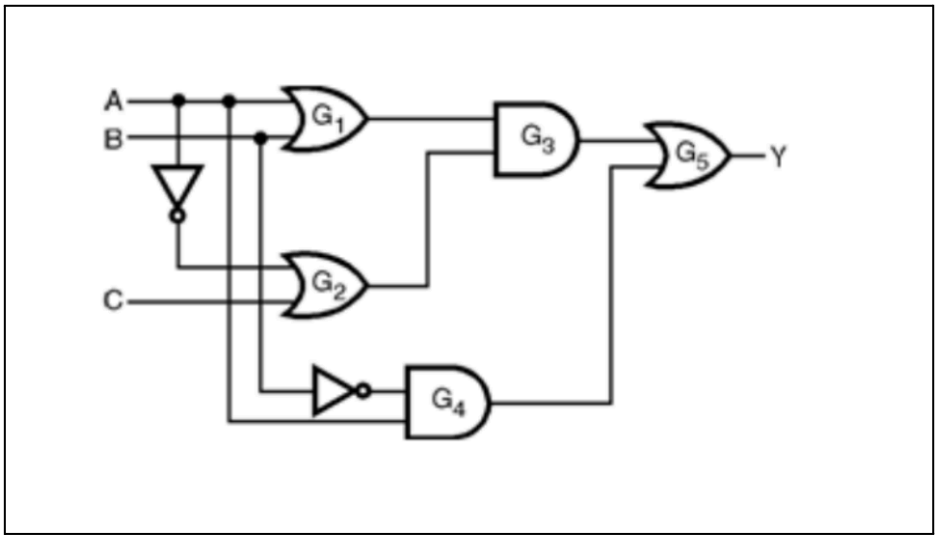
IITGN

Digital Systems
LAB -7

Question: Implement the following circuit in Verilog in such a way that all the hazards can be viewed. Write the testbench such that all the static and dynamic hazards in the following circuit can be shown on the simulator. You can use appropriate delay values.



Verilog Code without Delays

```
`timescale 1ns / 1ps

module Hazard(A,B,C,out);
input A,B,C;
output out;
or G1(g1,A,B);
not N1(n1,A);
or G2(g2,n1,C);
and G3(g3, g1,g2);
not  N2(n2,B);
and G4(g4,n2,A);
or G5(out,g3,g4);
endmodule
```

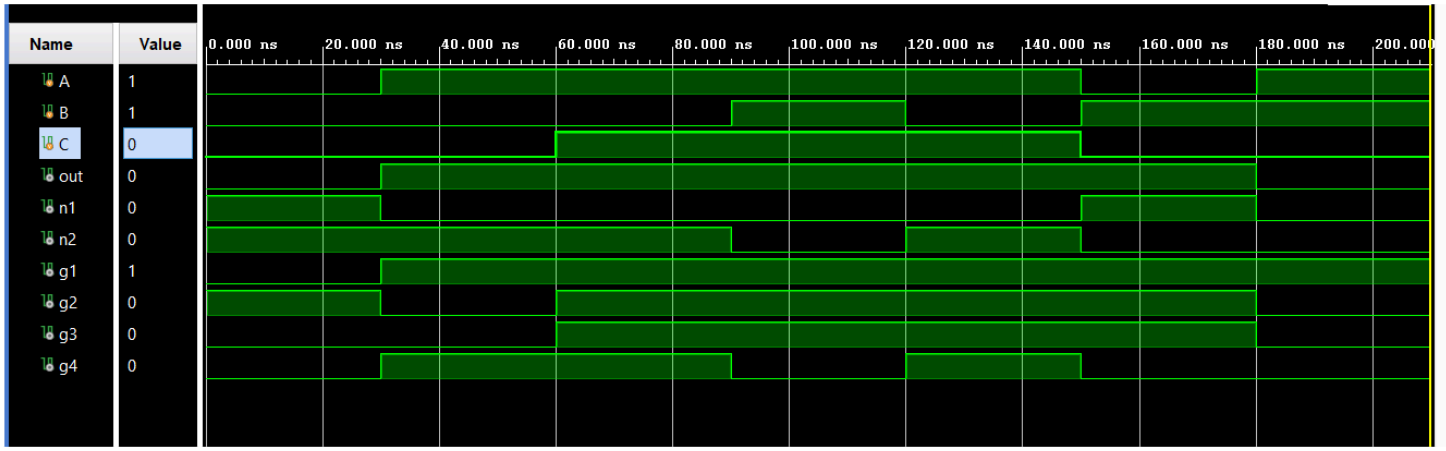
Verilog Code with delays added to NOT gates

```
`timescale 1ns / 1ps

module Hazard(A,B,C,out);
input A,B,C;
output out;
or G1(g1,A,B);
not #2  N1(n1,A);
or G2(g2,n1,C);
and G3(g3, g1,g2);
not #2 N2(n2,B);
and G4(g4,n2,A);
or G5(out,g3,g4);
endmodule
```

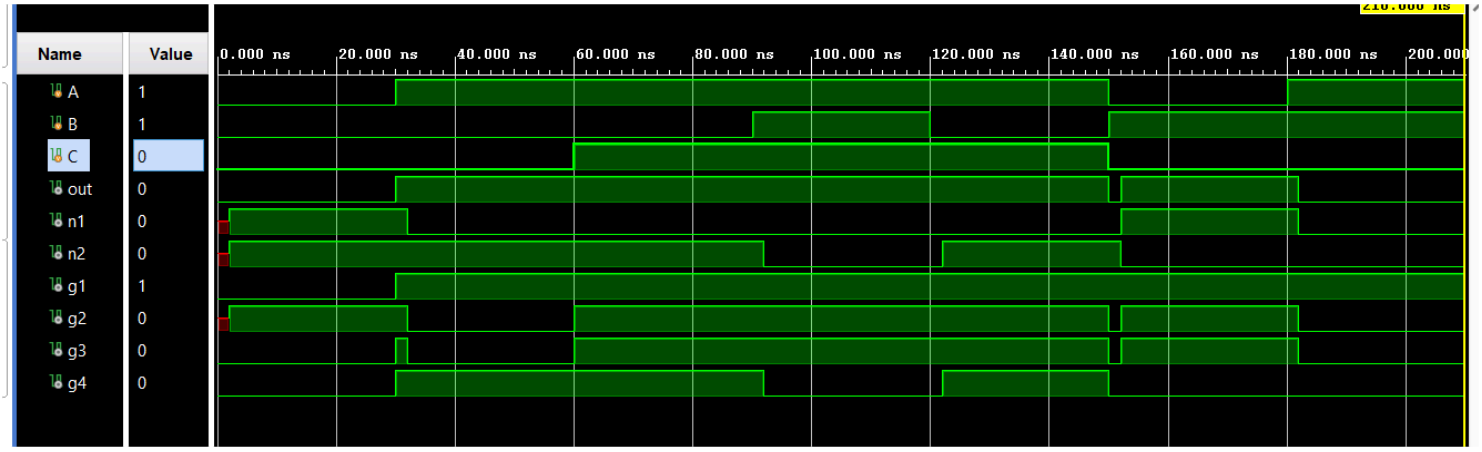
Test bench

```
`timescale 1ns / 1ps

module test();
reg A,B,C;
wire out;

Hazard uut(A,B,C,out);
initial
begin
    A=0;B=0;C=0;#30
    A=1;B=0;C=0;#30
    A=1;B=0;C=1;#30
    A=1;B=1;C=1;#30

    A=1;B=0;C=1;#30
    A=0;B=1;C=0;#30
    A=1;B=1;C=0;#30


$finish();
end
endmodule
```

Simulation without Hazard



Simulation with Hazard



We can see static-1 hazard at the output when we change two bits at a time from 101 → 010.
We can see a static - 0 hazard at g3 when only one bit changes from 000 → 100. Note that this hazard is not seen at output but in the internal wire g3.