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IITGN

Digital Systems
LAB Assignment 3

Question 1) For each of the questions, write a Verilog code. You also need to create a testbench and show the simulation results.

Design a 4-bit combined BCD/Binary Up/Down counter using Structural code. Use Toggle FFs for designing this synchronous counter.

The counter outputs are connected to a 4-bit Shift register. The shift register allows no-shift/left-shift/right-shift operations. The shifter code needs to be written as Behavioral code.
Write a top_module that instantiates counter and shift register appropriately with all the mode bits to allow selection of counter mode and shift mode.

T-Flip Flop

```
`timescale 1ns / 1ps
module T_ff(input T,input reset,input preset,input clk,output reg Qout);
always @(posedge clk or reset or preset)
    begin
        if(reset)
            Qout=0;
        else if(preset)
            Qout=1;
        else
            if(T)
                Qout <= ~Qout;
            else
                Qout <= Qout;
    end
endmodule
```

4bit-Counter

```
`timescale 1ns / 1ps
module BCD_counter(clk,en, reset, Mode, Q[3:0]);
input clk,reset,Mode,en;
output [3:0]Q;

T_ff inst1 (1&en, clk, reset| (Mode&(Q[0] & Q[3])), (Mode&((Q[0]|Q[1]|Q[2]|Q[3]))),  Q[0]);
T_ff inst2((Mode^Q[0])&en, clk, reset | (Mode&(Q[0]&Q[3])) | (Mode&((Q[0]|Q[1]|Q[2]|Q[3]))) , 0, Q[1]);
T_ff inst3(((Mode^Q[1])&(Mode^Q[0])&en),clk, reset | (Mode&(Q[0]&Q[3])) | (Mode&((Q[0]|Q[1]|Q[2]|Q[3]))) , 0, Q[2]);
T_ff inst4(((Mode^Q[2])&(Mode^Q[1])&(Mode^Q[0])&en),clk, reset | (Mode&(Q[0]&Q[3])) | (Mode&((Q[0]|Q[1]|Q[2]|Q[3]))) , 0,Q[3]);


endmodule
```

Shifter

```
`timescale 1ns / 1ps


module Shifter (clk,Qin[3:0],en,reset,Mode[1:0],Qout[3:0]);

input [3:0] Qin;
input clk,en,reset;
input [1:0]Mode;
output reg [3:0]Qout;

    always @(posedge clk)
    begin
        if (reset)
            Qout = 0;
        else if(en==1) begin
            if(Mode==0)
                Qout <= Qin;
            else if(Mode==1)
                Qout <= (Qout << 1);
            else
                Qout <= (Qout >> 1);
         end

         else
            Qout = Qin;
    end



endmodule
```

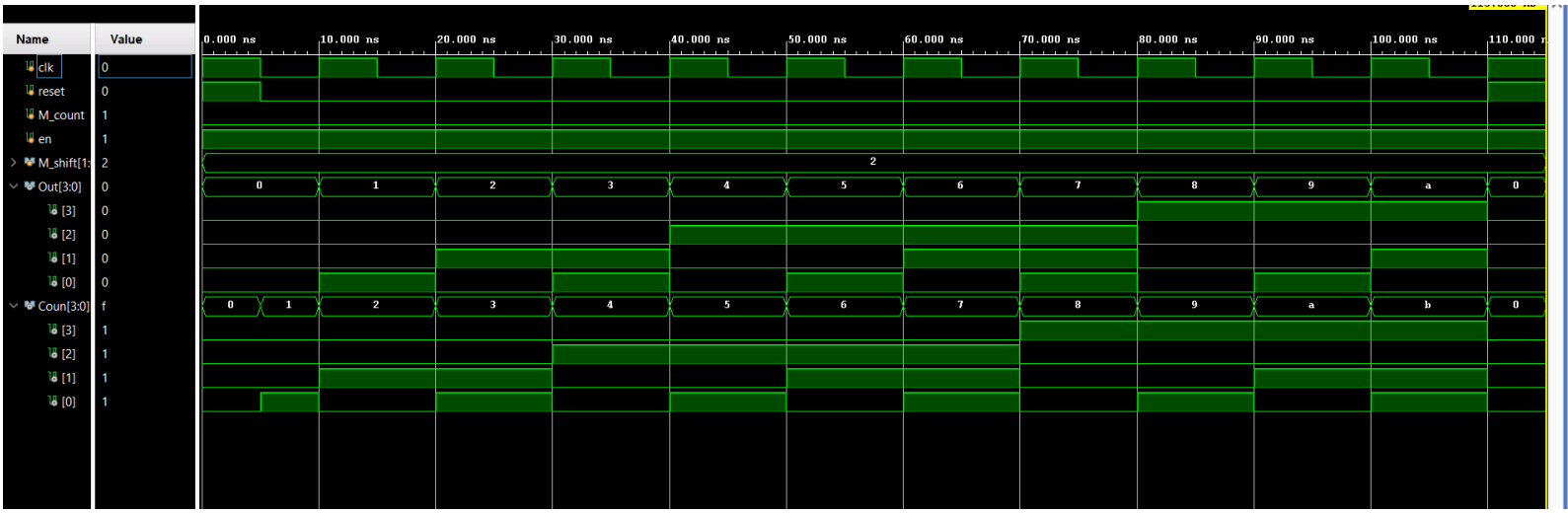
Top Module

```
`timescale 1ns / 1ps
module top_module(clk , en, reset, Mode_count, Mode_shift[1:0], Counter[3:0], Out[3:0]);

input clk,en,reset,Mode_count;
input [1:0]Mode_shift;
output [3:0] Counter, Out;

BCD_counter coun(clk,en,reset,Mode_count,Counter);
Shifter shift (clk,Counter, ~en, reset, Mode_shift,Out);

endmodule
```

Test Bench

```
1   `timescale 1ns / 1ps
2
3
4
5   module Counter4bit_tb;
6   reg clk,rst;
7   wire [3:0] count;
8
9   Counter4bit uut(
10      .clk(clk),
11
12      .rst(rst),
13
14      .count(count)
15  );
16
17  initial begin
18      clk=0;
19      forever #5 clk=~clk;
20  end
21
22  initial begin
23      rst=1;
24
25      #10 rst=0;
26      rst=0;
27      #200
28  $finish();
29  end
30
31  endmodule
```

Simulation



RTL Analysis
Schematics