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IITGN

Digital Systems
LAB 4

Question 1) Design a 4-bit Asynchronous counter with reset using structural code. You need to design a Toggle FF module using procedural statement (always @).

T-Flip Flop

```
`timescale 1ns / 1ps

module Toggle_FF(
input wire clk,
input wire T,
input wire rst,
output reg out
);

always @(posedge clk or posedge rst)
begin
if(rst)
    out<=1'b0;
else
    if(T)
        out<=~out;
    else
        out = out;

end

endmodule
```

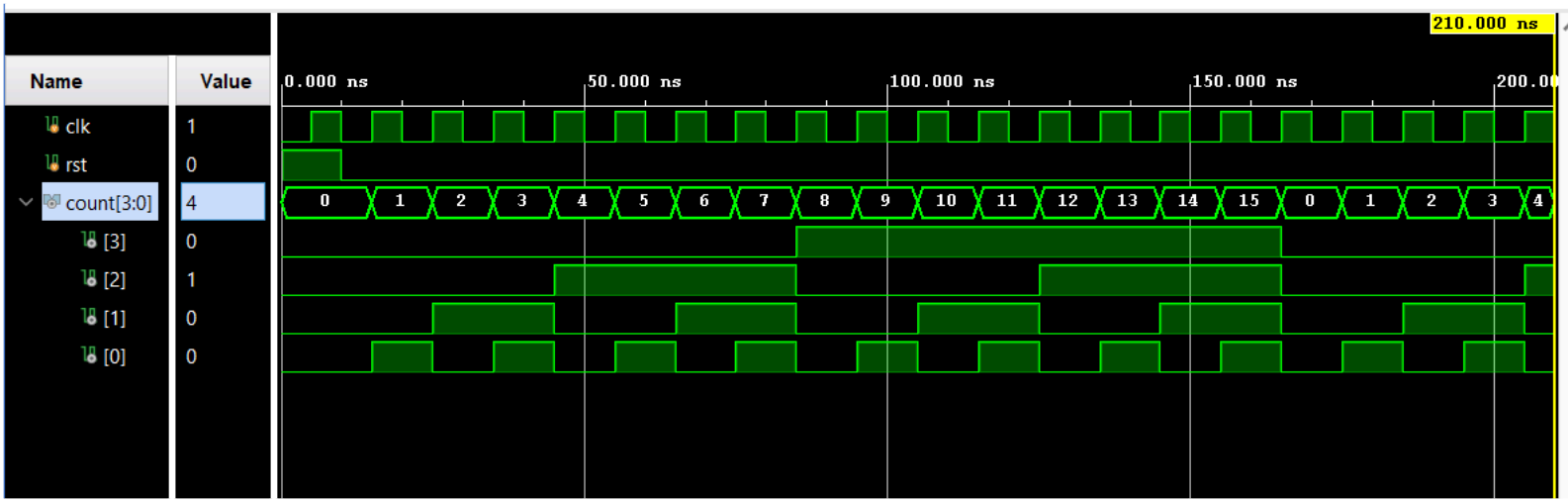
4bit-Counter

```
1   `timescale 1ns / 1ps
2
3
4
5   module Counter4bit(
6   input wire clk,
7   input wire rst,
8   input wire T,
9   output reg [3:0] count
10  );
11  wire [3:0] toggle;
12
13  Toggle_FF ff0(.clk(clk),.T(1) ,.rst(rst), .out(toggle[0]));
14  Toggle_FF ff1(.clk(~toggle[0]), .T(1),.rst(rst), .out(toggle[1]));
15  Toggle_FF ff2(.clk(~toggle[1]), .T(1),.rst(rst), .out(toggle[2]));
16  Toggle_FF ff3(.clk(~toggle[2]), .T(1),.rst(rst), .out(toggle[3]));
17
18  always @(*)
19  begin
20      count = toggle;
21  end
22  endmodule
23
```

Test Bench

```
1   `timescale 1ns / 1ps
2
3
4
5   module Counter4bit_tb;
6   reg clk,rst;
7   wire [3:0] count;
8
9   Counter4bit uut(
10      .clk(clk),
11
12      .rst(rst),
13
14      .count(count)
15  );
16
17  initial begin
18      clk=0;
19      forever #5 clk=~clk;
20  end
21
22  initial begin
23      rst=1;
24
25      #10 rst=0;
26      rst=0;
27      #200
28  $finish();
29  end
30
31  endmodule
```

Simulation


Name
Value
clk
1
rst
0
count[3:0]
4
[3]
0
[2]
1
[1]
0
[0]
0
0.000 ns
50.000 ns
100.000 ns
150.000 ns
210.000 ns
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4