भारतीय प्रौद्योगिकी संस्थान गांधीनगर
पालज, गांधीनगर, गुजरात 382 055
INDIAN INSTITUTE OF TECHNOLOGY GANDHINAGAR
PALAJ, GANDHINAGAR, GUJARAT 382 055

Name : Bhavik Patel
Roll no. : 22110047

IITGN

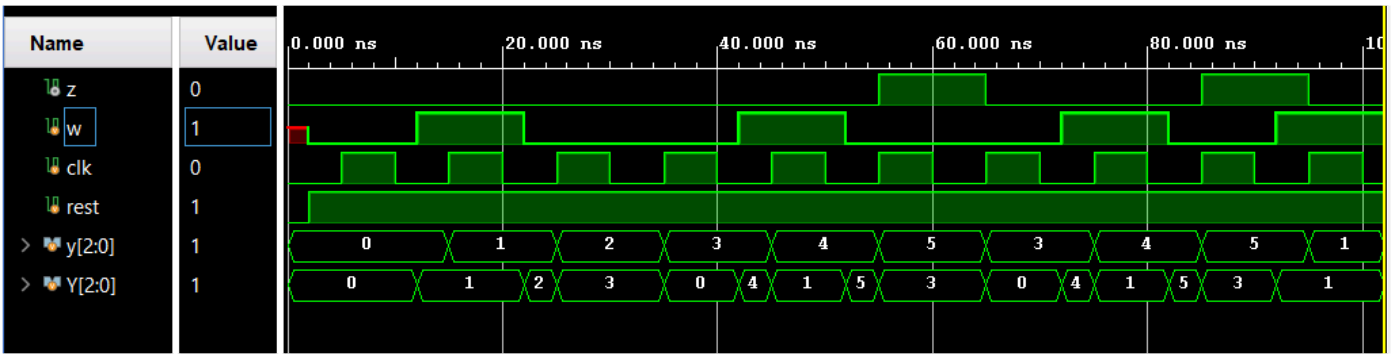
Digital Systems
LAB -10

Question:
Implement a Moore and Mealy machine that can detect 10010. The FSM has one input and one output. Show the implemented designs on FPGA. The pattern should be given through a switch and the output should be shown on the LED (which can turn on when the pattern is detected).

Moore Machine Verilog Code

```
`timescale 1ns / 1ps
module Moore_10010(clk,rest,w,z);
input clk,rest,w;
output z;
reg [2:0]y,Y;

parameter [2:0]A=3'b000,B=3'b001,C=3'b010,D=3'b011,E=3'b100,F=3'b101;

//Define the next state combinational logic
always @(w or y)
    case(y)
        A: if(w) Y=B;
            else Y=A;
        B: if(w) Y=B;
            else Y=C;
        C: if(w) Y=B;
            else Y=D;
        D: if(w) Y=E;
            else Y=A;
        E: if(w) Y=B;
            else Y=F;
        F: if(w) Y=B;
            else Y=D;
        default: Y=2'bxx;
    endcase


//Define sequential block
always @(negedge rest or posedge clk)
    if(rest==0)
        y<=A;
    else
        y<=Y;

    //Define output
    assign z=(y[0] && (~y[1]) && y[2]);

endmodule
```

Simulation of Moore Machine



FPGA Implementation:

Link to⟶Video

Reports:

```
Timing Report

Slack:                    inf
  Source:                 y_reg[0]/C
                            (rising edge-triggered cell FDCE)
  Destination:            z
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        7.945ns  (logic 4.085ns (51.413%)  route 3.860ns (48.587%))
  Logic Levels:           3  (FDCE=1 LUT3=1 OBUF=1)
```

On-Chip	Power (W)	Used	Available	Utilization (%)
Slice Logic	0.053	48	---	---
LUT as Logic	0.019	4	20800	0.02
CARRY4	0.016	7	8150	0.09
Register	0.013	31	41600	0.07
BUFG	0.006	1	32	3.13
Others	0.000	3	---	---
Signals	0.095	43	---	---
I/O	0.905	5	106	4.72
Static Power	0.074			
Total	1.127			

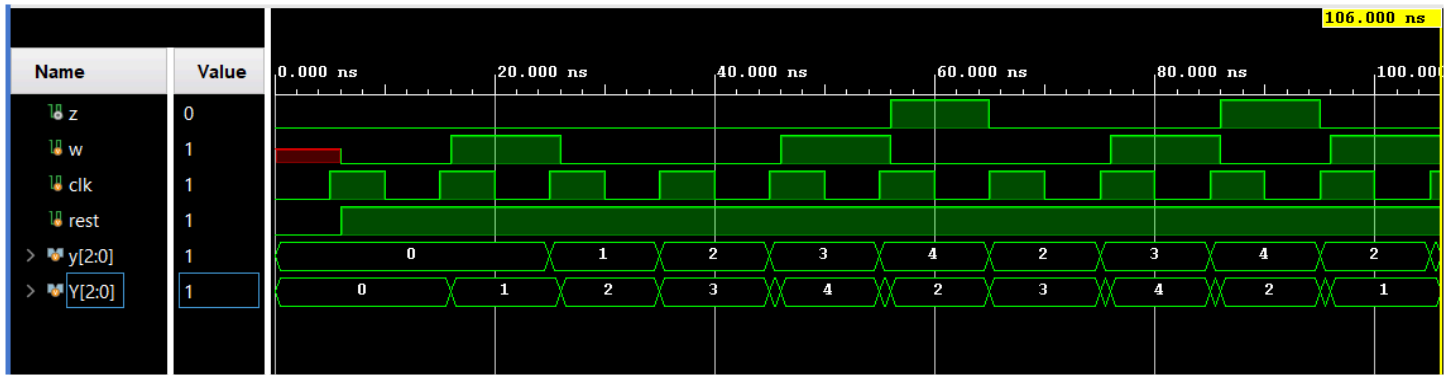
1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs	4	0	20800	0.02
LUT as Logic	4	0	20800	0.02
LUT as Memory	0	0	9600	0.00
Slice Registers	31	0	41600	0.07
Register as Flip Flop	31	0	41600	0.07
Register as Latch	0	0	41600	0.00
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

Mealy Machine Verilog Code

```
`timescale 1ns / 1ps
module Mealy_10010(clk,rest,w,z);
input clk,rest,w;
output reg z;
reg [2:0]y,Y;

parameter [2:0]A=3'b000,B=3'b001,C=3'b010,D=3'b011,E=3'b100;

//Define the next state combinational logic
always @(w or y)    begin
    case(y)
        A: if(w) begin
            Y=B;z=0;
         end
        else begin
            Y=A;z=0;
        end
        B: if(w) begin
            Y=B;z=0;
         end
        else begin
            Y=C;z=0;
        end
        C: if(w) begin
            Y=B;z=0;
         end
        else begin
            Y=D;z=0;
        end
        D: if(w) begin
            Y=E;z=0;
         end
        else begin
            Y=A;z=0;
        end
        E: if(w) begin
            Y=B;z=0;
         end
        else begin
            Y=C;z=1;
        end
        default:begin Y=2'bxx; z=0; end
    endcase
end

//Define sequential block
always @(negedge rest or posedge clk)
    if(rest==0) begin
        y<=A;z=0; end
    else
        y<=Y;
endmodule
```

Simulation for Mealy Machine



FPGA Implementation:

Link to → Video

Reports

On-Chip	Power (W)	Used	Available	Utilization (%)
Slice Logic	0.064	48	---	---
LUT as Logic	0.029	4	20800	0.02
CARRY4	0.016	7	8150	0.09
Register	0.013	31	41600	0.07
BUFG	0.006	1	32	3.13
Others	0.000	3	---	---
Signals	0.095	43	---	---
I/O	0.850	5	106	4.72
Static Power	0.074			
Total	1.083			

```
Timing Report

Slack:                    inf
  Source:                 inst2/counter_reg[27]/C
                            (rising edge-triggered cell FDRE)
  Destination:            slow_clk
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        8.790ns  (logic 4.039ns (45.955%)  route 4.751ns (54.045%))
  Logic Levels:           2  (FDRE=1 OBUF=1)
```

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs	4	0	20800	0.02
LUT as Logic	4	0	20800	0.02
LUT as Memory	0	0	9600	0.00
Slice Registers	31	0	41600	0.07
Register as Flip Flop	31	0	41600	0.07
Register as Latch	0	0	41600	0.00
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

Test bench

For Moore Machine

```
`timescale 1ns / 1ps
module test_tb();
wire z;
reg w,clk,rest;

Moore_10010 uut(clk,rest,w,z);
initial
begin
clk=0;
    forever #5 clk=~clk;
end

initial
begin
rest=0;
#2 rest=1;
w=0;#10
w=1;#10
w=0;#10
w=0;#10
w=1;#10
w=0;#10
w=0;#10
w=1;#10
w=0;#10
w=1;#10
$finish();
end
endmodule
```

For Mealy Machine

```
`timescale 1ns / 1ps
module test_tb();
wire z;
reg w,clk,rest;

Mealy_10010 uut(clk,rest,w,z);
initial
begin
clk=0;
    forever #5 clk=~clk;
end

initial
begin
rest=0;
#6 rest=1;
w=0;#10
w=1;#10
w=0;#10
w=0;#10
w=1;#10
w=0;#10
w=0;#10
w=1;#10
w=0;#10
w=1;#10
$finish();
end
endmodule
```