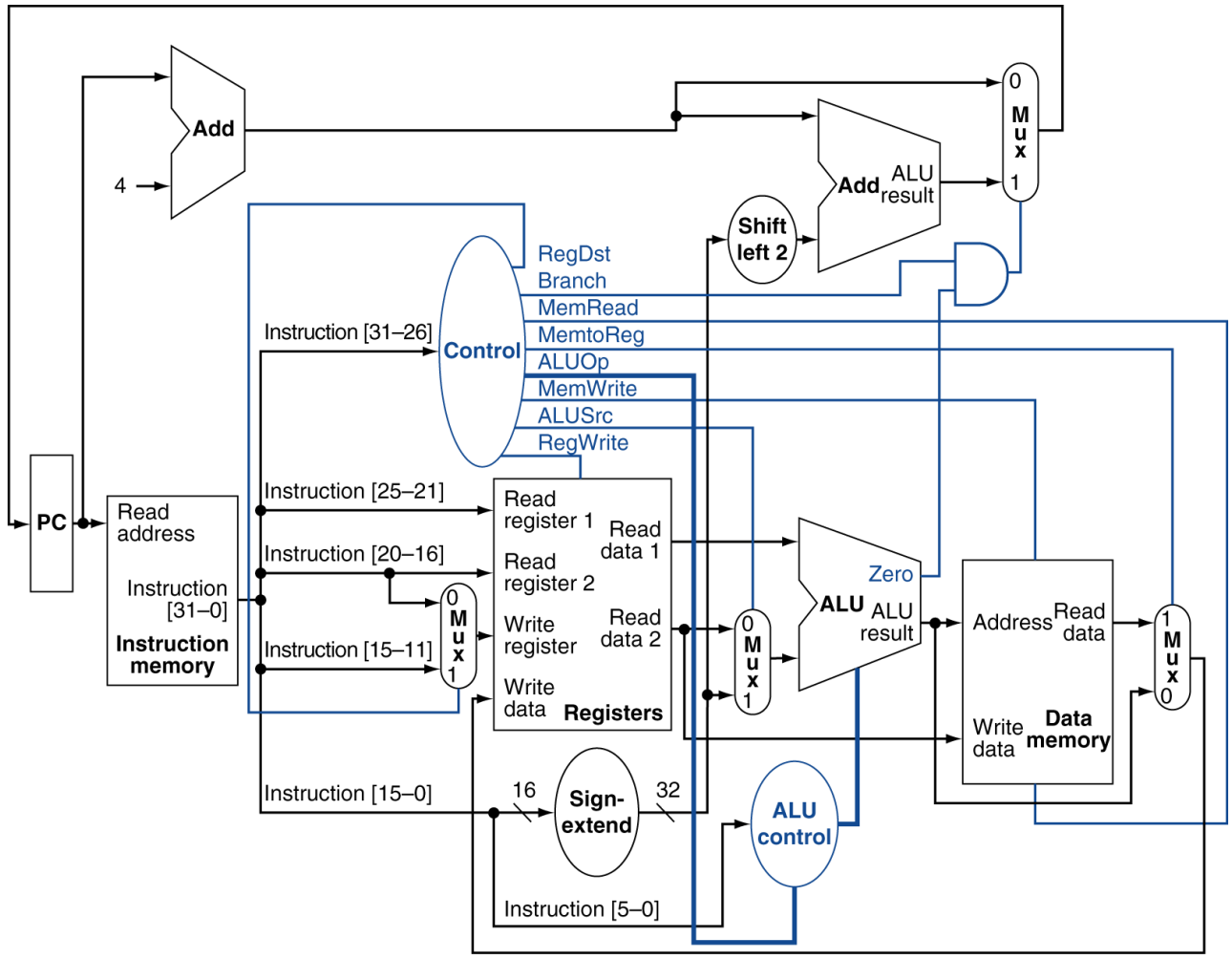

For the MIPS single cycle datapath, complete the following control table with entries 0, 1, or X for don't care.

	add	and	lw	sw	beq	addi
RegDst						
Branch						
MemRead						
MemtoReg						
ALUOp						
MemWrite						
ALUSrc						
RegWrite						