Brian Phan

Homework 09   88, 190

5.2)   3, 180, 43, 2, 191, 14, 181, 44, 186, 253

5.2.2)

Address(word)		Tag(cache)	Index	Cache	H/M
3	0x00000000 ... 00011	0x0000...000	001	1	M
180	0x00...000001011010|0|	0x00...1011	010	2	M
43	0x000. 000010101|1|	0x000...010	101	5	M
2	0x000....0000000010	0x000...000	001	1	H
191	0x000...0001011 111|1|	0x000...01011	111	7	M
88	0x000...00001 01100|0|	0x000...0101	100	4	M
190	0x000...0001011 111 |0|	0x00..01011	111	7	H
14	0x000...00000 111 |0|	0x00...000	111	7	M
181	0x000 ...0001011 010|1|	0x00...01011	010	2	H
44	0x000...00010 110|0|	0x000...010	110	6	M
186	0x00...00001011 101|0|	0x000...01011	101	5	M
253	0x000...00001111 110|1|	0x00...01111	110	6	M

5.3.1) $2^{offset} = 2^5 / 2^2 = 8 \text{ words}$

5.3.2) $2^{index} = 2^5 = 32 \text{ lines}$

5.6.1) Clock Rate = 1/(L1 Hit)

   P1 : 1/0.66 ns = 1.51 GHz

   P2 : 1/0.90 ns = 1.11 GHz

5.6.2) Avg Mem Access Time = Hit Rate · Hit Time + Miss Rate · Miss Time

   P1 :   6.21 ns = 92%(0.66ns) + 8%(70ns)

   P2   5.05 ns = 94%(0.90 ns) + 6%(70ns)

5.13.1)   0   2   4   8   10   12   14   16   0

M ————————————————————→

LRU   [0 Hits]

0   ~~10~~   0

2   12

4   14

8   16

5.13.2)   0   2   4   8   10   12   14   16   0

                                                H

MRU   [1 HIT]

0 —

2

4

~~8~~ ~~10~~ ~~12~~ ~~14~~ 16