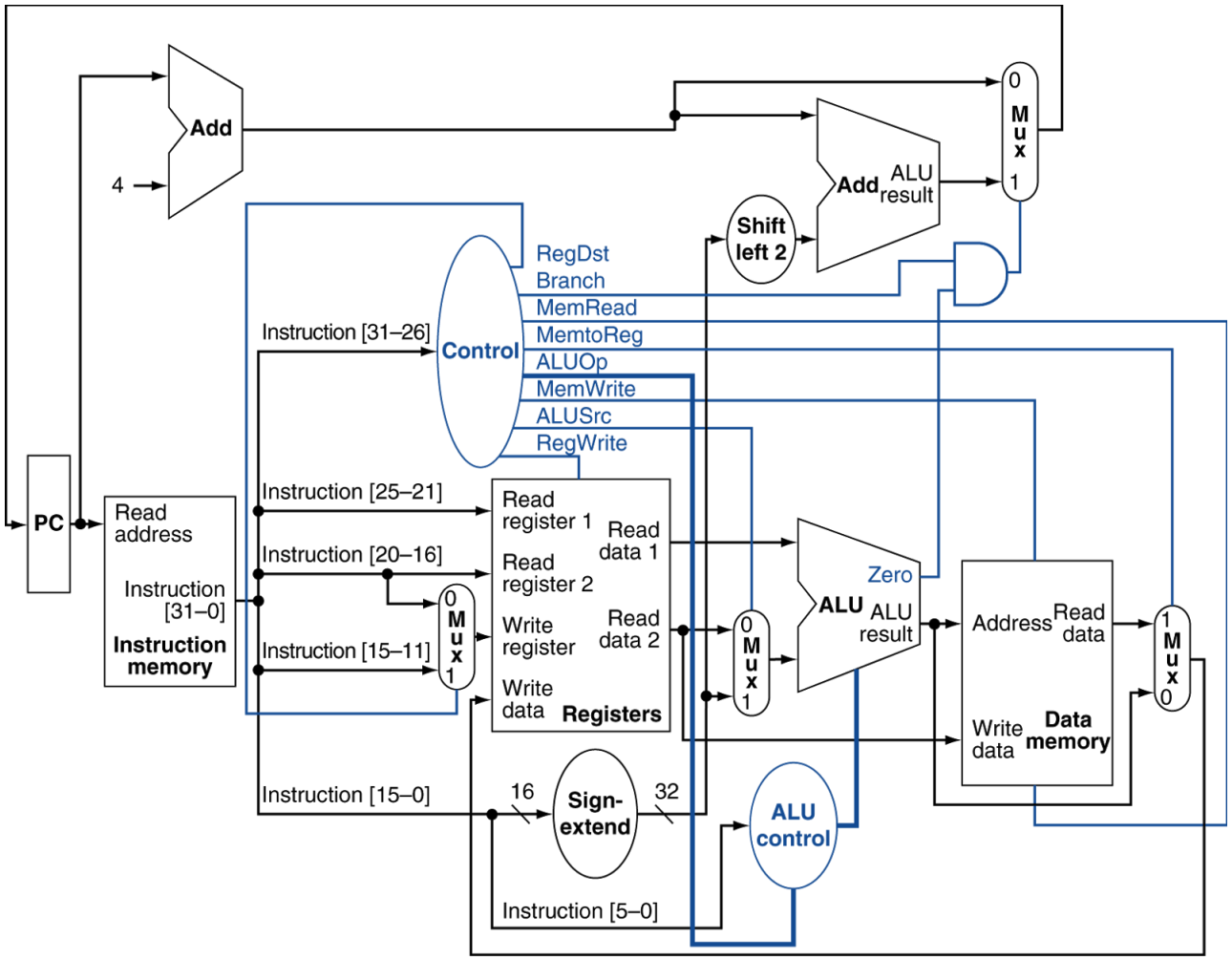
Add
4
0
M
u
x
1
Add
ALU result
Shift left 2
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Instruction [31–26]
Control
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
16
Sign-extend
32
ALU control
Zero
ALU
ALU result
Address
Read data
Write data
Data memory

For the MIPS single cycle datapath, complete the following control table with entries 0, 1, or X for don't care.

	add	and	lw	sw	beq	addi
RegDst	1	1	0	X	X	0
Branch	0	0	0	0	1	0
MemRead	0	0	1	0	0	0
MemtoReg	0	0	1	X	X	0
ALUOp	add	and	add	add	sub	add
MemWrite	0	0	0	1	0	0
ALUSrc	0	0	1	1	0	1
RegWrite	1	1	1	0	0	1