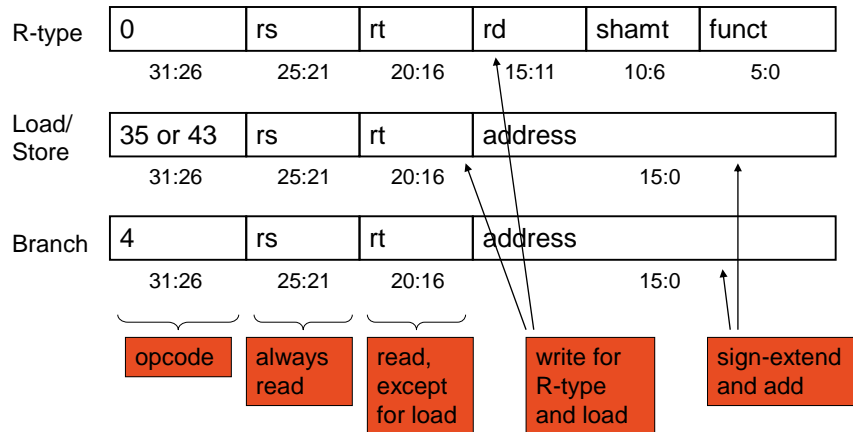


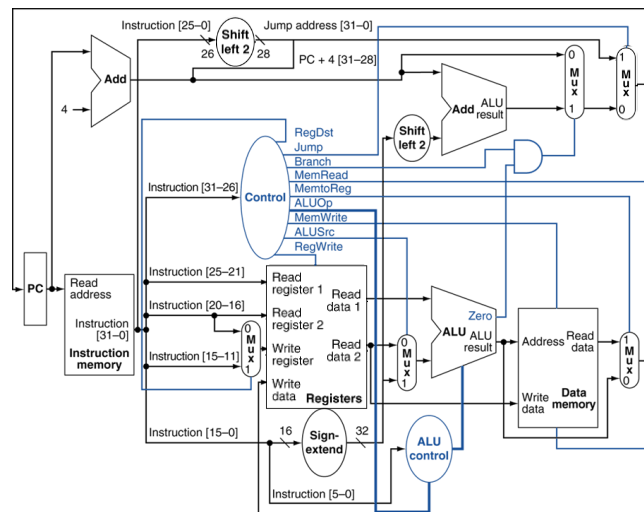
The Main Control Unit

Control signals derived from instruction



CSULB

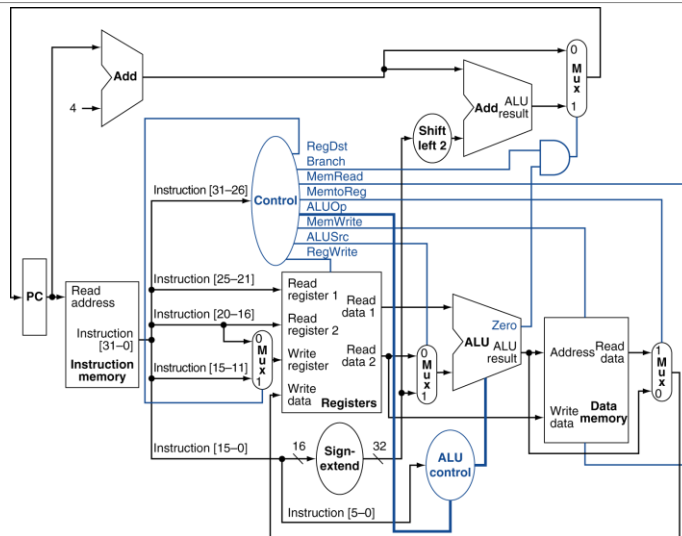
Datapath With Control



CSULB

R-Type Instruction

R-type	0	rs	rt	rd	shamt	funct
	31:26	25:21	20:16	15:11	10:6	5:0

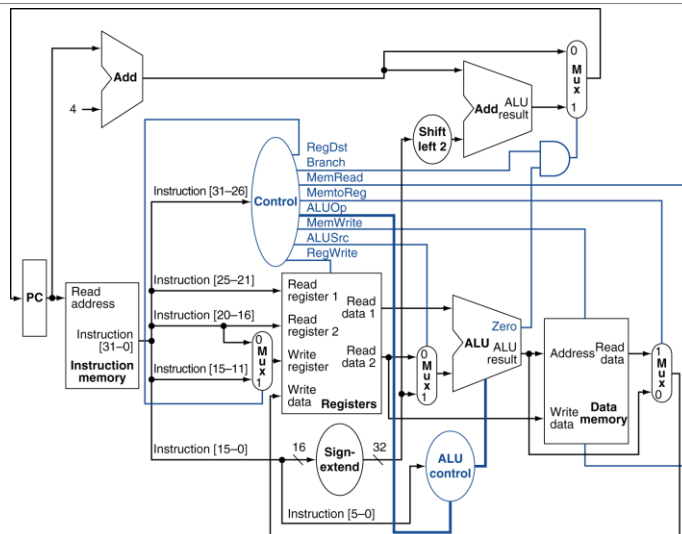


	add	and
RegDst	1	1
Branch	0	0
MemRead	0	0
MemtoReg	0	0
ALUOp	add	and
MemWrite	0	0
ALUSrc	0	0
RegWrite	1	1

CSULB

lw/sw Instruction

Load/Store	35 or 43	rs	rt	address
	31:26	25:21	20:16	15:0



	lw	sw
RegDst	0	X
Branch	0	0
MemRead	1	0
MemtoReg	1	X
ALUOp	add	add
MemWrite	0	1
ALUSrc	1	1
RegWrite	1	0

CSULB