**Control Signals**

PC Logic Controls:

PCtoReg: JAL, JALR

RegToPC: JALR, JR

Jump: J, JAL, JR, JALR

branchZero: BEQZ

branch: BEQZ, BNEZ

Register Controls:

RegDst: Replaced by RType

RegWrite: Replaced by RType

RType: (new control signal, combines 3 existing ones on the datapath) 1 for R-Type Instructions

Data MEmory Controls:

DSize[0]: LW, SW

DSize[1]: LW, SW, LH, SH, LHU

MemToReg: LW, LH, LHU, LB, LBU

MemWrite: SH, SW, SB

ALU Operation/Execution Stage Controls:

ALUCtrl: SEE SEPARATE DOCUMENT

Mul: MULT, MULTU

extOp: 0 for unsigned instructions (MULTU, ADDU, ADDIU, SUBU, etc)

LHIOp: LHI

ALUSrc: No longer exists, now uses the RType control signal

Notes:

* “branch” has replaced “branchOrJmp” on our datapath
* RegWrite, ALUSrc have been combined and called RType
* Terminals of mux have been flipped for mux that had ALUSrc as selector (since a 1 means an R-Type instruction)