V1743
Registers
Description

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MOD. V1743

16 CHANNEL 12 BIT
3.2 GS/S DIGITIZER

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Change Document Record

Date	Revision	Changes
06 March 2015	00	Initial release
02 February 2016	01	Updated § **1.7**, § **1.8**, § **1.42**. Added § **1.49**

1. VME Interface

The following sections describe in detail the content of the accessible V1743 and VX1743 digitizer registers.

Table 1.1: VME64 and VME64X x743 versions

Board Model	Description
V1743	16 Ch. 12 bit 3.2GS/s Switched-Capacitor Digitizer: 7 events/ch (1kS/event), EP3C16, SE
VX1743	16 Ch. 12 bit 3.2GS/s Switched-Capacitor Digitizer: 7 events/ch (1kS/event), EP3C16, SE

Note: Because of its architecture, each SAMLONG chip manages two adjacent input channels which are referred to as a group. Basing on that, the settings of those registers in this document whose name begins with “Group n”, apply to a 2-channel group. For the V1743, the index “n” can be 0 (channel 0 and 1), 1 (channels 2 an 3), 2 (channels 4 and 5), 3 (channels 6 and 7), 4 (channels 8 and 9), 5 (channels 10 and 11), 6 (channels 12 and 13), 7 (channels 14 and 15).

Note: Bit fields that are not described in the register bit map are reserved and must not be over written by the User.

For a detailed description of the V1743 hardware and principle of operating, please refer to the digitizer User Manual that is web available.

1.1. Registers address map

Table 1.2: Address Map for the Model V1743

REGISTER NAME	ADDRESS	ASIZE	DSIZE	MODE	H_RES	S_RES	CLR
EVENT READOUT BUFFER	0x0000-0x0FFC	A24/A32/A64	D32	R	X	X	X
Group n EEPROM ACCESS	0x1n0C	A24/A32	D32	R/W			
Group n TEST	0x1n24	A24/A32	D32	R/W	X	X	
Group n SAM DATA	0x1n28	A24/A32	D32	R/W	X	X	
Group n PULSE ENABLE	0x1n2C	A24/A32	D32	R/W	X	X	
Group n POSTTRIGGER	0x1n30	A24/A32	D32	R/W	X	X	
Group n PULSE PATTERN	0x1n34	A24/A32	D32	R/W	X	X	
Group n TRIGGER GATE	0x1n38	A24/A32	D32	R/W	X	X	
Group n TRIGGER	0x1n3C	A24/A32	D32	R/W	X	X	
Group n SAMPLING FREQUENCY	0x1n40	A24/A32	D32	R/W	X	X	
Group n RECORDING DEPTH	0x1n44	A24/A32	D32	R/W	X	X	
Group n CHARGE THRESHOLD	0x1n48	A24/A32	D32	R/W	X	X	
Group n DAC SPI DATA	0x1n54	A24/A32	D32	R/W	X	X	
Group n CHARGE REFERENCE CELL	0x1n58	A24/A32	D32	R/W	X	X	
Group n CLEAR EVENT FIFOS	0x1n5C	A24/A32	D32	W			
Group n FIFO FLAGS STATUS	0x1n60	A24/A32	D32	R	X	X	
Group n FCR STATUS	0x1n68	A24/A32	D32	R	X	X	
Group n RATE COUNTERS Ch0	0x1n6C	A24/A32	D32	R	X	X	
Group n EEPROM WRITE PROTECT	0x1n78	A24/A32	D32				
Group n CHARGE LENGTH	0x1n80	A24/A32	D32	R/W	X	X	
Group n SAM ADDRESS	0x1n84	A24/A32	D32	R/W	X	X	
DAUGHTERBOARD FW REVISION	0x1n8C	A24/A32	D32	R			
Group n RATE COUNTERS Ch1	0x1n94	A24/A32	D32	R	X	X	
CHANNEL CONFIGURATION	0x8000	A24/A32	D32	R/W	X	X	
CHANNEL CONFIGURATION BIT SET	0x8004	A24/A32	D32	W			
CHANNEL CONFIGURATION BIT CLEAR	0x8008	A24/A32	D32	W			
GROUP RESET FRONT END FPGA	0x8010	A24/A32	D32	R/W			
GROUP ARM ACQUISITION	0x8018	A24/A32	D32	W			
GROUP PULSE_CHANNELS	0x801C	A24/A32	D32	W			
GROUP CONTROL	0x8070	A24/A32	D32	R/W	X	X	

REGISTER NAME	ADDRESS	ASIZE	DSIZE	MODE	H_RES	S_RES	CLR
GROUP PRETRIGGER	0x8074	A24/A32	D32	R/W	X	X	
GROUP RESET_SAM	0x807C	A24/A32	D32	W			
ACQUISITION CONTROL	0x8100	A24/A32	D32	R/W	X	X	
ACQUISITION STATUS	0x8104	A24/A32	D32	R			
SW TRIGGER	0x8108	A24/A32	D32	W			
TRIGGER SOURCE ENABLE MASK	0x810C	A24/A32	D32	R/W	X	X	
FRONT PANEL TRIGGER OUT ENABLE MASK	0x8110	A24/A32	D32	R/W	X	X	
FRONT PANEL I/O DATA	0x8118	A24/A32	D32	R/W	X	X	
FRONT PANEL I/O CONTROL	0x811C	A24/A32	D32	R/W	X	X	
CHANNEL ENABLE MASK	0x8120	A24/A32	D32	R/W	X	X	
ROC FPGA FIRMWARE REVISION	0x8124	A24/A32	D32	R			
EVENT STORED	0x812C	A24/A32	D32	R	X	X	X
SET MONITOR DAC	0x8138	A24/A32	D32	R/W	X	X	
SW CLK SYNC	0x813C	A24/A32	D32	W			
BOARD INFO	0x8140	A24/A32	D32	R			
MONITOR DAC MODE	0x8144	A24/A32	D32	R/W	X	X	
EVENT SIZE	0x814C	A24/A32	D32	R	X	X	X
MEMORY BUFFER ALMOST FULL LEVEL	0x816C	A24/A32	D32	R/W	X	X	
RUN START STOP DELAY	0x8170	A24/A32	D32	R/W	X	X	
BOARD FAIL STATUS	0x8178	A24/A32	D32	R	X	X	
FRONT PANEL LVDS I/O NEW FEATURES	0x81A0	A24/A32	D32	R/W	X	X	
VME CONTROL	0xEF00	A24/A32	D32	R/W	X		
VME STATUS	0xEF04	A24/A32	D32	R			
BOARD ID	0xEF08	A24/A32	D32	R/W	X	X	
MULTICAST BASE ADDRESS & CONTROL	0xEF0C	A24/A32	D32	R/W	X		
RELOCATION ADDRESS	0xEF10	A24/A32	D32	R/W	X		
INTERRUPT STATUS ID	0xEF14	A24/A32	D32	R/W	X		
INTERRUPT EVENT NUMBER	0xEF18	A24/A32	D32	R/W	X	X	
BLT EVENT NUMBER	0xEF1C	A24/A32	D32	R/W	X	X	
SCRATCH	0xEF20	A24/A32	D32	R/W	X	X	
SW RESET	0xEF24	A24/A32	D32	W			
SW CLEAR	0xEF28	A24/A32	D32	W			

REGISTER NAME	ADDRESS	ASIZE	DSIZE	MODE	H_RES	S_RES	CLR
CONFIGURATION RELOAD	0xEF34	A24/A32	D32	W			
CONFIGURATION ROM	0xF000-0xF088	A24/A32	D32	R			

1.2. Configuration ROM (0xF000-0xF088; r)

The following registers contain some module's information (D32 accessible, read only):

- **OUI**: manufacturer identifier (IEEE OUI)
- **Version**: purchased version
- **Board ID**: Board identifier
- **Revision**: hardware revision identifier
- **Serial MSB**: serial number (MSB)
- **Serial LSB**: serial number (LSB)

Table 1.3: ROM Address Map for the Model V1743

Description	Address	Bits	Content
checksum	0xF000	[7:0]	0xA4
checksum_length2	0xF004	[7:0]	0x00
checksum_length1	0xF008	[7:0]	0x00
checksum_length0	0xF00C	[7:0]	0x20
constant2	0xF010	[7:0]	0x83
constant1	0xF014	[7:0]	0x84
constant0	0xF018	[7:0]	0x01
c_code	0xF01C	[7:0]	0x43
r_code	0xF020	[7:0]	0x52
oui2	0xF024	[7:0]	0x00
oui1	0xF028	[7:0]	0x40
oui0	0xF02C	[7:0]	0xE6
vers	0xF030	[7:0]	V1743: A0
form factor	0xF034	[7:0]	VME64 boards: 0x00 VME64X boards: 0x01
boarID1	0xF038	[7:0]	0x16
boarID0	0xF03C	[7:0]	0x6F
revis3	0xF040	[31:0]	0x00
revis2	0xF044	[31:0]	0x00
revis1	0xF048	[31:0]	0x00
revis0	0xF04C	[7:0]	0x01
FLASH type	0xF050	[7:0]	0x01
sernum1	0xF080	[7:0]	0x00
sernum0	0xF084	[7:0]	0x16
VCXO type	0xF088	[31:0]	0x0 = AD9510 with 1 GHz 0x1 = AD9510 with 500 MHz (not programmable) 0x2 = AD9510 with 500 MHz (programmable)

These data are written into one Flash page; at Power ON, the Flash content is loaded into the Configuration RAM, where it is available for readout.

1.3. Group n EEPROM Access (0x1n0C; r/w)

Bit	Function
[31:9]	*reserved*
[8]	Flag: END_OF_VALID_DATA for write accesses
[7:0]	Data to be written to or read from EEPROM

This register permits accessing the EEPROM where various information about the daughterboard is stored (refer to the Data Correction paragraph of the V1743 User Manual).
Write access to the EEPROM must be performed as a series of single accesses to the register, because bytes will be sent sequentially to the memory until the flag END_OF_VALID_DATA goes high. The two first bytes correspond respectively to the MSB and LSB of the EEPROM internal address. They have to be sent systematically to set the address. The following bits correspond to data bytes and are required only for write accesses. END_OF_VALID_DATA has to be set to 0 except for the last data word where it has to be set to 1, including the second address word in the case of setting the address before a read command (in this case there is indeed no data word).
See also the EEPROM WRITE PROTECT register (§ **1.16**).

⚠ CAUTION: Its use is reserved to experienced Users, since a wrong value written in the calibration dedicated part of the memory will erase the module's calibration pattern.

1.4. Group n Test (0x1n24; r/w)

Bit	Function
[31:0]	*reserved* (**access test only**)

1.1. Group n SAM Data (0x1n28; r/w)

Bits	Function
[31:0]	SAMLONG Internal register value to write or read.

A write access (respectively a read access) to this register provokes a write access (respectively a read access) via an SPI-like frame to the SAMLONG Internal Register specified in the *Group n SAM Address* register within the bits[7:0] (see § **1.18**). The number of bits to write (respectively to read) is also given in the same *Group n SAM ADDRESS* register within the bits[7:0].

1.2. Group n Pulse Enable (0x1n2C; r/w)

Bits	Function
[31:3]	*reserved*
[2]	PULSE_SOURCE 0 = source is VME or Optical link 1 = source is external trigger input on TRG-IN
[1]	EN_PULSE_CH_1: enables sending the pulse pattern to channel 1 0 = disabled (default) 1 = enabled
[0]	EN_PULSE_CH_0: enables sending the pulse pattern to channel 0 0 = disabled (default) 1 = enabled

This 3-bit register permits controlling the source and destination of the pulses internally sent to the board inputs. Both channels can be enabled independently. The common triggering source of the pulses is defined by bit[2]. The pulse pattern is defined by *the Group n Pulse Pattern* register (see § **1.4**).

1.3. Group n PostTrigger (0x1n30; r/w)

Bit	Function
[31:8]	*reserved*
[7:0]	POSTTRIG (default value is 1)

- Bits[7:0] contain the value of the delay added to the trigger in the front-end FPGA before the acquisition is stopped. Units are in periods of the SAMLONG chips write clock (see V1743 userl Manual).

1.4. Group n Pulse Pattern (0x1n34; r/w)

Bit	Function
[31:16]	*reserved*
[15:0]	PULSE PATTERN (default 1)

- Bits[15:0] describe the pattern sent in the pulser mode. The 16 bits are sent sequentially to the pulse generators located on the board inputs with LSB first. Outside the pulse sequence, the level is pulled to zero.

1.5. Group n Trigger Gate (0x1n38; r/w)

Bit	Function
[31:8]	*reserved*
[7:0]	GATE LENGTH (default 1)

- Bits[7:0] permit fixing the width N of the gate built in each channel when the discriminator has crossed its threshold. The window begins upon the threshold crossing of the signal on the edge defined in *Group n Trigger* register (see § **1.6**) and ends up after 10ns + N clock periods of the master clock sent to the SAMLONG chip (5ns @ 3.2GS/s, 10ns @ 1.6GS/s, 20ns @ 800MHz, 40ns @ 400MHz). This window is instantaneously retriggerable. The corresponding pulse is sent to the motherboard in order to participate in the trigger decision.

Note: This paramter is not valid when operating in Charge Mode.

1.6. Group n Trigger (0x1n3C; r/w)

Bit	Function
[31:8]	*reserved*
[7]	EDGE_CH_1 0 = rising edge (default) 1 = falling edge
[6]	EN_CH_1 0 = Ch1 doesn't take part in the trigger decision 1 = Ch1 participates in the trigger decision
[5]	EDGE_CH_0 0 = rising edge (default) 1 = falling edge
[4]	EN_CH_0 0 = Ch0 doesn't take part in the trigger decision 1 = Ch0 participates in the trigger decision
[3]	LOGIC_TYPE 0 => "OR" (default) 1 => "AND" (2 by 2)
[2:0]	**Must be 1**

- Bits[7:0] permit controlling the self-trigger conditions.

1.7. Group n Sampling Frequency (0x1n40; r/w)

Bit	Function
[31:2]	*reserved*
[1:0]	SAMPLING_FREQUENCY 0 => 3.2 GS/s 1 => 1.6 GS/s (default) 2 => 0.8 GS/s 3 => 0.4 GS/s

- Bits[1:0] permit controlling the sampling frequency in the SAMLONG chip. Default value at power-up is 1.

WARNING: when sampling at 3.2 or 1.6 GS/S, bit[3] of SAMLONG internal control register 2 (DisIntVctrlN & VDLL) has to be set to 0 whereas it has to be set to 1 when sampling at 800 MS/s or below.

1.8. Group n Recording Depth (0x1n44; r/w)

Bit	Function
[31:7]	*reserved*
[6:0]	NB_OF_COLUMNS_TO_READ (default 64)

- Bits[6:0] permit fixing the number of columns of 16 cells which will be read in the SAMLONG chip for each event. Default is 64, which corresponds to 1024 samples (full depth).

Note: set the same value of recording depth for each channel.

1.9. Group n Charge Threshold (0x1n48; r/w)

Bit	Function
[31:23]	*reserved*
[22:0]	CHARGE_THRESHOLD (default 64)

- Bits[22:0] fix the value of the threshold applied to the event charge in order to enable its writing into the charge FIFO. The value is in ADC counts coded in two's complement. It is relative to the signal baseline in the event (such baseline is arbitrary taken as the first 16 cells of the event). For positive threshold values, charge has to be above the threshold, while it has to be below for negative threshold values.

Note: No time stamp is stored in correspondence of the suppressed events due to the charge threshold setting.

1.10. Group n DAC SPI Data (0x1n54; w)

Bit	Function
[31:24]	*reserved*
[23:20]	Command Code = 0x3 (Write and Update)
[19:16]	DAC selection (see below)
[15:0]	DAC Value

A write access to this register provokes a write access via an SPI frame to the four-channel 16-bit DAC. Each individual DAC is internally selected via the “DAC selection” bits[19:16] as follows:

0001 => DAC A: Discriminator Threshold Channel 0
0010 => DAC B: Discriminator Threshold Channel 1
0100 => DAC C: DC Offset Channel 0
1000 => DAC D: DC Offset Channel 1
1111 => all DACs

The voltage output covers the range from -1.25 V to 1.25 V. The value 0x0000 corresponds to +1.25 V, 0x8000 to 0 V and 0xFFFF to -1.25 V.

1.11. Group n Charge Reference Cell (0x1n58; r/w)

Bit	Function
[31:10]	*reserved*
[9:0]	REF_CELL_FOR_CHARGE (see below)

- Bits[9:0] fix the relative position of the reference cell used for starting the charge calculation in the FPGA. Details are reported in the “**Running in Charge Mode**” paragraph of the V1743 User Manual. See also the *Group n Charge Length* register (§ **1.17**)

1.12. Group n Clear Event FIFOs (0x1n5C; w)

Writing to this address, provokes the clearing of the event FIFOs located in the front-end FPGA. Data bits have no meaning.

⚠ **WARNING:** This operation may cause communications errors between the daughterboard and the motherboard.

1.13. Group n FIFO Flags Status (0x1n60; r)

Bit	Function
[31:4]	*reserved*
[3]	Full* flag Event Buffer MSB (active low)
[2]	Empty* flag Event Buffer MSB (active low)
[1]	Full* flag Event Buffer (active low)
[0]	Empty* flag Event Buffer (active low)

The Event Buffer contains 24-bit words which correspond to Waveform data. The Event Buffer MSB contains a subset of control bytes (refer to the "**Event Structure**" paragraph of the V1743 User Manual).

1.14. Group n FCR Status (0x1n68; r)

Bit	Function
[31:10]	*reserved*
[9:0]	FIRST CELL READ

- Bits[9:0] permit reading the value of the so-called "FCR" register, which tags the location of the first cell read by the SAMLONG chip for the current event. FCR is also automatically put in the event data (refer to the "**Event Structure**" paragraph of the V1743 User Manual).

1.15. Group n Rate Counters Ch0 (0x1n6C; r/w)

Bit	Function
[31:16]	TIME_COUNTER Ch0
[15:0]	HIT_COUNTER Ch0

HIT_COUNTER and TIME_COUNTER are 16-bit counters used to calculate the hit rate linked to the activity on the channel (first channel of the "n" group) since the last event. HIT_COUNTER counts the number of times the input discriminator has be toggling since the last event, whereas TIME_COUNTER counts the time in units of 1µs (refer to the "**Event Structure**" paragraph of the V1743 User Manual). The first counter saturating blocks the other. Taking care of memorizing this information long enough in the software, this measurement can range from 0.1 Hz to > ~400 MHz.
See also the *Group n Rate Counters Ch1* register (§ **1.20**).

1.16. EEPROM Write Protect (0x1n78; r/w)

Bit	Function
[31:1]	*reserved*
[0]	1 = EEPROM Write Protection ENABLED 0 = EEPROM Write Protection DISABLED

This register permits enabling the access to the EEPROM where various information about the daughterboard is stored (refer to the "**Data Correction**"paragraph of the V1743 User Manual).

See also the *EEPROM Access* register (§ **1.3**).

⚠ **CAUTION:** Its use is reserved to experienced Users, since a wrong value written in the calibration dedicated part of the memory will erase the module's calibration pattern.

1.17. Group n Charge Length (0x1n80; r/w)

Bit	Function
[31:16]	*reserved*
[15:0]	CHARGE_LENGTH (see below)

- Bits[9:0] fix the total number of data samples used for the integration of the event charge. See also the *Group n Charge Reference Cell* register (§ **1.11**).

1.18. Group n SAM Address (0x1n84; r/w)

Bit	Function
[31:16]	*reserved*
[15:8]	SAM register Number of bits
[7:0]	SAM Register Address to access

This register specifies the internal register of the SAMLONG chip to be accessed and how many bits to write or read.

The access to the specified SAMLONG internal register can then be performed by accessing the *Group n SAM Data* register (see § **1.1**).

1.19. Daughterboard FW Revision (0x1n8C; r)

Bit	Function
[31:16]	*reserved*
[15:12]	Board Version
[11:8]	Firmware Version
[7:0]	*reserved*

Firmware Revision is coded on 2 sets of 4 bits: bits[15:12] correspond to board version, and bits[11:8] to Firmware version.

1.20. Group n Rate Counters Ch1 (0x1n94; r/w)

Bit	Function
[31:16]	TIME_COUNTER Ch1
[15:0]	HIT_COUNTER Ch1

HIT_COUNTER and TIME_COUNTER are 16-bit counters used to calculate the hit rate linked to the activity on the channel (first channel of the "n" group) since the last event. HIT_COUNTER counts the number of times the input discriminator has be toggling since the last event, whereas TIME_COUNTER counts the time in units of 1µs (refer to the "**Event Structure**"paragraph of the V1743 User Manual). The first counter saturating blocks the other. Taking care of memorizing this information long enough in the software, this measurement can range from 0.1 Hz to > ~400 MHz.
See also the *Group n Rate Counters Ch0* register (§ **1.15**).

1.21. Channel Configuration (0x8000; r/w)

Bit	Function
[31:9]	*reserved*
[8]	Individual Trigger: **Must be 1**
[7:0]	*reserved*

⚠ **WARNING:** Bit[8] of this register must be seto to 1 by the user for a proper operating.

1.22. Channel Configuration Bit Set (0x8004; w)

Bit	Function
[31:0]	Bits set to 1 means that the corresponding bits in the Channel Configuration register are set to 1.

1.23. Channel Configuration Bit Clear (0x8008; w)

Bit	Function
[31:0]	Bits set to 1 means that the corresponding bits in the Channel Configuration register are set to 0.

1.24. Group Reset Front-End FPGA (0x8010; w)

Writing to this address provokes the reset of all the counters, state machines and buffers of the front-end FPGA. Registers are not touched. Data bits have no meaning.

1.25. Group Arm Acquisition (0x8018; w)

Writing to this address provokes the launching of the acquisition run. Data bits have no meaning.

1.26. Group Pulse Channels (0x801C; w)

Writing to this address provokes the frame pulsing of all channels (see also § **1.2** and § **1.4**). Data bits have no meaning.

1.27. Group Control (0x8070; w / 0x1n70; r)

Bit	Function
[31:6]	**Must be 0**
[5]	Disable Baseline Suppression 0 = baseline suppression enabled (default) 1 = baseline suppression disabled
[4]	Enable charge Integration 0 = charge integration disabled (default) 1 = charge integration enabled
[3]	Enable Rate Counters 0 = rate counters disabled (default) 1 = rate counters enabled
[2]	Auto Restart 0 = disabled (default) 1 = auto restart
[1:0]	**Must be 0**

- Bit[2]: setting this bit to 1, permits restarting the acquisition automatically after the readout of an event.
- Bit[3] permits enabling the functioning of the trigger rate monitor counters.
- Bit[4] permits enabling the normal functioning of the charge integration system. In this mode, the interrupt is sent only when one of the charge FIFOs gets full. Exclusive from bit[5].
- Bit[5] permits disabling the functioning of the baseline suppression of the charge integration system.

1.28. Group PreTrigger (0x8074;w / 0x1n74; r)

Bit	Function
[31:8]	*reserved*
[7:0]	PRETRG

- Bits[7:0] register fixes the delay between the starting of the SAMLONG sampling clock and the enabling of the trigger, in units of ADC clock periods (100 ns). It corresponds to the safe stabilization delay for the chip's DLLs. Its default value is 100, which corresponds to 10 µs at 3.2 GS/s.

⚠ **CAUTION**: This register is heartly recommended not to be touched by Users (only expert use for debug).

1.29. Group Reset SAM (0x807C; w)

Writing to this address provokes the complete reset of the SAMLONG chips, including registers. Data bits have no meaning.

⚠ **CAUTION**: This register is heartly recommended not to be touched by Users.

1.30. Acquisition Control (0x8100; r/w)

Bit	Function
[31:12]	*reserved*
[11]	LVDS RunIn Mode: 0 = Start on RunIn level 1 = Start on RunIn rising edge **Note:** this bit is meaningless if the LVDS new features are disabled (see § **1.48**).
[10]	*reserved*
[9]	LVDS VetoIn enable: 0 = VetoIn disabled 1 = VetoIn enabled **Note:** this bit is meaningless if the LVDS new features are disabled (see § **1.48**).
[8]	LVDS BusyIn enable: 0 = BusyIn disabled 1 = BusyIn enabled **Note:** this bit is meaningless if the LVDS new features are disabled (see § **1.48**).
[7:6]	*reserved*
[5]	Memory Full Mode: 0 = NORMAL (default): board becomes full, whenever all buffers are full 1 = ONE BUFFER FREE: board becomes full, whenever N-1buffers are full; N = nr. of blocks
[4]	*reserved*
[3]	Trigger Counting Mode 0 = COUNT ONLY ACCEPTED TRIGGERS 1 = COUNT ALL TRIGGERS
[2]	Acquisition Start / Arm: 0 = Acquisition STOP (if bits[1:0]=00); Acquisition DISARMED (others) 1 = Acquisition RUN (if bits[1:0]=00); Acquisition ARMED (others)
[1:0]	Start/Stop Mode: 00 = SW CONTROLLED 01 = S-IN CONTROLLED 10 = FIRST TRIGGER CONTROLLED 11 = LVDS CONTROLLED

- Bits [1:0] set the START / STOP mode:
  00 -> SW CONTROLLED MODE (default). Sart and Stop of Run take place on SW command, that is by setting/resetting bit[2].
  01 -> S-IN CONTROLLED MODE. If the acquisition is armed (i.e. bit[2] = 1), then Run starts when S-IN is asserted and stops when S-IN returns inactive. If bit[2] = 0, the acquisition is always off.
  10 -> FIRST TRIGGER CONTROLLED MODE. If the acquisition is armed (i.e. bit[2] = 1), then Run starts on the first trigger pulse (rising edge on TRG-IN); this pulse is not used as trigger, actual triggers start from the second pulse. The stop of Run must be SW controlled (i.e. bit[2] = 0).

11 -> LVDS CONTROLLED MODE. Like 01 but using LVDS I/Os (RUN) instead of S-IN.

- Bit [2] sets the Acquisition Start / Arm. When bits[1:0] = 00, this bit acts as a Run Start/Stop (0 = stopped; 1 = running). When bits[1:0] = 01, 10, 11, this bit arms the acquisition (0 = disarmed; 1 = armed); the actual Start/Stop is controlled by an external signal.
- Bit [5] set the Memory Full Mode. When 0 (NORMAL mode), the board is full when all buffers are full. When 1 (ONE BUFFER FREE mode), the board is full whenever N_{blk} -1 Buffers are full (N_{blk} is the number of blocks).

1.31. Acquisition Status (0x8104; r)

Bit	Function
[31:17]	*reserved*
[16]	TRG-IN Status: Read current logical level on TRG-IN
[15]	S-IN Status: Read current logical level on S-IN
[14:9]	reserved
[8]	Board Ready: Board readiness for acquisition (PLL and ADCs are synchronised correctly). 0 = Board is not ready to start acquisition 1 = Board is ready to start acquisition This bit should be checked after software reset to ensure that the board will enter immediatly run mode after RUN mode setting; otherwise a latency between RUN mode setting and Acquisition start might occur.
[7]	PLL Unlock Detect: PLL unlock flag. 0 = PLL has had an unlock condition since the last register read access 1 = PLL hasn't had any unlock condition since the last register read access. **Note:** flag can be restored to 1 via read access *to VME Status* register (see § **1.51**)
[6]	PLL Bypass mode: 0 = PLL is not bypassed 1 = PLL is bypassed: the VCXO frequency directly drives the clock ditribution tree.
[5]	Clock source: 0 = Internal (PLL uses the internal 50 MHz oscillator as a reference) 1 = External (PLL uses the external clock as a reference)
[4]	EVENT FULL: it is set to 1 as the maximum nr. of events to be read is reached
[3]	EVENT READY: it is set to 1 as at least one event is available to readout
[2]	Acquisition Status: It reflects the status of the acquisition. 0 = Acquisition is stopped 1 = Acquisition is running
[1:0]	*reserved*

1.32. Software Trigger (0x8108; w)

Bit	Function
[31:0]	A write access (whatever value) to this location generates a trigger via software

1.33. Trigger Source Enable Mask (0x810C; r/w)

Bit	Function
[31]	Software Trigger Enable: 0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	External Trigger Enable: 0 = External Trigger Disabled 1 = External Trigger Enabled
[29:24]	*reserved*
[23:20]	Coincidence window
[19:10]	*reserved*
[9:8]	Common Trigger Logic: 00 = global trigger is the OR of the enabled trigger requests 01 = global trigger is the AND of the enabled trigger requests 10 = global trigger is the MAJORITY of the enabled trigger requests 11 = *unused*
[7]	Trigger request 7 Enable (upon the Ch 15 and Ch 14 self triggers): 0 = Trigger request is not sensed for global trigger generation 1 = Trigger request participates in the global trigger generation
[6]	Trigger request 6 Enable (upon the Ch 13 and Ch 12 self triggers): 0 = Trigger request is not sensed for global trigger generation 1 = Trigger request participates in the global trigger generation
[5]	Trigger request 5 Enable (upon the Ch 11 and Ch 10 self triggers): 0 = Trigger request is not sensed for global trigger generation 1 = Trigger request participates in the global trigger generation
[4]	Trigger request 4 Enable (upon the Ch 9 and Ch 8 self triggers): 0 = Trigger request is not sensed for global trigger generation 1 = Trigger request participates in the global trigger generation
[3]	Trigger request 3 Enable (upon the Ch 7 and Ch 6 self triggers): 0 = Trigger request is not sensed for global trigger generation 1 = Trigger request participates in the global trigger generation
[2]	Trigger request 2 Enable (upon the Ch 5 and Ch 4 self triggers): 0 = Trigger request is not sensed for global trigger generation 1 = Trigger request participates in the global trigger generation
[1]	Trigger request 1 Enable (upon the Ch 3 and Ch 2 self triggers): 0 = Trigger request is not sensed for global trigger generation 1 = Trigger request participates in the global trigger generation
[0]	Trigger request 0 Enable (upon the Ch 1 and Ch 0 self triggers): 0 = Trigger request is not sensed for global trigger generation 1 = Trigger request participates in the global trigger generation

- Bits[7:0] enable the trigger request generation. Each trigger request is generated upon of the channel self-triggers from two adjacent channels according to the logic configurable by the *Group n Trigger* register (see § **1.6**). The self-trigger is a pulse of programmable width (see § **1.5**) issued when the input signal exceeds threshold. Bit[0] enables the trigger request 0, based on the CH0 and CH1 self-triggers; bit[1] enables the trigger request 1, based on the CH2 and CH3 self-triggers, and so on. For details, please refer to the "**Trigger Management**" paragraph of the V1743 User Manual.
- Bits[9:8] permit configuring the logic to generate the common trigger from the enabled trigger requests.
- Bits[23:20] set the coincidence window linearly in steps of the Trigger clock (10ns).
- Bit[30] controls the EXTERNAL TRIGGER ENABLE. When enabled, the board can sense TRG-IN signals.
- Bit[31] controls the SW TRIGGER ENABLE. When enabled, the board can sense software triggers (see § **1.32**).

1.34. Front Panel Trigger Out Enable Mask (0x8110; r/w)

Bit	Function
[31]	Software Trigger Out Enable: 0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	External Trigger Out Enable: 0 = External Trigger Disabled 1 = External Trigger Enabled
[29]	LVDS Trigger Enable: 0 = LVDS Trigger Disabled 1 = LVDS Trigger Enabled
[28:13]	*reserved*
[12:10]	MAJORITY Level. Sets the majority level if bits[9:8] = 10. Allowed values are between 0 and 7.
[9:8]	TRG-OUT Generation Logic: 00 = TRG-OUT is the OR of the enabled trigger requests 01 = TRG-OUT is the AND of the enabled trigger requests 10 = TRG-OUT is the MAJORITY of the enabled trigger requests 11 = *not used*
[7]	Trigger Request 7 Out Enable: 0 = Trigger request 7 disabled 1 = Trigger request 7 enabled
[6]	Trigger Request 6 Out Enable: 0 = Trigger request 6 disabled 1 = Trigger request 6 enabled
[5]	Trigger Request 5 Out Enable: 0 = Trigger request 5 disabled 1 = Trigger request 5 enabled
[4]	Trigger Request 4 Out Enable: 0 = Trigger request 4 disabled 1 = Trigger request 4 enabled
[3]	Trigger Request 3 Out Enable: 0 = Trigger request 3 disabled 1 = Trigger request 3 enabled
[2]	Trigger Request 2 Out Enable: 0 = Trigger request 2 disabled 1 = Trigger request 2 enabled
[1]	Trigger Request 1 Out Enable: 0 = Trigger request 1 disabled 1 = Trigger request 1 enabled
[0]	Trigger Request 0 Out Enable: 0 = Trigger request 0 disabled 1 = Trigger request 0 enabled

- Bits[7:0] enable the trigger requests to partecipate in generating a TRG-OUT front panel signal. Bit[0] enables trigger request 0 (related to CH0 and CH1) to partecitape in the TRG-OUT generation, bit[1] enables trigger request 1 (related to CH2 and CH3) to partecipate in the TRG-OUT generation, and so on. The logic to generate the TRG-OUT signal basing on the enabled trigger requests is configured through the bits[9:8].
- Bit[29] controls the LVDS Trigger signals when programmed as output. If enabled, they are the trigger requests coming directly from the mezzanines (see the V1743 User Manual).
- Bit[30] controls the EXTERNAL TRIGGER ENABLE. It enables/disables the board to generate the TRG-OUT.
- Bit[31] controls the SW TRIGGER ENABLE. It enables/disables the board to generate TRG-OUT (see § **1.32**).

1.35. Front Panel I/O Data (0x8118; r/w)

Bit	Function
[15:0]	Front Panel I/O Data

Allows to read out the logic level of LVDS I/Os and set the logic level of LVDS Outputs if the pins are configured as general purpose input/output (REGISTER mode described in the V1743 User Manual).

1.36. Front Panel I/O Control (0x811C; r/w)

Bit	Function
[31:20]	*reserved*
[19:18]	Motherboard Virtual Probe select (to be propagated onto TRG-OUT): 00 = RUN: the signal is active when the acquisition is running. This option can be used to synchronize the start/stop of the acquisition through the TRG-OUT->TR-IN or TRG-OUT->S-IN daisy chain. 01 = CLKOUT: this clock is synchronous with the sampling clock of the ADC and this option can be used to align the phase of the clocks in different boards. 10 = CLK Phase 11 = Board BUSY
[17:16]	TRG-OUT Mode select: 00 = Trigger (TRG-OUT propagates the internal trigger sources according to the Front Panel Trigger Out Enable Mask register (see § **1.34**). 01 = Motherboard probes (TRG-OUT is used to propagate signals of the motherboards, according to the bits[19:18]. 10 = Channel probes (TRG-OUT is used to propagate signals of the mezzanines (Channel Signal Virtual Probe). 11 = S-IN propagation
[15]	TRG-OUT Mode: 0 = TRG-OUT is an internal signal (according to bits[17:16]) 1 = TRG-OUT is a test logic level set via bit[14]
[14]	Force TRG-OUT: 0 = Force TRG-OUT to 0 1 = Force TRG-OUT to 1 Sets TRG-OUT test logical level if bit[15] = 1.
[13:12]	*reserved*
[11]	TRG-IN direct to mezzanines (channels): 0 = Standard operating 1 = TRG-IN sent directly to the mezzanines
[10]	TRG-IN signal edge disable: 0 = TRG-IN signal formed as a pulse 1 = TRG-IN signal not formed
[9]	LVDS I/Os Pattern Latch Mode: 0 = Pattern (i.e. 16-pin LVDS status) is latched when the (internal) global trigger is sent to channels, in consequence of an external trigger. It accounts for post-trigger settings and input latching delays. 1 = Pattern (i.e. 16-pin LVDS status) is latched when the external trigger arrives.
[8]	LVDS I/Os New Features select: 0 = LVDS old features (default) 1 = LVDS new features **Note:** refer to the V1743 User Manual for descriptions
[7:6]	LVDS I/O signal configuration (old features): 00 = General Purpose I/O 01 = Programmed I/O 10 = Pattern mode: LVDS signals are inputs and their value is written into header PATTERN field.

Bit	Function
	11 = *reserved* **Note:** bits[7:6] are meaningful only if bit[8] = 0.
[5]	LVDS I/Os [15:12] direction: 0 = inputs 1 = outputs
[4]	LVDS I/Os [11:8] direction: 0 = inputs 1 = outputs
[3]	LVDS I/Os [7:4] direction: 0 = inputs 1 = outputs
[2]	LVDS I/Os [3:0] direction: 0 = inputs 1 = outputs
[1]	LVDS I/Os enable: 0= enabled 1= High impedance
[0]	LEMO I/Os (TRG-IN, S-IN, TR-OUT) electrical levels: 0 = NIM I/O Levels 1 =TTL I/O Levels

- Bits [5:2] are meaningful for General Purpose use only.

1.37. Channel Enable Mask (0x8120; r/w)

Bit	Function
[31:16]	*reserved*
[15]	Channel 15 enable: 0 = Channel 15 disabled (i.e. it doesn't contribute to events) 1 = Channel 15 enabled (i.e. it contributes to events)
[14]	Channel 14 enable: 0 = Channel 14 disabled (i.e. it doesn't contribute to events) 1 = Channel 14 enabled (i.e. it contributes to events)
[13]	Channel 13 enable: 0 = Channel 13 disabled (i.e. it doesn't contribute to events) 1 = Channel 13 enabled (i.e. it contributes to events)
[12]	Channel 12 enable: 0 = Channel 12 disabled (i.e. it doesn't contribute to events) 1 = Channel 12 enabled (i.e. it contributes to events)
[11]	Channel 11 enable: 0 = Channel 11disabled (i.e. it doesn't contribute to events) 1 = Channel 11 enabled (i.e. it contributes to events)
[10]	Channel 10 enable: 0 = Channel 10 disabled (i.e. it doesn't contribute to events) 1 = Channel 10 enabled (i.e. it contributes to events)
[9]	Channel 9 enable: 0 = Channel 9 disabled (i.e. it doesn't contribute to events) 1 = Channel 9 enabled (i.e. it contributes to events)
[8]	Channel 8 enable: 0 = Channel 8 disabled (i.e. it doesn't contribute to events) 1 = Channel 8 enabled (i.e. it contributes to events)
[7]	Channel 7 enable: 0 = Channel 7 disabled (i.e. it doesn't contribute to events) 1 = Channel 7 enabled (i.e. it contributes to events)
[6]	Channel 6 enable: 0 = Channel 6 disabled (i.e. it doesn't contribute to events) 1 = Channel 6 enabled (i.e. it contributes to events)
[5]	Channel 5 enable: 0 = Channel 5 disabled (i.e. it doesn't contribute to events) 1 = Channel 5 enabled (i.e. it contributes to events)
[4]	Channel 4 enable: 0 = Channel 4 disabled (i.e. it doesn't contribute to events) 1 = Channel 4 enabled (i.e. it contributes to events)
[3]	Channel 3 enable: 0 = Channel 3 disabled (i.e. it doesn't contribute to events) 1 = Channel 3 enabled (i.e. it contributes to events)
[2]	Channel 2 enable: 0 = Channel 2 disabled (i.e. it doesn't contribute to events) 1 = Channel 2 enabled (i.e. it contributes to events)
[1]	Channel 1 enable: 0 = Channel 1 disabled (i.e. it doesn't contribute to events) 1 = Channel 1 enabled (i.e. it contributes to events)
[0]	Channel 0 enable: 0 = Channel 0 disabled (i.e. it doesn't contribute to events) 1 = Channel 0 enabled (i.e. it contributes to events)

Enabled channels provide the samples which are stored into the events (and not erased).

⚠ **WARNING:** The mask cannot be changed while acquisition is running.

1.38. ROC FPGA Firmware Revision (0x8124; r)

Bit	Function
[31:16]	Revision date in Y/M/DD format
[15:8]	Firmware Revision (X)
[7:0]	Firmware Revision (Y)

- Bits [31:16] contain the Revision date in Y/M/DD format.
- Bits [15:0] contain the firmware revision number coded on 16 bit (X.Y format).

1.39. Event Stored (0x812C; r)

Bit	Function
[31:0]	This register contains the number of events currently stored in the Output Buffer

1.40. Set Monitor DAC (0x8138; r/w)

Bit	Function
[31:0]	*reserved*
[11:0]	DAC value (12bit)

This register allows to set the DAC value when the Voltage Level Mode is selected (see § **1.43**). LSB = 0.244 mV, terminated on 50 Ohm.

1.41. SW Clock Sync (0x813C; w)

Bit	Function
[31:0]	Software Sync Command

A write access to this register, with any value, forces the PLL to re-align all the clock outputs with the reference clock. In case of Daisy chain clock distribution among boards, during the initialization and configuration, the reference clocks along the Daisy chain can be unstable and a temporary loss of lock may occur in the PLLs; although the lock is automatically recovered once the reference clocks return stable, it is not guaranteed that the phase shift returns to a known state. This command allows the board to restore the correct phase shift between the CLK-IN and the internal clocks.

Note: the command must be issued starting from the fisrt to the last board in the clock chain.

1.42. Board Info (0x8140; r)

Bit	Function
[31:24]	*reserved*
[23:16]	Equipped number of groups: 0x08 (8 groups)
[15:8]	Memory Size: 0x01
[7:0]	Board type (743 family): 0x09

1.43. Monitor DAC Mode (0x8144; r/w)

Bit	Function
[31:3]	*reserved*
[2:0]	Analog Monitor Output mode: 000 = Trigger Majority Mode 001 = Test Mode 010 = *reserved* 011 = Buffer Occupancy Mode 100 = Voltage Level Mode Others = *reserved* **Note:** refer to the V1743 User Manual for descriptions

1.44. Event Size (0x814C; r)

Bit	Function
[31:0]	Event Size (in 32-bit words)

It represents the current available event in 32-bit words. The value is updated after the complete readout of each event.

1.45. Memory Buffer Almost Full Level (0x816C, r/w)

Bit	Function
[31:12]	*reserved*
[10:0]	LEVEL

This register allows to set the level for the Almost Full generation. If this register is set to 0, the Almost Full is a FULL. Meaningful values are in the range 0÷6.

1.46. Run/Start/Stop Delay (0x8170; r/w)

Bit	Function
[31:0]	RUN/START/STOP Delay (expressed in trigger clock cycles)

When the start of Run is given synchronously to several boards connected in Daisy chain, it is necessary to compensate for the delay in the propagation of the Start (or Stop) signal through the chain. This register sets the delay, expressed in trigger clock cycles (i.e. 8 ns for the V1743 models) between the arrival of the Start signal at the input of the board (either on S-IN or TRG-IN) and the actual start of Run. The delay is usually zero for the last board in the chain and rises going backward along the chain.

1.47. Board Fail Status (0x8178; r)

Bit	Function
[31:5]	*reserved*
[4]	PLL Lock Loss: 0 = No error 1 = A PLL lock loss occurred
[3:0]	Internal Communication Timeout: 0000 = No Error Any other case means a timeout occurred

This register monitors a set of board errors.

Note: In case of problems with the board, the user can monitor this resister and contact CAEN for support (see the board User Manual or visit CAEN website for contacts).

1.48. Front Panel LVDS I/O New Features (0x81A0: r/w)

Bit	Function
[31:16]	*reserved*
[15:12]	LVDS I/O 15..12 pin configuration
[11:8]	LVDS I/O 11..8 pin configuration
[7:4]	LVDS I/O 7..4 pin configuration
[3:0]	LVDS I/O 3..0 pin configuration

- Bits[15:0] register allows to set the new LVDS I/O features by groups of four (4), if bit[8]=1 in the Front Panel I/O Control register (see § **1.36**).

Note: The LVDS I/O new fatures are supported only from revision 3.8 of the ROC FPGA firmware on.
The possible configurations are:
– 0000 = REGISTER
– 0001 = TRIGGER
– 0010 = nBUSY/nVETO
– 0011 = OLD STYLE
Please, refer to the V1743 User Manual for details.

1.49. Buffer Occupancy Output Gain (0x81B4: r/w)

Bit	Function
[31:4]	*reserved*
[3:0]	Value (default is 0)

- When the Buffer Occupancy mode is programmed (see § **1.43**), a voltage level is output on the front panel MON/Σ Lemo connector which increments by fixed steps of 0.976 mV once a memory buffer is filled with an event. V1743 features a fixed memory organization of 7 buffers, so the output level can range from 0 to 6.832 mV over a complete dynamics of 1 V. Bits[3:0] of this register allow to apply a multiplication factor to the fixed step of the ouptut voltage level. The permitted register values belong to the range [0:A], where the multiplicaiton factor is 2^{value}.

Note: this register is not supported by ROC FPGA firmware revisions lower than **4.9**.

1.50. VME Control (0xEF00; r/w)

Bit	Function
[31:9]	*reserved*
[8]	Extended Block Transfer enable: 0 = Extended Block Transfer Space disabled 1 = Extended Block Transfer Space enabled
[7]	Interrupt Release mode: 0 = Release On Register Access (RORA). This is the default mode, where interrupts are removed by disabling them either by setting VME Interrupt Level to 0 (VME Interrupts) or by setting Optical Link Interrupt Enable = 0. 1 = Release On Acknowledge (ROAK). Interrupts are automatically disabled at the end of a VME interrupt acknowledge cycle (INTACK cycle). **Note:** ROAK mode is supported only for VME interrupts. ROAK mode is not supported on interrupts generated over Optical Link.
[6]	VME Base Address Relocation: 0 = Address Relocation disabled (VME Base Address is set by the on-board rotary switches (see V1743 User Manual) 1 = Address Relocation enabled (VME Base Address is set by the Relocation Address register; see § **1.54**).
[5]	VME Align64 Mode: 0 = 64-bit aligned readout mode disabled 1 = 64-bit aligned readout mode disabled enabled
[4]	VME Bus Error / Event Aligned Readout enable: 0 = VME Bus Error / Event Aligned Readout disabled (the module sends a DTACK signal until the CPU inquires the module). 1 = VME Bus Error / Event Aligned Readout enabled (the module is enabled either to generate a Bus Error to finish a block transfer or during the empty buffer read out in D32).
[3]	Optical Link Interrupt Enable: 0 = Optikal Link interrupts disabled 1 = Optical Link interrupts enabled
[2:0]	VME Interrupt level: 0 = VME interrupts are disabled

- Bits[2:0] set VME interrupt level (1-7).
- Bit[3] enables interrupt generation over the CONET optical link.
- Bit[8] selects the Memory Interval allocated for Block Transfers. If disabled, block transfer region is a 4kB in the 0x0000 – 0x0FFC interval. If enabled, block transfer is a 16 MB in the 0x00000000 – 0xFFFFFFFC interval. In Extended mode, the board VME Base Address is only set via the on-board [31:28] rotart switches or the bits[31:28] of Relocation Address register.

1.51. VME Status (0xEF04; r)

Bit	Function
[31:3]	*reserved*
[2]	0 = BERR FLAG: no Bus Error has occurred 1 = BERR FLAG: a Bus Error has occurred (this bit is re-set after a status register read out)
[1]	reserved
[0]	Event Ready: 0 = No Data Ready; 1 = Event Ready

1.52. Board ID (0xEF08; r/w)

Bit	Function
[31:5]	*reserved*
[4:0]	GEO

The Meaning of the register depends on which VME crate it is inserted in:

- VME64X versions: this register can be accessed in read mode only and contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the Board ID field of the Event header (see the V1743 User Manual).
- Other versions: this register can be accessed both in read and write mode; it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the Board ID field of the Event header (see the V1743 User Manual).

1.53. MCST Base Address and Control (0xEF0C; r/w)

Bit	Function
[31:10]	*reserved*
[9:8]	Board Position in Daisy chain: 00 = Board disabled 01 = Last board 10 = First board 11 = Intermediate board
[7:0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, i.e. the address used in MCST/CBLT operations.

- Bits[9:8] allow to set up the board for Daisy chaining.

1.54. Relocation Address (0xEF10; r/w)

Bit	Function
[31:16]	*reserved*
[15:0]	These bits contain the A31…A16 bits of the address of the module. If relocation address is enabled, this register sets the VME Base Address of the module.

1.55. Interrupt Status ID (0xEF14; r/w)

Bit	Function
[31:0]	This register contains the STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle.

1.56. Interrupt Event Number (0xEF18; r/w)

Bit	Function
[31:10]	*reserved*
[9:0]	INTERRUPT EVENT NUMBER

This register sets the number of events that cause an interrupt request. If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of events > INTERRUPT EVENT NUMBER.

1.57. BLT Event Number (0xEF1C; r/w)

Bit	Function
[31:16]	*reserved*
[15:0]	This register contains the number of complete events which has to be transferred for each block transfer (via VME BLT/CBLT cycles or block readout through Optical Link). Allowed setting is between 0 (meaning no limit) and 1023.

1.58. Scratch (0xEF20; r/w)

Bit	Function
[31:0]	Scratch (*to be used to write/read words for VME test purposes*)

1.59. Software Reset (0xEF24; w)

Bit	Function
[31:0]	A write access to this location of any value, allows to perform a software reset. All registers are set to default values (i.e. actual settings are lost).

1.60. Software Clear (0xEF28; w)

Bit	Function
[31:0]	A write access to this location of any value, clears all the internal memories. Registers value are not changed.

1.61. Configuration Reload (0xEF34; w)

Bit	Function
[31:0]	A write access to this register of any value, causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.