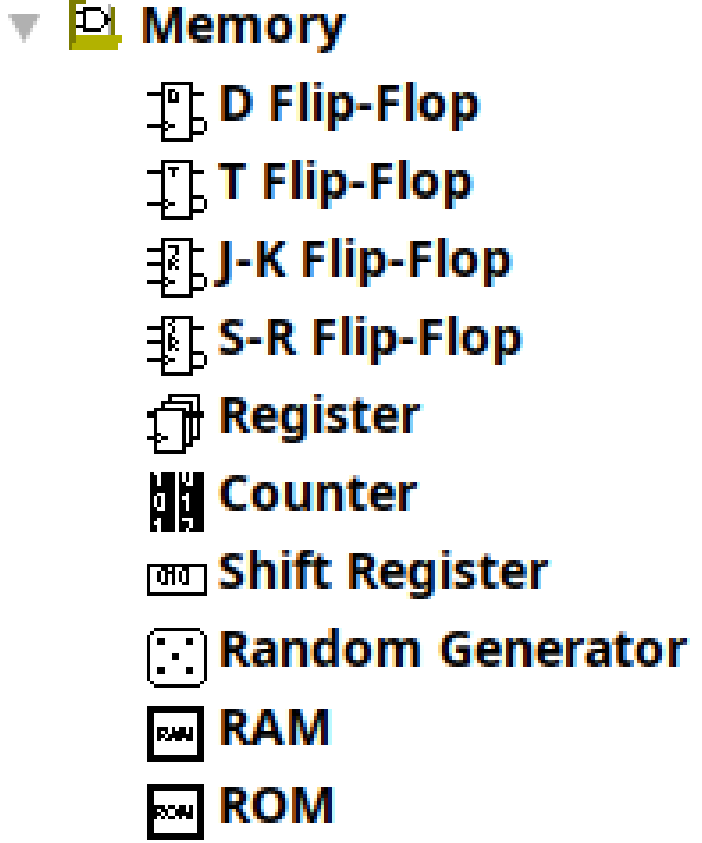
Lab 8: Register File

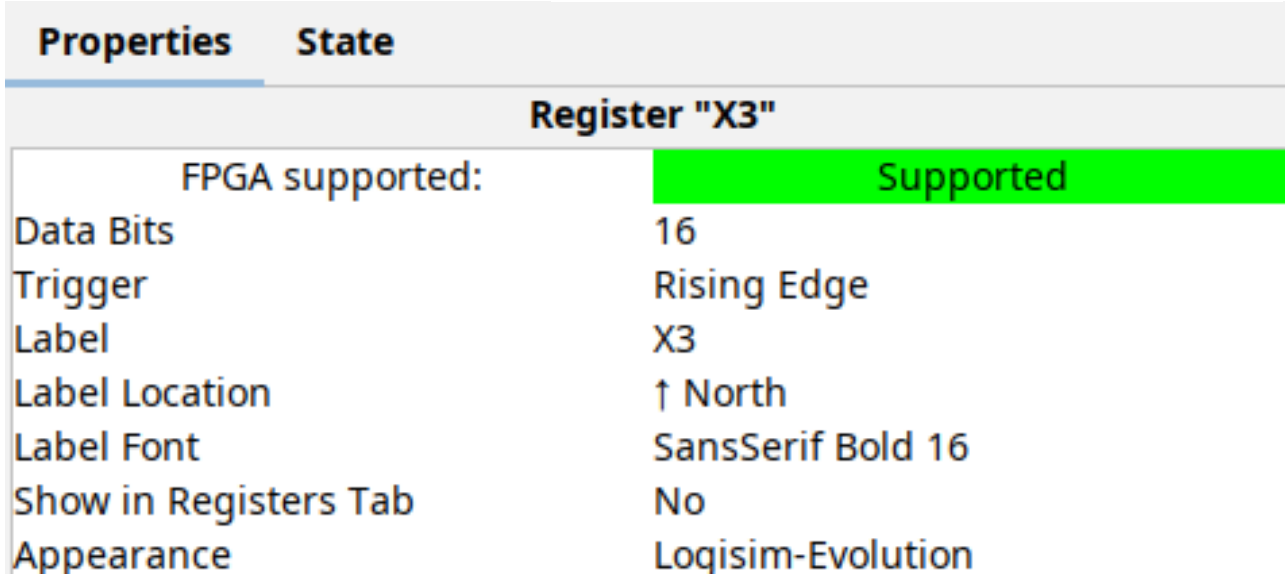
By: CS 382 CAs

Registers

Register Basics

- A register stores an individual sequence of bits for use during program runtime.
- Registers are made of many simple 1-bit latches stitched together, connected to common data lines, write signals, and clock domains.
- Logisim provides registers in the component list.
- Logisim allows the register properties to be modified from the properties section on the left.

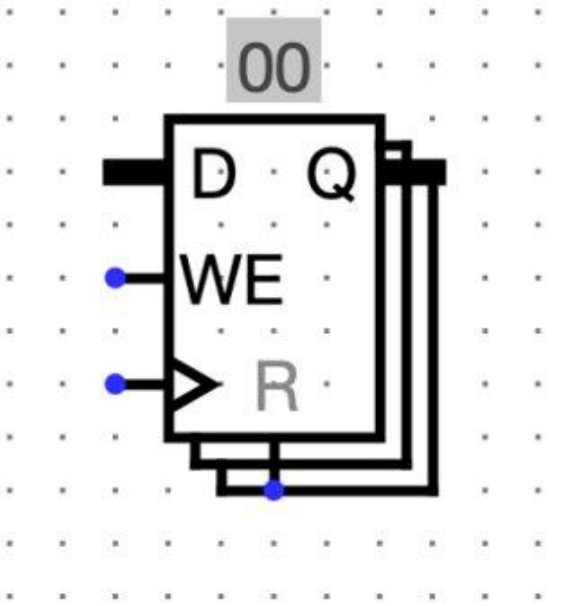




Register Ports

Register Ports

- The ports for a register are as follows.
  - D: The data to be written to the register, must have an equal number of incoming bits as the register stores.
  - WE: A boolean 1-bit signal enabling the ability to write the data in D to the register.
  - Triangle: A clock signal to time the register writes, the register will write when the clock signal rises.
  - Q: The data read from the register, always active. Must also be of the same width as the register itself.
  - R: When active, resets the register value to 0 (extraneous).



Your Assignment

Your assignment

- Construct a register file in Logisim Evolution as per the lab spec.
- The register file must contain four registers, each of which can store a byte, as well as two read ports.

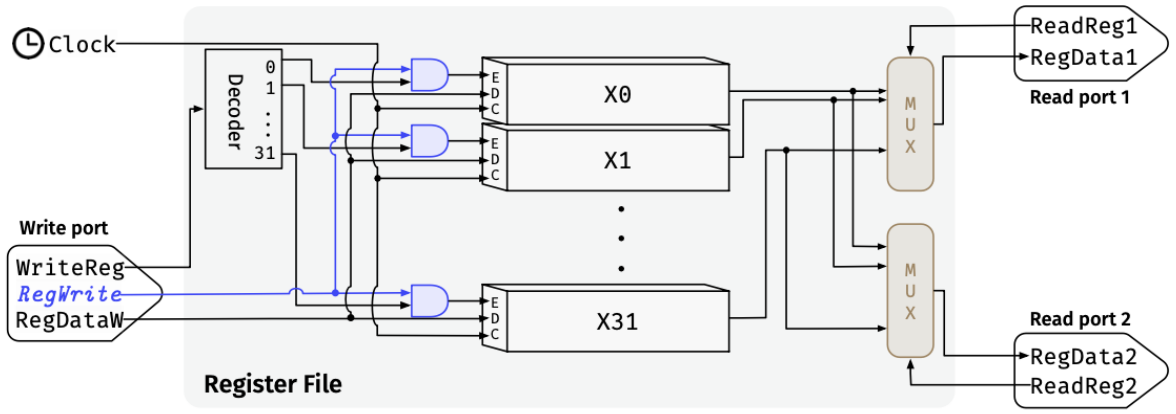


Figure 3.14: A little more detailed register file.

Simulation

Simulation

- To simulate go to Simulate -> Timing Diagram, followed by Simulate -> Auto Tick Enabled (Ctrl + K).
- Observe that each clock cycle has a rising and falling edge, pay attention to how the register value changes at these edges.