



RD50 HV-CMOS Meeting

DESY-TB results

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Overview

When: 22.04.-29.4.2024

Where: DESY test beam facility

Measured Sensors

MPW4

- 2x topside biased (HEPHY, Liverpool)
- 2x backside biased (HEPHY, NIKHEF)

Performed Measurements

- High statistic runs
- Threshold Scans
- Bias voltage Scans
- Rotation scans

Beam

Particles: electrons

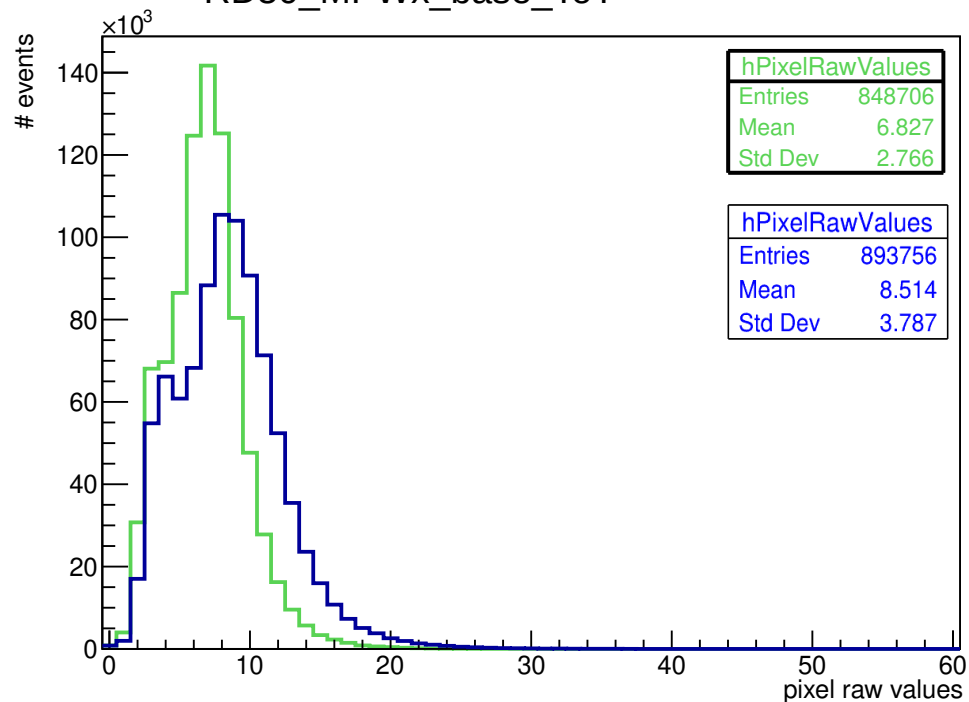
Energy: 4.2 GeV

Rate: ~10 kHz

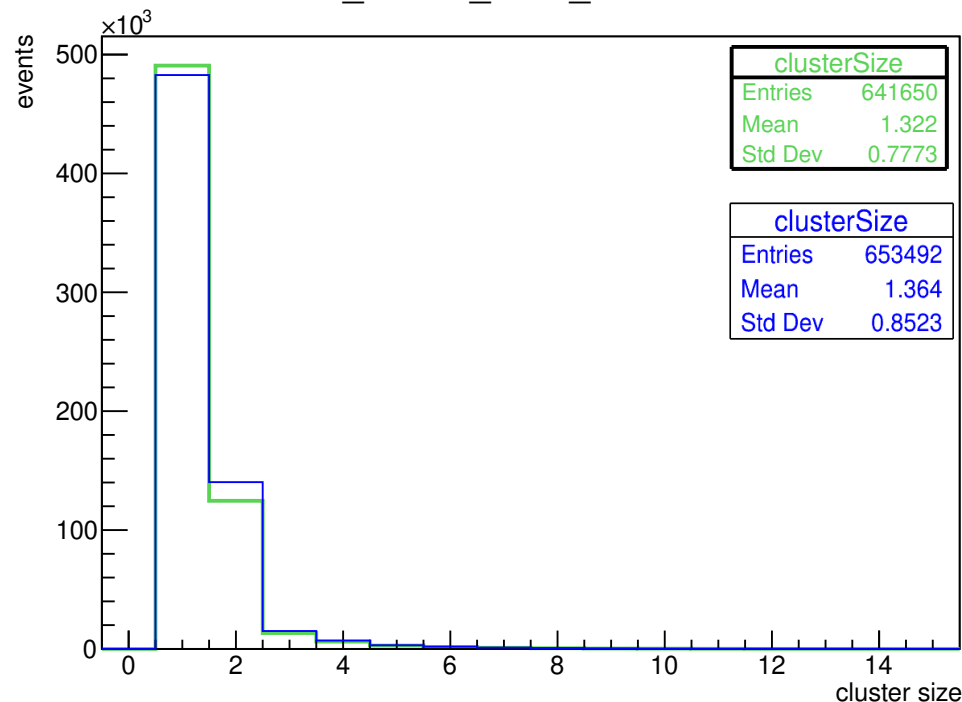
ToT and cluster size

Bias voltage: 190 V
Threshold: 20/40 mV
LSB = 25 ns

RD50_MPWx_base_ToT



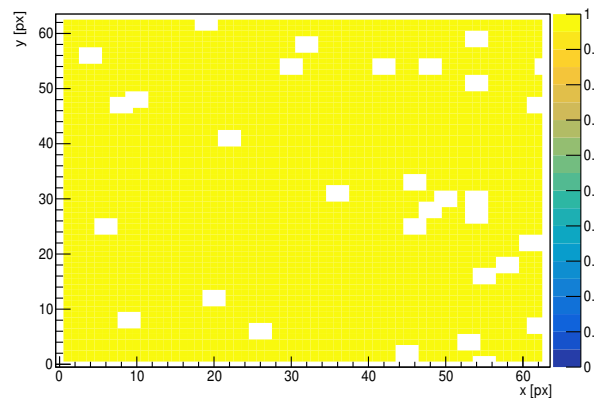
RD50_MPWx_base_0 Cluster size



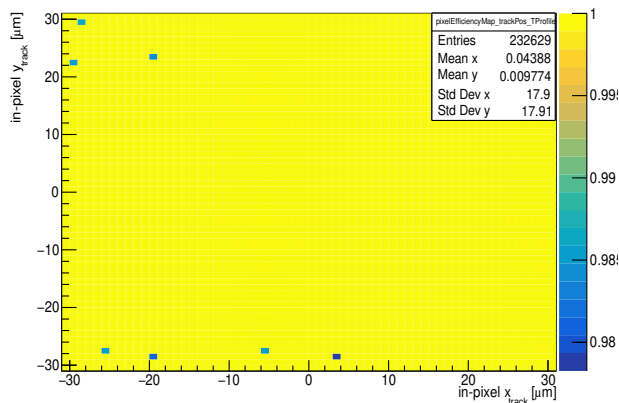
HEPHY topside biased
HEPHY backside biased

Efficiencies

RD50_MPWx_base_0 Chip efficiency map



RD50_MPWx_base_0 Pixel efficiency map

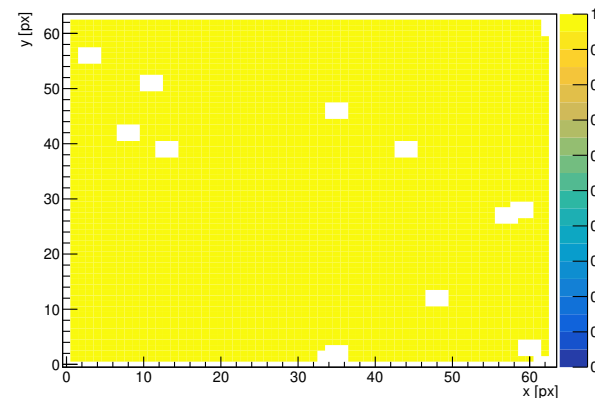


backside

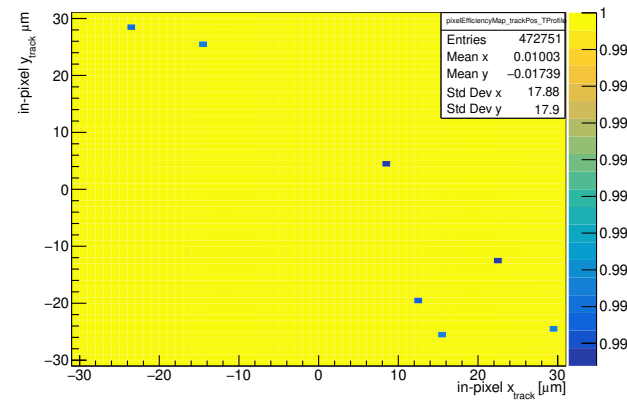
HEPHY topside biased

- Total efficiency: 99.9985 %
- Masked pixels: 14
- Used tracks: 472751
- Missed tracks: 7

RD50_MPWx_base_0 Chip efficiency map



RD50_MPWx_base_0 Pixel efficiency map



topside

Residuals

Residual in local X

Std Dev

binary resolution: 17.89 μm

Range: -110 μm to 110 μm

HEPHY topside biased: 18.24 μm

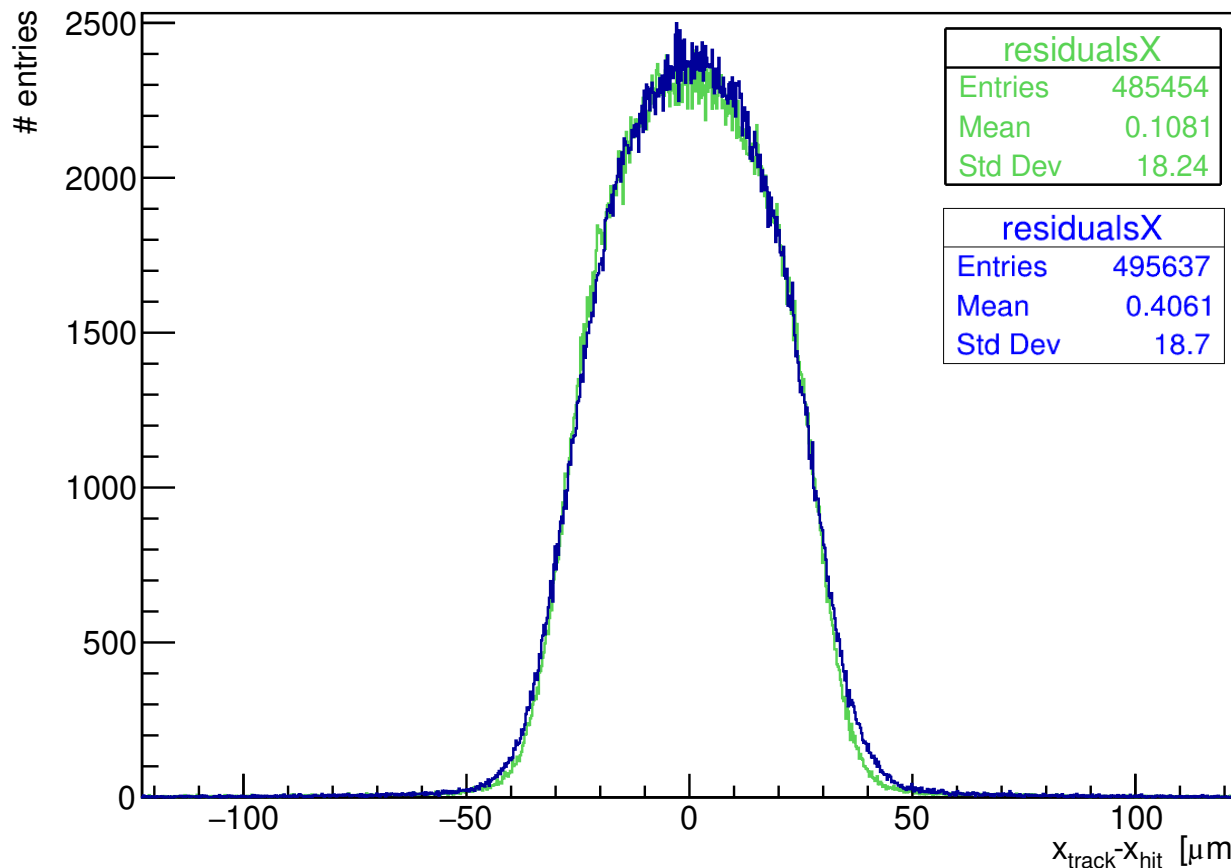
HEPHY backside biased: 18.70 μm

Range: no cuts

HEPHY topside biased: 19.09 μm

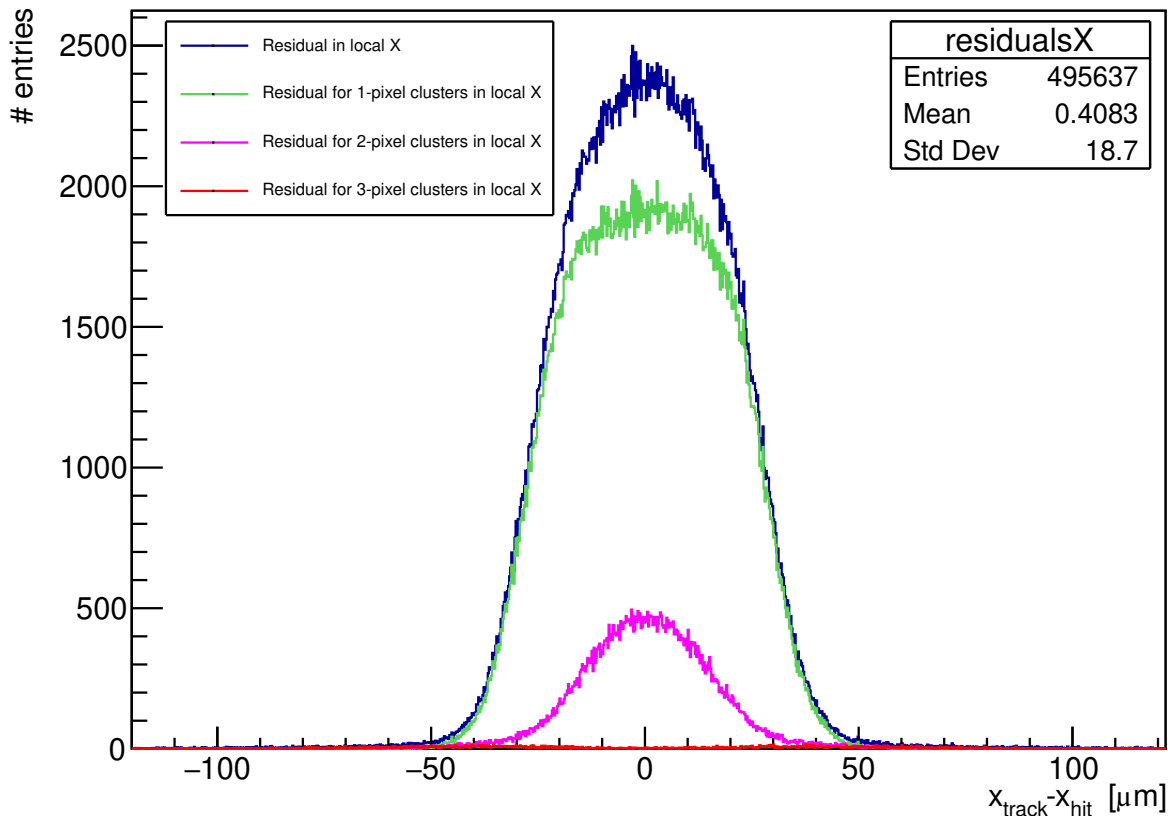
HEPHY backside biased: 20.01 μm

HEPHY topside biased
HEPHY backside biased

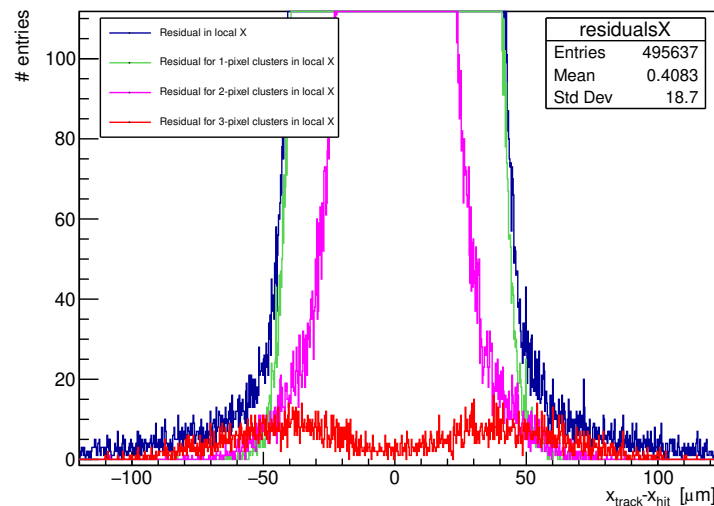


Residuals by clusters

Residual in local X



Residual in local X



Std dev (range: -110 μm to 110 μm)

- All clusters: 18.70 μm
- 1-pixel clusters: 17.95 μm
- 2-pixel clusters: 15.60 μm
- 3-pixel clusters: 49.13 μm

Comparison HEPHY backside biased with Liverpool topside biased

HV scan

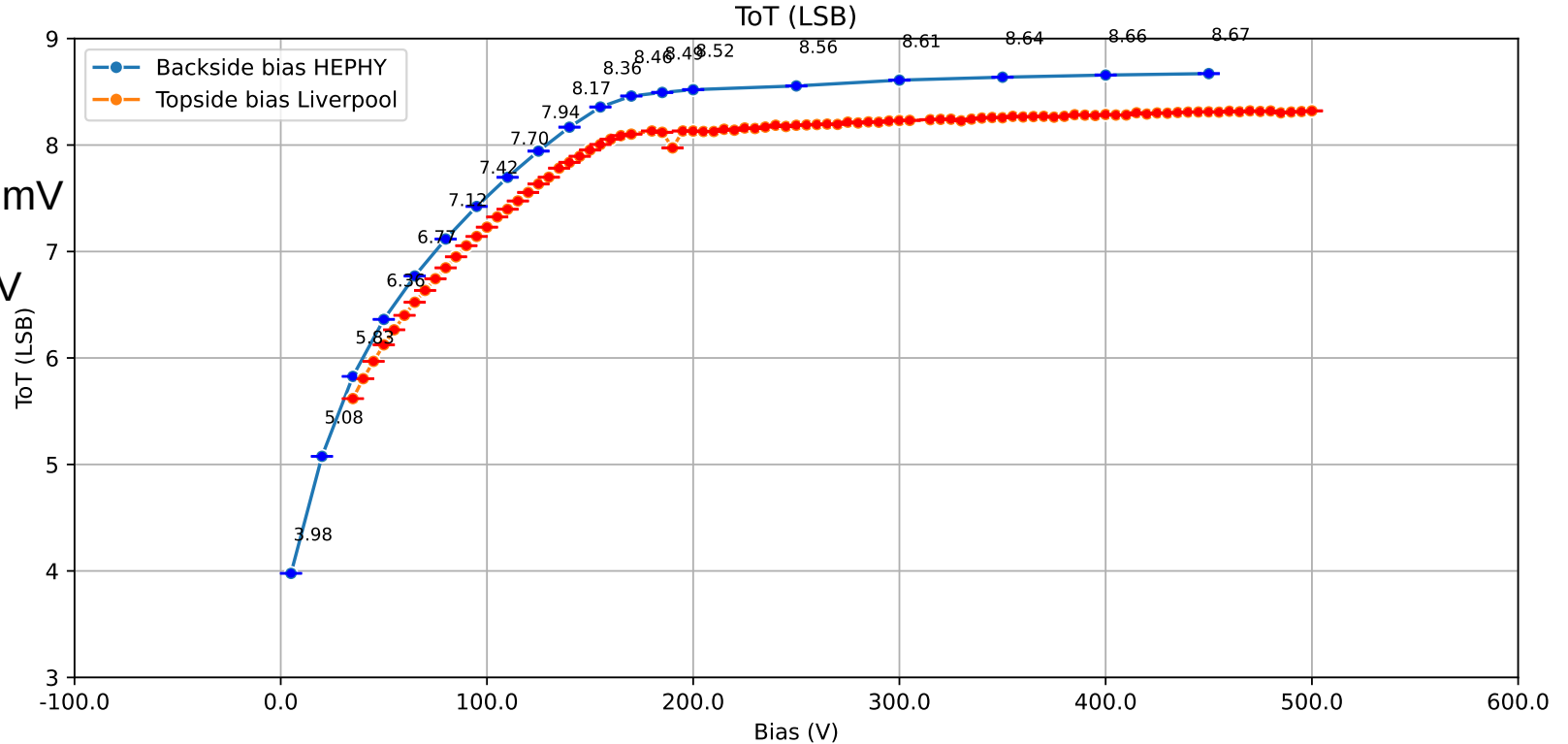
- Threshold: 30/40 mV
- Cluster size increases till 200 V => full depletion
- Decrease after this point due to increasing strength of E-field



Comparison HEPHY backside biased with Liverpool topside biased

HV scan

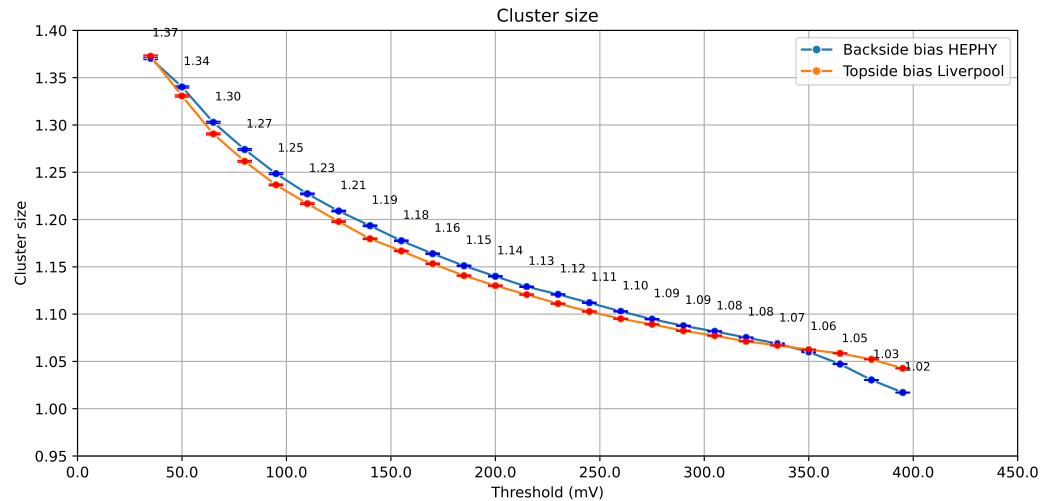
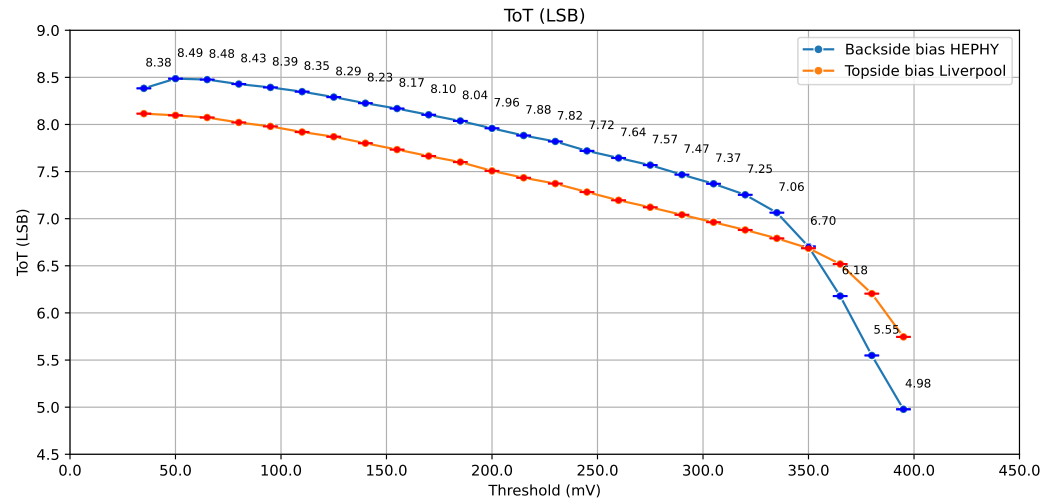
- Threshold: 30/40 mV
- Saturation at 200V
=> full depletion



Comparison HEPHY backside biased with Liverpool topside biased

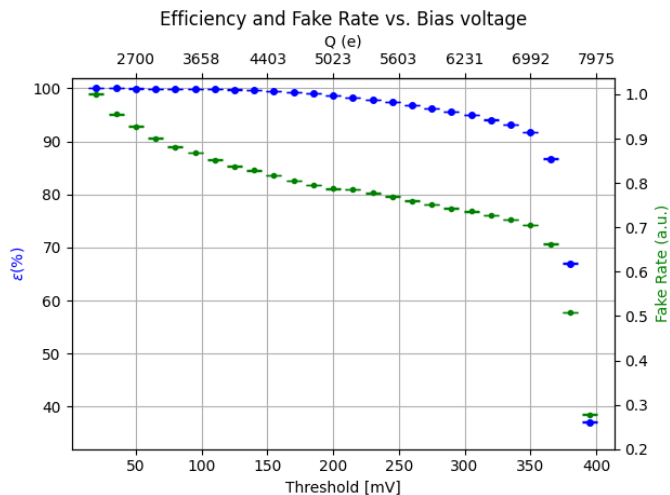
Threshold scan

- Bias voltage: 190 V

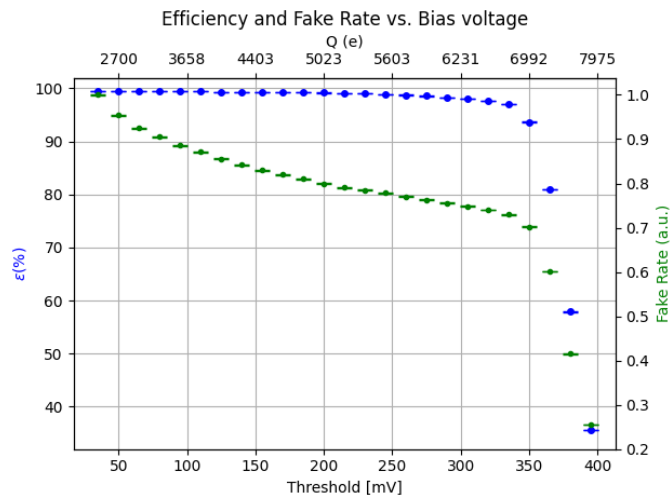


Threshold Scans

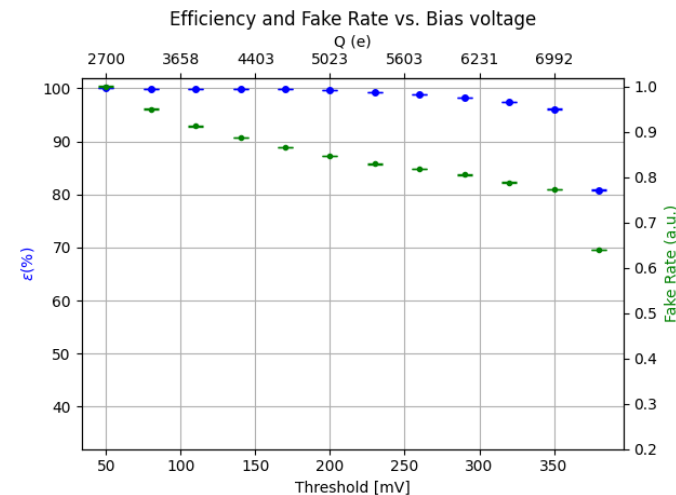
Bias voltage: 190 V



HEPHY topside biased

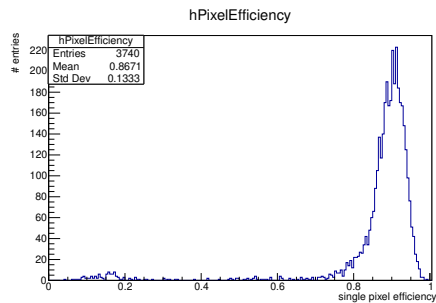


HEPHY backside biased

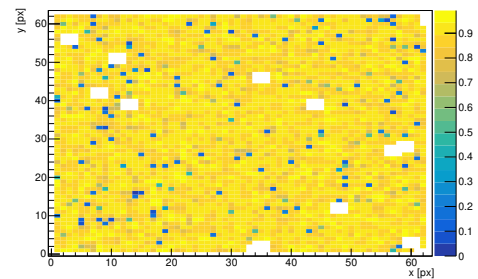


NIKHEF backside biased
biased from top

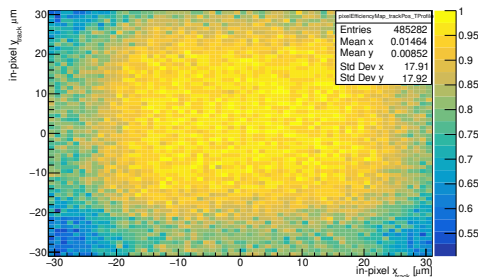
HEPHY topside biased
Threshold: 365 mV
Eff: 86 %



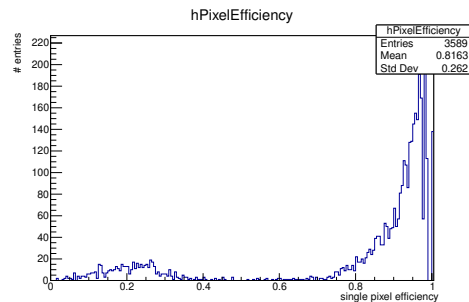
RD50_MPWx_base_0 Chip efficiency map



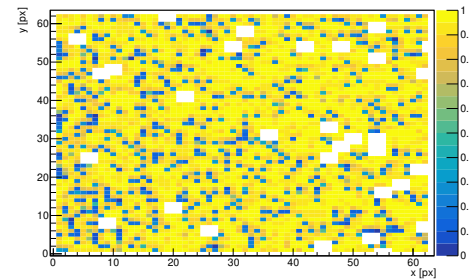
RD50_MPWx_base_0 Pixel efficiency map



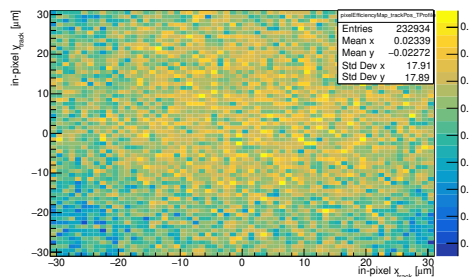
HEPHY backside biased
Threshold: 365 mV
Eff: 81 %



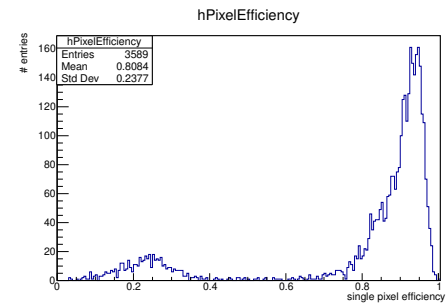
RD50_MPWx_base_0 Chip efficiency map



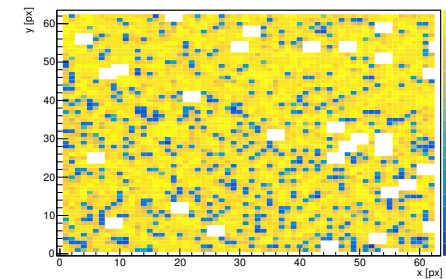
RD50_MPWx_base_0 Pixel efficiency map



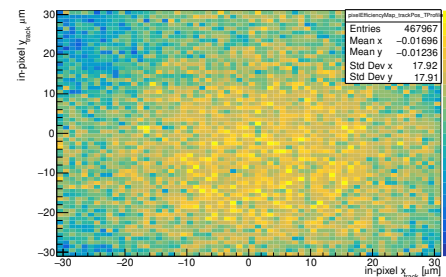
NIKHEF backside biased from top
Threshold: 380 mV
Eff: 80 %



RD50_MPWx_base_0 Chip efficiency map

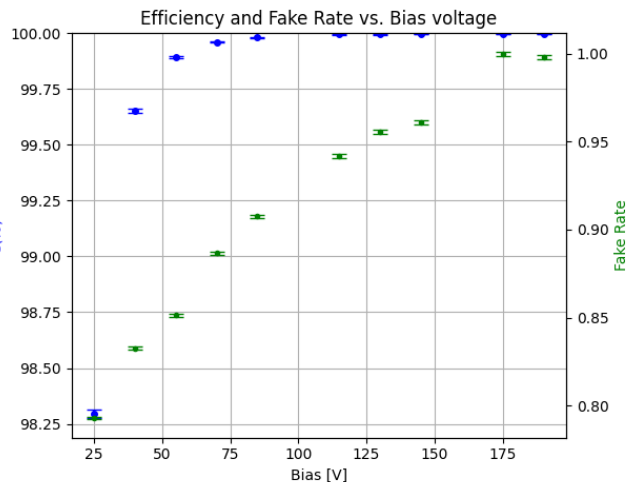


RD50_MPWx_base_0 Pixel efficiency map

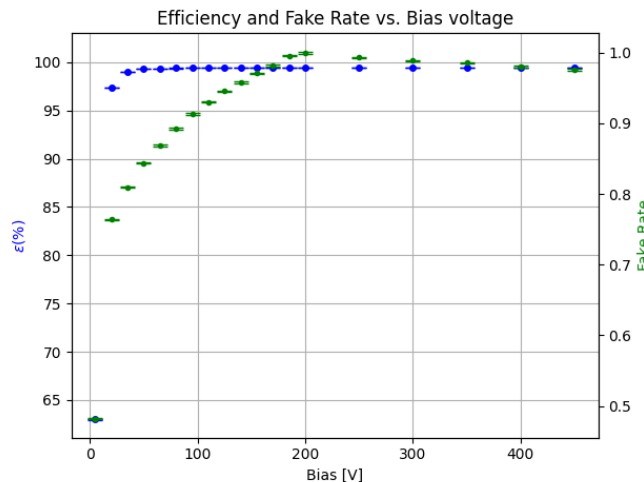


Bias Voltage Scans

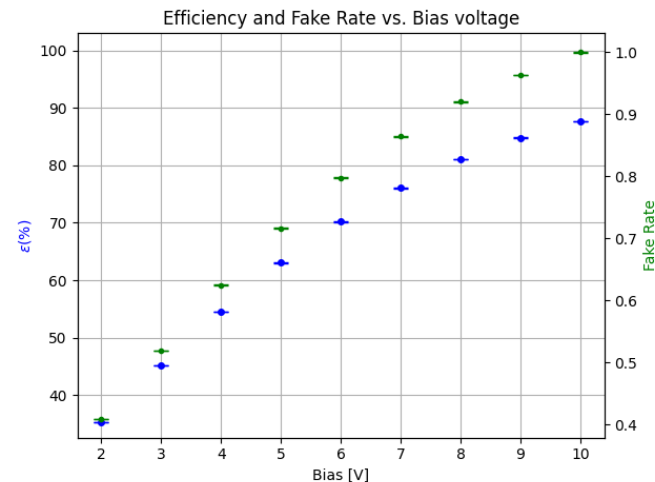
Attention: different scales!



HEPHY topside biased
Threshold: 20 mV
HV: 25-190 V

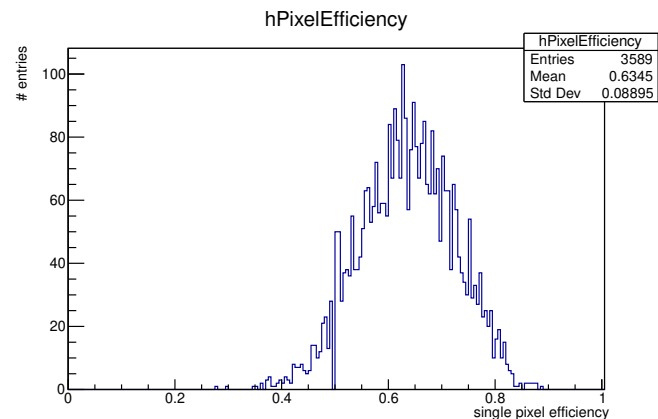


HEPHY backside biased
Threshold: 40 mV
HV: 5-450 V

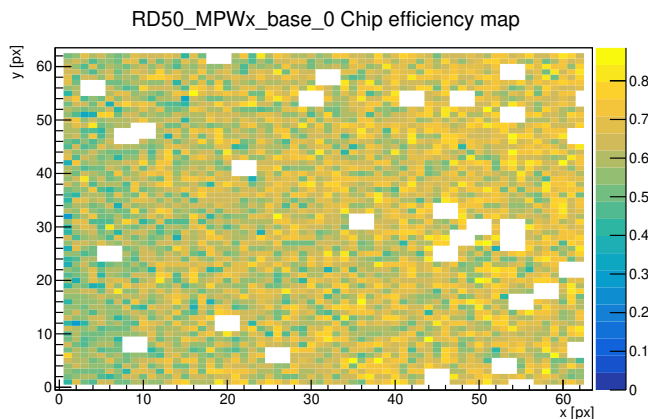


HEPHY backside biased
Threshold: 40 mV
HV: 2-10 V

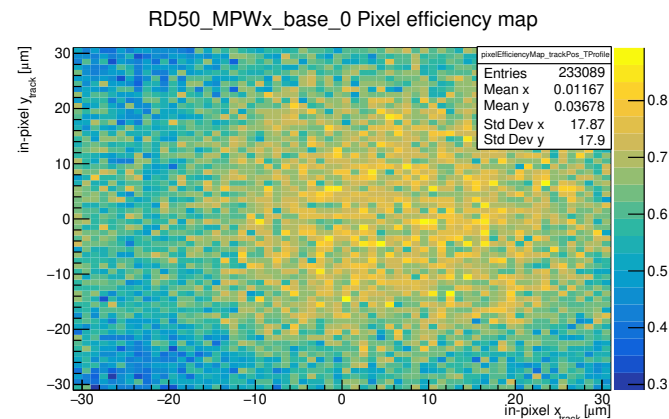
Loss of Efficiency



Single Pixel efficiency



Chip efficiency



Pixel efficiency

HEPHY backside biased

Threshold: 20 mV

HV: 5 V

Eff: 63 %