



RD50 HV-CMOS Meeting

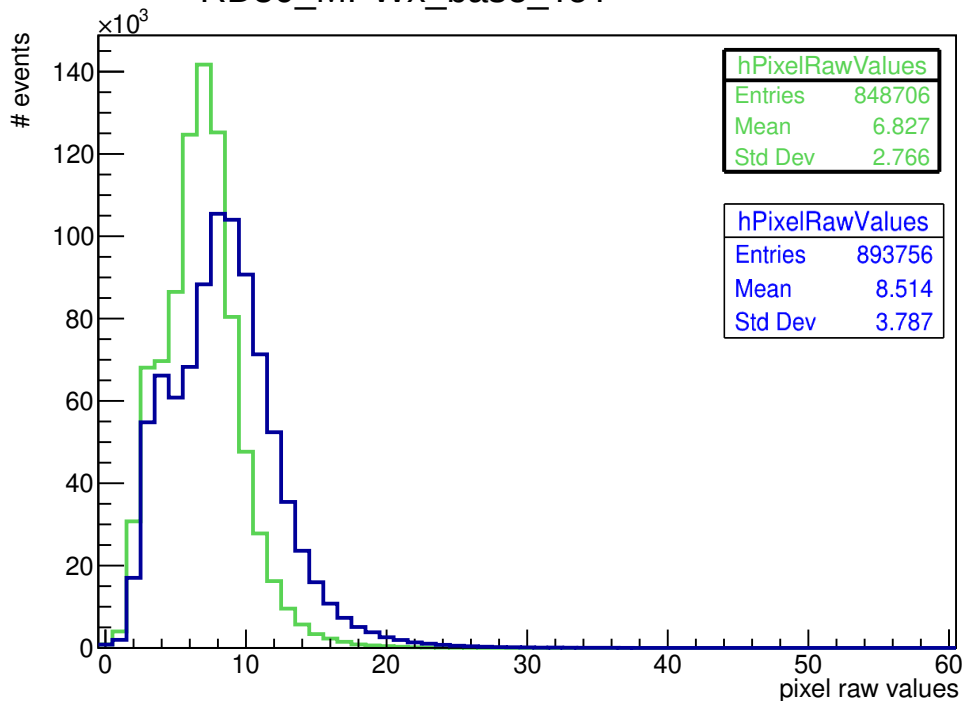
# DESY-TB results

Harald Handerkas

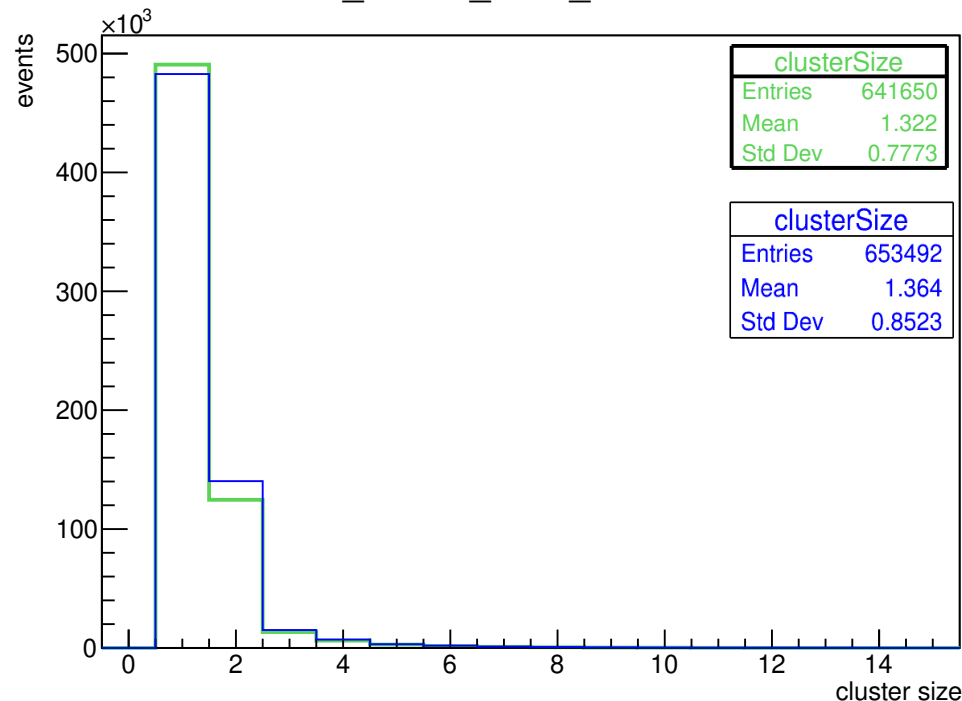
# ToT and cluster size

Bias voltage: 190 V  
Threshold: 20/40 mV  
LSB = 25 ns

RD50\_MPWx\_base\_ToT



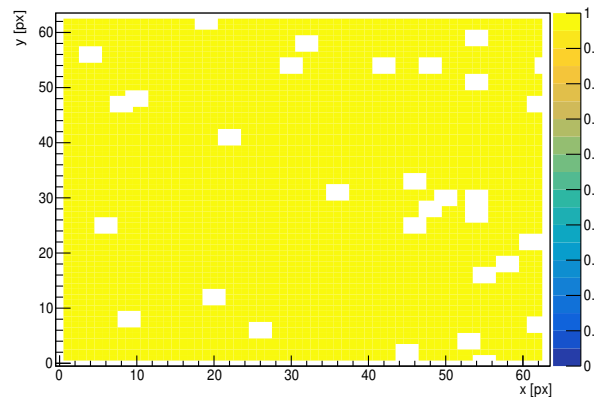
RD50\_MPWx\_base\_0 Cluster size



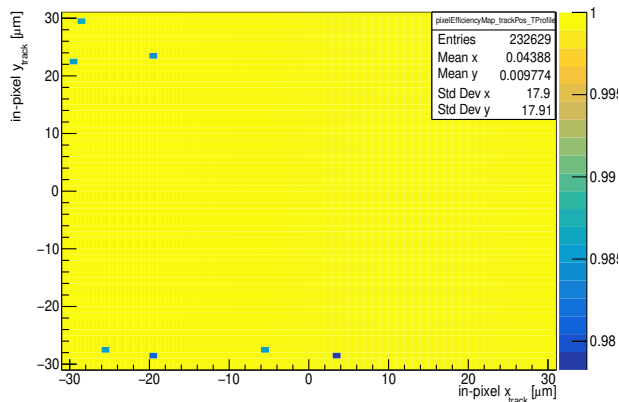
HEPHY topside biased  
HEPHY backside biased

# Efficiencies

RD50\_MPWx\_base\_0 Chip efficiency map



RD50\_MPWx\_base\_0 Pixel efficiency map

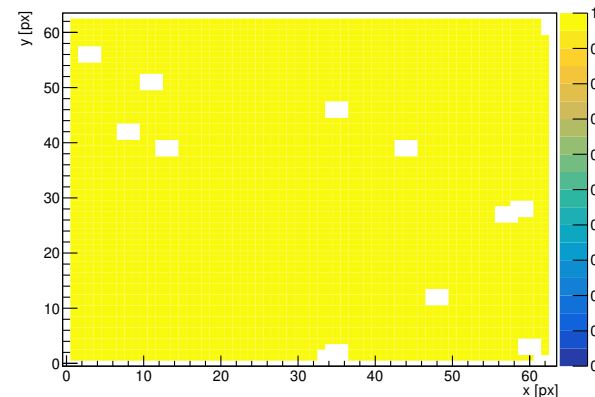


backside

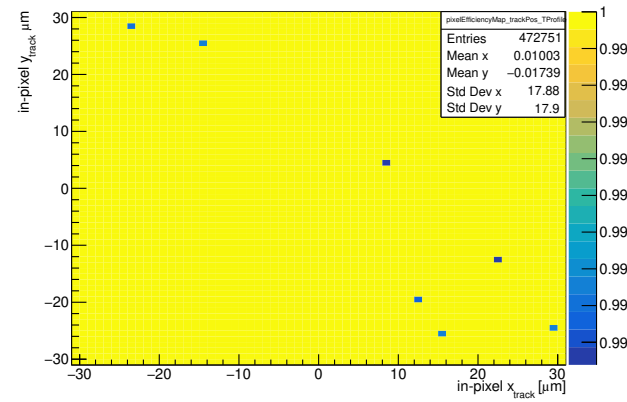
## HEPHY topside biased

- Total efficiency: 99.9985 %
- Masked pixels: 14
- Used tracks: 472751
- Missed tracks: 7

RD50\_MPWx\_base\_0 Chip efficiency map



RD50\_MPWx\_base\_0 Pixel efficiency map



topside

# Residuals

Residual in local X

## Std Dev

binary resolution: 17.89  $\mu\text{m}$

## Range: -110 $\mu\text{m}$ to 110 $\mu\text{m}$

HEPHY topside biased: 18.24  $\mu\text{m}$

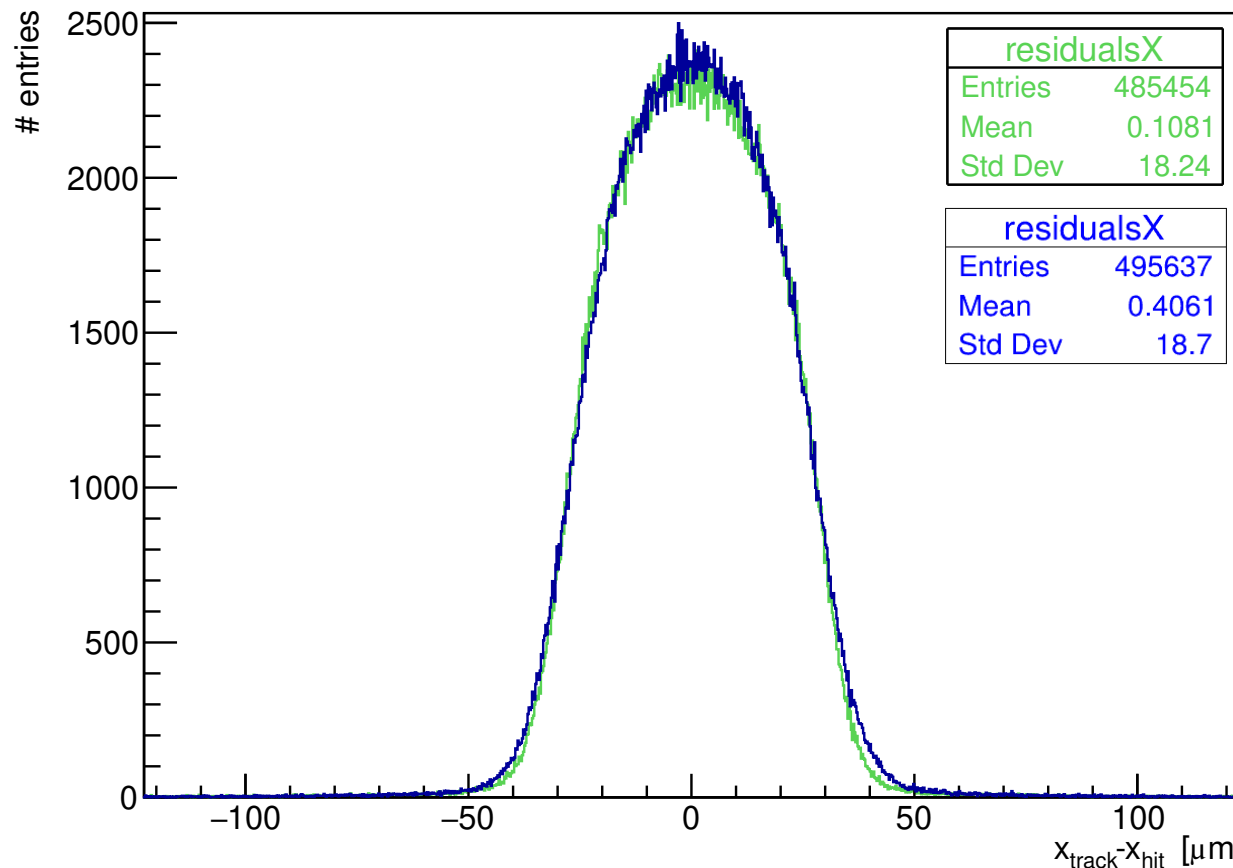
HEPHY backside biased: 18.70  $\mu\text{m}$

## Range: no cuts

HEPHY topside biased: 19.09  $\mu\text{m}$

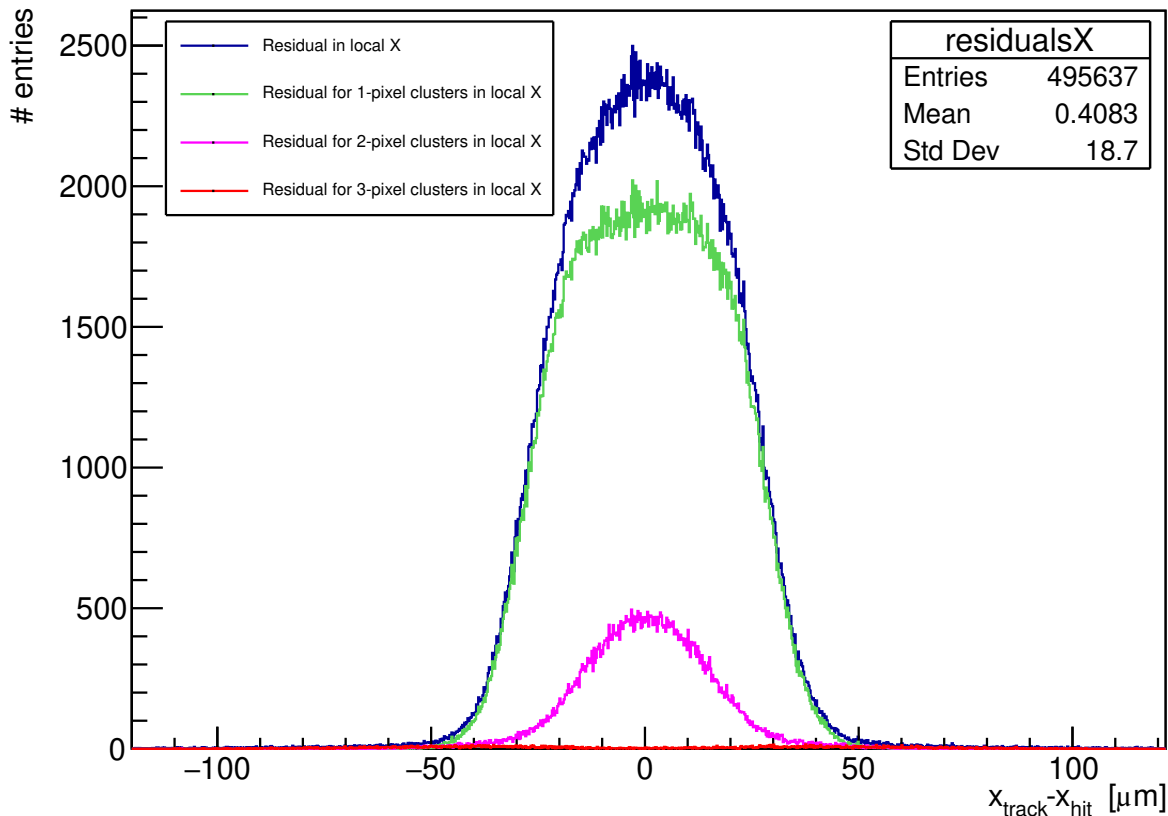
HEPHY backside biased: 20.01  $\mu\text{m}$

HEPHY topside biased  
HEPHY backside biased

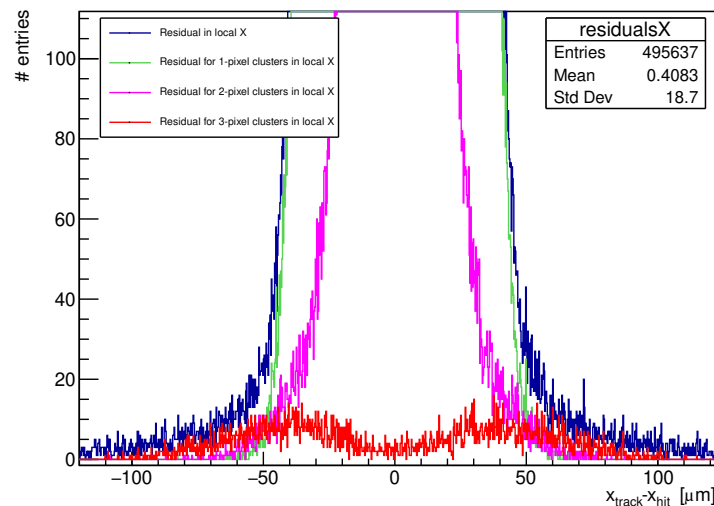


# Residuals by clusters

Residual in local X



Residual in local X



## Std dev (range: -110 $\mu\text{m}$ to 110 $\mu\text{m}$ )

- All clusters: 18.70  $\mu\text{m}$
- 1-pixel clusters: 17.95  $\mu\text{m}$
- 2-pixel clusters: 15.60  $\mu\text{m}$
- 3-pixel clusters: 49.13  $\mu\text{m}$

# Comparison HEPHY backside biased with Liverpool topside biased

## HV scan

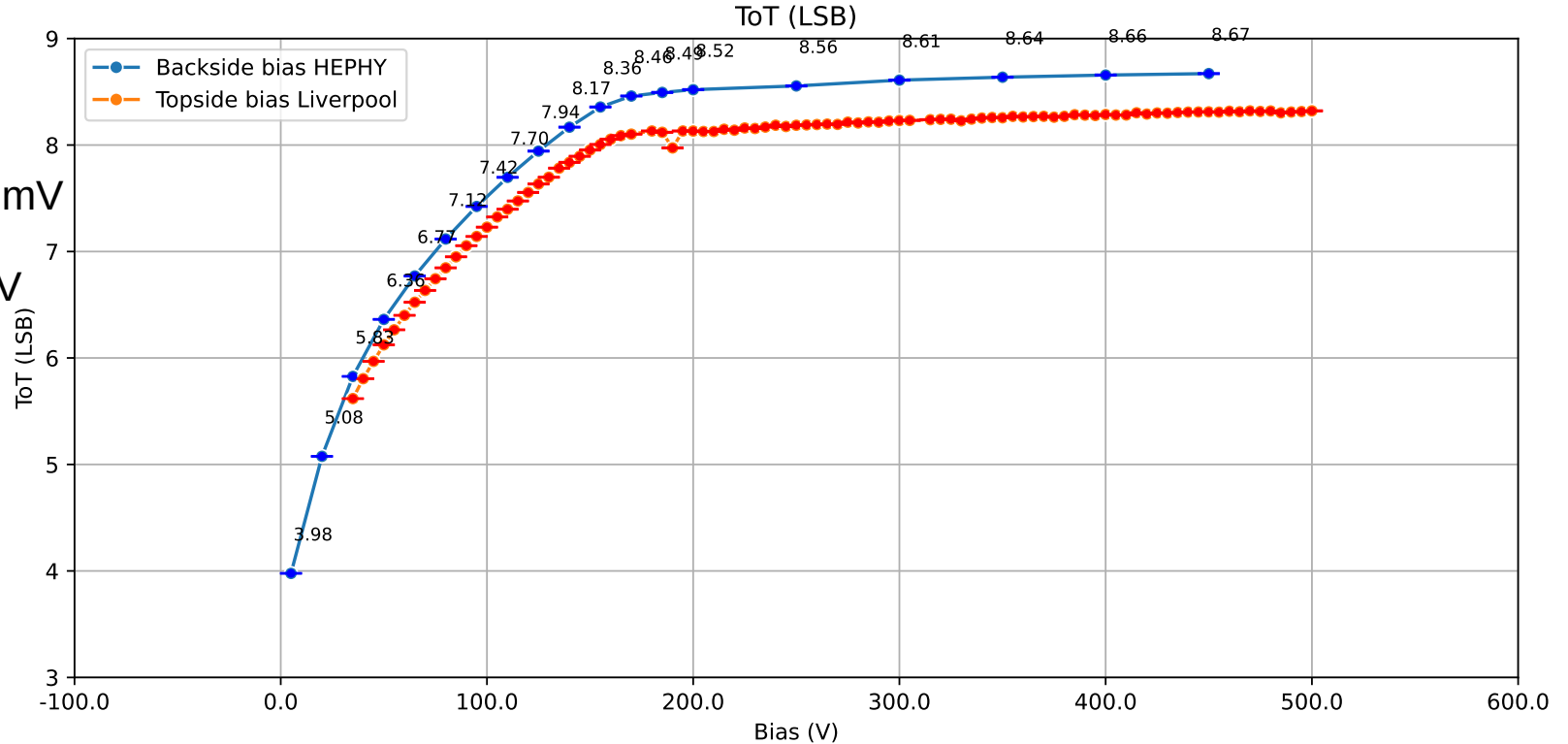
- Threshold: 30/40 mV
- Cluster size increases till 200 V => full depletion
- Decrease after this point due to increasing strength of E-field



# Comparison HEPHY backside biased with Liverpool topside biased

## HV scan

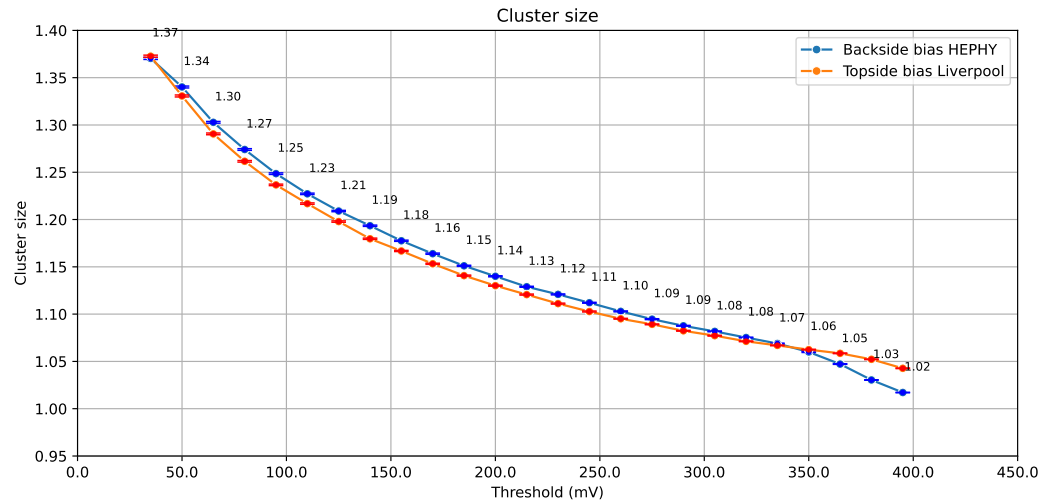
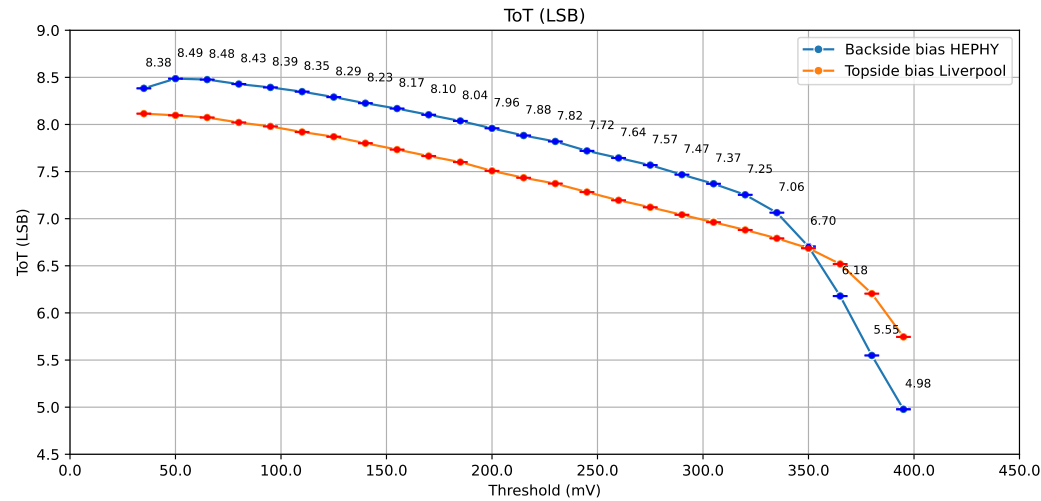
- Threshold: 30/40 mV
- Saturation at 200V  
=> full depletion



# Comparison HEPHY backside biased with Liverpool topside biased

## Threshold scan

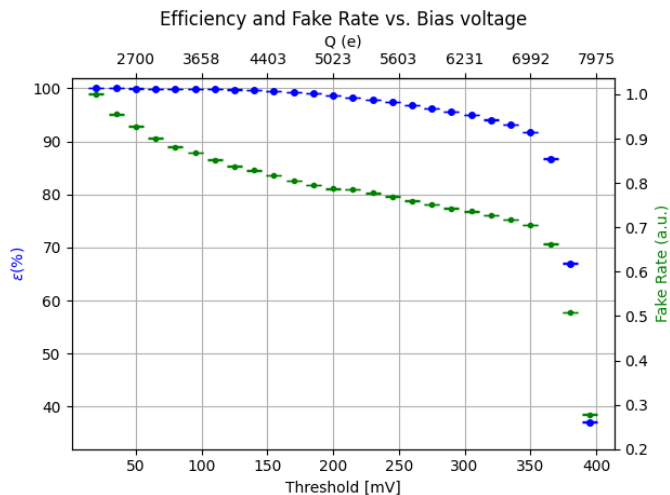
- Bias voltage: 190 V



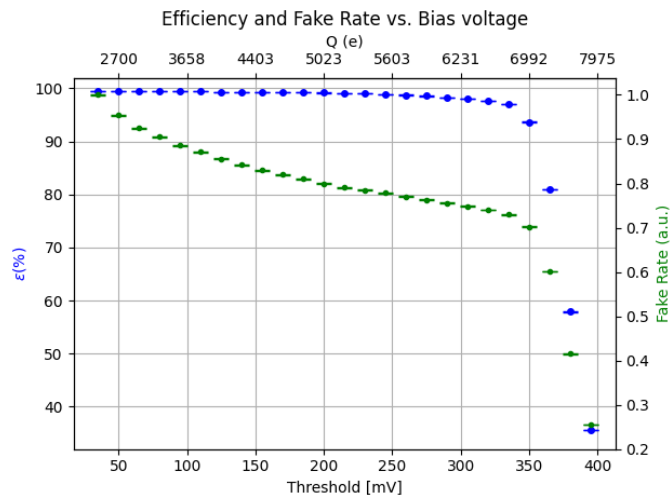


# Threshold Scans

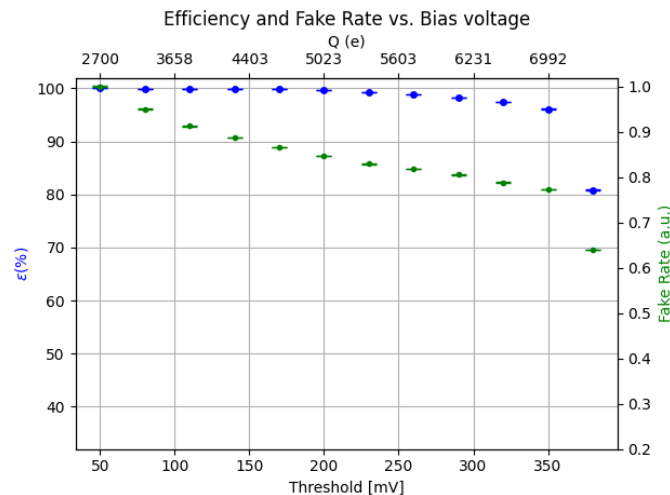
Bias voltage: 190 V



HEPHY topside biased



HEPHY backside biased

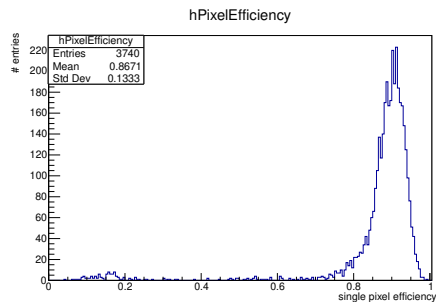


NIKHEF backside biased  
biased from top

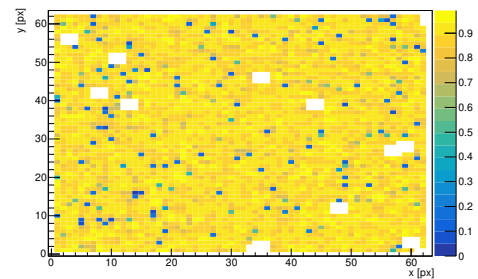
**HEPHY topside biased**  
Threshold: 365 mV  
Eff: 86 %

**HEPHY backside biased**  
Threshold: 365 mV  
Eff: 81 %

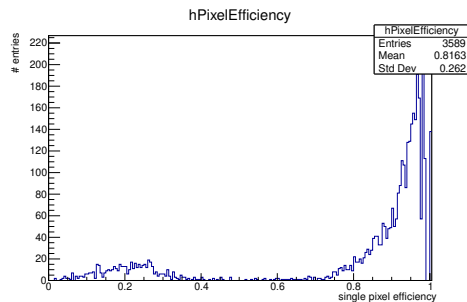
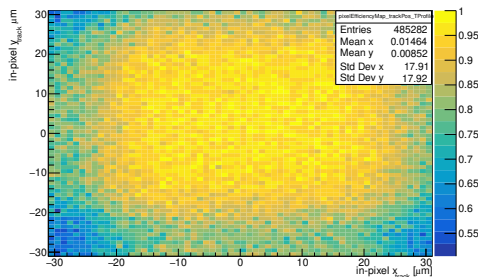
**NIKHEF backside biased from top**  
Threshold: 380 mV  
Eff: 80 %



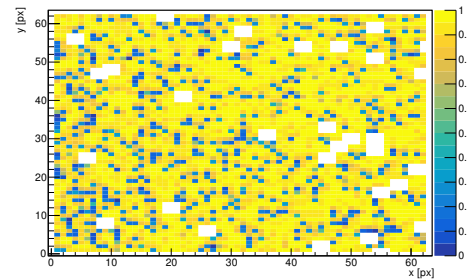
RD50\_MPWx\_base\_0 Chip efficiency map



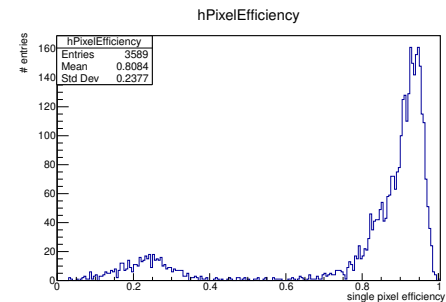
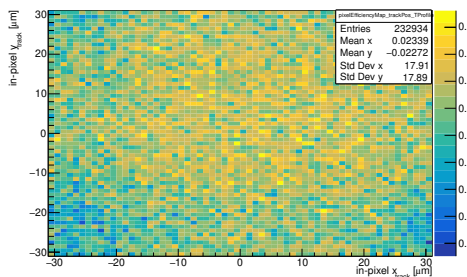
RD50\_MPWx\_base\_0 Pixel efficiency map



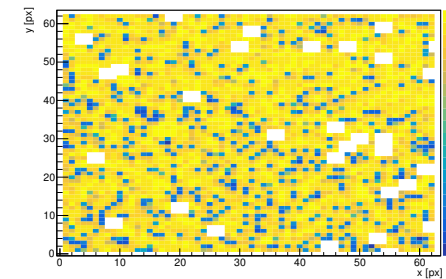
RD50\_MPWx\_base\_0 Chip efficiency map



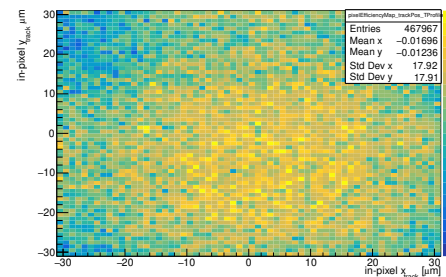
RD50\_MPWx\_base\_0 Pixel efficiency map



RD50\_MPWx\_base\_0 Chip efficiency map

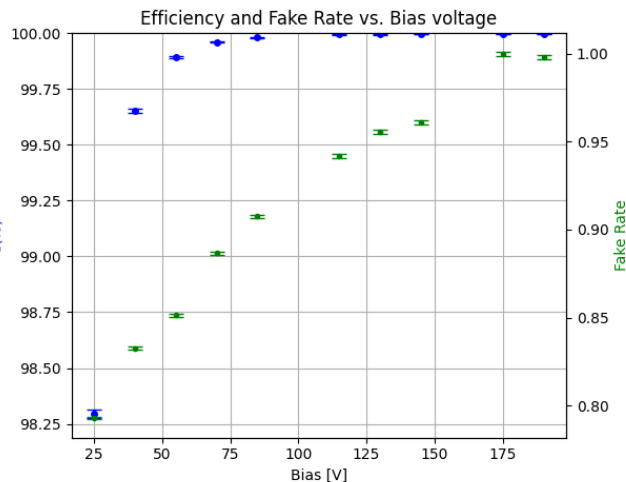


RD50\_MPWx\_base\_0 Pixel efficiency map



# Bias Voltage Scans

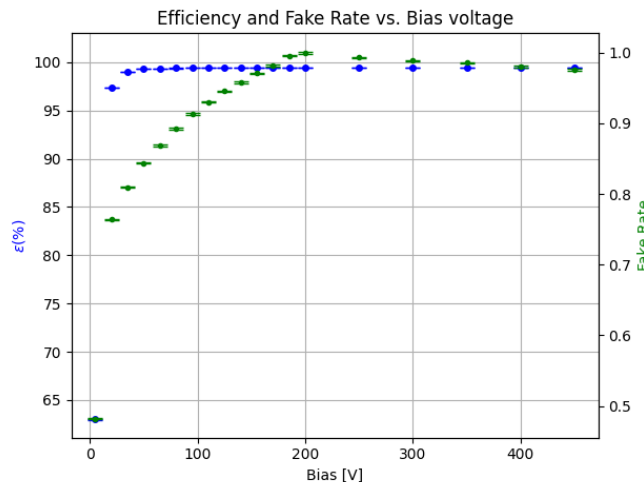
Attention: different scales!



**HEPHY topside biased**

Threshold: 20 mV

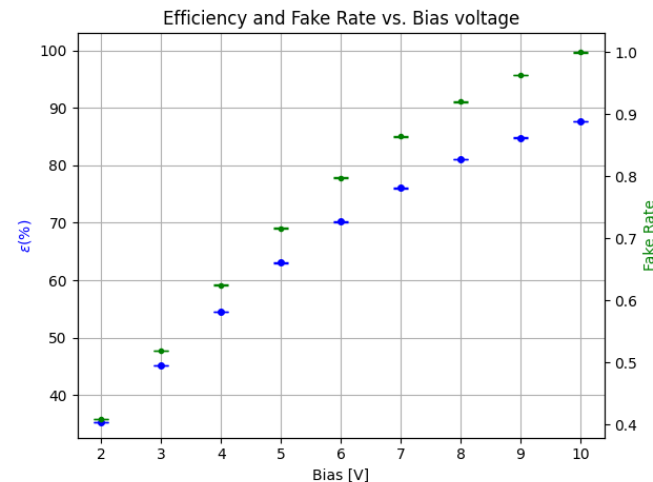
HV: 25-190 V



**HEPHY backside biased**

Threshold: 40 mV

HV: 5-450 V

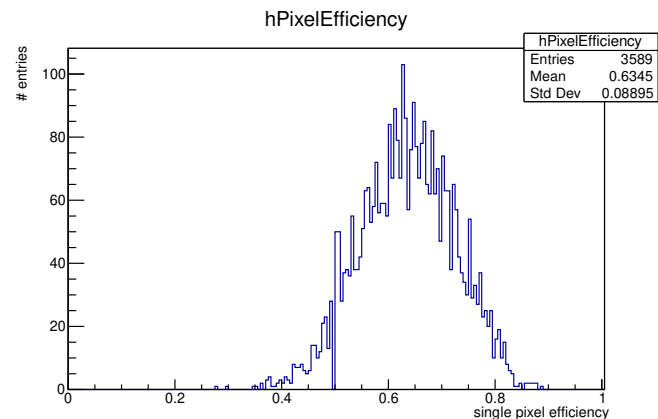


**HEPHY backside biased**

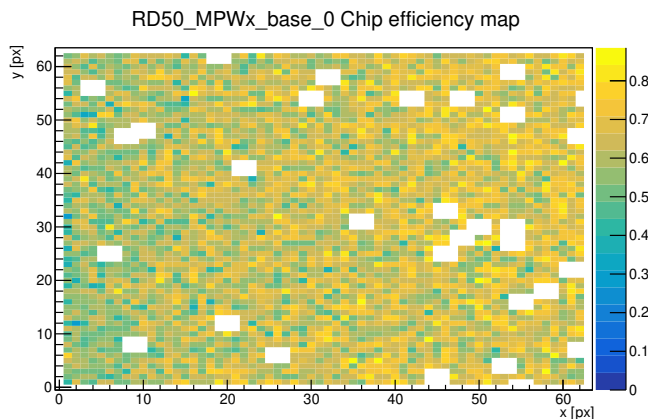
Threshold: 40 mV

HV: 2-10 V

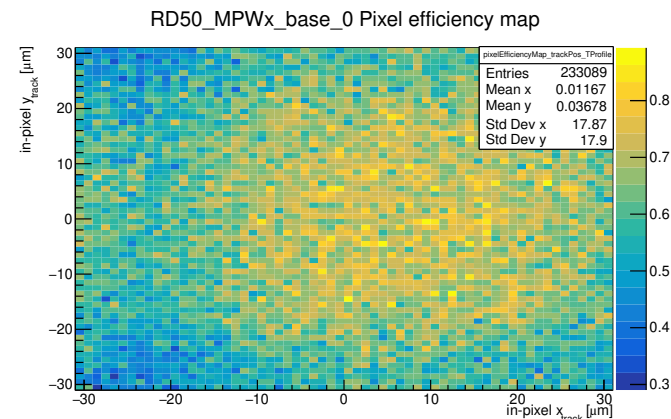
# Loss of Efficiency



Single Pixel efficiency



Chip efficiency



Pixel efficiency

**HEPHY backside biased**

Threshold: 20 mV

HV: 5 V

Eff: 63 %