Design a Moore Finite State Machine (FSM) with overlapping sequence detection for a sequential circuit.

Circuit Specifications:

- **Inputs:** Two single-bit inputs, X1 and X2.
- **Output:** One single-bit output, Z.
- **Initial Condition:** The initial output Z is 0.

Output Logic:
The output Z defaults to toggling its current value (i.e., if Z=0 it becomes 1, if Z=1 it becomes 0) unless one of the following two-step input sequences occurs:

1. **Sequence (X1,X2)=01 then (X1,X2)=11**: Upon detection of the second part of this sequence (11), the output Z **becomes 0**.
2. **Sequence (X1,X2)=10 then (X1,X2)=11**: Upon detection of the second part of this sequence (11), the output Z **becomes 1**.
3. **Sequence (X1,X2)=10 then (X1,X2)=01**: Upon detection of the second part of this sequence (01), the output Z **remains unchanged** from its value prior to this sequence.

Task:
Draw the state diagram for this Moore FSM. Ensure the design supports overlapping sequence detection, where the end of one detected sequence can serve as the beginning of another.