

2. Multi Clock Fan In

21 January 2025 10:35

Verilog Code

```
`timescale 1ns / 1ps
module multi_clk_fanin(
    input clk1,
    input clk2,
    input clk3,
    input in1,
    input in2,
    output reg out
);
    reg in1_d;
    always@(posedge clk1) begin
        in1_d <= in1;
    end
    reg in2_d,in_d1;
    always@(posedge clk2) begin
        in2_d <= in2;
    end
    assign in_d = in1_d & in2_d;
    always@(posedge clk3) begin
        in_d1 <= in_d;
        out <= in_d1;
    end
endmodule
```

XDC

```
set_property ASYNC_REG true [get_cells in_d1_reg]
set_property ASYNC_REG true [get_cells out_reg]
```

```
create_clock -period 10.000 -name clk1 -waveform {0.000 5.000} [get_ports clk1]
create_clock -period 20.000 -name clk2 -waveform {0.000 10.000} [get_ports clk2]
create_clock -period 40.000 -name clk3 -waveform {0.000 20.000} [get_ports clk3]
```

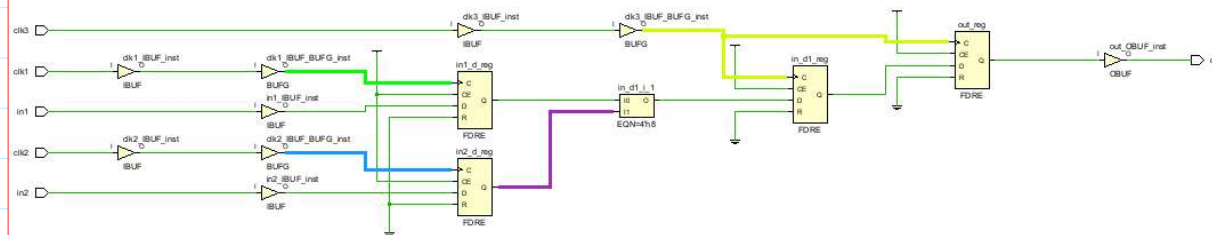
```
set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports in1]
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports in1]
```

```
set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports in2]
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports in2]
```

```
set_output_delay -clock [get_clocks clk3] -min -add_delay 0.600 [get_ports out]
set_output_delay -clock [get_clocks clk3] -max -add_delay 2.300 [get_ports out]
```

```
set_clock_groups -asynchronous -group [get_clocks clk1] -group [get_clocks clk2] -group [get_clocks clk3]
```

Schematic



CDC

Tcl Console | Messages | Log | Reports | Design Runs | **Timing** x

Summary (by type)

General Information	Severity	ID	Count	Description
Summary (by clock pair)	Critical	CDC-1	1	1-bit unknown CDC circuitry
Summary (by type)	Critical	CDC-10	2	Combinational logic detected before a synchronizer
Summary (by waived enc)				
CDC Details (3)				
clk1 to clk2 (1)				
clk1 to clk3 (1)				
clk2 to clk3 (1)				

Report CDC - cdc_1 (3 violations)

Here we can see that, there are two critical warning. So modification has to be done in the circuit.

STA

Design Timing Summary			
General Information	Setup	Hold	Pulse Width
Timer Settings			
Design Timing Summary	Worst Negative Slack (WNS): 5.895 ns	Worst Hold Slack (WHS): 0.045 ns	Worst Pulse Width Slack (WPWS): 4.500
Clock Summary (3)	Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000
Methodology Summary	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
> Check Timing (0)	Total Number of Endpoints: 3	Total Number of Endpoints: 3	Total Number of Endpoints: 7
> Intra-Clock Paths	All user specified timing constraints are met.		
Inter-Clock Paths			
Other Paths			
Report CDC - cdc_1 (3 violations)	Timing Summary - timing_1		

Solution to above problem

Verilog Code

```

`timescale 1ns / 1ps
module multi_clk_fanin(
    input clk1,
    input clk2,
    input clk3,
    input reset,
    input in1,
    input in2,
    output reg out
);

    reg ff_out1,ff_out3,ff_out4;
    reg ff_out2,ff_out5,ff_out6;
    reg resetn1,resetn2;
    reg ff_out21,ff_out22;
    always@(posedge clk3) begin
        resetn1 <= reset;
        resetn2 <= resetn1;
    end
    always@(posedge clk1 or posedge reset) begin
        if(reset) begin
            ff_out1 <= 'b0;
            ff_out3 <= 'b0;
            ff_out4 <= 'b0;
            ff_out5 <= 'b0;
        end else begin
            ff_out1 <= in1;
            ff_out3 <= ff_out2;
            ff_out4 <= ff_out3;
            ff_out5 <= ff_out4 & ff_out1;
        end
    end
    always@(posedge clk2) begin
        ff_out6 <= ff_out5;
        out <= ff_out6;
    end
    always@(posedge clk3 or posedge resetn2) begin
        if(resetn2) begin
            ff_out21 <= 'b0;
            ff_out22 <= 'b0;
            ff_out2 <= 'b0;
        end else begin
            ff_out21 <= in2;
            ff_out22 <= ff_out21;
            ff_out2 <= ff_out22;
        end
    end
endmodule

```

XDC File

```

set_property ASYNC_REG true [get_cells resetn1_reg]
set_property ASYNC_REG true [get_cells resetn2_reg]
set_property ASYNC_REG true [get_cells ff_out21_reg]
set_property ASYNC_REG true [get_cells ff_out22_reg]
set_property ASYNC_REG true [get_cells ff_out2_reg]
set_property ASYNC_REG true [get_cells ff_out3_reg]
set_property ASYNC_REG true [get_cells ff_out4_reg]
set_property ASYNC_REG true [get_cells ff_out5_reg]
set_property ASYNC_REG true [get_cells ff_out6_reg]
set_property ASYNC_REG true [get_cells out_reg]

create_clock -period 10.000 -name clk1 -waveform {0.000 5.000} [get_ports clk1]
create_clock -period 20.000 -name clk2 -waveform {0.000 10.000} [get_ports clk2]
create_clock -period 30.000 -name clk3 -waveform {0.000 15.000} [get_ports clk3]

set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports in1]

```

```

set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports in1]

set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports in2]
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports in2]

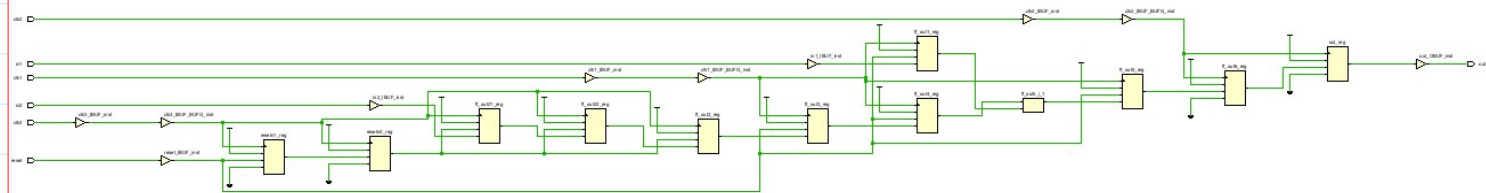
set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports reset]
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports reset]

set_output_delay -clock [get_clocks clk3] -min -add_delay 0.600 [get_ports out]
set_output_delay -clock [get_clocks clk3] -max -add_delay 2.300 [get_ports out]

set_clock_groups -asynchronous -group [get_clocks clk1] -group [get_clocks clk2] -group [get_clocks clk3]

```

Synth Result



CDC Result

Timing										
CDC Details										
<input checked="" type="checkbox"/> Critical warning (0) <input checked="" type="checkbox"/> Warning (0) <input checked="" type="checkbox"/> Info (4) Hide All										
General Information	Severity	ID	Description	Dep...	Exception	Source (From)	Destination (...)	Category	Source C...	Destinati...
Summary (by clock)	Info	CDC-3	1-bit synchronized with ASYNC_REG property	2	Asynch Clock Groups	ff_out2_reg/C	ff_out3_reg/D	Safe	clk3	clk1
Summary (by type)	Info	CDC-3	1-bit synchronized with ASYNC_REG property	2	Asynch Clock Groups	ff_out5_reg/C	ff_out6_reg/D	Safe	clk1	clk2
Summary (by waiver)	Info	CDC-3	1-bit synchronized with ASYNC_REG property	3	Asynch Clock Groups	in2	ff_out21_reg/D	Safe	clk1	clk3
CDC Details (4)	Info	CDC-3	1-bit synchronized with ASYNC_REG property	2	Asynch Clock Groups	reset	resetn1_reg/D	Safe	clk1	clk3
clk3 to clk1 (1)										
clk1 to clk2 (1)										
clk1 to clk3 (2)										
Report CDC - cdc_1 (4 violations)										

Problem Solved