

6. Synchronizer's

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A synchronizer is a device that samples an asynchronous signal and outputs a version of the signal that has transitions synchronized to a local or sample clock

Case 1: Normal Verilog Code where data is between two clocks

Verilog Code

```
module cdc1(  
    input wire clk1,  
    input wire clk2,  
    input wire d,  
    output reg out  
);  
    reg q;  
    always@(posedge clk1) begin  
        q <= d;  
    end  
    always@(posedge clk2) begin  
        out <= q;  
    end  
endmodule
```

XDC File

```
create_clock -period 10.000 -name clk1 -waveform {0.000 5.000} [get_ports clk1]  
create_clock -period 20.000 -name clk2 -waveform {0.000 10.000} [get_ports clk2]  
  
set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports d]  
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports d]  
  
set_output_delay -clock [get_clocks clk2] -min -add_delay 0.600 [get_ports out]  
set_output_delay -clock [get_clocks clk2] -max -add_delay 2.300 [get_ports out]  
set_clock_groups -asynchronous -group [get_clocks clk1] -group [get_clocks clk2]
```

STA Details

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.895 ns	Worst Hold Slack (WHS): 0.879 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 2	Total Number of Endpoints: 2	Total Number of Endpoints: 4
All user specified timing constraints are met.		

CDC Details

Tcl ConsoleMessagesLogReportsDesign RunsTiming x

Summary (by clock pair)

General Information

Summary (by clock pair)

Summary (by type)

Summary (by waived endpo

▼ CDC Details (1)

clk1 to clk2 (1)

Severity	Source Clock	Destination Clock	CDC Type	Exceptions	Endpoints	Safe	Unsafe	Unknown	No ASYNC
Critical	clk1	clk2	No Common Primary Clock	Asynch Clock Groups	1	0	0	1	

Sev...	ID	Description	Depth	Exception	Source (From)	Destin
Critical	CDC-1	1-bit unknown CDC circuitry	0	Asynch Clock Groups	q_reg/C	out_re

The major error in the above code is it is unable to understand that is 1-bit Unknown CDC Circuitry

Let us overcome the above issue by adding an synchronizer.

Case 2: Using an Synchronizer

Verilog Code

```
`timescale 1ns / 1ps
module cdc1(
  input wire clk1,
  input wire clk2,
  input wire d,
  output reg out
);
  reg q;
  always@(posedge clk1) begin
    q <= d;
  end
  reg out1;
  always@(posedge clk2) begin
    out1 <= q;
    out <= out1;
  end
endmodule
```

XDC File

```
create_clock -period 10.000 -name clk1 -waveform {0.000 5.000} [get_ports clk1]
create_clock -period 20.000 -name clk2 -waveform {0.000 10.000} [get_ports clk2]

set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports d]
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports d]

set_output_delay -clock [get_clocks clk2] -min -add_delay 0.600 [get_ports out]
set_output_delay -clock [get_clocks clk2] -max -add_delay 2.300 [get_ports out]
set_clock_groups -asynchronous -group [get_clocks clk1] -group [get_clocks clk2]
```

CDC Reports

Sev...	ID	Description	Dep...	Exception	Source (From)	Destination (...)	Ca
Warning	CDC-2	1-bit synchronized with missing ASYNC_REG property	2	Asynch Clock Groups	q_reg/C	out1_reg/D	Sa

STA Reports

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.895 ns	Worst Hold Slack (WHS): 0.152 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 3	Total Number of Endpoints: 3	Total Number of Endpoints: 5
All user specified timing constraints are met.		

The problem in the above code is it is missing the ASYNC_REG Property. To overcome that issue, let us modify the above code.

Case 3: To overcome the problem of missing ASYNC_REG.

Why to use Missing ASYNC_REG :

Synchronizer registers must have their ASYNC_REG property set to TRUE in order to preserve the cells through any logic optimization during synthesis and implementation, and to optimize their placement for the best mean time between failure (MTBF) statistics. (UG912)

Verilog Code

```

`timescale 1ns / 1ps
module cdc1(
    input wire clk1,
    input wire clk2,
    input wire d,
    output reg out
);
    reg q;
    always@(posedge clk1) begin
        q <= d;
    end
    reg out1;
    always@(posedge clk2) begin
        out1 <= q;
        out <= out1;
    end
endmodule

```

XDC File

```

set_property ASYNC_REG true [get_cells out1_reg]
set_property ASYNC_REG true [get_cells out_reg]

create_clock -period 10.000 -name clk1 -waveform {0.000 5.000} [get_ports clk1]
create_clock -period 20.000 -name clk2 -waveform {0.000 10.000} [get_ports clk2]

set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports d]
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports d]

set_output_delay -clock [get_clocks clk2] -min -add_delay 0.600 [get_ports out]
set_output_delay -clock [get_clocks clk2] -max -add_delay 2.300 [get_ports out]
set_clock_groups -asynchronous -group [get_clocks clk1] -group [get_clocks clk2]

```

CDC Reports

The screenshot shows the Xilinx IDE interface with the 'Timing' tab selected. The 'Summary (by type)' pane displays a table with the following data:

Severity	ID	Count	Description
Info	CDC-3	1	1-bit synchronized with ASYNC_REG property

The left sidebar shows the project hierarchy with 'CDC Details (1)' expanded, showing 'clk1 to clk2 (1)'. The bottom status bar indicates 'Report CDC - cdc_1 (1 violation)'.

STA Reports

Tcl ConsoleMessagesLogReportsDesign RunsTiming x

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (2)

Methodology Summary

Check Timing (0)

Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

Setup

Worst Negative Slack (WNS): 5.895 ns

Total Negative Slack (TNS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 3

Hold

Worst Hold Slack (WHS): 0.045 ns

Total Hold Slack (THS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 3

Pulse Width

Worst Pulse Width Slack (WPWS): 4.500 ns

Total Pulse Width Negative Slack (TPWS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 5

All user specified timing constraints are met.

Timing Summary - timing_1 xReport CDC - cdc_1 (1 violation) x

Case 4 Muti Bit Synchronizers

Verilog Code

```
`timescale 1ns / 1ps
module cdc1(
    input wire clk1,
    input wire clk2,
    input wire [1:0]d,
    output reg [1:0]out
);
    reg [1:0]q;
    always@(posedge clk1) begin
        q <= d;
    end
    reg [1:0]out1;
    always@(posedge clk2) begin
        out1 <= q;
        out <= out1;
    end
endmodule
```

XDC File

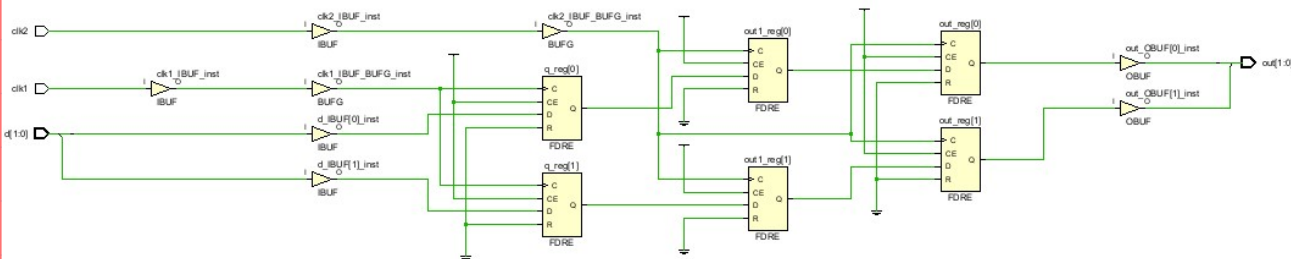
```
set_property ASYNC_REG true [get_cells out1_reg[*]]
set_property ASYNC_REG true [get_cells out_reg[*]]

create_clock -period 10.000 -name clk1 -waveform {0.000 5.000} [get_ports clk1]
create_clock -period 20.000 -name clk2 -waveform {0.000 10.000} [get_ports clk2]

set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports d[*]]
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports d[*]]

set_output_delay -clock [get_clocks clk2] -min -add_delay 0.600 [get_ports out[*]]
set_output_delay -clock [get_clocks clk2] -max -add_delay 2.300 [get_ports out[*]]
set_clock_groups -asynchronous -group [get_clocks clk1] -group [get_clocks clk2]
```

Schematic



CDC Report

Summary (by type)			
Severity	ID	Count	Description
Warning	CDC-6	1	Multi-bit synchronized with ASYNC_REG property

The reason for the above error is

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Keywords
Synchronizer

- Multi-Bit Synchronizer
- Asynchronous
- Reset Synchronizer

bus segments with continuous indexes that match a same CDC rule.

It is essential to understand that having a register-based synchronizer on a bus does not make the domain crossing safe for the bus. This is the reason the CDC rule CDC-6 is a Warning, as the tool cannot decide whether or not the topology is adequate for the design. It is up to the designer to confirm the safety of the CDC.

If the bus is Gray coded, it is safe to use a register-based synchronizer on all the bits of the bus as long as the adequate timing constraints have been set on the bus to make sure that no more than one data at a time can be captured by the receiving domain.

If the bus is not Gray coded, other synchronizer topologies should be used instead, such as CE Controlled CDC or MUX Controlled CDC.

Drawback : We cannot synchronize a pulse, from quick clock domain to moderate clock domain.
(Input clock_a = 10ns, clock_b = 20ns)

Therefore a pulse cannot be detected
To overcome this problem we go for Toggle Synchronizer.