

# 1. Combinational logic detected before a synchronizer

20 January 2025 18:10

## Verilog Code

```
`timescale 1ns / 1ps
module Comb_logic_sync(
    input clk1,
    input clk2,
    input in1,
    input in2,
    input din,
    output reg out
);
    reg q1;
    always@(posedge clk1) begin
        q1 <= din;
    end
    wire q2;
    assign q2 = q1 && in1 && in2;
    reg q3;
    always@(posedge clk2) begin
        q3 <= q2;
        out <= q3;
    end
endmodule
```

## XDC File

```
set_property ASYNC_REG true [get_cells q3_reg]
set_property ASYNC_REG true [get_cells out_reg]

create_clock -period 10.000 -name clk1 -waveform {0.000 5.000} [get_ports clk1]
create_clock -period 20.000 -name clk2 -waveform {0.000 10.000} [get_ports clk2]

set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports din]
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports din]

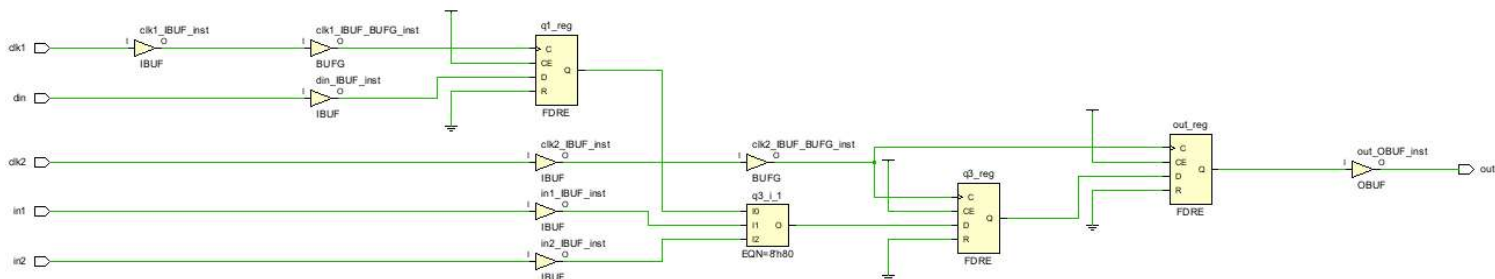
set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports in1]
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports in1]

set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports in2]
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports in2]

set_output_delay -clock [get_clocks clk1] -min -add_delay 0.600 [get_ports out]
set_output_delay -clock [get_clocks clk1] -max -add_delay 2.300 [get_ports out]

set_clock_groups -asynchronous -group [get_clocks clk1] -group [get_clocks clk2]
```

## Schematic



## CDC Result

Tcl ConsoleMessagesLogReportsDesign RunsTiming x

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clk1 to clk2

☒ Critical warning (1)

☒ Warning (0)

☒ Info (0)

Hide All

⚙

General Information

Summary (by clock pair)

Summary (by type)

Summary (by waived endpo

▼ CDC Details (1)

clk1 to clk2 (1)

Severity ^1	ID	Description	Depth	Exception	Source (From)	Destination (To)	Category
🟡 Critical	CDC-10	Combinational logic detected before a synchronizer	2	Asynch Clock Groups	q1_reg/C	q3_reg/D	Unsafe

The problem in the above circuit is here is an Combinational block before the synchronizer. This is not

Allowed. To overcome it, we need to use a flipflop after the combinational logic.

## Verilog Code

```
`timescale 1ns / 1ps
module Comb_logic_sync(
    input clk1,
    input clk2,
    input in1,
    input in2,
    input din,
    output reg out
);
    reg q1,q4;
    wire q2;
    always@(posedge clk1) begin
        q1 <= din;
        q4 <= q1 && in1 && in2;
    end
    reg q3;
    always@(posedge clk2) begin
        q3 <= q4;
        out <= q3;
    end
endmodule
```

## XDC

```
set_property ASYNC_REG true [get_cells q3_reg]
set_property ASYNC_REG true [get_cells out_reg]
```

```
create_clock -period 10.000 -name clk1 -waveform {0.000 5.000} [get_ports clk1]
create_clock -period 20.000 -name clk2 -waveform {0.000 10.000} [get_ports clk2]
```

```
set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports din]
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports din]
```

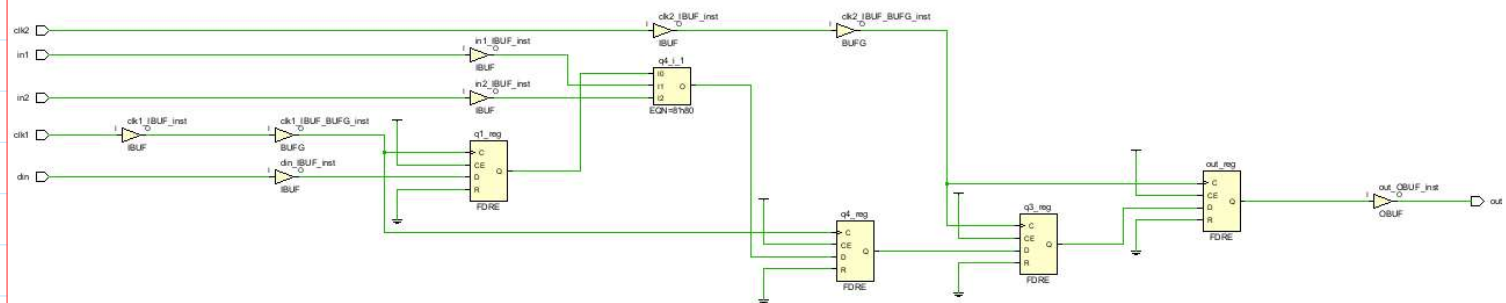
```
set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports in1]
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports in1]
```

```
set_input_delay -clock [get_clocks clk1] -min -add_delay 2.000 [get_ports in2]
set_input_delay -clock [get_clocks clk1] -max -add_delay 4.000 [get_ports in2]
```

```
set_output_delay -clock [get_clocks clk2] -min -add_delay 0.600 [get_ports out]
set_output_delay -clock [get_clocks clk2] -max -add_delay 2.300 [get_ports out]
```

```
set_clock_groups -asynchronous -group [get_clocks clk1] -group [get_clocks clk2]
```

## Schematic



## CDC

Tcl Console Messages Log Reports Design Runs Timing x

clk1 to clk2

General Information

Summary (by clock pair)

Summary (by type)

Summary (by waived endpoints)

▼ CDC Details (1)

clk1 to clk2 (1)

Severity	ID	Description	Depth	Exception	Source (From)	Destination (To)	Category
Info	CDC-3	1-bit synchronized with ASYNC_REG property	2	Asynch Clock Groups	q4_reg/C	q3_reg/D	Safe

## STA

Tcl Console Messages Log Reports Design Runs Timing x

Design Timing Summary

General Information  
Timer Settings  
Design Timing Summary  
Clock Summary (2)  
Methodology Summary  
Check Timing (0)  
Intra-Clock Paths  
clk1  
Setup 5.859 ns (2)  
Hold 0.313 ns (2)  
Pulse Width 4.500 ns (11)  
clk2  
Inter-Clock Paths

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.859 ns	Worst Hold Slack (WHS): 0.045 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 4	Total Number of Endpoints: 4	Total Number of Endpoints: 6

All user specified timing constraints are met.

Timing Summary - timing\_1 x Report CDC - cdc\_1 (1 violation) x

Problem Solved.