Verilog Assignment-2 Q2 Report

Design and Simulation of GCD Calculation Module

We have to design a Verilog module for calculating the Greatest Common Divisor (GCD) of two 8-bit numbers, A and B. The module, named Calculate_GCD, was later tested using a testbench (testbench.v) in the Vivado simulation environment.

Design Overview

The design.v Verilog module was designed to compute the GCD of two 8-bit numbers, A and B, using the Euclidean algorithm. It also provides two outputs, a_change and b_change, which indicate when the input values A and B change.

Calculate_GCD Module Details

The Calculate_GCD module is designed to calculate the Greatest Common Divisor (GCD) of two 8-bit numbers, A and B, using the well-known Euclidean algorithm.
Input Signals:
A (8 bits): Represents the first 8-bit number for GCD calculation.
B (8 bits): Represents the second 8-bit number for GCD calculation.
Clk: A clock signal for synchronous operation.
Output Signals:
C (8 bits): Represents the output GCD value, which is also an 8-bit number.
a_change (8 bits): Indicates when the input value A changes.
b_change (8 bits): Indicates when the input value B changes.
Internal Registers:
temp_A (8 bits): An internal register to store the current value of A
temp_B (8 bits): An internal register to store the current value of B
GCD Calculation:
The module employs a clocked process to perform the GCD calculation.
It uses the Euclidean algorithm, repeatedly subtracting the smaller of temp_A and temp_B from the larger until they are equal. The result is stored in C.
Whenever A or B changes, the current values are stored in temp_A and temp_B.
Additionally, a_change and b_change are updated .

Testbench Overview

The testbench.v module was created to verify the functionality of the design.v module. It simulates different scenarios to test the GCD calculation for various input values. The testbench monitors and displays the values of a_change, b_change, C (GCD), and Clk (clock) during simulation. In the test bench module, inputs given in Calculate_GCD module are defined as registers and the outputs are defined as wires

Test Cases

Test 1:
A is set to 4, B is set to 12.
Simulation is run for 100 time units.
Results: a_change is 4, b_change is 12, and C is equal to 4 (GCD of 4 and 12).

Test 2:
A is updated to 14, B is updated to 35.
Simulation is run for 100 time units.
Results: a_change is 14, b_change is 35, and C is equal to 7 (GCD of 14 and 35).