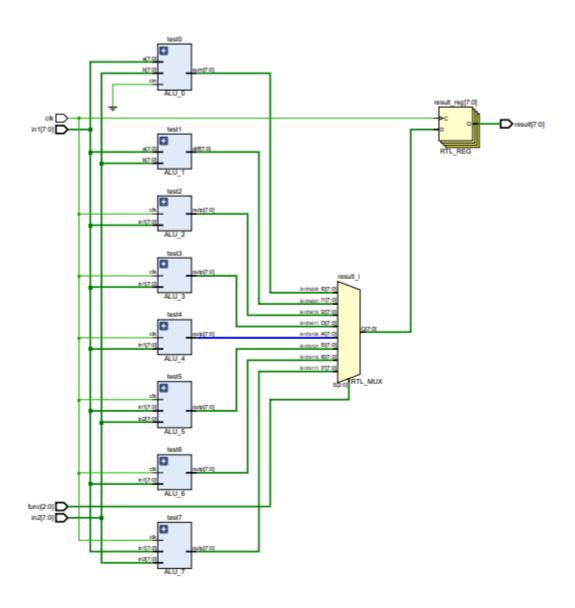
Project Report



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Top Level Module:

First we will write the top level module as module Top (in1, in2, func, clk, result); which takes inputs as 2 8-bit numbers in1,in2, a 3 bit input func which is used to choose one of the 8 functionalities and input clk used for synchronization, and the output result is declared as reg.

Sub Modules:

We write the 8 functionalities in 8 sub modules namely module ALU_0,module ALU_1,...module ALU_7 . Now , we initialize these sub modules in the top level module and we will declare 8 wires temp0,temp1,....temp7(which are declared as wires) to store the output of the submodules. Then we will use the switch case of input func to select the function and the output which is stored in the wire temp, and its value is assigned to the result.

Test Bench:

In TestBench.v, we gave inputs in1,in2 and func(ranging from 0 to 9) to choose an operation to be performed for in1 and in2.

For the input , in1=12, in2=12, func=0,clk ,function ALU_0 is triggered and hence , result will be assigned in1+in2, hence the output is 24.

For the input , in1=12, in2=8, func=1,clk ,function ALU_1 is triggered and hence , result will be assigned in1-in2, hence the output is 4.

For the input , in1=8, in2=12, func=2,clk ,function ALU_2 is triggered and hence , result will be assigned in1, hence the output is 8.

For the input, in1=8, in2=12, func=3,clk, function ALU_3 is triggered and hence, result will be assigned in 1<<1, hence the output is 8<<1=16.

For the input , in1=8, in2=12, func=4,clk , function ALU_4 is triggered and hence , result will be assigned in 1>>1, hence the output is 8<<1=4.

For the input , in1=8, in2=12, func=5,clk , function ALU_5 is triggered and hence , result will be assigned in1 AND in2, hence the output is in1 & in2=8.

For the input , in1=8, in2=12, func=6,clk , function ALU_6 is triggered and hence , result will be assigned \sim in1, hence the output is \sim (00001000)=247.

For the input, in1=8, in2=12, func=7,clk, function ALU_7 is triggered and hence, result will be assigned in1 | in2, hence the output is (8|12)=14.