Verilog Assignment -5 Report

Module substractor(y0, x0, bin, bout, diff) takes a 8-bit input 'x0' and a 8-bit input 'y0' and calculates the difference, we have to call this twice.

We are given a 32 bit input x and we have to find out the value of x/255 which is a 32 bit output y.

We will use y=256y-x

We will break this 32 bit input x as four bytes as , x3=x[0:7], x2=x[8:15], x1=x[16:23] , x0=x[24:31]

Similarly y as y={y3,y2,y1,y0};
256*y can be calculated by shifting y to 8 bits left, i.e, 256y= y3 y2 y1 y0 00000000
256y-x= y3 y2 y1 y0 00000000
(-) x3 x2 x1 x0
—----------
y3 y2 y1 y0
—----------
Using this logic , we design a Top_level module to calculate the value of y which takes input as x and outputs y.

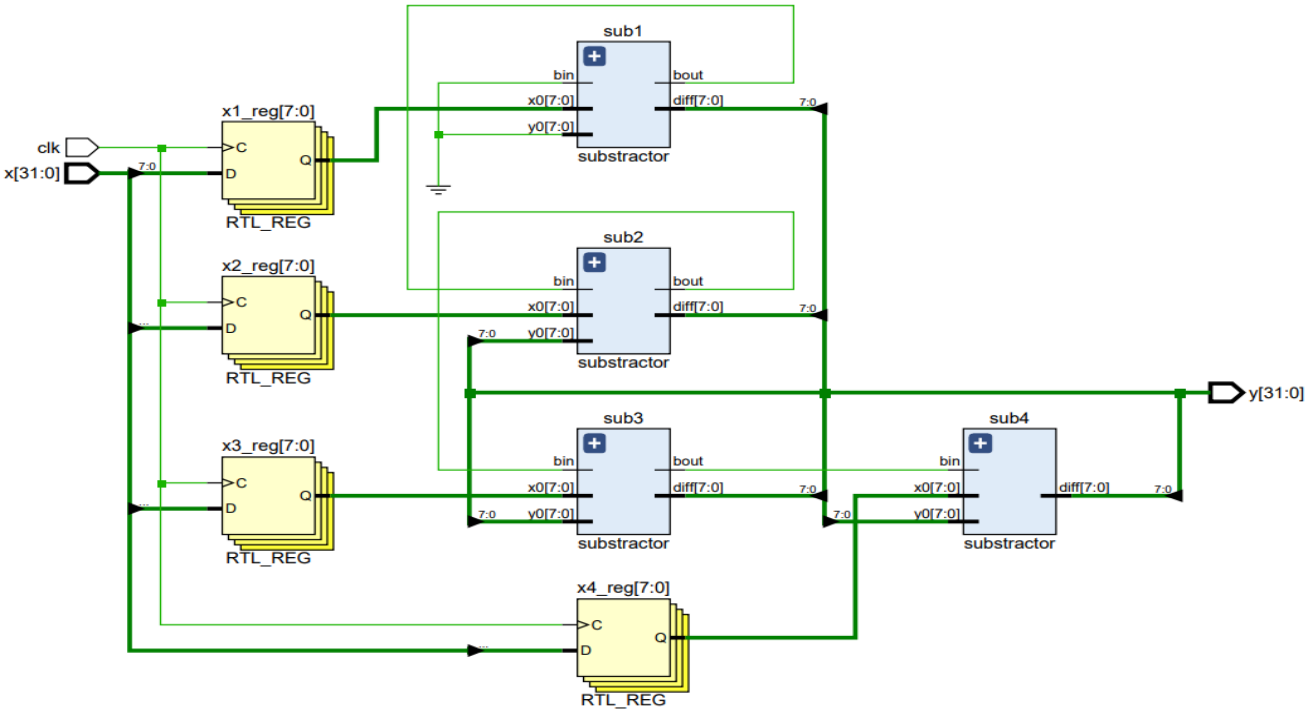
We will instantiate the subtractor module 3 times to calculate y2,y1,y0 each at a time.
To calculate the value of y0 , we will call :

```
substractor sub1(.y0(8'b00000000), .x0(x1), .bin(1'b0), .bout(b1), .diff(y1));
substractor sub2(.y0(y1), .x0(x2), .bin(b1), .bout(b2), .diff(y2));
substractor sub3(.y0(y2), .x0(x3), .bin(b2), .bout(b3), .diff(y3));
substractor sub4(.y0(y3), .x0(x4), .bin(b3), .bout(b4), .diff(y4));
```

Finally y is the concatenation of y3 y2 y1 y0 i.e, y={y3,y2,y1,y0}.

TestBench.v

Input 1: x=510 y=2
Input2: x=2550 y=10


clk
x[31:0]
7:0
x1_reg[7:0]
C
D
Q
RTL_REG
x2_reg[7:0]
RTL_REG
x3_reg[7:0]
RTL_REG
x4_reg[7:0]
RTL_REG
sub1
bin
bout
x0[7:0]
y0[7:0]
diff[7:0]
substractor
sub2
substractor
sub3
substractor
sub4
substractor
y[31:0]