Project Report
Verilog Assignment 6

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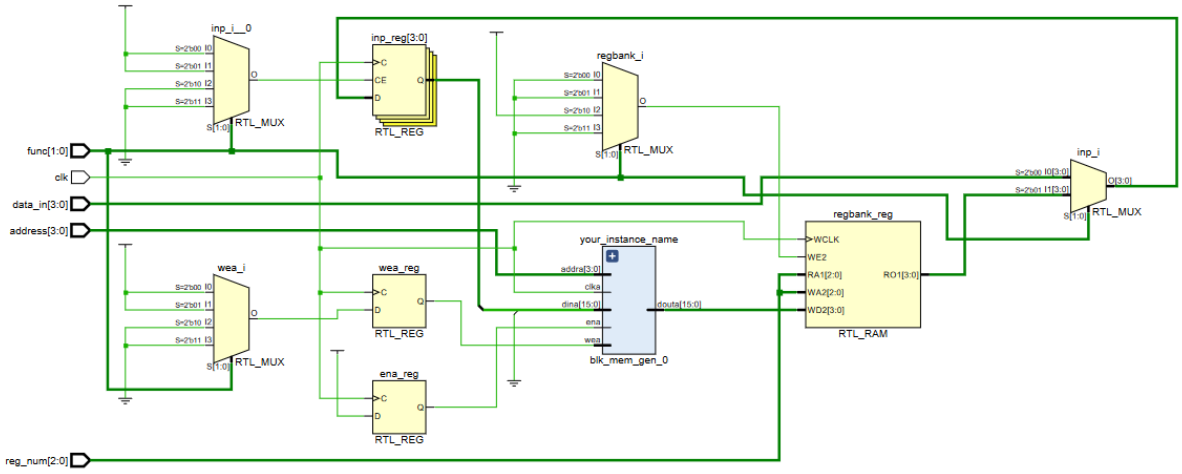
Diagram :



We have to design and implement an interface between an 8x4 register bank and a 16x4 memory system, enabling data transfer through specified read and write control signals

First ,create a 16x4 memory system in Vivado, by setting the number of bits required to 4 to address 16 memory blocks. The generated blk_mem_gen_0 has its inputs as input wire .clka(clock), input wire .ena which is read control signal, input wire [0 : 0] wea which is the write control signal, input wire [3 : 0] address, input wire [3 : 0] data_in which is the 4-bit data input, and an output data_out

Implementation :

Design.sv

Top Level module(opcode,reg_num,dina,clka,addra) declares a Verilog module with inputs as input opcode which refers to a 2 bit number to select the operation to be performed, a 3 bit input reg_num,a 4-bit data input, clock clk, and a 4-bit address register.We also define reg[3:0] regbank[0:7] which has 8 four bit registers.

When the opcode is set to :->

2'b00 : it triggers the first operation which reads a 4-bit data and stores it into a specified memory location with a 4-bit address.
Therefore , read signal ena and write signal wea are set to 1, and dina is set to the 4 bit data input

2'b01: It triggers the second operation which states, given a register number and a memory address, transfer data from register to memory.
Therefore, read signal ena write signal wea are set to 1, and inp=regbank[reg_num];

2'b10: It triggers the third operation which states, given a register number and a memory address, transfer the data from memory to register.
Therefore, only the read signal is set to 1 and regbank[reg_num]=douta is done.

2'b11: It triggers the fourth operation which states, given a memory address, display the contents of the memory location.
Therefore we set read input to 1 , and display the data output from dout as $display($time," dout is %d",douta)

TestBench.sv

Test Case 1:

func=0, address =1, data_in=4 (data_in stored in memory address)

- In this step we are storing the value of data_in i.e 4 in the specified memory i.e address 1

Test Case 2:

func=3,

- In this step we are displaying the content of the memory location, and since the address is still one , the contents we have just put in data_in will be displayed

Test Case 3:

func=2, reg_num=1 (transfer data from memory to register)

- In this step we transfer the memory form the memory address which is 1 to the specified register number which is 1

Test Case 4:

func=1, address=5, reg_num=1 (transfer data from register to memory)

- In this step we transfer the memory form the reg_num to the corresponding memory location address which is 5

Test Case 5:

func=3, address=5

- In this step we are going to display the contents in the memory location address which is 5, since we have transferred the register memory into the memory address 5 in the previous step, that will be displayed .