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Project Report
Verilog Assignment 4

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Given 2 8-bit numbers as inputs , we have to return the output as per Booth's Multiplication Algorithm.

Working of the Module:

module BoothMul(clk, rst, start, A, M, valid, Z); declares a Verilog module named BoothMul with inputs as input clk,input rst,input start, input A,M and outputs as output Z and output valid.

We declare Z, next_Z, Z_temp , next_state, pres_state, valid, next_valid,temp,next_temp,count, next_count as registers. Z, next_Z, and Z_temp are used to hold the current and next values of the result and temporary values during calculations. temp and next_temp are used to hold and update temporary values during multiplication, and count and next_count are used to keep track of the bit position being processed. There is also a register valid and next_valid to hold and update the validity of the result. IDLE is set to 1'b0, and START is set to 1'b1.

There is an always block that is sensitive to the positive edge of the clock (posedge clk) or the negative edge of the reset (negedge rst). It handles the reset condition (if (!rst)) by setting various registers to their initial values. When not in reset, it updates the output registers based on their next values.

Then we run a nested case statement based on the temp variable, which represents the current operation to be performed in the Booth algorithm.
Depending on the value of temp, it performs either subtraction or addition operation and calculates the new value for Z_temp.
We then update various registers based on the values of count and Z_temp for the current state.

Test Bench:

The Verilog testbench booth_tb simulates the BoothMul module with several test cases, verifying its functionality for different input values.

The testbench initializes the inputs, triggers multiplication with different test cases, waits for the output to become valid (posedge valid), and then compares the computed results.
Inputs A,M,start,clk,rst are declared as registers and output Z is declared as wire.

Test cases:

A=5 , M=3, output=15
A=5, B=-3 , output = -15
A=-5, B=-3 , output = 15
A=0, B=-3 , output = 0