LAB 1 – Introduction to Xilinx/AMD Vivado, VHDL and Nexys Board

Learning Objectives

- Getting started with Xilinx/AMD Vivado tools and Nexys 4/DDR/A7 FPGA board
- Learn basics of VHDL design entry.
- Understand the use of functional simulation, synthesis and testbeds.
- Understand the concept of FPGA programming.

This lab contains two parts:

1. Part 1: A semi-guided and step-by-step tutorial to be familiar with the hardware and software tools. Teaching staff will guide students for this part with supporting learning material presented on Blackboard.
2. Part 2: An individual lab task which is assessed.

Part 1: A semi-guided tutorial for tools (to be completed in week 1)

Complete the tutorial activities from 1.1-1.5 on Blackboard under prac 1 folder. Teaching staff will provide explanations and will guide you through these steps. You must complete these tutorial activities first before attempting the assessed lab task given below.

Part 2: Lab Task – 4-input Majority Vote Function (to be completed in week 2)

In this task, you are required to provide a VHDL dataflow description, simulate, synthesise and test a 4-input Majority Vote function where the output F is high if and only if the majority (i.e., 3 or more) of inputs A, B, C, D are set to high (a 3-input example was done in lecture 1). Complete the following steps and submit a report containing the required items.

(a) Provide the truth table with inputs A, B, C, D and output F (required in the report)
(b) Describe the design in VHDL with dataflow abstraction (required in the report)
(c) Perform the functional simulation. Provide the following in your report:
    (i) Evidence of correct functional simulation with clearly visible simulation waveform outputs from Vivado. Must include all 16 input combinations.
    (ii) One simulation scenario where a 10ns output delay is modelled (for simulation purposes) in your dataflow description – i.e., the output should change after a propagation delay of *10ns* from the respective input change.
    (iii) Evidence of self-checking testbench (with assert/report statement) with one example showing an error – i.e., create an error on purpose in your design file and show that it is captured in your simulation output on the Tcl console.
(d) Perform synthesis and implementation. Provide the following in your report:
    (i) RTL schematic (obtained after RTL analysis/elaborate design step)
    (ii) Synthesis schematic (obtained after synthesis)
    (iii) FPGA resource summary after implementation step
(e) [Optional – not assessed] Test your design on Nexys board with inputs A, B, C, D connected to switches SW0-SW3, respectively and output F connected to LED0.

Submission and Assessment

You will be assessed based on a report submission followed by oral assessment. Submit a short report (electronically typeset) in PDF format via Blackboard containing the following:

- Short introduction to the task [1 mark]
- Block diagram of the design with properly labelled inputs, outputs, and their sizes [1 mark]
- Truth table for the given task [1 mark]
- VHDL description of the design – may be included in an appendix [3 marks]
- Functional simulation with items (c)-(i), (c)-(ii), (c)-(iii) mentioned above [4 marks]
- Synthesis/Implementation results with items (d)-(i), (d)-(ii), (d)-(iii) above [3 marks]
- Short conclusion identifying any issues, potential improvements and/or your reflection of the task [1 mark]
- References if any

The report should not be just a collection of screenshots, but with proper explanation of figures/results with some discussion. The report is **due on Monday 5/08/2024 4:00 pm AEST**.

Oral assessment: Conducted during scheduled lab sessions in week 3. You need to explain your design to teaching staff followed by some Q&A to check the understanding of your work. Marks for the oral assessment will be distributed as follows:

0: No knowledge of the design **(total mark capped at 0)**
1: Very little knowledge of the design **(total mark capped at 50%)**
2: Reasonable knowledge of the design
3: Good knowledge of the design
4: Excellent knowledge of the design

Total mark for this lab is out of 18, subject to oral assessment caps as above and any late penalties as outlined in the ECP. If you do not attend/complete the oral assessment, your marks for this lab will be capped at 0.