Laboratory Assignment 2: Transistors as Switches

ECE 0201: Digital Circuits and Systems

45 Points

Name

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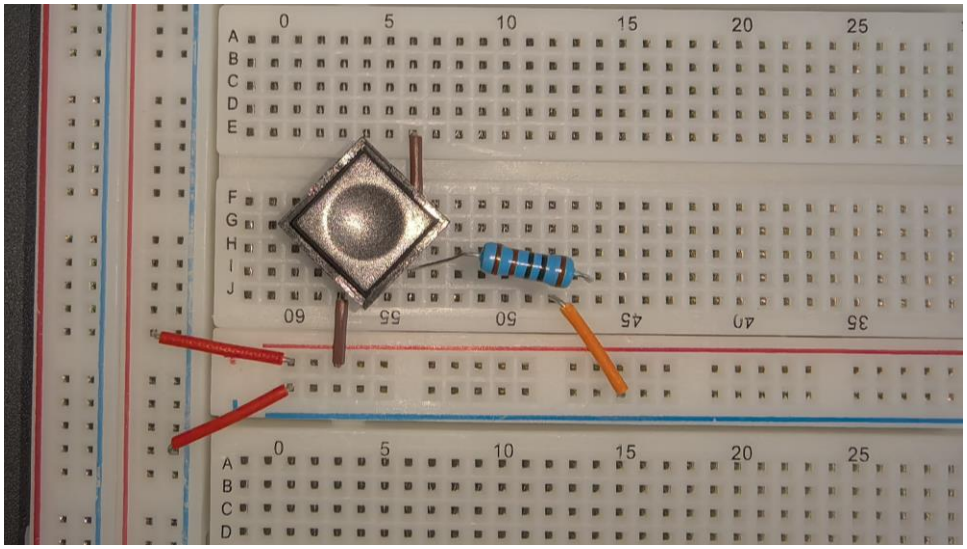
Submission Checklist:

- ☐ Write within boxes, do not move boxes
- ☐ Write your full name in the box above
- ☐ Save this file as a PDF before uploading, keep the number of pages (**13**) unchanged
- ☐ Note “TO BE CONTINUED” in the answer box if you used the extra pages (11-13)

Part I: Building a General Logic Source (1 point)

[(A) Insert a picture of your build of the circuit in Figure 1] (0.5 points)

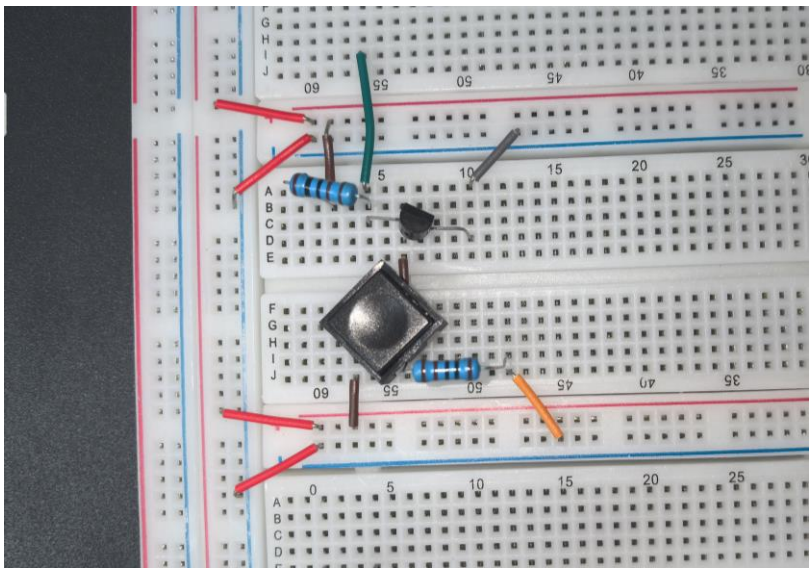


[(B) Fill out the following information] (0.5 point)

V_x when the switch is closed = 4.9978V
V_x when the switch is opened = -0.038mV

Part II: The NMOS Inverter (9 points)

[(A) Insert a picture of your build of the circuit in Figure 6] (0.5 points)



[(B) Fill out the following information] (1.0 points)

S1	V_{in}	V_{out}	LED (on/off)
Open	-0.013mV	4.9753V	ON
Closed	4.9842V	8.042mV	OFF

[(C) Select a logic abstraction and draw a truth table for logical values (0/1)] (2 points)

Logic abstraction: NOT gate

S1	Result
0	1
1	0

Note:

for S1, open is 0, close is 1

for result(LED), ON is 1, OFF is 0

The result is **opposed** to the input, which can be regarded as **NOT gate**.

NMOS Inverter with R1 = 10kΩ (5.5 points)

[(A) Fill out the following information] (1.0 points)

S1	V_{in}	V_{out}	LED (on/off)
Open	-0.007mV	4.9708V	ON
Closed	4.9978V	0.921mV	OFF

[(B) Select a logic abstraction and draw a truth table for logical values (0/1)] (2 points)

Logic abstraction: NOT gate

S1	Result
0	1
1	0

Note:

for S1, open is 0, close is 1

for result(LED), ON is 1, OFF is 0

The result is **opposed** to the input, which can be regarded as **NOT gate**.

[(C) Compare V_{in} and V_{out} measurements to V_{DD} and GND. Explain, in terms of known circuit laws, the values you obtained.] (1.5 points)

When **V_{in} is big enough**, there is **enough voltage differences between G and S** of the NMOS, the NMOS will operate as if it were a **closed switch**, so the **V_{out} is small**, the **LED is off**.

When **V_{in} is small**, there is **not enough voltage differences**, the NOMS will act as an **open switch**, so the **V_{out} is large**, the **LED is on**.

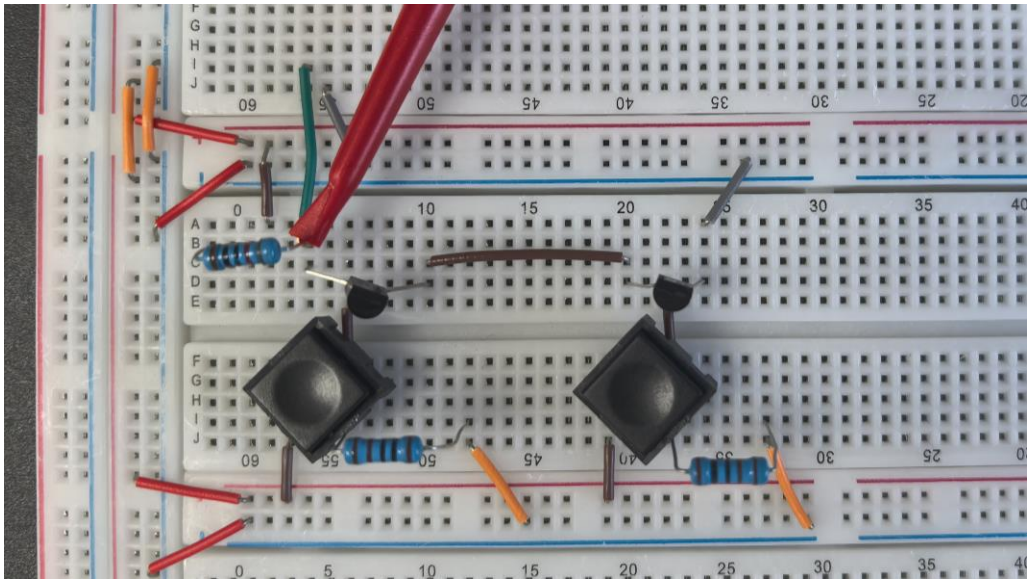
[(D) Explain why the measured voltage (V_{out}) changes with resistance.] (1 point)

When the **MOSFET is OFF**, the resistor (R) and voltmeter are connected in series. Since the **voltmeter has a constant internal resistance and the resistor's resistance increases**, an increase in R will result in a **larger voltage drop** across R, leaving a smaller voltage for the voltmeter to measure.

When **the MOSFET is ON**, a larger R **reduces the current** flowing through the circuit. Consequently, the voltmeter will detect a **smaller voltage drop**, reflecting the diminished current.

Part III: The NMOS NAND Gate (9.5 points)

[(A) Insert a picture of your build of the circuit] (0.5 points)



[(B) Fill out the following information] (2 points)

S1 (A)	S2 (B)	V_{out}	LED (on/off)
Open	Open	4.9753V	ON
Open	Closed	4.9748V	ON
Closed	Open	4.9752V	ON
Closed	Closed	15.000mV	OFF

[(C) Select a logic abstraction and draw a truth table for logical values (0/1)] (2 points)

Logic abstraction: NAND gate

S1	S2	Result
0	0	1
0	1	1
1	0	1
1	1	0

Note:

for switches (S1,S2), open is 0, close is 1

for result(LED), ON is 1, OFF is 0

The result is 0 **if and only** if two inputs are **both** 1, which can be regarded as **NAND gate**.

NMOS NAND Gate with R1 = 10kΩ (5 points)

[(A) Fill out the following information] (2 points)

S1 (A)	S2 (B)	V_{out}	LED (on/off)
Open	Open	4.9708V	ON
Open	Closed	4.9703V	ON
Closed	Open	4.9703V	ON
Closed	Closed	1.781mV	OFF

[(B) Select a logic abstraction and draw a truth table for logical values (0/1)] (2 points)

Logic abstraction: NAND gate

S1	S2	Result
0	0	1
0	1	1
1	0	1
1	1	0

Note:

for switches (S1,S2), open is 0, close is 1

for result(LED), ON is 1, OFF is 0

The result is 0 **if and only** if two inputs are **both** 1, which can be regarded as **NAND gate**.

[(C) Which resistor value works better in this circuit in terms of the circuit's logic output (High/Low)? Why?] (1 point)

The **smaller resistor value (1kΩ)** works better than the larger one for R1 in this NAND gate circuit.

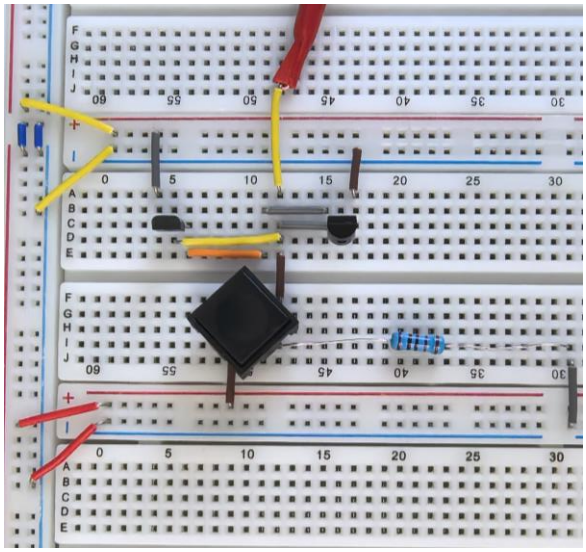
The **smaller R1 (10kΩ)** provides **stronger pull-up capability** when the MOSFETs are off, which **ensures the output (V_{out}) is pulled firmly to the High level** even when driving light loads, minimizing voltage drops caused by loads.

The **larger R1 (10kΩ)** weakens the pull-up ability, making V_{out} **more susceptible to voltage drops** under load, which could **blur the distinction** between High and Low levels.

[(D) Demonstrate your circuit to the TA for the first Lab 2 check-off .] (7 points)

Part IV: The CMOS Inverter (5.5 points)

[(A) Insert a picture of your build of the circuit] (0.5 points)



[(B) Fill out the following information] (1.0 points)

S1	V_A	V_{out}	LED (on/off)
Open	-0.036mV	4.9758V	ON
Closed	4.9979V	19.436mV	OFF

[(C) Select a logic abstraction and draw a truth table for logical values (0/1)] (2 points)

Logic abstraction: NOT gate

S1	Result
0	1
1	0

Note:

for S1, open is 0, close is 1

for result(LED), ON is 1, OFF is 0

The result is **opposed** to the input, which can be regarded as **NOT gate**.

[(D) How does one switch control 2 transistors? Under what conditions are both transistors turned on? Why?] (2 points)

Both transistors share the same control signal because **their gates(G) are connected together** and driven by the same voltage V_A.

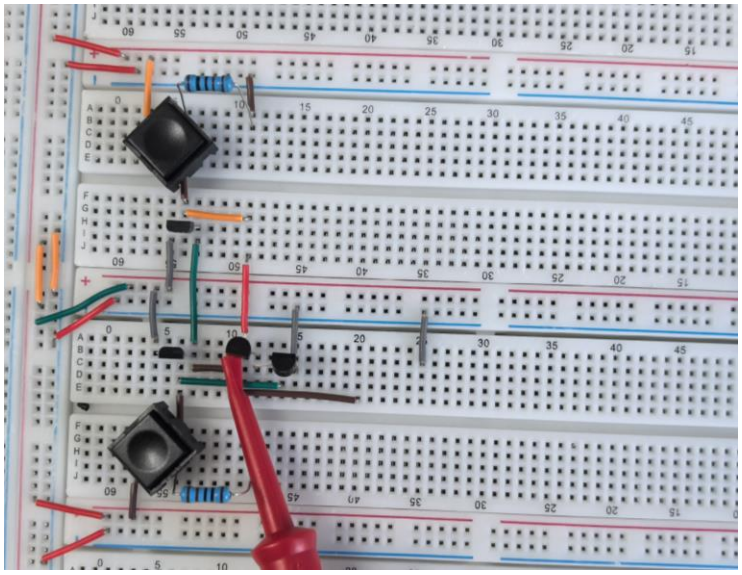
When $\boldsymbol{V_A = 0V}$, the PMOS has a negative gate-to-source voltage and **turns on**, while the NMOS has zero gate-to-source voltage and **remains off**. When $\boldsymbol{V_A = 5V}$, the **PMOS turns off** and the **NMOS turns on**.

When V_A is at a mid-level voltage, **both transistors meet their conduction conditions** and are **on** simultaneously.

This happens because the PMOS conducts when **its gate is lower than its source**, and the NMOS conducts when **its gate is higher than its source**.

Part V: The CMOS NAND Gate (20 points)

[(A) Insert a picture of your build of the circuit] (0.5 points)



[(B) Fill out the following information] (2 points)

S1 (A)	S2 (B)	V_A	V_B	V_{out}	LED (on/off)
Open	Open	0.014mV	0.991V	4.9080V	ON
Open	Closed	0.063mV	4.998V	4.998V	ON
Closed	Open	4.909V	0.728V	4.907V	ON
Closed	Closed	4.905V	4.919V	0.991mV	OFF

[(C) Select a logic abstraction and draw a truth table for logical values (0/1)] (2 points)

Logic abstraction: NAND gate

S1	S2	Result
0	0	1
0	1	1
1	0	1
1	1	0

Note:

for switches (S1,S2), open is 0, close is 1

for result(LED), ON is 1, OFF is 0

The result is 0 **if and only** if two inputs are **both** 1, which can be regarded as **NAND gate**.

[(D) What is the difference between an NMOS NAND gate and a CMOS NAND gate?] (1.5 points)

An **NMOS NAND gate** uses only NMOS transistors with pull-up resistors, so it **consumes power when it stand-by** and **cannot** drive a full logic high.
A **CMOS NAND gate** uses both PMOS and NMOS transistors in **complementary pairs**, so it **can** drive a full logic high, and very **low static power consumption**.

[(E) Demonstrate your circuit to the TA for the second Lab 2 check-off.] (7 points)

EXTRA PAGES

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