**Laboratory Assignment 3: Integrated Circuit Digital Logic Gates**

**ECE 0201: Digital Circuits and Systems**

**45 Points**

**Name**

张鹤扬 Stefan Zhang

**Submission Checklist:**

 Write within boxes, do not move boxes

 Write your full name in the box above

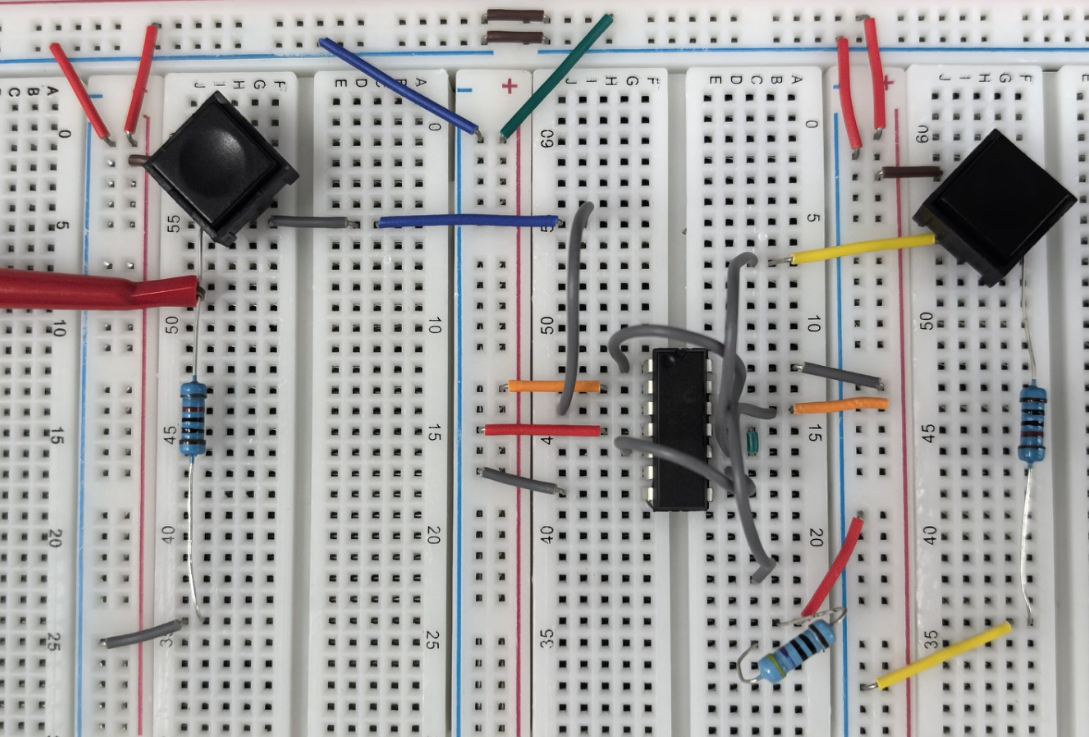
 Save this file as a PDF before uploading, keep the number of pages (**9**) unchanged

 Note “TO BE CONTINUED” in the answer box if you used the extra pages (7-9)

**Part I: Integrated Circuits (9 points)**

**2-input NAND gate using CD4007**

[(A) Insert a picture of your build of the circuit in Figure 5] (2 points)



[(B) Fill out the following information] (4 points)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| S1 (A) | S2 (B) | VA | VB | VOut | LED (on/off) |
| Open | Open | -0.005mV | 0.2675mV | 4.9989V | ON |
| Open | Closed | 0.001mV | 4.9989V | 4.9989V | ON |
| Closed | Open | 4.9986V | 0.0769mV | 4.9987V | ON |
| Closed | Closed | 4.9985V | 4.9985V | 0.891mV | OFF |

[(C) Select a logic abstraction, draw a truth table for the inputs and outputs] (3 points)

Logic abstraction: NAND gate

Input for switches: open is 0, closed is 1

Output for LED: ON is 1, OFF is 0

The chart shows that the output is 0 only if two switches are closed, which can be regarded as NAND logic gate.

|  |  |  |
| --- | --- | --- |
| S1 | S2 | Result |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Part II: 7400-Series Logic C (10 points)**

[(A) Fill out the following information] (2 points)

Number of transistors in the 7402: 16

[(B) Insert a picture of your circuit] (2 points)

架子上整齐的摆放着一些物品

AI 生成的内容可能不正确。

[(C) Fill out the following table] (4 points)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S1 | S2 | VA | VB | VOut |
| Open | Open | 8.720mV | 8.204mV | 4.9987V |
| Open | Closed | 0.456mV | 4.9978V | 5.070mV |
| Closed | Open | 4.9978V | 0.049mV | 2.448mV |
| Closed | Closed | 4.9978V | 4.9976V | 0.299mV |

[(D) Draw a truth table for the gate] (2 points)

Logic abstraction: NOR gate

Input for switches: open is 0, closed is 1

Output for LED: ON is 1, OFF is 0

The chart shows that the output is 1 only if two switches are open, which can be regarded as NOR logic gate.

|  |  |  |
| --- | --- | --- |
| S1 | S2 | Result |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**Part III: Design of an Exclusive-OR Circuit (26 points)**

[(A) Draw a truth table for a 2-input exclusive-OR (XOR) gate] (2 points)

Input for switches: open is 0, closed is 1

Output for LED: ON is 1, OFF is 0

|  |  |  |
| --- | --- | --- |
| S1 | S2 | Result |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

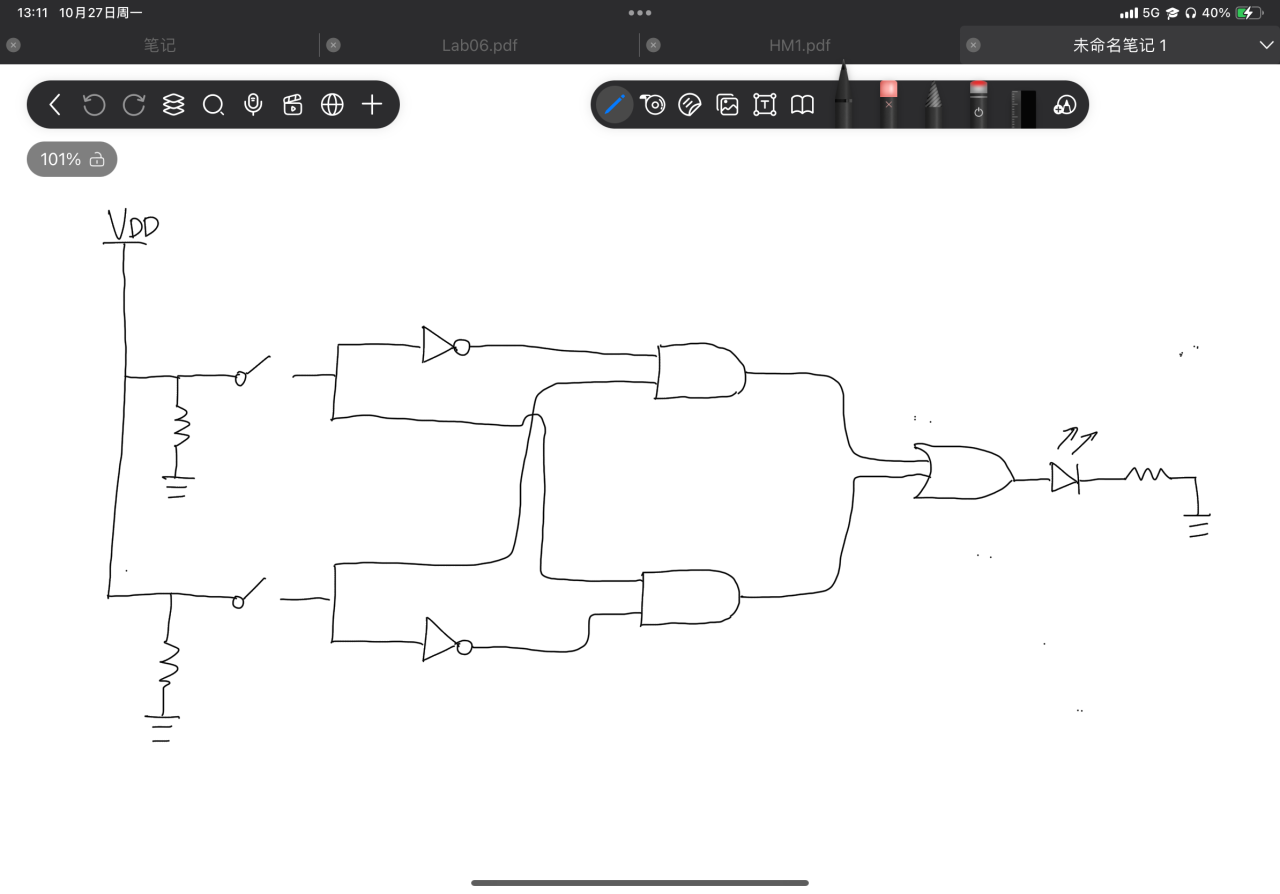
[(B) Write a logic function that represents the exclusive-OR operation] (2 points)

B

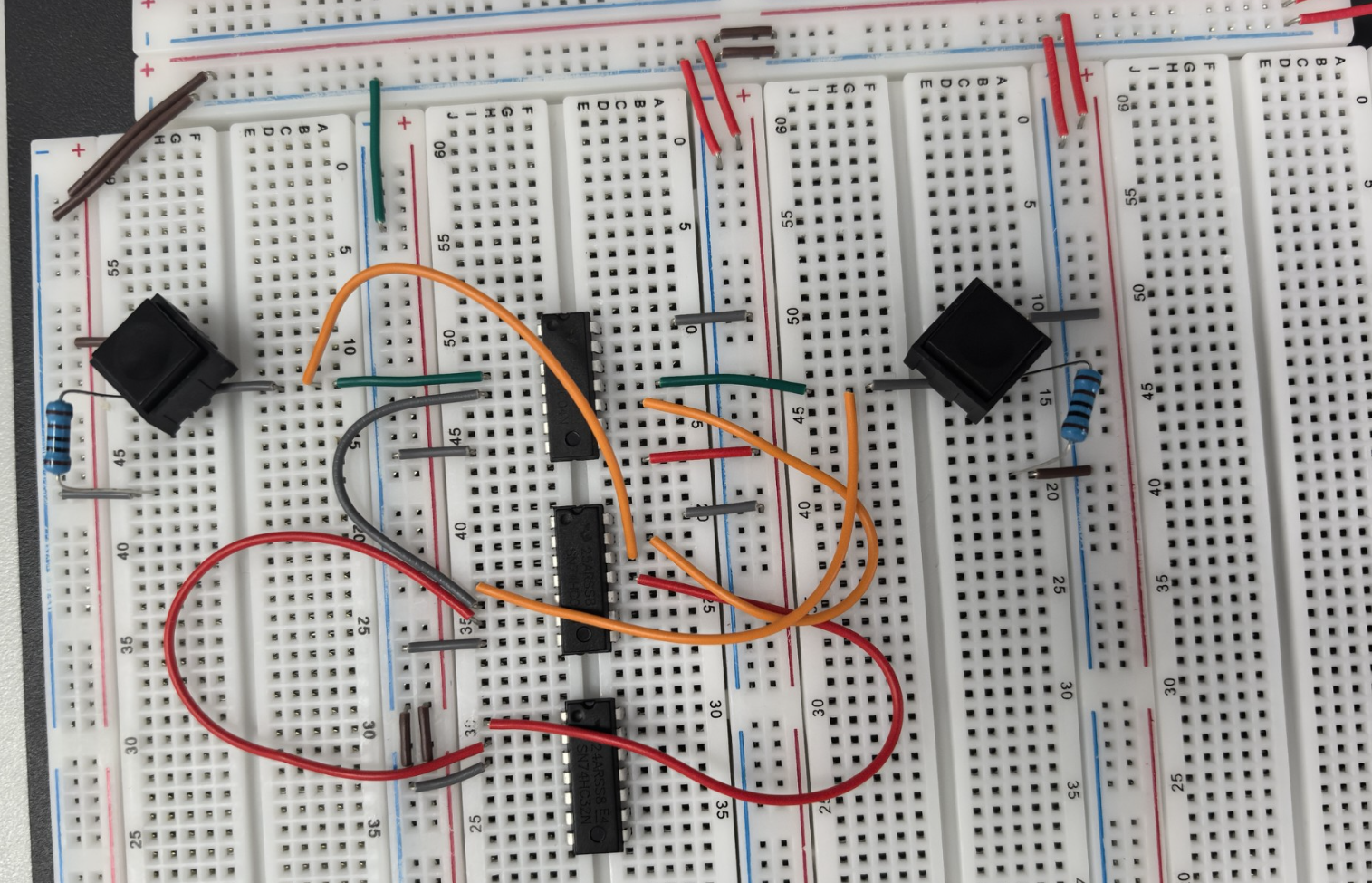
F

A

[(C) Draw a circuit that implements your logic function for the exclusive-OR operation] (2 points)



[(D) Insert a picture of your circuit] (2 points)



[(E) Fill out the following table] (4 points)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| S1 | S2 | VA | VB | VOut | LED (on/off) |
| Open | Open | 0.007mV | 0.006mV | 3.753mV | OFF |
| Open | Closed | 1.626mV | 4.9941V | 4.5053V | ON |
| Closed | Open | 4.9932V | 0.534mV | 4.5071V | ON |
| Closed | Closed | 4.9972V | 4.9973V | 4.967mV | OFF |

[(F) Draw a truth table of your circuit] (2 points)

Input for switches: open is 0, closed is 1

Output for LED: ON is 1, OFF is 0

|  |  |  |
| --- | --- | --- |
| S1 | S2 | Result |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The chart indicates that the output is 1 when two input are different.

**[(G) Demonstrate constructed circuit to TA for check-off] (12 points)**

**EXTRA PAGES**

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