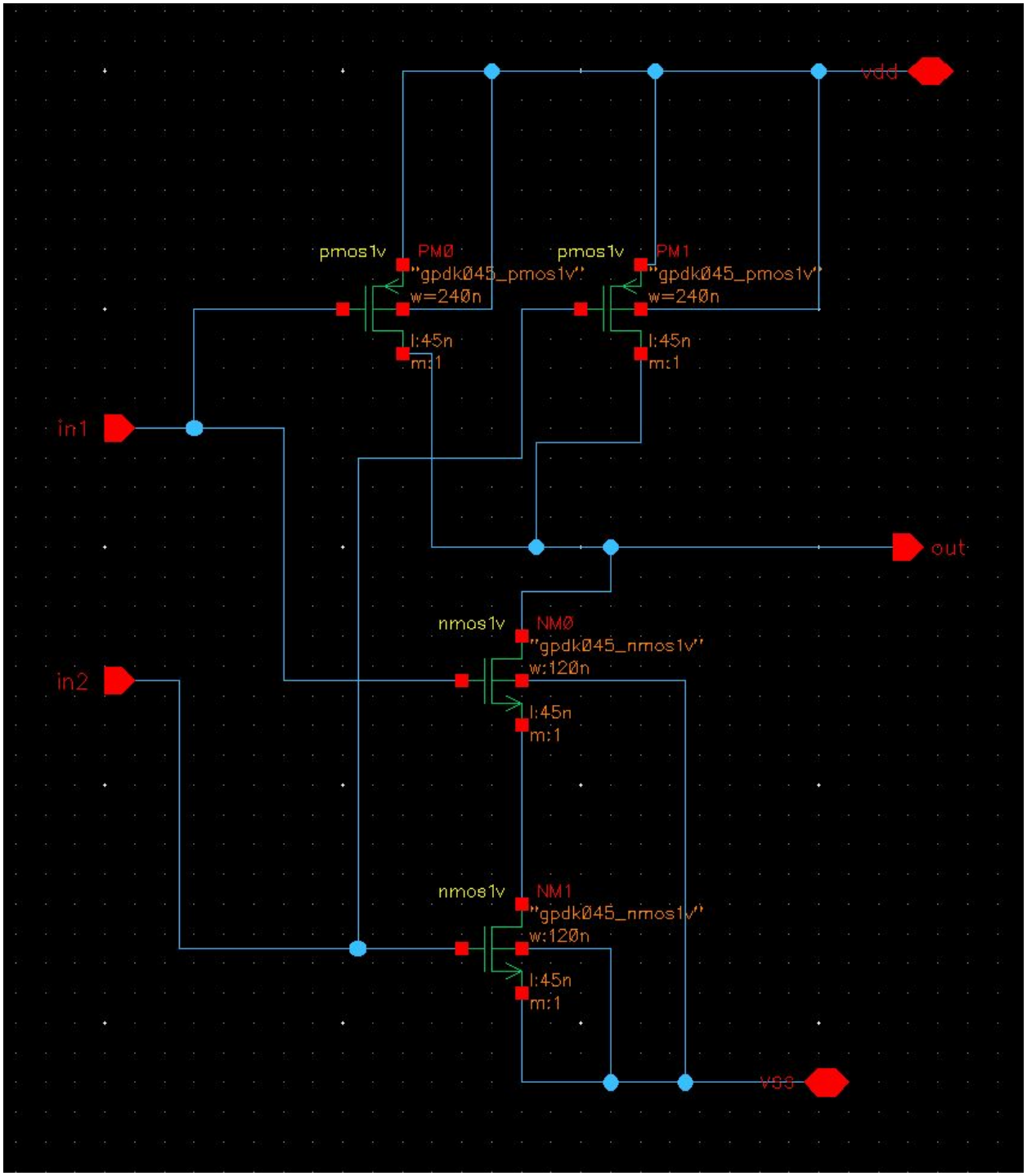
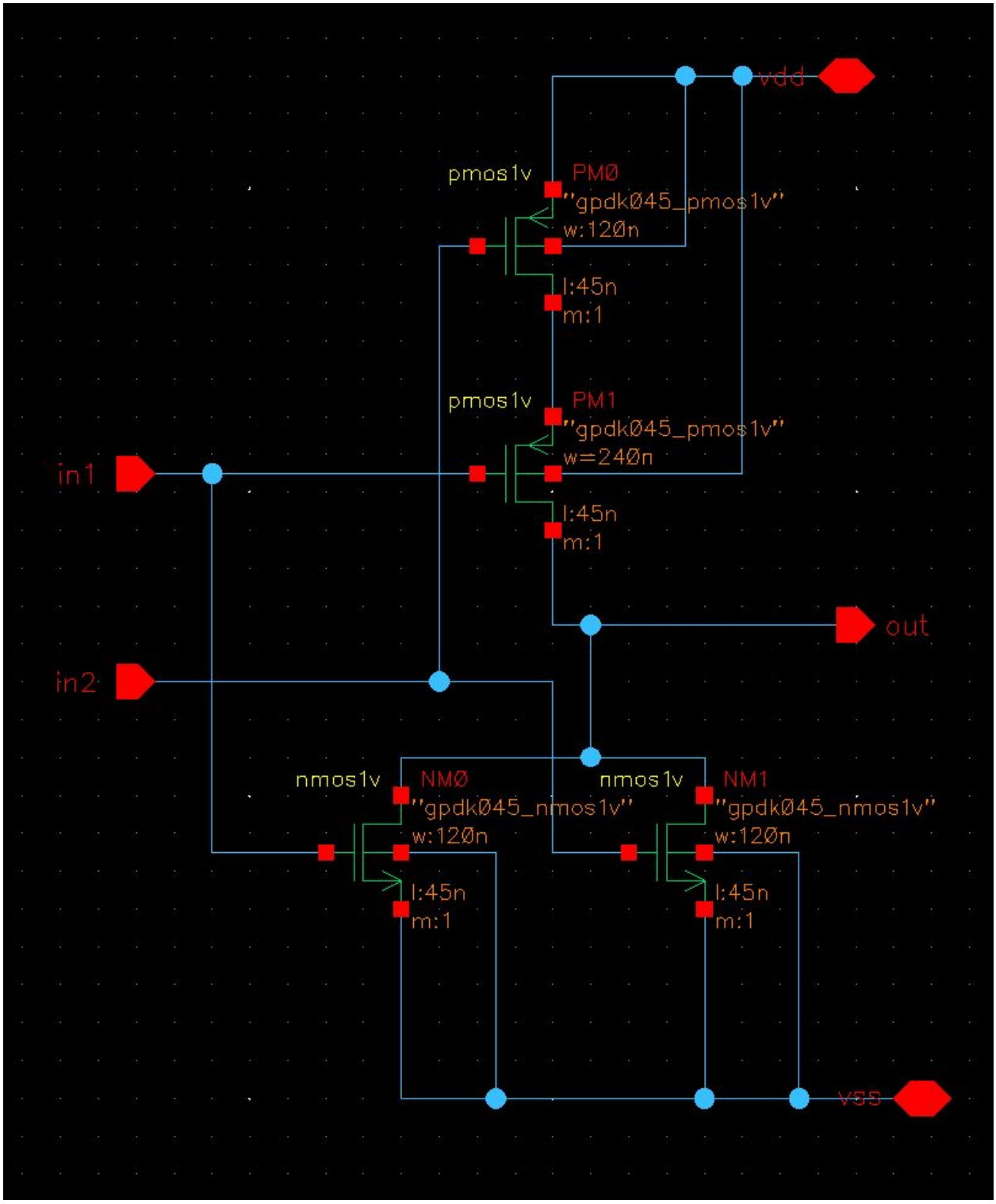
Bradley Newby
ECE 423
November 18th, 2020

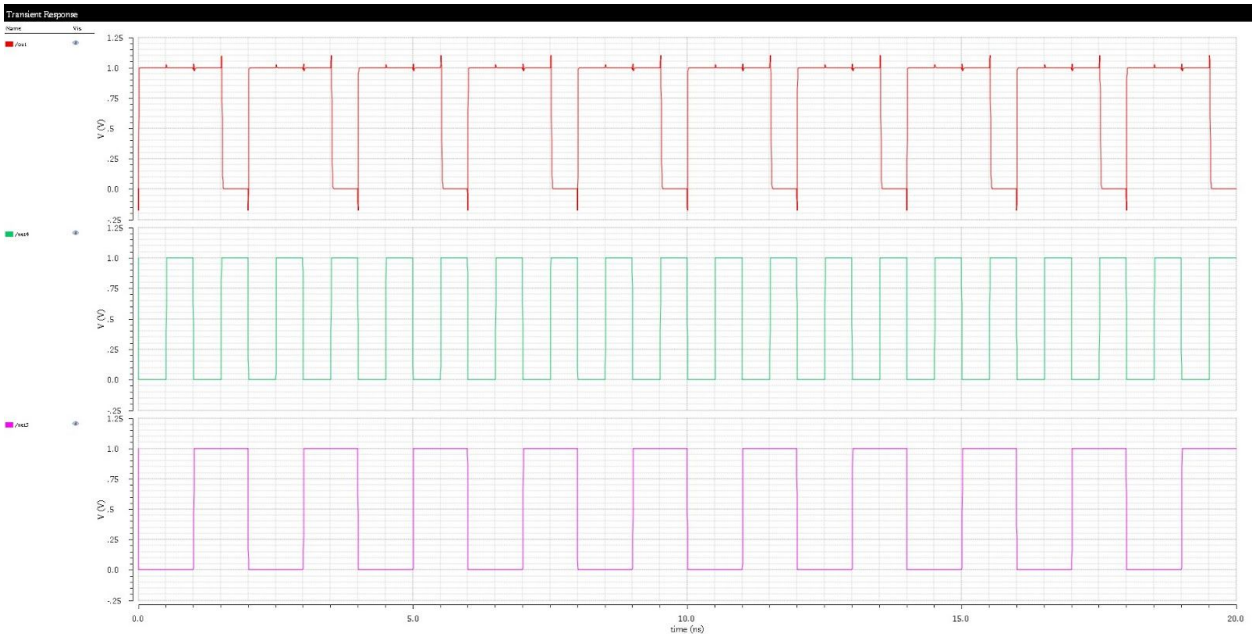
Lab 2



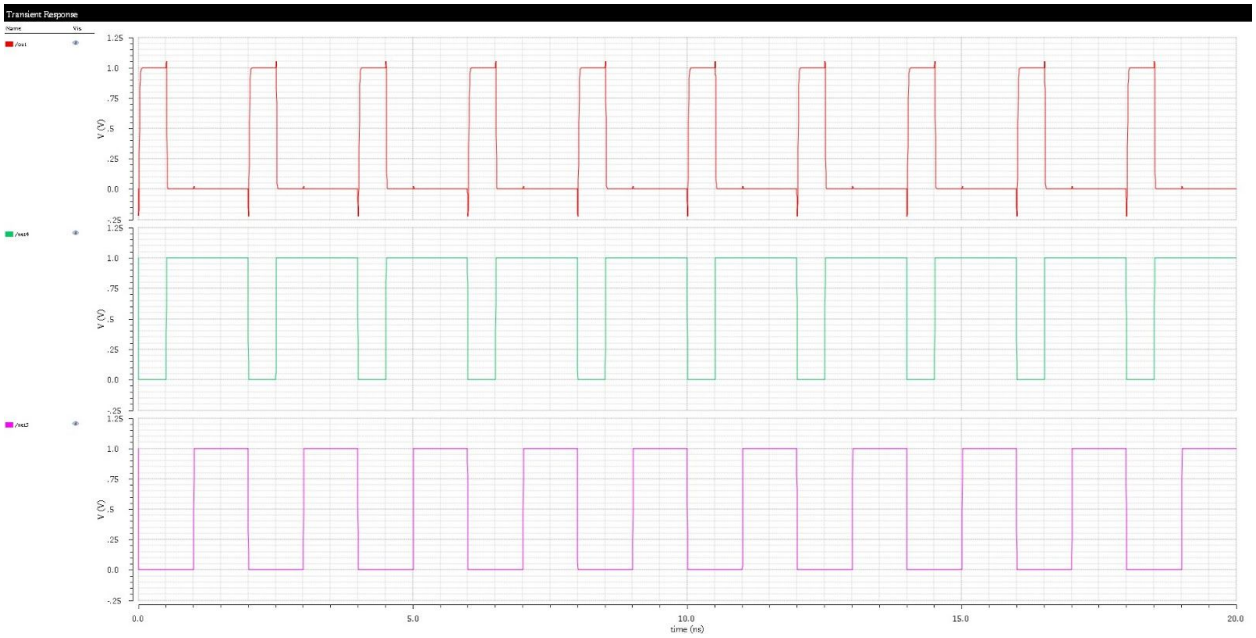
Nand Schematic



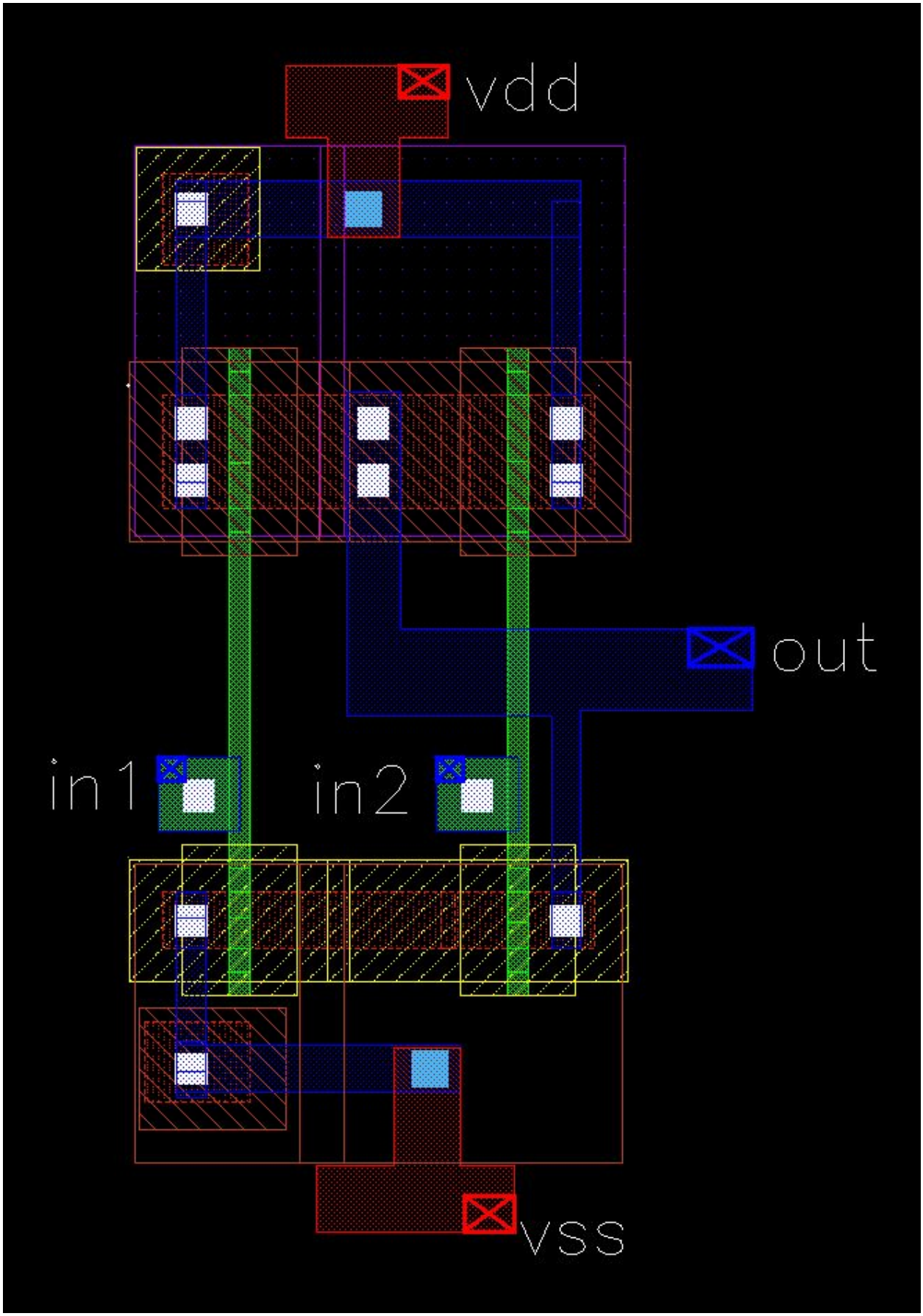
NOR Schematic



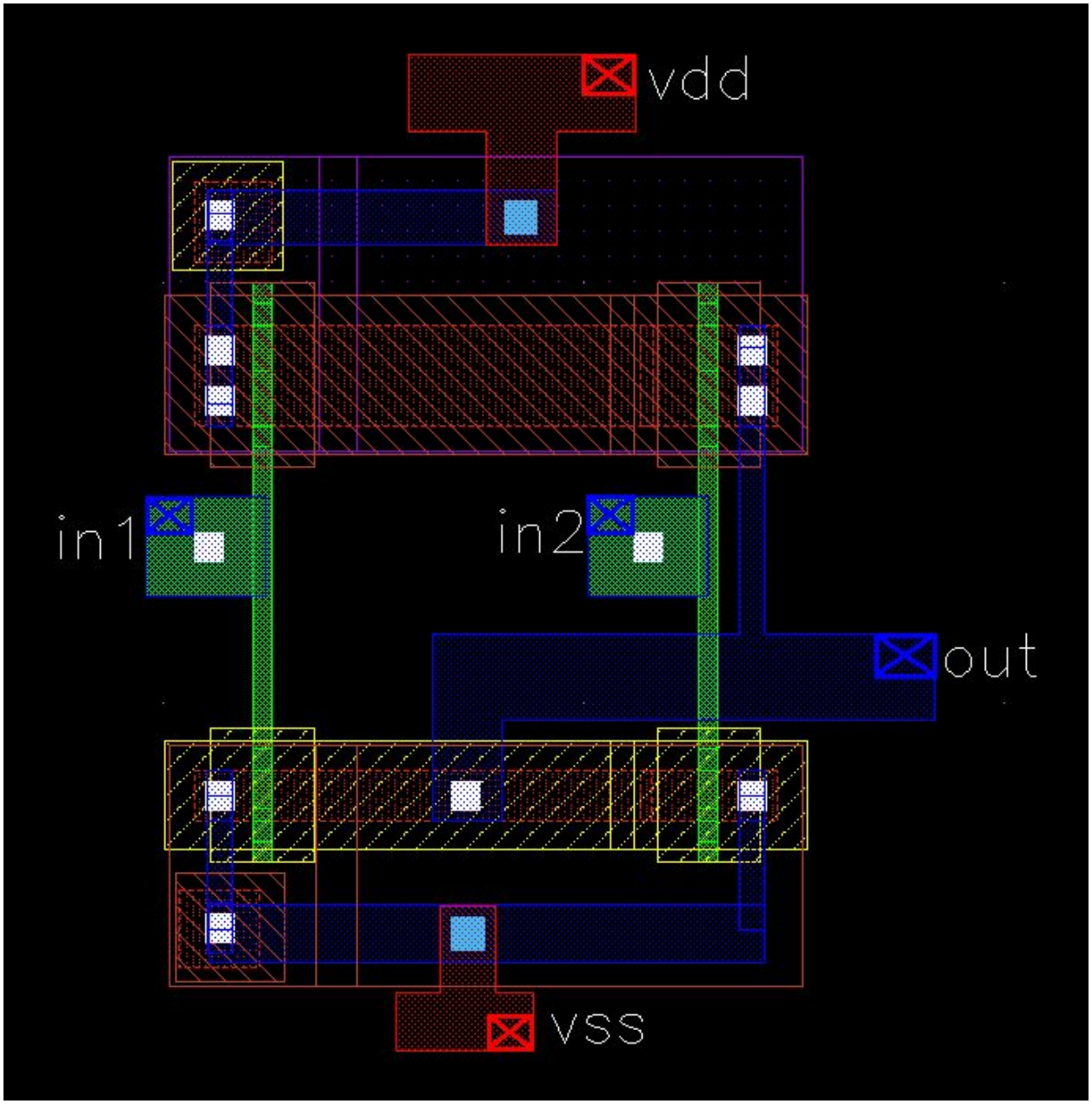
NAND Transient Analysis



NOR Transient Analysis

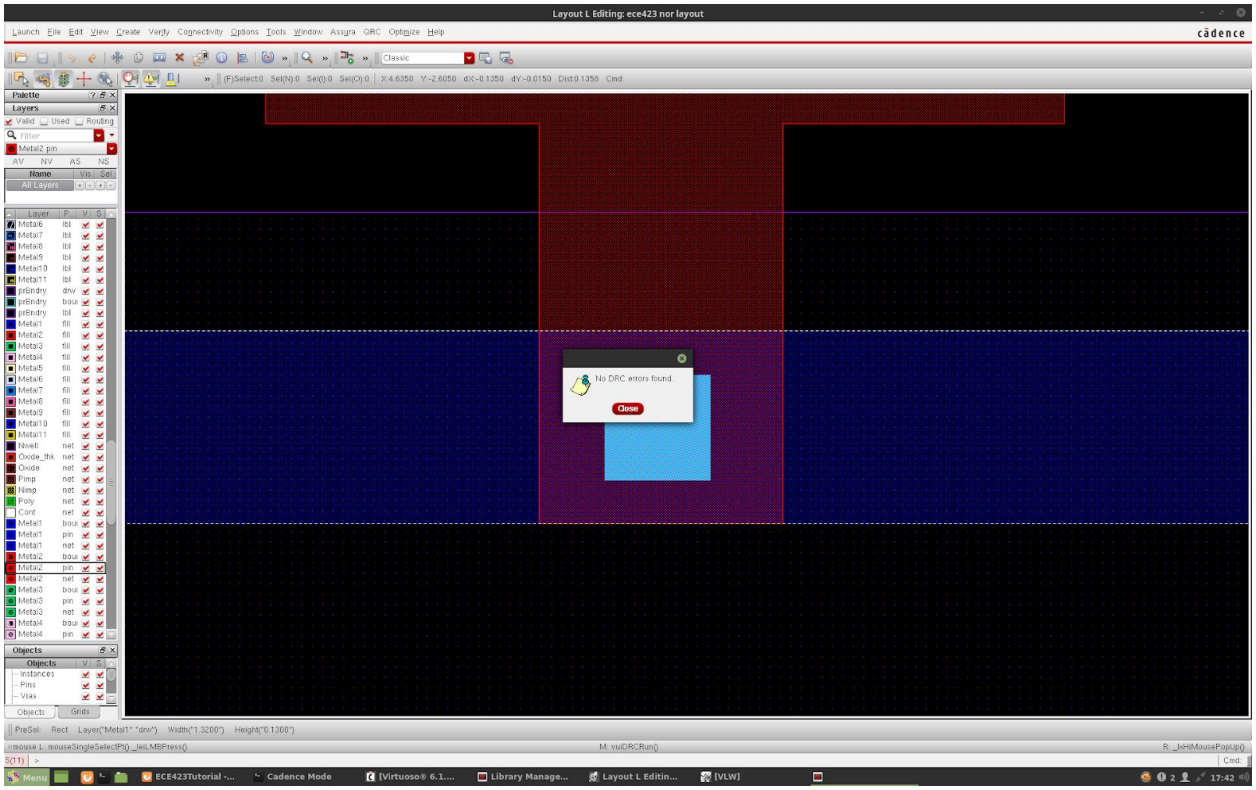

vdd
out
in1
in2
vss

Nand Layout



NOR Layout

NAND DRC



NOR DRC

```
********************************************************************************
****** nand schematic ece423  <vs>  nand layout ece423
********************************************************************************

Filter/Reduce statistics only. Network matching was OK.

Pre-expand Statistics
=====================                          Original
Cell/Device                                schematic  layout
(nmos1v) MOS                                       2       2
(pmos1v) MOS                                       2       2
                                             ------  ------
Total                                              4       4

Reduce Statistics
=================                              Original            Reduced
Cell/Device                                schematic  layout   schematic  layout
(nmos1v) MOS                                       2       2           0       0
(pmos1v) MOS                                       2       2           0       0
(nmos1v:SerMos2#1) MosBlk                          -       -           1       1
(pmos1v:ParMos2#1) MosBlk                          -       -           1       1
                                             ------  ------      ------  ------
Total                                              4       4           2       2

Schematic and Layout Match
```

NAND LVS

```
********************************************************************************
****** nor schematic ece423  <vs>  nor layout ece423
********************************************************************************

Filter/Reduce statistics only. Network matching was OK.

Pre-expand Statistics
=====================                          Original
Cell/Device                                schematic  layout
(nmos1v) MOS                                       2       2
(pmos1v) MOS                                       2       2
                                             ------  ------
Total                                              4       4

Reduce Statistics
=================                              Original            Reduced
Cell/Device                                schematic  layout   schematic  layout
(nmos1v) MOS                                       2       2           0       0
(pmos1v) MOS                                       2       2           0       0
(nmos1v:ParMos2#1) MosBlk                          -       -           1       1
(pmos1v:SerMos2#1) MosBlk                          -       -           1       1
                                             ------  ------      ------  ------
Total                                              4       4           2       2

Schematic and Layout Match
```

NOR LVS