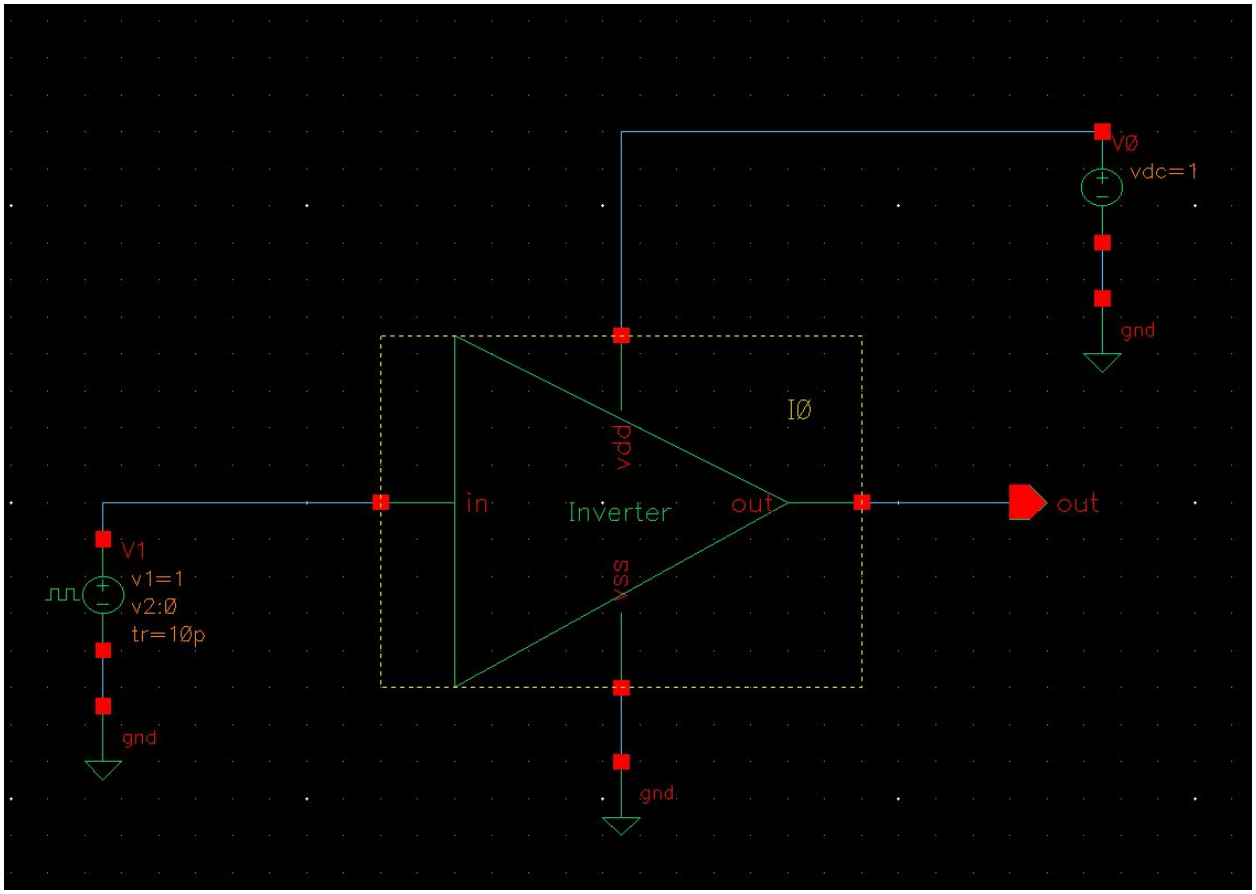
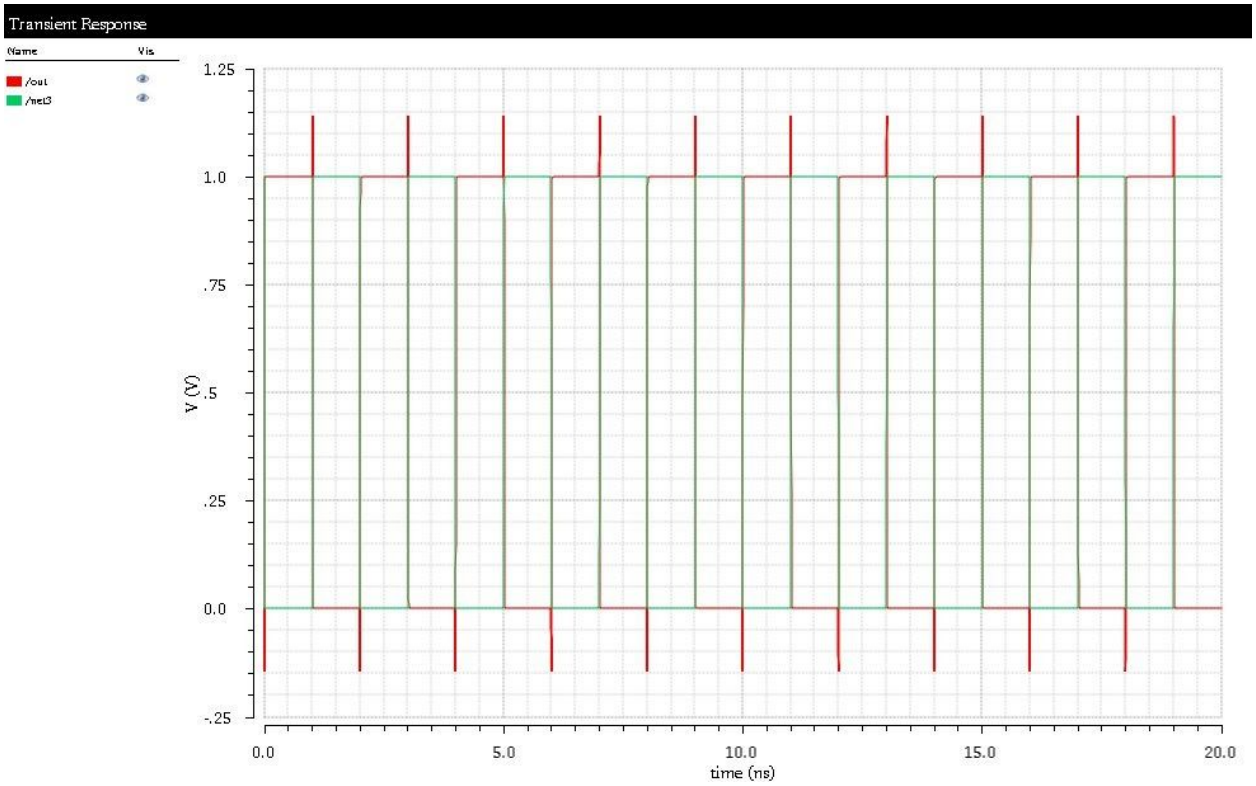
Brad Newby
ECE 423
November 18th, 2020

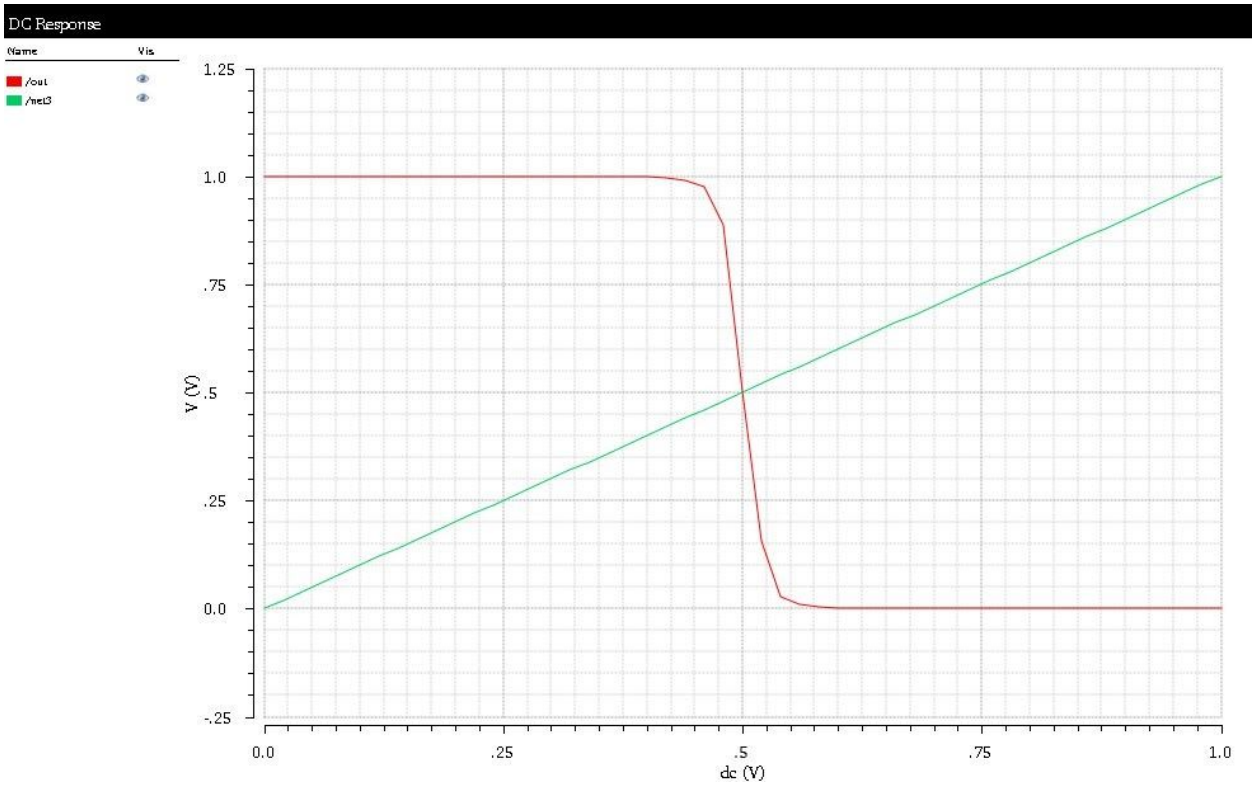
Lab 1



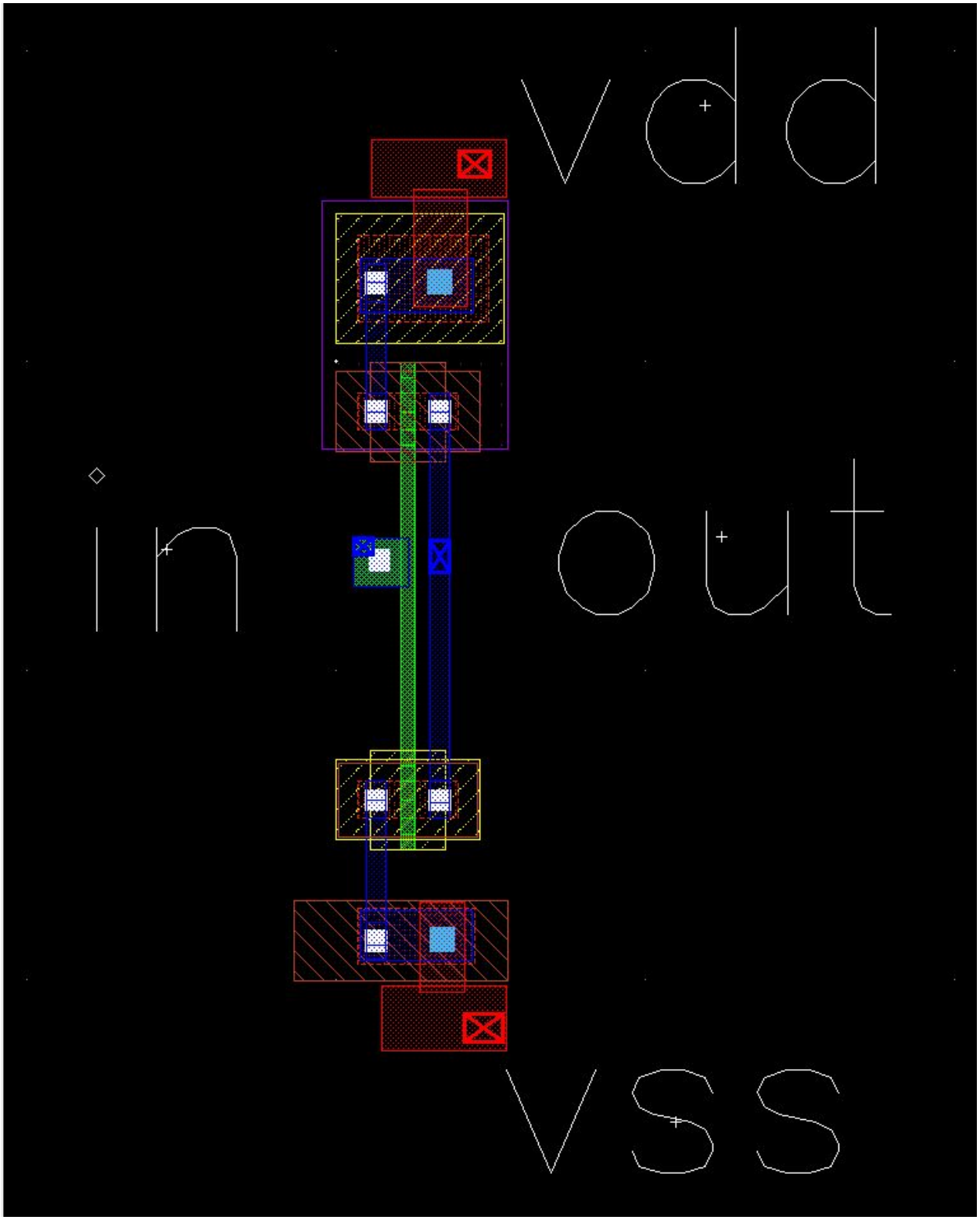
Inverter Schematic



Transient Simulation of schematic



DC Analysis



Layout

DRC no errors

Assura LVS Error Report

File Help

cadence

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********************************************************************************
****** Inverter schematic ece423  <vs>  Inverter layout ece423
********************************************************************************

Filter/Reduce statistics only. Network matching was OK.

Pre-expand Statistics
=====================                          Original
Cell/Device                                schematic  layout
(nmos1v) MOS                                       1       1
(pmos1v) MOS                                       1       1
                                             ------  ------
Total                                              2       2

Reduce Statistics
=================                              Original            Reduced
Cell/Device                                schematic  layout   schematic  layout
(nmos1v) MOS                                       1       1          1       1
(pmos1v) MOS                                       1       1          1       1
                                             ------  ------     ------  ------
Total                                              2       2          2       2

Schematic and Layout Match
```

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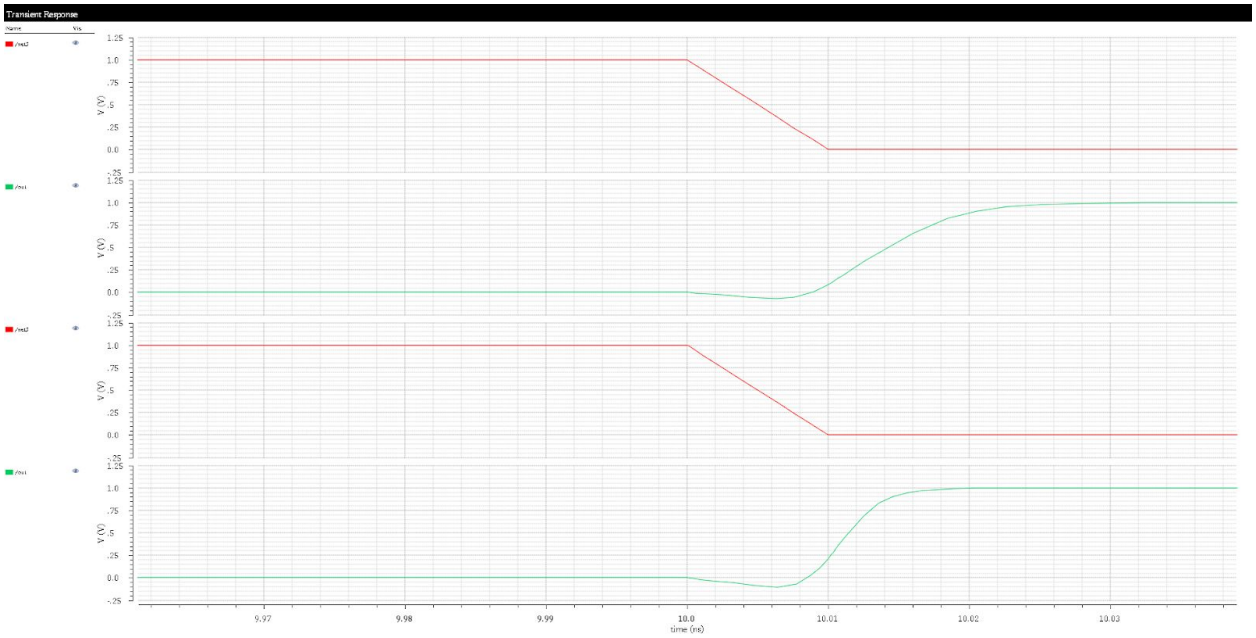
Lvs Report

QRC report



Layout Transient Simulation