

## 聯絡

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## 熱門技能

CyberSecurity

Security

SystemVerilog

# Brad Chen

聯發科 Design Verification Engineer

台灣 Taiwan 新竹市

## 經歷

### 聯發科

Design Verification Engineer

2022 年 6 月 - Present (3 年 2 個月)

新竹 東區, 篤行一路1號

Product Experience:

Dimensity 9300, Dimensity 9400, Dimensity 8400, Dimensity Auto, and more.

Responsibilities:

Verified secure engine and root-of-trust (RoT) boot flow, including cryptographic modules such as AES, SHA, RSA, and ECC.

Contributed to ISO 21434 (automotive cybersecurity) and ISO 26262 (functional safety) compliance verification and reporting.

IP Verification: Used constrained-random verification (CRV) in SystemVerilog/UVM for crypto engines.

SoC Verification: Verified root-of-trust boot-up scenarios using C-based directed tests.

### 群聯電子 PHISON Electronics

Firmware Engineer

2020 年 11 月 - 2022 年 3 月 (1 年 5 個月)

台灣 竹南

Product Experience:

PS5020-E20, PS5022-E22 (Automotive, ISO 26262), PS5026-E26, X2

Responsibilities:

Conducted FPGA-based verification of the secure engine, focusing on cryptographic operations such as encryption/decryption, SHA, RSA, and ECC sign/verify.

Developed and validated the security software library, implementing cryptographic algorithms for confidentiality, integrity, and authentication.

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## 學歷

### 國立成功大學

Master's degree, computer science and information engineering · (2017 年 9 月 - 2020 年 6 月)

### 國立台灣海洋大學

Bachelor's degree, Harbor and River Engineering · (2013 年 9 月 - 2017 年 6 月)