```
vsim -gui work.sisc tb
# vsim -gui work.sisc tb
# Start time: 15:24:26 on Mar 02,2025
# Loading work.sisc tb
# Loading work.sisc
# Loading work.alu
# Loading work.rf
# Loading work.statreg
# Loading work.mux32
# Loading work.ctrl
run -all
# IR=00000000 | R1=00000000 | R2=00000000 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=xxxxxxxx
# IR=00000000 | R1=00000000 | R2=00000000 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000000
# IR=21100001 | R1=00000000 | R2=00000000 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000000
# IR=21100001 | R1=00000000 | R2=00000000 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0011 | WB SEL=0 | RF WE=0 | Write Data=00000000
# IR=21100001 | R1=00000000 | R2=00000000 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0010 | WB SEL=0 | RF WE=0 | Write Data=00000001
# IR=21100001 | R1=00000000 | R2=00000000 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=00000001
# IR=21100001 | R1=00000001 | R2=00000000 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000000
# IR=11211000 | R1=00000001 | R2=00000000 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000000
# IR=11211000 | R1=00000001 | R2=00000000 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0001 | WB SEL=0 | RF WE=0 | Write Data=00000002
# IR=11211000 | R1=00000001 | R2=00000000 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000002
# IR=11211000 | R1=00000001 | R2=00000000 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=00000002
# IR=11211000 | R1=00000001 | R2=00000002 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000002
# IR=1b322000 | R1=00000001 | R2=00000002 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000002
# IR=1b322000 | R1=00000001 | R2=00000002 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0001 | WB SEL=0 | RF WE=0 | Write Data=00000008
# IR=1b322000 | R1=00000001 | R2=00000002 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000008
```

//Console transcript (Braden Miller & Scott Pearson)

```
# IR=1b322000 | R1=00000001 | R2=00000002 | R3=00000000 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=00000008
# IR=1b322000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000008
# IR=12412000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000008
# IR=12412000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=00000000 | R5=00000000 |
ALU OP=0001 | WB SEL=0 | RF WE=0 | Write Data=ffffffff
# IR=12412000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=ffffffff
# IR=12412000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=00000000 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=ffffffff
# IR=12412000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=fffffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=ffffffff
# IR=1a443000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=fffffff | R5=00000000 |
ALU_OP=0000 | WB_SEL=0 | RF_WE=0 | Write_Data=ffffffff
# IR=1a443000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=fffffff | R5=00000000 |
ALU OP=0001 | WB SEL=0 | RF WE=0 | Write Data=00ffffff
# IR=1a443000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=fffffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00ffffff
# IR=1a443000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=fffffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=00ffffff
# IR=1a443000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=00fffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00ffffff
# IR=17234000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=00fffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00ffffff
# IR=17234000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=00fffff | R5=00000000 |
ALU OP=0001 | WB SEL=0 | RF WE=0 | Write Data=00fffff7
# IR=17234000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=00fffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00fffff7
# IR=17234000 | R1=00000001 | R2=00000002 | R3=00000008 | R4=00fffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=00fffff7
# IR=17234000 | R1=00000001 | R2=00fffff7 | R3=00000008 | R4=00ffffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00fffff7
# IR=14220000 | R1=00000001 | R2=00fffff7 | R3=00000008 | R4=00ffffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00fffff7
# IR=14220000 | R1=00000001 | R2=00fffff7 | R3=00000008 | R4=00ffffff | R5=00000000 |
ALU OP=0001 | WB SEL=0 | RF WE=0 | Write Data=ff000008
# IR=14220000 | R1=00000001 | R2=00fffff7 | R3=00000008 | R4=00ffffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=ff000008
# IR=14220000 | R1=00000001 | R2=00fffff7 | R3=00000008 | R4=00ffffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=ff000008
# IR=14220000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=00fffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=ff000008
```

```
# IR=19421000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=00fffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=ff000008
# IR=19421000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=00fffff | R5=00000000 |
ALU OP=0001 | WB SEL=0 | RF WE=0 | Write Data=fe000011
# IR=19421000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=00fffff | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=fe000011
# IR=19421000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=00fffff | R5=00000000 |
ALU_OP=0000 | WB_SEL=0 | RF_WE=1 | Write_Data=fe000011
# IR=19421000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=fe000011 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=fe000011
# IR=15524000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=fe000011 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=fe000011
# IR=15524000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=fe000011 | R5=00000000 |
ALU OP=0001 | WB SEL=0 | RF WE=0 | Write Data=ff000019
# IR=15524000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=fe000011 | R5=00000000 |
ALU_OP=0000 | WB_SEL=0 | RF_WE=0 | Write_Data=ff000019
# IR=15524000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=fe000011 | R5=00000000 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=ff000019
# IR=15524000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=ff000019
# IR=16324000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=ff000019
# IR=16324000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=fe000011 | R5=ff000019 |
ALU OP=0001 | WB SEL=0 | RF WE=0 | Write Data=fe000000
# IR=16324000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=fe000000
# IR=16324000 | R1=00000001 | R2=ff000008 | R3=00000008 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=fe000000
# IR=16324000 | R1=00000001 | R2=ff000008 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=fe000000
# IR=00000000 | R1=00000001 | R2=ff000008 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=fe000000
# IR=00000000 | R1=00000001 | R2=ff000008 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000000
# IR=21100001 | R1=00000001 | R2=ff000008 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000000
# IR=21100001 | R1=00000001 | R2=ff000008 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0011 | WB SEL=0 | RF WE=0 | Write Data=00000000
# IR=21100001 | R1=00000001 | R2=ff000008 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0010 | WB SEL=0 | RF WE=0 | Write Data=00000001
# IR=21100001 | R1=00000001 | R2=ff000008 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=00000001
# IR=21100001 | R1=00000001 | R2=ff000008 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU_OP=0000 | WB_SEL=0 | RF_WE=0 | Write_Data=00000000
```

```
# IR=12211000 | R1=00000001 | R2=ff000008 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000000
# IR=12211000 | R1=00000001 | R2=ff000008 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0001 | WB SEL=0 | RF WE=0 | Write Data=00000000
# IR=12211000 | R1=00000001 | R2=ff000008 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000000
# IR=12211000 | R1=00000001 | R2=ff000008 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=00000000
# IR=12211000 | R1=00000001 | R2=00000000 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000000
# IR=12201000 | R1=00000001 | R2=00000000 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=00000000
# IR=12201000 | R1=00000001 | R2=00000000 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0001 | WB SEL=0 | RF WE=0 | Write Data=ffffffff
# IR=12201000 | R1=00000001 | R2=00000000 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU_OP=0000 | WB_SEL=0 | RF_WE=0 | Write_Data=ffffffff
# IR=12201000 | R1=00000001 | R2=00000000 | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=ffffffff
# IR=12201000 | R1=00000001 | R2=fffffff | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=ffffffff
# IR=18311000 | R1=00000001 | R2=fffffff | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=ffffffff
# IR=18311000 | R1=00000001 | R2=fffffff | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0001 | WB SEL=0 | RF WE=0 | Write Data=80000000
# IR=18311000 | R1=00000001 | R2=ffffffff | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU_OP=0000 | WB_SEL=0 | RF_WE=0 | Write_Data=80000000
# IR=18311000 | R1=00000001 | R2=fffffff | R3=fe000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=80000000
# IR=18311000 | R1=00000001 | R2=ffffffff | R3=80000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=80000000
# IR=11423000 | R1=00000001 | R2=fffffff | R3=80000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=80000000
# IR=11423000 | R1=00000001 | R2=ffffffff | R3=80000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0001 | WB SEL=0 | RF WE=0 | Write Data=7fffffff
# IR=11423000 | R1=00000001 | R2=fffffff | R3=80000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=7fffffff
# IR=11423000 | R1=00000001 | R2=fffffff | R3=80000000 | R4=fe000011 | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=1 | Write Data=7fffffff
# IR=11423000 | R1=00000001 | R2=fffffff | R3=80000000 | R4=7ffffff | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=7fffffff
# IR=f0000000 | R1=00000001 | R2=fffffff | R3=80000000 | R4=7ffffff | R5=ff000019 |
ALU OP=0000 | WB SEL=0 | RF WE=0 | Write Data=7fffffff
# Halt.
```

- # ** Note: \$stop : //iowa.uiowa.edu/shared/engineering/home/bmiller38/Documents/comp arch and org/ProjectPart1/ctrl.v(115)
- # Time: 890 ns Iteration: 0 Instance: /sisc_tb/uut/ctrl_instance