

Processor Checkpoint Description

For my image below, there is a certain process I used to properly annotate my RTL design so far. At the top, there is a legend containing a few different circles. These circles correlate to circles drawn on the image of the processor given in class as well as circles drawn on my RTL design at the bottom of the page. The circles mostly describe inputs and outputs for the processor.v file that are sent to the Wrapper.v file. Considering that my design below is of the processor itself and not the wrapper file, the register file and the memory elements are not shown. Instead, the outputs to the reg file and the memory elements are highlighted. Below this legend, you can see the image of the processor given in class. It is transparent to better see the lines going throughout it. I drew purple lines from each component on this image to the corresponding component on my RTL design. Each of these purple lines has another purple line connected to it, allowing me to write a short description of each component as well. I know it seems a little convoluted, but it was the best way for me to visualize my design and correlate it to what we learned in class.

- Data to write to regfile

--- Address to RAM

--- Addresses to read from regfile

--- Which instruction to grab from ROM

--- Register to write to in regfile
- Data to write to RAM

