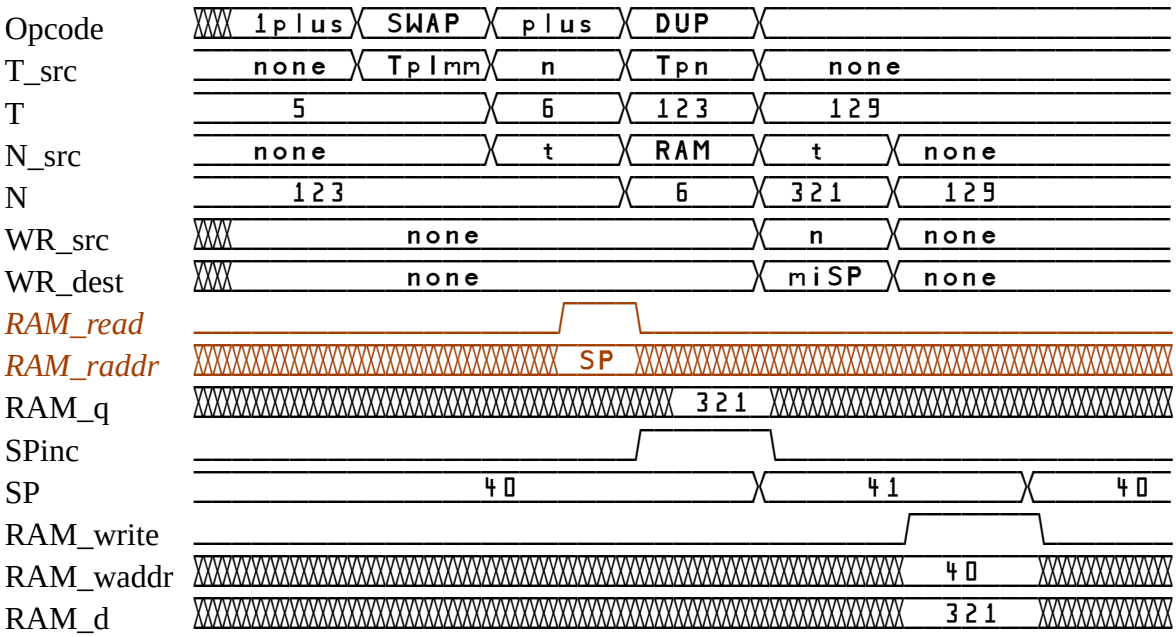
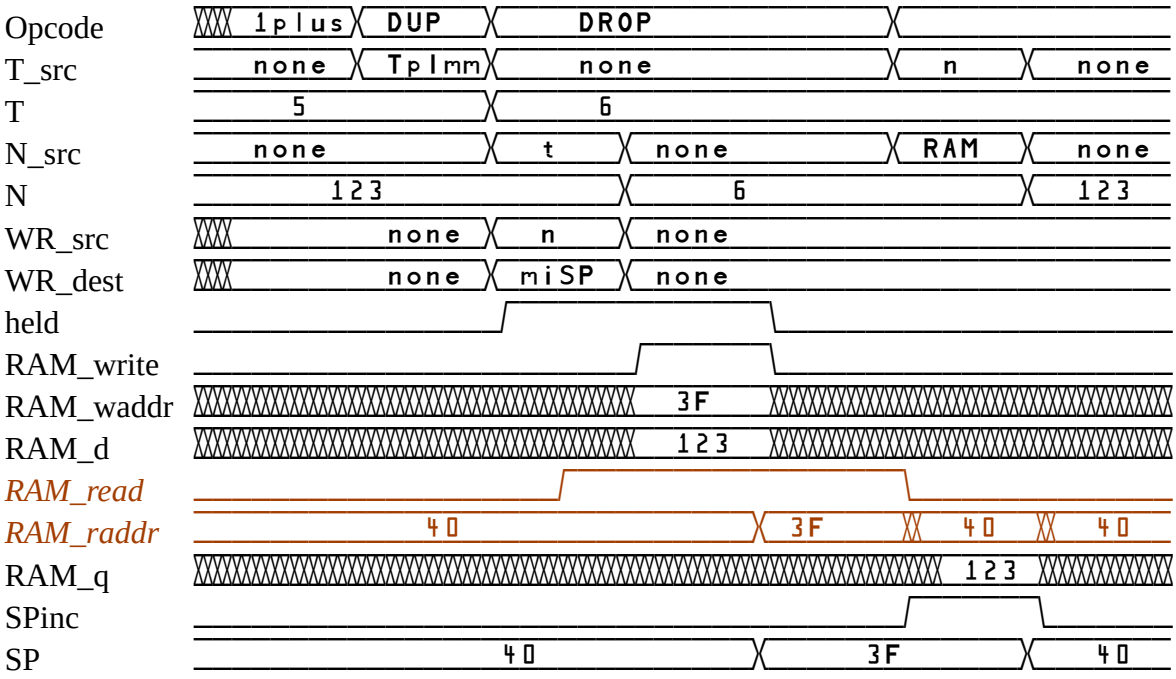
Block RAM

Block RAM uses synchronous read, whose signals are asynchronously decoded from **opcode**. Synchronous opcode decoding sets up the sources for various registers. For example, **new_T** indicates that **T** is to be loaded from 1 of 16 sources.

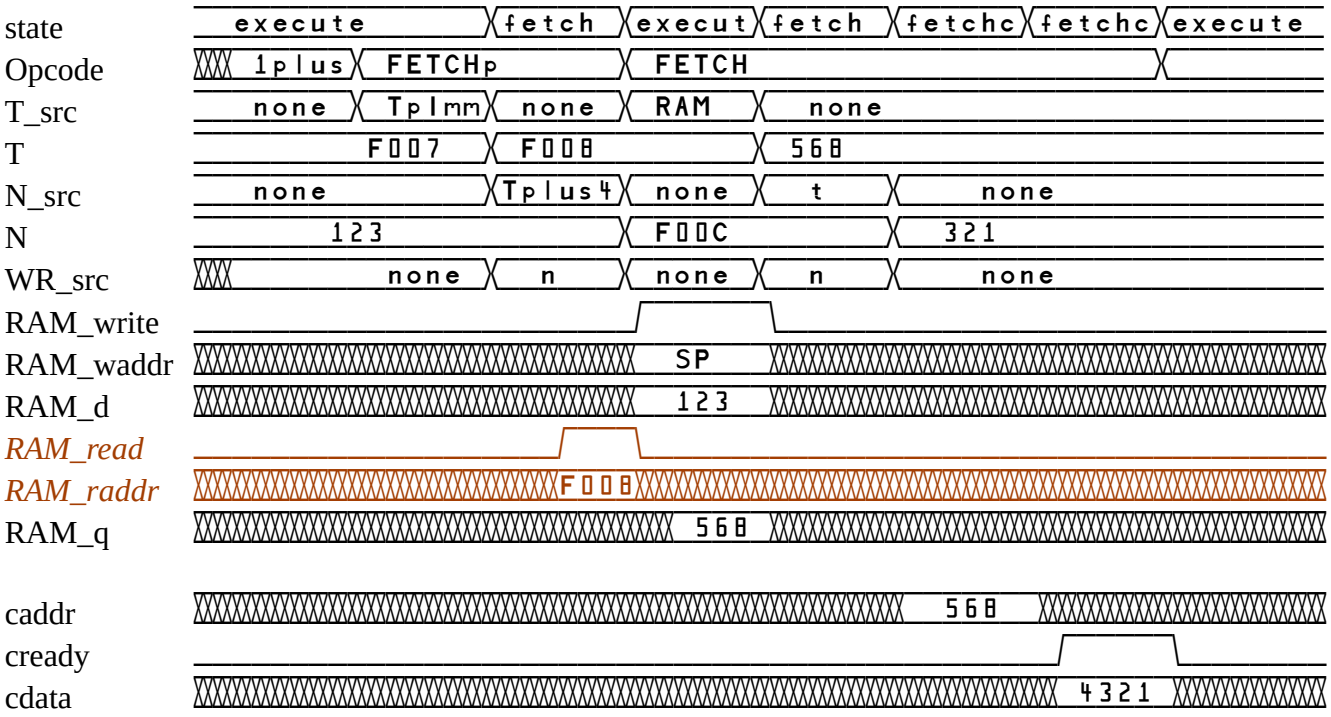
DROP followed by DUP:



DUP followed by DROP: To prevent DROP's read from occurring before DUP's write, "WR_src" must be "none" to allow decoding when is a read is expected. If single-port RAM is used, decoding must also be held off while **RAM_write** is high.



Fetch needs T before it can start a read. @+ (a – a+4 n).
The fetch state checks T and fetches from ROM space (instead) if necessary.



ROM

The ROM interface uses CADDR, CDATA, and CREADY. It's the CPU's interface to large ROM. When CADDR changes, CREADY drops until CDATA matches the new data. Usually it's a synchronous-read ROM. A dumb version would not look ahead: