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bjl134
EECS 395
Homework 4

```
# @ 7 ns: Beginning simulation...
# @ 7 ns: Loading file ../scripts/b.txt...
# @ 7 ns: Loading file ../scripts/a.txt...
# @ 143 ns: Comparing file ../scripts/c.txt
# @ 269 ns: Simulation completed.
# Total simulation cycle count: 131
# Total error count: 0
```

Flow Status	Successful - Tue Nov 3 15:22:11 2015	
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Web Edition	
Revision Name	fifo_multiply_top	
Top-level Entity Name	fifo_multiply_top	
Family	Cyclone IV E	
Device	EP4CE115F29C7	
Timing Models	Final	
Total logic elements	6,323 / 114,480 (6 %)	
Total combinational functions	4,320 / 114,480 (4 %)	
Dedicated logic registers	4,261 / 114,480 (4 %)	
Total registers		4261
Total pins	106 / 529 (20 %)	
Total virtual pins		0
Total memory bits	6,144 / 3,981,312 (< 1 %)	
Embedded Multiplier 9-bit elements	48 / 532 (9 %)	
Total PLLs	0 / 4 (0 %)	