Brady Lee – bjl134
EECS 395
Homework 3

	Naive	Inner Unroll	Inner 2 Unroll	Unroll
Cycle count	513	513	129	129
Logic Elements	428	1313	5634	246111
Registers	304	785	1819	4237
Memory	6144	6144	6144	6144
Multipliers	6	48	384	532

Naive implementation

Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Web Edition
Revision Name	matrix_multiply_top
Top-level Entity Name	matrix_multiply_top
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	428 / 114,480 (< 1 %)
Total combinational functions	311 / 114,480 (< 1 %)
Dedicated logic registers	304 / 114,480 (< 1 %)
Total registers	304
Total pins	126 / 529 (24 %)
Total virtual pins	0
Total memory bits	6,144 / 3,981,312 (< 1 %)
Embedded Multiplier 9-bit elements	6 / 532 (1 %)
Total PLLs	0 / 4 (0 %)

@ 4 ns: Loading file ../scripts/b.txt...
@ 4 ns: Loading file ../scripts/a.txt...
@ 136 ns: Beginning simulation...
@ 1162 ns: Simulation completed.
@ 1165 ns: Comparing file ../scripts/c.txt
Total simulation cycle count: 513
Total error count: 0

Optimization Level 1

Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Web Edition
Revision Name	matrix_multiply_top
Top-level Entity Name	matrix_multiply_top
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	1,313 / 114,480 (1 %)
Total combinational functions	1,226 / 114,480 (1 %)
Dedicated logic registers	785 / 114,480 (< 1 %)
Total registers	785
Total pins	126 / 529 (24 %)
Total virtual pins	0
Total memory bits	6,144 / 3,981,312 (< 1 %)
Embedded Multiplier 9-bit elements	48 / 532 (9 %)
Total PLLs	0 / 4 (0 %)

@ 4 ns: Loading file ../scripts/b.txt...
@ 4 ns: Loading file ../scripts/a.txt...
@ 136 ns: Beginning simulation...
@ 1162 ns: Simulation completed.
@ 1165 ns: Comparing file ../scripts/c.txt
Total simulation cycle count: 513
Total error count: 0

Optimization Level 2

Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Web Edition
Revision Name	matrix_multiply_top
Top-level Entity Name	matrix_multiply_top
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	5,634 / 114,480 (5 %)
Total combinational functions	4,302 / 114,480 (4 %)
Dedicated logic registers	1,819 / 114,480 (2 %)
Total registers	1819
Total pins	126 / 529 (24 %)
Total virtual pins	0
Total memory bits	6,144 / 3,981,312 (< 1 %)
Embedded Multiplier 9-bit elements	384 / 532 (72 %)
Total PLLs	0 / 4 (0 %)

```
# @ 4 ns: Loading file ../scripts/b.txt...
# @ 4 ns: Loading file ../scripts/a.txt...
# @ 136 ns: Beginning simulation...
# @ 394 ns: Simulation completed.
# @ 397 ns: Comparing file ../scripts/c.txt
# Total simulation cycle count: 129
# Total error count: 0
```

Optimization Level 3

Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Web Edition
Revision Name	matrix_multiply_top
Top-level Entity Name	matrix_multiply_top
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	246,111 / 114,480 (215 %)
Total combinational functions	241,991 / 114,480 (211 %)
Dedicated logic registers	4,237 / 114,480 (4 %)
Total registers	4237
Total pins	126 / 529 (24 %)
Total virtual pins	0
Total memory bits	6,144 / 3,981,312 (< 1 %)
Embedded Multiplier 9-bit elements	532 / 532 (100 %)
Total PLLs	0 / 4 (0 %)

```
# @ 4 ns: Loading file ../scripts/b.txt...
# @ 4 ns: Loading file ../scripts/a.txt...
# @ 136 ns: Beginning simulation...
# @ 394 ns: Simulation completed.
# @ 397 ns: Comparing file ../scripts/c.txt
# Total simulation cycle count: 129
# Total error count: 0
```