Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Web Edition
Revision Name	udp_read_top
Top-level Entity Name	udp_read_top
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	75 / 114,480 (< 1 %)
Total combinational functions	67 / 114,480 (< 1 %)
Dedicated logic registers	40 / 114,480 (< 1 %)
Total registers	40
Total pins	42 / 529 (8 %)
Total virtual pins	0
Total memory bits	8,192 / 3,981,312 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)