Analog Electronic Circuits (EC2.103) : Endsem exam

[redacted]

Date : 6^{th} July, 2022, Duration : 3 Hours, Max. Marks : 30

Instructions:

- Clearly write your assumptions (if any)
- Numerical answers must be correct upto **two places** of decimal to get any credit
- Refrain from copying
- You can use your textbooks, lecture notebooks and own handwritten short notes in the exam hall
- Use of mobile phone and computers are not allowed during this exam

1. Consider the negative feedback loop as shown in Fig. 1. The amplifier has a voltage gain transfer function defined as $A(s) = \frac{A_0}{1+\frac{s}{p_1}}$, whereas the feedback factor is β. Derive the closed loop transfer function $H(s) = \frac{v_{out}}{v_{in}}(s)$. Draw the Bode plots for A(s) and H(s) on same axis and clearly mark pole locations and magnitude levels. Comment on the gain bandwidth trade-off using your plots. [3 Mark]

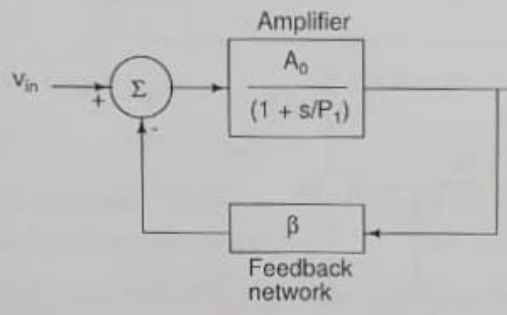

Figure 1

2. Consider the circuits shown in Figure 2.

   (a) Draw small signal model of the amplifier shown in Fig. 2(a) and derive small signal voltage gain. [1 Mark]

   (b) Draw small signal model of the amplifier shown in Fig. 2(b) and derive small signal voltage gain. [1 Mark]

   (c) Draw voltage transfer characteristics of the circuit shown in Fig. 2(c) by sweeping v_{in} from -VDD to +VDD. Clearly show the voltage levels (input and output) on the plot. [2 Mark]

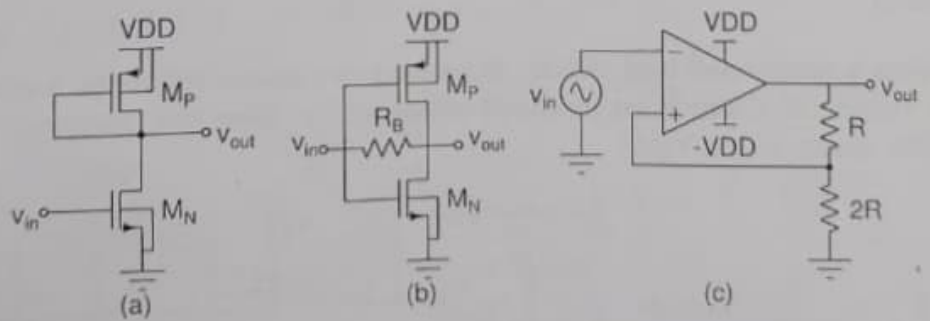

Figure 2

3. Consider the circuit shown in Figure 3.

   (a) Suppose v_{in1} is swept from 0 V to 2 V, while $v_{in2}(> 0V)$ is kept constant. Plot v_{out} vs v_{in1} for the fixed v_{in2}. Clearly state your assumptions (if any). [2 Mark]

(b) Suppose v_{in2} is swept from 0 V to 2 V, while $v_{in1} (> V_T)$ is kept constant. Plot v_{out} vs v_{in2} for the fixed v_{in1}. Clearly state your assumptions (if any). [2 Mark]

(c) Find small signal equivalent impedances Z_1 and Z_2 as shown in the figure. Clearly state your assumptions (if any). [2 Mark]

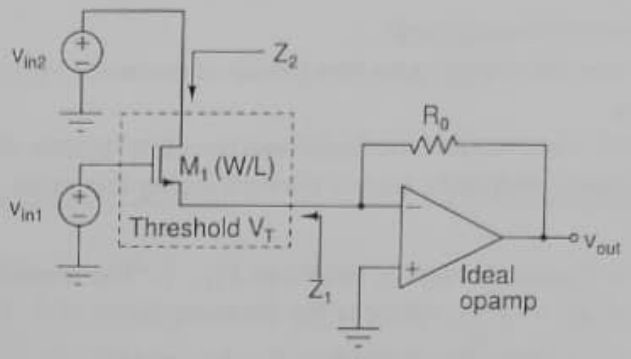

Figure 3

4. Consider the common source amplifier topology shown in Fig. 4.

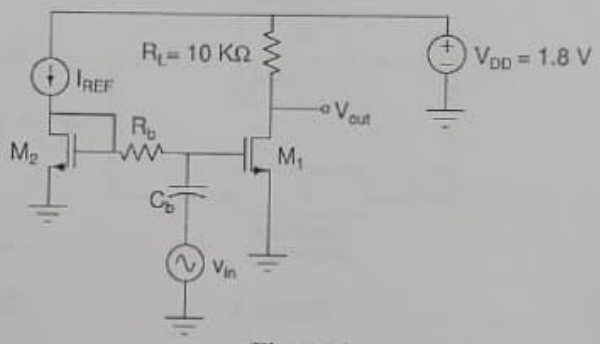

Figure 4

(a) Draw the small signal equivalent of the circuit and derive the small signal dc voltage gain of the amplifier. [2 Mark]

(b) Design the amplifier (shown in Fig. 4) with a resistive load of 10 kΩ for a voltage gain > 5 and an overdrive voltage (of input transistor) of 200 mV. The minimum input signal frequency is 100 Hz. Show the design procedure with calculations for sizes of transistors $((\frac{W}{L})_1, (\frac{W}{L})_2)$, I_{REF}, C_b and R_b. What is the overall power consumed by your amplifier. Assume $\mu_n C_{ox} = 250\ \mu A/V^2$, $V_T = 0.5$ V. You can ignore channel length modulation. Clearly write your assumptions (if any). [4 Mark]

5. Fig. 5 depicts a sample and hold circuit. It contains two opamp followers, a capacitor C=100 pF, an NMOS switch (M_1), which has threshold voltage of V_T. Slew rate (maximum rate of change of output) of the opamp is 100 V/μs.

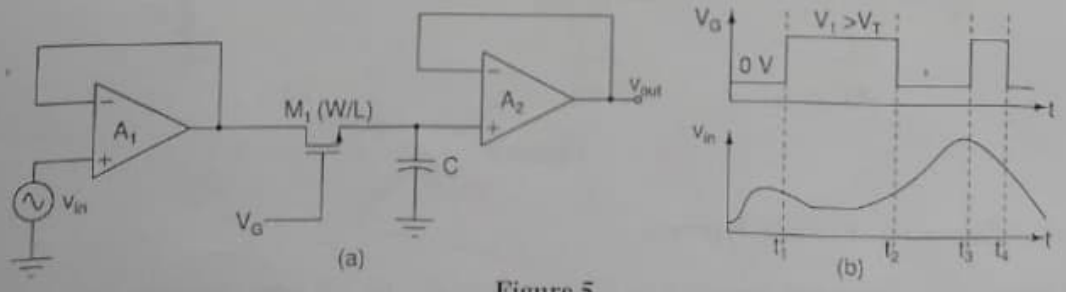

Figure 5

(a) Plot v_{out} for given v_{in} and V_G. Clearly mark amplitudes, time stamps (t_1, t_2, t_3, t_4) and plot all three graphs (V_G, v_{in} and v_{out}). Describe the function of this circuit? [2 Mark]

(b) How the value of v_{out} at t_3 will change from its value at t_2 if capacitor is made 10 times bigger than the initial value. Will it change at faster rate? [1 Mark]

(c) Suppose that the capacitor is made extremely small (1 pF) such that opamp follower A1 starts delivering maximum current (I_{max}) to the capacitor. Find the value of I_{max}. [2 Mark]

6. Consider the circuits shown in Figures 6(a) and (b), where V_{os} depicts the offset voltage of the opamp.

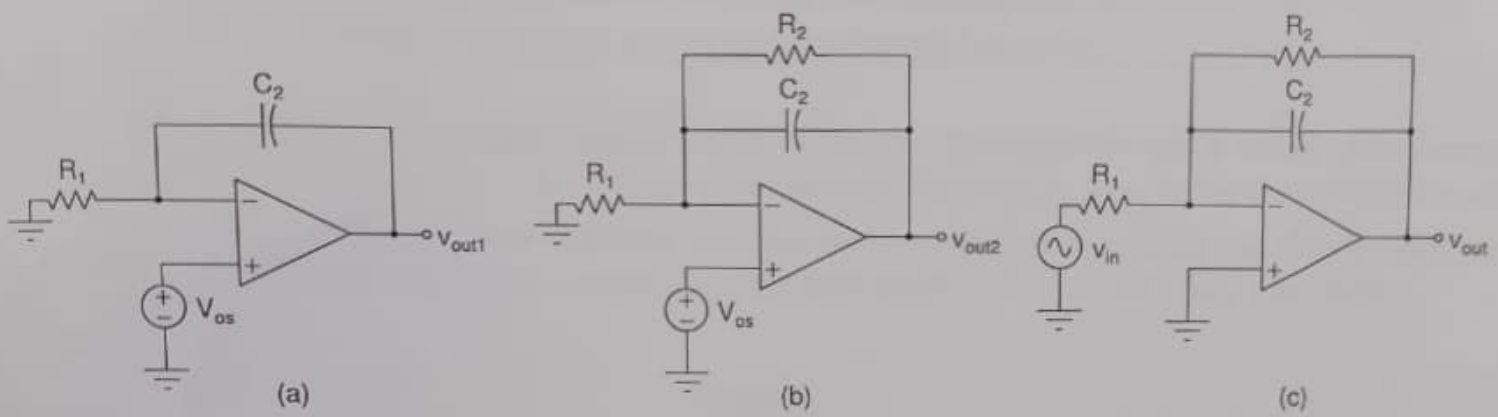

Figure 6

(a) Derive the transfer functions $H_1(s) = \frac{v_{out1}}{V_{os}}(s)$ and $H_2(s) = \frac{v_{out2}}{V_{os}}(s)$. Find pole locations and DC gains from the two transfer functions. [2 Mark]

(b) For a given value of $V_{OS} = 2$ mV, plot v_{out1} and v_{out2} with respect to time by clearly showing the steady state values. [1 Mark]

(c) For circuit shown in Fig. 6(c), derive the transfer functions $H(s) = \frac{v_{out}}{v_{in}}(s)$. Give Bode magnitude plot for $H(s)$. For what frequency, this circuit behaves as a good integrator (transfer function will have pole at origin). It is given that $v_{in}(t) = Asin(2\pi f_0)t$ V, $R_2 = 1\ k\Omega$, $C_2 = 1\ \mu$F. Give approximate plots of $v_{out}(t)$ for (i) $f_0 = 10\ kHz$ and (ii) $f_0 = 50\ Hz$. [3 Mark]

Good luck !!