End-Sem: Monsoon2022: VLSI Digital (EC2.201)

Max. Time: 180 Mins [9:00 AM to 12:00] Max. Marks: 100 Date: 21/11/2022

Note(s): No query is allowed during exam.

Write your assumptions (if any) for each question.

Q1. Suppose, CVEST research center at IIIT Hyderabad is offering to license you its patented non-inverting buffer circuit shown in **Fig. 1.** Graphically derive the transfer characteristics for this buffer. Assume $\beta_n = \beta_p$ and $V_{tn} = |V_{tp}| = V_t$. Why is it a bad circuit idea? **[5 Marks]** [CO-3]

Q2. For the MOS based circuit shown in **Fig. 2.** Where the gate voltage of p-channel MOS is kept constant at 3V, while the gate voltage (V_G) of n-channel MOS is increased from zero. Consider, for both the transistors, the magnitude of threshold voltage is 1V, and the product of trans-conductance parameter and W/L ratio (i.e., $\mu n. C_{ox}. W/L$) is 1 mA/V^2.
Now, for small increase in V_G beyond 3V, point out the region of operation of each MOSFET.
Justify you answer with proper explanation/equations. **[5 Marks]** [CO-2]

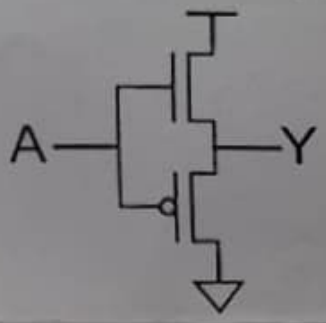


Fig. 1

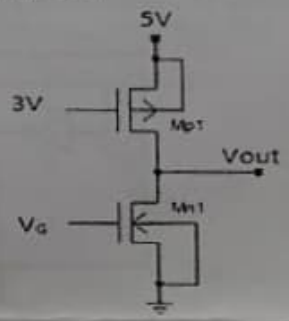


Fig. 2

Q3. (a) Draw the CMOS gate for $f(A, B, C, D) = \overline{(A + B + C).D}$. **[3 Marks]** [CO-5]

(b) Realize W = AB+CD+EF using **[3+3=6 Marks]** [CO-3]

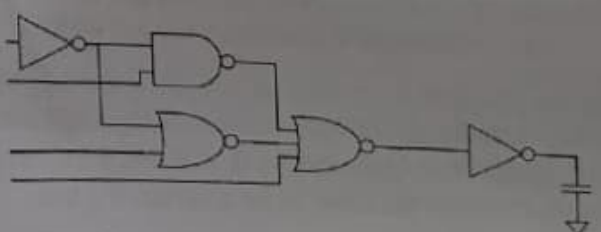
i. NAND gates of any size
ii. Two input NAND gates only

(c) In a CMOS inverter, PMOS is tied to the ground. Draw the transfer characteristics of the inverter, by varying PMOS width and explain. **[4 Marks]** [CO-2]

(d) Which and when do you prefer: high V_t or low V_t? Suggest a way to dynamically alter V_t in a CMOS invertor. **[2 Marks]** [CO-4]

(e) The gate to source voltage (V_{GS}) of a MOSFET with threshold voltage (V_T) of 400mV, working in Saturation region in 900mV, and the observed drain current (I_D) is 1mA. Now, calculate the drain current for an applied V_{GS} of 1400mV, assuming the MOSFET is operating in saturation region. Neglect the channel length modulation effect. **[4 Marks]** [CO-3]

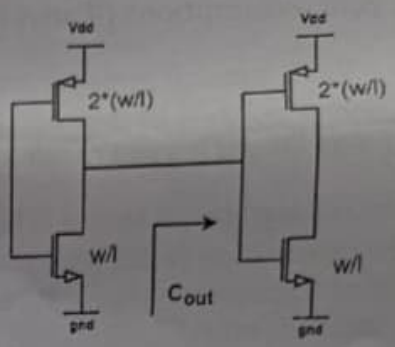
Q4. (a) What is the significance of activity factor in chip design? Which net has the highest activity factor? Find the switching probabilities and the activity factors for the given circuit. **[5 Marks]** [CO-6]



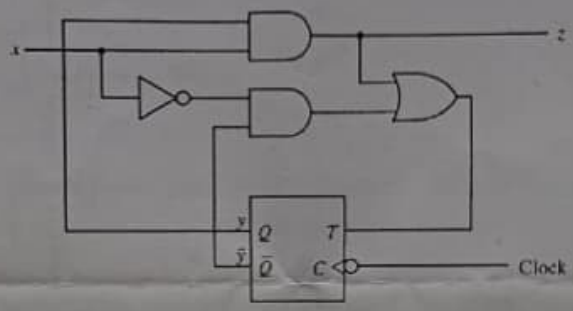
(b). Consider a following inverter design. The driver inverter and the load inverter are of unit size (1x size). The intrinsic delay of the driver is 20ps. Assume the load capacitance looking from the output of the driver inverter is 4fF. The driving strength (k) of the inverter is 4ps/fF for unit size inverter. Calculate the delay for the entire circuit for the following specifications:

- Unit size (1x) driver and load inverter.
- When the size of the driver is doubled (2x).
- When the size of the load inverter is doubled (2x).

[5 Marks] [CO-4]



Q5. (a). Show the response of the circuit at $x = 01101000$. Assume initial $y = 0$. **[4 Marks]** [CO-6]



(b). In a sequence detector sequential circuit with single bit input x and output z, a sequence is applied to $x = 15'h1212$ to produce the output sequence (in 15 clock cycles) on $z = 15'h909$. Identify the sequence being detected and give the state diagram of the circuit. **[6 Marks]** [CO-6]

(c). Using two 2:1 multiplexors, draw and explain when a false path can occur. **[4 Marks]** [CO-5]

(d). A water container can be either full or empty. Design a circuit to describe the relation between two water containers. **[4 Marks]** [CO-5]

Q6. [6 Marks + 5 Marks = 11 Marks] [CO-6]

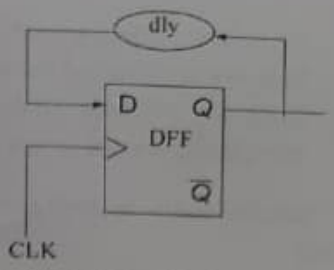
(a) In an ice-cream shop four ice-cream flavours are available vanilla, strawberry, chocolate and butterscotch. A customer can choose flavours by pressing a set of three keys.

1. If no key is pressed, they get vanilla by default
2. If 1 key is pressed they get vanilla+ Some other flavour
3. If 2 keys are pressed, they get vanilla+2 other flavours
4. If 3 keys are pressed, they get all flavours

They are charged according to the extra number of flavours they opt for. Each additional flavour (Except vanilla) costs Rs. 2. Design a system using a full adder and multiplier to calculate the cost. (The costs for all the above four cases will be 0, 2, 4 and 6 respectively). **Hint:** Use Full adder to find the number of ones in input, considering input to be a series of 3 bits.

(b) Following flipflops are available

	FF1	FF2	FF3
Clock to Q delay(ns)	5	6	8
Setup time(ns)	3	4	2
Hold time(ns)	2	1	1



Let dly = 0, which of the flip flops can be used if the available clock period is (a) 5ns (b) 8ns (c) 15ns.

Q7. [6 Marks + 6Marks = 12 Marks] [CO-3, CO-6]

(a) The block diagram shown in Fig. 7(a) has one input "IN" which is coming serially @ clock, "CLK". It has 4 outputs A, B, C & D. A will be 1 if IN has even number of 1's & even number of 0's. Similarly, B will be 1 for even 1's odd 0's, C for odd 1's even 0's and D for both odd. Give the FSM required to design the block.

(b) Draw the state diagram for a circuit that outputs a "1" if the aggregate serial binary input is divisible by 5. For instance, if the input stream is 1, 0, 1, we output a "1" (since 101 is 5). If we then get a "0", the aggregate total is 10, so we output another "1" (and so on). Refer Fig. 7(b).

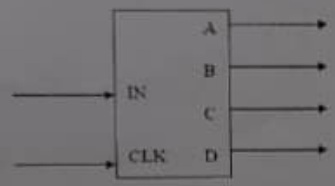


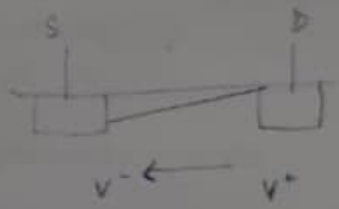
Fig. 7(a)

Input Sequence	Value	Output
1 1	1	0
0 10	2	0
1 101	5	1
0 1010	10	1
1 10101	21	0

Fig. 7(b)

Q8. [4 Marks + 6 Marks] [CO-5, CO-6]

(a) Consider the following two statements (S1 and S2) about the internal condition in n-channel MOSFET operating in non-saturated (i.e., linear or ohmic or active) region.



S1: The inversion charge decreases from Source to Drain.
S2: The channel potential increases from Source to Drain.

Which of the following is correct?

i. S1 is true, but S2 is false
ii. S1 is false, but S2 is true
iii. Both S1 and S2 are true
iv. Both S1 and S2 are false.

(b) Design a circuit that operates a safety alarm in a car to ensure seatbelts are fastened and doors are locked. Whenever the driver and/or passenger seats are occupied and the seatbelts are not fastened when the car's Ignition is on, it will sound an alarm. Also, if the seats are occupied and doors are not closed properly while the ignition is on, it will sound an alarm. That is alarm is on when-

i. Driver seat is occupied, ignition is on, and seatbelt is not fastened, but all the doors are locked properly.
ii. Driver seat is occupied, ignition is on, and seatbelt is not fastened, but one or many doors are not locked properly.
iii. Driver seat is occupied, ignition is on, and seatbelt is fastened, but one or many doors are not locked properly.
iv. Driver and Passenger seats are occupied, and ignition is on and seatbelts of either driver or passenger or both are not fastened but all the doors are locked properly.

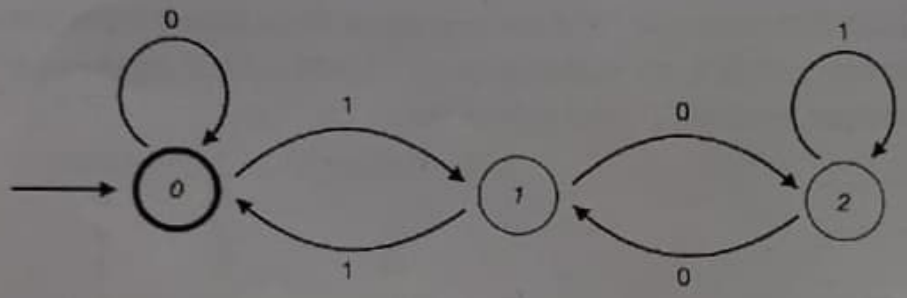
v. Driver and Passenger seats are occupied, ignition is on and seatbelts of either driver or passenger or both are not fastened but one or many doors are not locked properly.

vi. Driver and Passenger seats are occupied, ignition is on and seatbelts of both are fastened but one or many doors are not locked properly.

(Note - Take the output as don't care when ignition is on, driver seat is unoccupied and passenger seat is occupied)

Q9. [6 Marks + 4 Marks = 10 Marks] [CO-3, CO-6]

(a) Consider a "divisible-by-3" FSM that accepts a binary number entered one bit at a time, most significant bit first. The FSM has a one-bit output that indicates if the number entered so far is divisible by 3. If the value of the number entered so far is N, then after the digit b is entered, the value of the new number N' is 2N + b. This leads to the following state-transition diagram where the states are labelled with the value of N mod 3



i. Construct a truth table for the FSM logic. Inputs include the state bits (i.e., 00, 01, or 11) and the next (least significant) bit of the number; outputs include the next state bits and the output.

ii. Based on the truth table, implement the FSM using D flip-flops.

(b) Calculate maximum clock frequency of the circuit in Fig. 9(b).

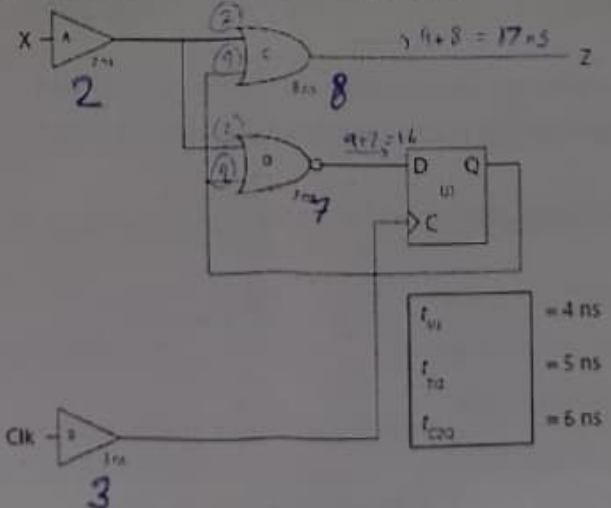


Fig. 9 (b)