7 REGISTER MAP

The following table lists the register map for the ICM-20649, for user banks 0, 1, 2, 3.

7.1 USER BANK 0 REGISTER MAP:

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	0	WHO_AM_I	R	WHO_AM_I[7:0]							
03	3	USER_CTRL	R/W	DMP_EN	FIFO_EN	I2C_MST_EN	I2C_IF_DIS	DMP_RST	SRAM_RST	I2C_MST_RST	-
05	5	LP_CONFIG	R/W		I2C_MST_CYCLE	ACCEL_CYCLE	GYRO_CYCLE	-			
06	6	PWR_MGMT_1	R/W	DEVICE_RESET	SLEEP	LP_EN	-	TEMP_DIS	CLKSEL[2:0]		
07	7	PWR_MGMT_2	R/W	-		DISABLE_ACCEL			DISABLE_GYRO		
0F	15	INT_PIN_CFG	R/W	INT1_ACTL	INT1_OPEN	INT1_LATCH_INT_EN	INT_ANYRD_2CLEAR	ACTL_FSYNC	FSYNC_INT_MODE_EN	BYPASS_EN	-
10	16	INT_ENABLE	R/W	REG_WOF_EN	-		DMP_INT2_EN	WOM_INT_EN	PLL_RDY_EN	DMP_INT1_EN	I2C_MST_INT_EN
11	17	INT_ENABLE_1	R/W	INT2_ACTL	INT2_OPEN	INT2_LATCH_EN	-				RAW_DATA_0_RDY_EN
12	18	INT_ENABLE_2	R/W	-			FIFO_OVERFLOW_EN[4:0]				
13	19	INT_ENABLE_3	R/W	-			FIFO_WM_EN[4:0]				
17	23	I2C_MST_STATUS	R/C	PASS_THROUGH	I2C_SLV4_DONE	I2C_LOST_ARB	I2C_SLV4_NACK	I2C_SLV3_NACK	I2C_SLV2_NACK	I2C_SLV1_NACK	I2C_SLV0_NACK
19	25	INT_STATUS	R/C	-				WOM_INT	PLL_RDY_INT	DMP_INT1	I2C_MST_INT
1A	26	INT_STATUS_1	R/C	-							RAW_DATA_0_RDY_INT
1B	27	INT_STATUS_2	R/C	-			FIFO_OVERFLOW_INT[4:0]				
1C	28	INT_STATUS_3	R/C	-			FIFO_WM_INT[4:0]				
28	40	DELAY_TIMEH	R	DELAY_TIMEH[7:0]							
29	41	DELAY_TIMEL	R	DELAY_TIMEL[7:0]							
2D	45	ACCEL_XOUT_H	R	ACCEL_XOUT_H[7:0]							
2E	46	ACCEL_XOUT_L	R	ACCEL_XOUT_L[7:0]							
2F	47	ACCEL_YOUT_H	R	ACCEL_YOUT_H[7:0]							
30	48	ACCEL_YOUT_L	R	ACCEL_YOUT_L[7:0]							
31	49	ACCEL_ZOUT_H	R	ACCEL_ZOUT_H[7:0]							
32	50	ACCEL_ZOUT_L	R	ACCEL_ZOUT_L[7:0]							
33	51	GYRO_XOUT_H	R	GYRO_XOUT_H[7:0]							
34	52	GYRO_XOUT_L	R	GYRO_XOUT_L[7:0]							
35	53	GYRO_YOUT_H	R	GYRO_YOUT_H[7:0]							
36	54	GYRO_YOUT_L	R	GYRO_YOUT_L[7:0]							
37	55	GYRO_ZOUT_H	R	GYRO_ZOUT_H[7:0]							
38	56	GYRO_ZOUT_L	R	GYRO_ZOUT_L[7:0]							
39	57	TEMP_OUT_H	R	TEMP_OUT_H[7:0]							
3A	58	TEMP_OUT_L	R	TEMP_OUT_L[7:0]							
3B	59	EXT_SLV_SENS_DATA_00	R	EXT_SLV_SENS_DATA_00[7:0]							
3C	60	EXT_SLV_SENS_DATA_01	R	EXT_SLV_SENS_DATA_01[7:0]							
3D	61	EXT_SLV_SENS_DATA_02	R	EXT_SLV_SENS_DATA_02[7:0]							
3E	62	EXT_SLV_SENS_DATA_03	R	EXT_SLV_SENS_DATA_03[7:0]							
3F	63	EXT_SLV_SENS_DATA_04	R	EXT_SLV_SENS_DATA_04[7:0]							
40	64	EXT_SLV_SENS_DATA_05	R	EXT_SLV_SENS_DATA_05[7:0]							
41	65	EXT_SLV_SENS_DATA_06	R	EXT_SLV_SENS_DATA_06[7:0]							
42	66	EXT_SLV_SENS_DATA_07	R	EXT_SLV_SENS_DATA_07[7:0]							
43	67	EXT_SLV_SENS_DATA_08	R	EXT_SLV_SENS_DATA_08[7:0]							
44	68	EXT_SLV_SENS_DATA_09	R	EXT_SLV_SENS_DATA_09[7:0]							
45	69	EXT_SLV_SENS_DATA_10	R	EXT_SLV_SENS_DATA_10[7:0]							
46	70	EXT_SLV_SENS_DATA_11	R	EXT_SLV_SENS_DATA_11[7:0]							
47	71	EXT_SLV_SENS_DATA_12	R	EXT_SLV_SENS_DATA_12[7:0]							
48	72	EXT_SLV_SENS_DATA_13	R	EXT_SLV_SENS_DATA_13[7:0]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
49	73	EXT_SLV_SENS_DATA_14	R	EXT_SLV_SENS_DATA_14[7:0]							
4A	74	EXT_SLV_SENS_DATA_15	R	EXT_SLV_SENS_DATA_15[7:0]							
4B	75	EXT_SLV_SENS_DATA_16	R	EXT_SLV_SENS_DATA_16[7:0]							
4C	76	EXT_SLV_SENS_DATA_17	R	EXT_SLV_SENS_DATA_17[7:0]							
4D	77	EXT_SLV_SENS_DATA_18	R	EXT_SLV_SENS_DATA_18[7:0]							
4E	78	EXT_SLV_SENS_DATA_19	R	EXT_SLV_SENS_DATA_19[7:0]							
4F	79	EXT_SLV_SENS_DATA_20	R	EXT_SLV_SENS_DATA_20[7:0]							
50	80	EXT_SLV_SENS_DATA_21	R	EXT_SLV_SENS_DATA_21[7:0]							
51	81	EXT_SLV_SENS_DATA_22	R	EXT_SLV_SENS_DATA_22[7:0]							
52	82	EXT_SLV_SENS_DATA_23	R	EXT_SLV_SENS_DATA_23[7:0]							
66	102	FIFO_EN_1	R/W	-				SLV_3_FIFO_EN	SLV_2_FIFO_EN	SLV_1_FIFO_EN	SLV_0_FIFO_EN
67	103	FIFO_EN_2	R/W	-			ACCEL_FIFO_EN	GYRO_Z_FIFO_EN	GYRO_Y_FIFO_EN	GYRO_X_FIFO_EN	TEMP_FIFO_EN
68	104	FIFO_RST	R/W	-			FIFO_RESET[4:0]				
69	105	FIFO_MODE	R/W	-			FIFO_MODE[4:0]				
70	112	FIFO_COUNTH	R	-			FIFO_CNT[12:8]				
71	113	FIFO_COUNTL	R	FIFO_CNT[7:0]							
72	114	FIFO_R_W	R/W	FIFO_R_W[7:0]							
74	116	DATA_RDY_STATUS	R/C	WOF_STATUS	-			RAW_DATA_RDY[3:0]			
76	118	FIFO_CFG	R/W	-							FIFO_CFG
7F	127	REG_BANK_SEL	R/W	-		USER_BANK[1:0]		-			

7.2 USER BANK 1 REGISTER MAP:

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02	2	SELF_TEST_X_GYRO	R/W	XG_ST_DATA[7:0]							
03	3	SELF_TEST_Y_GYRO	R/W	YG_ST_DATA[7:0]							
04	4	SELF_TEST_Z_GYRO	R/W	ZG_ST_DATA[7:0]							
0E	14	SELF_TEST_X_ACCEL	R/W	XA_ST_DATA[7:0]							
0F	15	SELF_TEST_Y_ACCEL	R/W	YA_ST_DATA[7:0]							
10	16	SELF_TEST_Z_ACCEL	R/W	ZA_ST_DATA[7:0]							
14	20	XA_OFFS_H	R/W	XA_OFFS[14:7]							
15	21	XA_OFFS_L	R/W	XA_OFFS[6:0]							-
17	23	YA_OFFS_H	R/W	YA_OFFS[14:7]							
18	24	YA_OFFS_L	R/W	YA_OFFS[6:0]							-
1A	26	ZA_OFFS_H	R/W	ZA_OFFS[14:7]							
1B	27	ZA_OFFS_L	R/W	ZA_OFFS[6:0]							-
28	40	TIMEBASE_CORRECTION_PLL	R/W	TBC_PLL[7:0]							
7F	127	REG_BANK_SEL	R/W	-		USER_BANK[1:0]		-			

7.3 USER BANK 2 REGISTER MAP:

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	0	GYRO_SMPLRT_DIV	R/W	GYRO_SMPLRT_DIV[7:0]							
01	1	GYRO_CONFIG_1	R/W	-		GYRO_DLPFCFG[2:0]			GYRO_FS_SEL[1:0]		GYRO_FCHOICE
02	2	GYRO_CONFIG_2	R/W	-		XGYRO_CTEN	YGYRO_CTEN	ZGYRO_CTEN	GYRO_AVGCFG[2:0]		
03	3	XG_OFFS_USRH	R/W	X_OFFS_USER[15:8]							
04	4	XG_OFFS_USRL	R/W	X_OFFS_USER[7:0]							
05	5	YG_OFFS_USRH	R/W	Y_OFFS_USER[15:8]							
06	6	YG_OFFS_USRL	R/W	Y_OFFS_USER[7:0]							
07	7	ZG_OFFS_USRH	R/W	Z_OFFS_USER[15:8]							
08	8	ZG_OFFS_USRL	R/W	Z_OFFS_USER[7:0]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
09	9	ODR_ALIGN_EN	R/W	-							ODR_ALIGN_EN
10	16	ACCEL_SMPLRT_DIV_1	R/W	-				ACCEL_SMPLRT_DIV[11:8]			
11	17	ACCEL_SMPLRT_DIV_2	R/W	ACCEL_SMPLRT_DIV[7:0]							
12	18	ACCEL_INTEL_CTRL	R/W	-						ACCEL_INTEL_EN	ACCEL_INTEL_MODE_INT
13	19	ACCEL_WOM_THR	R/W	WOM_THRESHOLD[7:0]							
14	20	ACCEL_CONFIG	R/W	-		ACCEL_DLPFCFG[2:0]			ACCEL_FS_SEL[1:0]		ACCEL_FCHOICE
15	21	ACCEL_CONFIG_2	R/W	-			AX_ST_EN_REG	AY_ST_EN_REG	AZ_ST_EN_REG	DEC3_CFG[1:0]	
52	82	FSYNC_CONFIG	R/W	DELAY_TIME_EN	-	WOF_DEGLITCH_EN	WOF_EDGE_INT	EXT_SYNC_SET[3:0]			
53	83	TEMP_CONFIG	R/W	-					TEMP_DLPFCFG[2:0]		
54	84	MOD_CTRL_USR	R/W	-							REG_LP_DMP_EN
7F	127	REG_BANK_SEL	R/W	-		USER_BANK[1:0]		-			

7.4 USER BANK 3 REGISTER MAP:

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	0	I2C_MST_ODR_CONFIG	R/W	-				I2C_MST_ODR_CONFIG[3:0]			
01	1	I2C_MST_CTRL	R/W	MULT_MST_EN	-		I2C_MST_P_NSR	I2C_MST_CLK[3:0]			
02	2	I2C_MST_DELAY_CTRL	R/W	DELAY_ES_SHADOW	-		I2C_SLV4_DELAY_EN	I2C_SLV3_DELAY_EN	I2C_SLV2_DELAY_EN	I2C_SLV1_DELAY_EN	I2C_SLV0_DELAY_EN
03	3	I2C_SLV0_ADDR	R/W	I2C_SLV0_RNW	I2C_ID_0[6:0]						
04	4	I2C_SLV0_REG	R/W	I2C_SLV0_REG[7:0]							
05	5	I2C_SLV0_CTRL	R/W	I2C_SLV0_EN	I2C_SLV0_BYTE_SW	I2C_SLV0_REG_DIS	I2C_SLV0_GRP	I2C_SLV0_LENG[3:0]			
06	6	I2C_SLV0_DO	R/W	I2C_SLV0_DO[7:0]							
07	7	I2C_SLV1_ADDR	R/W	I2C_SLV1_RNW	I2C_ID_1[6:0]						
08	8	I2C_SLV1_REG	R/W	I2C_SLV1_REG[7:0]							
09	9	I2C_SLV1_CTRL	R/W	I2C_SLV1_EN	I2C_SLV1_BYTE_SW	I2C_SLV1_REG_DIS	I2C_SLV1_GRP	I2C_SLV1_LENG[3:0]			
0A	10	I2C_SLV1_DO	R/W	I2C_SLV1_DO[7:0]							
0B	11	I2C_SLV2_ADDR	R/W	I2C_SLV2_RNW	I2C_ID_2[6:0]						
0C	12	I2C_SLV2_REG	R/W	I2C_SLV2_REG[7:0]							
0D	13	I2C_SLV2_CTRL	R/W	I2C_SLV2_EN	I2C_SLV2_BYTE_SW	I2C_SLV2_REG_DIS	I2C_SLV2_GRP	I2C_SLV2_LENG[3:0]			
0E	14	I2C_SLV2_DO	R/W	I2C_SLV2_DO[7:0]							
0F	15	I2C_SLV3_ADDR	R/W	I2C_SLV3_RNW	I2C_ID_3[6:0]						
10	16	I2C_SLV3_REG	R/W	I2C_SLV3_REG[7:0]							
11	17	I2C_SLV3_CTRL	R/W	I2C_SLV3_EN	I2C_SLV3_BYTE_SW	I2C_SLV3_REG_DIS	I2C_SLV3_GRP	I2C_SLV3_LENG[3:0]			
12	18	I2C_SLV3_DO	R/W	I2C_SLV3_DO[7:0]							
13	19	I2C_SLV4_ADDR	R/W	I2C_SLV4_RNW	I2C_ID_4[6:0]						
14	20	I2C_SLV4_REG	R/W	I2C_SLV4_REG[7:0]							
15	21	I2C_SLV4_CTRL	R/W	I2C_SLV4_EN	I2C_SLV4_BYTE_SW	I2C_SLV4_REG_DIS	I2C_SLV4_DLY[4:0]				
16	22	I2C_SLV4_DO	R/W	I2C_SLV4_DO[7:0]							
17	23	I2C_SLV4_DI	R	I2C_SLV4_DI[7:0]							
7F	127	REG_BANK_SEL	R/W	-		USER_BANK[1:0]		-			

8 REGISTER DESCRIPTIONS

This section describes the function and contents of each register within the ICM-20649.

Note: The device will come up in sleep mode upon power-up.

8.1 USR BANK 0 REGISTER MAP

8.1.1 WHO_AM_I

Name: WHO_AM_I
Address: 0 (00h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0xE1

BIT	NAME	FUNCTION
7:0	WHO_AM_I[7:0]	Register to indicate to user which device is being accessed. The value for ICM-20649 is 0xE1

8.1.2 USER_CTRL

Name: USER_CTRL
Address: 3 (03h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	DMP_EN	1 – Enables DMP features. 0 – DMP features are disabled after the current processing round has completed.
6	FIFO_EN	1 – Enable FIFO operation mode. 0 – Disable FIFO access from serial interface. To disable FIFO writes by DMA, use FIFO_EN register. To disable possible FIFO writes from DMP, disable the DMP.
5	I2C_MST_EN	1 – Enable the I²C Master I/F module; pins ES_DA and ES_SCL are isolated from pins SDA/SDI and SCL/ SCLK. 0 – Disable I²C Master I/F module; pins ES_DA and ES_SCL are logically driven by pins SDA/SDI and SCL/ SCLK.
4	I2C_IF_DIS	1 – Reset I²C Slave module and put the serial interface in SPI mode only.
3	DMP_RST	1 – Reset DMP module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20 MHz clock.
2	SRAM_RST	1 – Reset SRAM module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20 MHz clock.
1	I2C_MST_RST	1 – Reset I²C Master module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20 MHz clock. **Note**: This bit should only be set when the I²C master has hung. If this bit is set during an active I²C master transaction, the I²C slave will hang, which will require the host to reset the slave.
0	-	Reserved.

8.1.3 LP_CONFIG

Name: LP_CONFIG
Address: 5 (05h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x40

BIT	NAME	FUNCTION
7	-	Reserved.
6	I2C_MST_CYCLE	1 - Operate I^2C master in duty cycled mode. ODR is determined by I2C_MST_ODR_CONFIG register. 0 – Disable I^2C master duty cycled mode.
5	ACCEL_CYCLE	1 – Operate ACCEL in duty cycled mode. ODR is determined by ACCEL_SMPLRT_DIV register. 0 – Disable ACCEL duty cycled mode.
4	GYRO_CYCLE	1 – Operate GYRO in duty cycled mode. ODR is determined by GYRO_SMPLRT_DIV register. 0 – Disable GYRO duty cycled mode.
3:0	-	Reserved.

8.1.4 PWR_MGMT_1

Name: PWR_MGMT_1
Address: 6 (06h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x41

BIT	NAME	FUNCTION
7	DEVICE_RESET	1 – Reset the internal registers and restores the default settings. Write a 1 to set the reset; the bit will auto clear.
6	SLEEP	When set, the chip is set to sleep mode (in sleep mode all analog is powered off). Clearing the bit wakes the chip from sleep mode.
5	LP_EN	The LP_EN only affects the digital circuitry, it helps to reduce the digital current when sensors are in LP mode. Please note that the sensors themselves are set in LP mode by the LP_CONFIG register settings. Sensors in LP mode, and use of LP_EN bit together help to reduce overall current. The bit settings are: 1: Turn on low power feature. 0: Turn off low power feature. LP_EN has no effect when the sensors are in low-noise mode.
4	-	Reserved.
3	TEMP_DIS	When set to 1, this bit disables the temperature sensor.
2:0	CLKSEL[2:0]	**Code** **Clock Source** 0 Internal 20 MHz oscillator 1-5 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 6 Internal 20 MHz oscillator 7 Stops the clock and keeps timing generator in reset **Note**: CLKSEL[2:0] should be set to 1~5 to achieve full gyroscope performance.

8.1.5 PWR_MGMT_2

Name: PWR_MGMT_2
Address: 7 (07h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved.
5:3	DISABLE_ACCEL	Only the following values are applicable: 111 – Accelerometer (all axes) disabled. 000 – Accelerometer (all axes) on.
2:0	DISABLE_GYRO	Only the following values are applicable: 111 – Gyroscope (all axes) disabled. 000 – Gyroscope (all axes) on.

8.1.6 INT_PIN_CFG

Name: INT_PIN_CFG
Address: 15 (0Fh)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	INT1_ACTL	1 – The logic level for INT1 pin is active low. 0 – The logic level for INT1 pin is active high.
6	INT1_OPEN	1 – INT1 pin is configured as open drain. 0 – INT1 pin is configured as push-pull.
5	INT1_LATCH__EN	1 – INT1 pin level held until interrupt status is cleared. 0 – INT1 pin indicates interrupt pulse is width 50 µs.
4	INT_ANYRD_2CLEAR	1 – Interrupt status in INT_STATUS is cleared (set to 0) if any read operation is performed. 0 – Interrupt status in INT_STATUS is cleared (set to 0) only by reading INT_STATUS register. This bit only affects the interrupt status bits that are contained in the register INT_STATUS, and the corresponding hardware interrupt. This bit does not affect the interrupt status bits that are contained in registers INT_STATUS_1, INT_STATUS_2, INT_STATUS_3, and the corresponding hardware interrupt.
3	ACTL_FSYNC	1 – The logic level for the FSYNC pin as an interrupt to the ICM-20649 is active low. 0 – The logic level for the FSYNC pin as an interrupt to the ICM-20649 is active high.
2	FSYNC_INT_MODE_EN	1 – This enables the FSYNC pin to be used as an interrupt. A transition to the active level described by the ACTL_FSYNC bit will cause an interrupt. The status of the interrupt is read in the I²C Master Status register PASS_THROUGH bit. 0 – This disables the FSYNC pin from causing an interrupt.
1	BYPASS_EN	When asserted, the I2C_MASTER interface pins (ES_CL and ES_DA) will go into 'bypass mode' when the I²C master interface is disabled.
0	-	Reserved.

8.1.7 INT_ENABLE

Name: INT_ENABLE
Address: 16 (10h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	REG_WOF_EN	1 – Enable wake on FSYNC interrupt 0 – Function is disabled.
6:5	-	Reserved
4	DMP_INT2_EN	1 – Enable DMP interrupt to propagate to interrupt pin 2. 0 – Function is disabled.
3	WOM_INT_EN	1 – Enable interrupt for wake on motion to propagate to interrupt pin 1. 0 – Function is disabled.
2	PLL_RDY_EN	1 – Enable PLL RDY interrupt (PLL RDY means PLL is running and in use as the clock source for the system) to propagate to interrupt pin 1. 0 – Function is disabled.
1	DMP_INT1_EN	1 – Enable DMP interrupt to propagate to interrupt pin 1. 0 – Function is disabled.
0	I2C_MST_INT_EN	1 – Enable I^2C master interrupt to propagate to interrupt pin 1. 0 – Function is disabled.

8.1.8 INT_ENABLE_1

Name: INT_ENABLE_1
Address: 17 (11h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	INT2_ACTL	1 – The logic level for INT2 pin is active low. 0 – The logic level for INT2 pin is active high.
6	INT2_OPEN	1 – INT2 pin is configured as open drain. 0 – INT2 pin is configured as push-pull.
5	INT2_LATCH_EN	1 – INT2 pin level held until interrupt status is cleared. 0 – INT2 pin indicates interrupt pulse is width 50 µs.
4:1	-	Reserved.
0	RAW_DATA_0_RDY_EN	1 – Enable raw data ready interrupt from any sensor to propagate to interrupt pin 1. 0 – Function is disabled.

8.1.9 INT_ENABLE_2

Name: INT_ENABLE_2
Address: 18 (12h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved.
4:0	FIFO_OVERFLOW_EN[4:0]	1 – Enable interrupt for FIFO overflow to propagate to interrupt pin 1. 0 – Function is disabled.

8.1.10 INT_ENABLE_3

Name: INT_ENABLE_3
Address: 19 (13h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved.
4:0	FIFO_WM_EN[4:0]	1 – Enable interrupt for FIFO watermark to propagate to interrupt pin 1. 0 – Function is disabled.

8.1.11 I2C_MST_STATUS

Name: I2C_MST_STATUS
Address: 23 (17h)
Type: USR0
Bank: 0
Serial IF: R/C
Reset Value: 0x00

BIT	NAME	FUNCTION
7	PASS_THROUGH	Status of FSYNC interrupt – used as a way to pass an external interrupt through this chip to the host. If enabled in the INT_PIN_CFG register by asserting bit FSYNC_INT_MODE_EN, this will cause an interrupt. A read of this register clears all status bits in this register.
6	I2C_SLV4_DONE	Asserted when I^2C slave 4's transfer is complete, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted, and if the SLV4_DONE_INT_EN bit is asserted in the I2C_SLV4_CTRL register.
5	I2C_LOST_ARB	Asserted when I^2C slave loses arbitration of the I^2C bus, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted.
4	I2C_SLV4_NACK	Asserted when slave 4 receives a NACK, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted.
3	I2C_SLV3_NACK	Asserted when slave 3 receives a NACK, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted.
2	I2C_SLV2_NACK	Asserted when slave 2 receives a NACK, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted.
1	I2C_SLV1_NACK	Asserted when slave 1 receives a NACK, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted.
0	I2C_SLV0_NACK	Asserted when slave 0 receives a NACK, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted.

8.1.12 INT_STATUS

Name: INT_STATUS
Address: 25 (19h)
Type: USR0
Bank: 0
Serial IF: R/C
Reset Value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved.
3	WOM_INT	1 – Wake on motion interrupt occurred.
2	PLL_RDY_INT	1 – Indicates that the PLL has been enabled and is ready (delay of 4 ms ensures lock).
1	DMP_INT1	1 – Indicates the DMP has generated INT1 interrupt.
0	I2C_MST_INT	1 - Indicates I^2C master has generated an interrupt.

8.1.13 12.1.13 INT_STATUS_1

Name: INT_STATUS_1
Address: 26 (1Ah)
Type: USR0
Bank: 0
Serial IF: R/C
Reset Value: 0x00

BIT	NAME	FUNCTION
7:1	-	Reserved.
0	RAW_DATA_0_RDY_INT	1 – Sensor Register Raw Data, from all sensors, is updated and ready to be read.

8.1.14 INT_STATUS_2

Name: INT_STATUS_2
Address: 27 (1Bh)
Type: USR0
Bank: 0
Serial IF: R/C
Reset Value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved.
4:0	FIFO_OVERFLOW_INT[4:0]	1 – FIFO Overflow interrupt occurred.

8.1.15 INT_STATUS_3

Name: INT_STATUS_3
Address: 28 (1Ch)
Type: USR0
Bank: 0
Serial IF: R/C
Reset Value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved.
4:0	FIFO_WM_INT[4:0]	1 – Watermark interrupt for FIFO occurred.

8.1.16 DELAY_TIMEH

Name: DELAY_TIMEH
Address: 40 (28h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	DELAY_TIMEH[7:0]	High-byte of delay time between FSYNC event and the 1st gyro ODR event (after the FSYNC event). Reading DELAY_TIMEH will lock DELAY_TIMEH and DELAY_TIMEL from the next update. Reading DELAY_TIMEL will unlock DELAY_TIMEH and DELAY_TIMEL to take the next update due to an FSYNC event.

8.1.17 DELAY_TIMEL

Name: DELAY_TIMEL
Address: 41 (29h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	DELAY_TIMEL[7:0]	Low-byte of delay time between FSYNC event and the 1st gyro ODR event (after the FSYNC event). Reading DELAY_TIMEH will lock DELAY_TIMEH and DELAY_TIMEL from the next update. Reading DELAY_TIMEL will unlock DELAY_TIMEH and DELAY_TIMEL to take the next update due to an FSYNC event. Delay time in µs = (DELAY_TIMEH * 256 + DELAY_TIMEL) * 0.9645

8.1.18 ACCEL_XOUT_H

Name: ACCEL_XOUT_H
Address: 45 (2Dh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_XOUT_H[7:0]	High Byte of Accelerometer X-axis data.

8.1.19 ACCEL_XOUT_L

Name: ACCEL_XOUT_L
Address: 46 (2Eh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_XOUT_L[7:0]	Low Byte of Accelerometer X-axis data. To convert the output of the accelerometer to acceleration measurement use the formula below: X_acceleration = ACCEL_XOUT/Accel_Sensitivity

8.1.20 ACCEL_YOUT_H

Name: ACCEL_YOUT_H
Address: 47 (2Fh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_YOUT_H[7:0]	High Byte of Accelerometer Y-axis data.

8.1.21 ACCEL_YOUT_L

Name: ACCEL_YOUT_L
Address: 48 (30h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_YOUT_L[7:0]	Low Byte of Accelerometer Y-axis data To convert the output of the accelerometer to acceleration measurement use the formula below: Y_acceleration = ACCEL_YOUT/Accel_Sensitivity

8.1.22 ACCEL_ZOUT_H

Name: ACCEL_ZOUT_H
Address: 49 (31h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_ZOUT_H[7:0]	High Byte of Accelerometer Z-axis data.

8.1.23 ACCEL_ZOUT_L

Name: ACCEL_ZOUT_L
Address: 50 (32h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_ZOUT_L[7:0]	Low Byte of Accelerometer Z-axis data. To convert the output of the accelerometer to acceleration measurement use the formula below: Z_acceleration = ACCEL_ZOUT/Accel_Sensitivity

8.1.24 GYRO_XOUT_H

Name: GYRO_XOUT_H
Address: 51 (33h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_XOUT_H[7:0]	High Byte of Gyroscope X-axis data.

8.1.25 GYRO_XOUT_L

Name: GYRO_XOUT_L
Address: 52 (34h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_XOUT_L[7:0]	Low Byte of Gyroscope X-axis data. To convert the output of the gyroscope to angular rate measurement use the formula below: X_angular_rate = GYRO_XOUT/Gyro_Sensitivity

8.1.26 GYRO_YOUT_H

Name: GYRO_YOUT_H
Address: 53 (35h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_YOUT_H[7:0]	High Byte of Gyroscope Y-axis data.

8.1.27 GYRO_YOUT_L

Name: GYRO_YOUT_L
Address: 54 (36h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_YOUT_L[7:0]	Low Byte of Gyroscope Y-axis data. To convert the output of the gyroscope to angular rate measurement use the formula below: Y_angular_rate = GYRO_YOUT/Gyro_Sensitivity

8.1.28 GYRO_ZOUT_H

Name: GYRO_ZOUT_H
Address: 55 (37h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_ZOUT_H[7:0]	High Byte of Gyroscope Z-axis data.

8.1.29 GYRO_ZOUT_L

Name: GYRO_ZOUT_L
Address: 56 (38h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_ZOUT_L[7:0]	Low Byte of Gyroscope Z-axis data. To convert the output of the gyroscope to angular rate measurement use the formula below: Z_angular_rate = GYRO_ZOUT/Gyro_Sensitivity

8.1.30 TEMP_OUT_H

Name: TEMP_OUT_H
Address: 57 (39h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	TEMP_OUT_H[7:0]	High Byte of Temp sensor data.

8.1.31 TEMP_OUT_L

Name: TEMP_OUT_L
Address: 58 (3Ah)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	TEMP_OUT_L[7:0]	Low Byte of Temp sensor data. To convert the output of the temperature sensor to degrees C use the following formula: TEMP_degC = ((TEMP_OUT – RoomTemp_Offset)/Temp_Sensitivity) + 21degC

8.1.32 EXT_SLV_SENS_DATA_00

Name: EXT_SLV_SENS_DATA_00
Address: 59 (3Bh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_00[7:0]	Sensor data read from external I^2C devices via the I^2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.33 EXT_SLV_SENS_DATA_01

Name: EXT_SLV_SENS_DATA_01
Address: 60 (3Ch)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_01[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.34 EXT_SLV_SENS_DATA_02

Name: EXT_SLV_SENS_DATA_02
Address: 61 (3Dh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_02[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.35 EXT_SLV_SENS_DATA_03

Name: EXT_SLV_SENS_DATA_03
Address: 62 (3Eh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_03[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.36 EXT_SLV_SENS_DATA_04

Name: EXT_SLV_SENS_DATA_04
Address: 63 (3Fh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_04[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.37 EXT_SLV_SENS_DATA_05

Name: EXT_SLV_SENS_DATA_05
Address: 64 (40h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_05[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.38 EXT_SLV_SENS_DATA_06

Name: EXT_SLV_SENS_DATA_06
Address: 65 (41h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_06[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.39 EXT_SLV_SENS_DATA_07

Name: EXT_SLV_SENS_DATA_07
Address: 66 (42h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_07[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.40 EXT_SLV_SENS_DATA_08

Name: EXT_SLV_SENS_DATA_08
Address: 67 (43h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_08[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.41 EXT_SLV_SENS_DATA_09

Name: EXT_SLV_SENS_DATA_09
Address: 68 (44h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_09[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.42 EXT_SLV_SENS_DATA_10

Name: EXT_SLV_SENS_DATA_10
Address: 69 (45h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_10[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.43 EXT_SLV_SENS_DATA_11

Name: EXT_SLV_SENS_DATA_11
Address: 70 (46h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_11[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.44 EXT_SLV_SENS_DATA_12

Name: EXT_SLV_SENS_DATA_12
Address: 71 (47h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_12[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.45 EXT_SLV_SENS_DATA_13

Name: EXT_SLV_SENS_DATA_13
Address: 72 (48h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_13[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.46 EXT_SLV_SENS_DATA_14

Name: EXT_SLV_SENS_DATA_14
Address: 73 (49h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_14[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.47 EXT_SLV_SENS_DATA_15

Name: EXT_SLV_SENS_DATA_15
Address: 74 (4Ah)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_15[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.48 EXT_SLV_SENS_DATA_16

Name: EXT_SLV_SENS_DATA_16
Address: 75 (4Bh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_16[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.49 EXT_SLV_SENS_DATA_17

Name: EXT_SLV_SENS_DATA_17
Address: 76 (4Ch)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_17[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.50 EXT_SLV_SENS_DATA_18

Name: EXT_SLV_SENS_DATA_18
Address: 77 (4Dh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_18[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.51 EXT_SLV_SENS_DATA_19

Name: EXT_SLV_SENS_DATA_19
Address: 78 (4Eh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_19[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.52 EXT_SLV_SENS_DATA_20

Name: EXT_SLV_SENS_DATA_20
Address: 79 (4Fh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_20[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.53 EXT_SLV_SENS_DATA_21

Name: EXT_SLV_SENS_DATA_21
Address: 80 (50h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_21[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.54 EXT_SLV_SENS_DATA_22

Name: EXT_SLV_SENS_DATA_22
Address: 81 (51h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_22[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.55 EXT_SLV_SENS_DATA_23

Name: EXT_SLV_SENS_DATA_23
Address: 82 (52h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_23[7:0]	Sensor data read from external I²C devices via the I²C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers.

8.1.56 FIFO_EN_1

Name: FIFO_EN_1
Address: 102 (66h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved.
3	SLV_3_FIFO_EN	1 – Write EXT_SENS_DATA registers associated to SLV_3 (as determined by I2C_SLV2_CTRL, I2C_SLV1_CTRL, and I2C_SL20_CTRL) to the FIFO at the sample rate. 0 – Function is disabled.
2	SLV_2_FIFO_EN	1 – Write EXT_SENS_DATA registers associated to SLV_2 (as determined by I2C_SLV0_CTRL, I2C_SLV1_CTRL, and I2C_SL20_CTRL) to the FIFO at the sample rate. 0 – Function is disabled.
1	SLV_1_FIFO_EN	1 – Write EXT_SENS_DATA registers associated to SLV_1 (as determined by I2C_SLV0_CTRL and I2C_SLV1_CTRL) to the FIFO at the sample rate. 0 – Function is disabled.
0	SLV_0_FIFO_EN	1 – Write EXT_SENS_DATA registers associated to SLV_0 (as determined by I2C_SLV0_CTRL) to the FIFO at the sample rate. 0 – Function is disabled.

8.1.57 FIFO_EN_2

Name: FIFO_EN_2
Address: 103 (67h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved.
4	ACCEL_FIFO_EN	1 – Write ACCEL_XOUT_H, ACCEL_XOUT_L, ACCEL_YOUT_H, ACCEL_YOUT_L, ACCEL_ZOUT_H, and ACCEL_ZOUT_L to the FIFO at the sample rate. 0 – Function is disabled.
3	GYRO_Z_FIFO_EN	1 – Write GYRO_ZOUT_H and GYRO_ZOUT_L to the FIFO at the sample rate. 0 – Function is disabled.
2	GYRO_Y_FIFO_EN	1 – Write GYRO_YOUT_H and GYRO_YOUT_L to the FIFO at the sample rate. 0 – Function is disabled.
1	GYRO_X_FIFO_EN	1 – Write GYRO_XOUT_H and GYRO_XOUT_L to the FIFO at the sample rate. 0 – Function is disabled.
0	TEMP_FIFO_EN	1 – Write TEMP_OUT_H and TEMP_OUT_L to the FIFO at the sample rate. 0– Function is disabled.

8.1.58 FIFO_RST

Name: FIFO_RST
Address: 104 (68h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved.
4:0	FIFO_RESET[4:0]	S/W FIFO reset. Assert and hold to set FIFO size to 0. Assert and de-assert to reset FIFO.

8.1.59 FIFO_MODE

Name: FIFO_MODE
Address: 105 (69h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved.
4:0	FIFO_MODE[4:0]	0 - Stream 1 - Snapshot When set to '1', when the FIFO is full, additional writes will not be written to FIFO. When set to '0', when the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data.

8.1.60 FIFO_COUNTH

Name: FIFO_COUNTH
Address: 112 (70h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved.
4:0	FIFO_CNT[12:8]	High Bits, count indicates the number of written bytes in the FIFO. Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL.

8.1.61 FIFO_COUNTL

Name: FIFO_COUNTL
Address: 113 (71h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	FIFO_CNT[7:0]	Low bits, count indicates the number of written bytes in the FIFO.

8.1.62 FIFO_R_W

Name: FIFO_R_W
Address: 114 (72h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	FIFO_R_W[7:0]	Reading from or writing to this register actually reads/writes the FIFO. For example, to write a byte to the FIFO, write the desired byte value to FIFO_R_W[7:0]. To read a byte from the FIFO, perform a register read operation and access the result in FIFO_R_W[7:0].

8.1.63 DATA_RDY_STATUS

Name: DATA_RDY_STATUS
Address: 116 (74h)
Type: USR0
Bank: 0
Serial IF: R/C
Reset Value: 0x00

BIT	NAME	FUNCTION
7	WOF_STATUS	Wake on FSYNC interrupt status. Cleared on read.
6:4	-	Reserved.
3:0	RAW_DATA_RDY[3:0]	Data from sensors is copied to FIFO or SRAM. Set when sequence controller kicks off on a sensor data load. Only bit 0 is relevant in a single FIFO configuration. Cleared on read.

8.1.64 FIFO_CFG

Name: FIFO_CFG
Address: 118 (76h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:1	-	Reserved.
0	FIFO_CFG	This bit should be set to 1 if interrupt status for each sensor is required.

8.1.65 REG_BANK_SEL

Name: REG_BANK_SEL
Address: 127 (7Fh)
Type: ALL
Bank: 0
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved.
5:4	USER_BANK[1:0]	Use the following values in this bit-field to select a USER BANK. 0: Select USER BANK 0 1: Select USER BANK 1 2: Select USER BANK 2 3: Select USER BANK 3
3:0	-	Reserved.

8.2 USR BANK 1 REGISTER MAP

8.2.1 SELF_TEST_X_GYRO

Name: SELF_TEST_X_GYRO
Address: 2 (02h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	XG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

8.2.2 SELF_TEST_Y_GYRO

Name: SELF_TEST_Y_GYRO
Address: 3 (03h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	YG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

8.2.3 SELF_TEST_Z_GYRO

Name: SELF_TEST_Z_GYRO
Address: 4 (04h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	ZG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

8.2.4 SELF_TEST_X_ACCEL

Name: SELF_TEST_X_ACCEL
Address: 14 (0Eh)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	XA_ST_DATA[7:0]	Contains self-test data for the X Accelerometer.

8.2.5 SELF_TEST_Y_ACCEL

Name: SELF_TEST_Y_ACCEL
Address: 15 (0Fh)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	YA_ST_DATA[7:0]	Contains self-test data for the Y Accelerometer.

8.2.6 SELF_TEST_Z_ACCEL

Name: SELF_TEST_Z_ACCEL
Address: 16 (10h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	ZA_ST_DATA[7:0]	Contains self-test data for the Z Accelerometer.

8.2.7 XA_OFFS_H

Name: XA_OFFS_H
Address: 20 (14h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: Trimmed on a per-part basis for optimal performance

BIT	NAME	FUNCTION
7:0	XA_OFFS[14:7]	Upper bits of the X accelerometer offset cancellation.

8.2.8 XA_OFFS_L

Name: XA_OFFS_L
Address: 21 (15h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: Trimmed on a per-part basis for optimal performance

BIT	NAME	FUNCTION
7:1	XA_OFFS[6:0]	Lower bits of the X accelerometer offset cancellation.
0	-	Reserved.

8.2.9 YA_OFFS_H

Name: YA_OFFS_H
Address: 23 (17h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: Trimmed on a per-part basis for optimal performance

BIT	NAME	FUNCTION
7:0	YA_OFFS[14:7]	Upper bits of the Y accelerometer offset cancellation.

8.2.10 YA_OFFS_L

Name: YA_OFFS_L
Address: 24 (18h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: Trimmed on a per-part basis for optimal performance

BIT	NAME	FUNCTION
7:1	YA_OFFS[6:0]	Lower bits of the Y accelerometer offset cancellation.
0	-	Reserved.

8.2.11 ZA_OFFS_H

Name: ZA_OFFS_H
Address: 26 (1Ah)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: Trimmed on a per-part basis for optimal performance

BIT	NAME	FUNCTION
7:0	ZA_OFFS[14:7]	Upper bits of the Z accelerometer offset cancellation.

8.2.12 ZA_OFFS_L

Name: ZA_OFFS_L
Address: 27 (1Bh)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: Trimmed on a per-part basis for optimal performance

BIT	NAME	FUNCTION
7:1	ZA_OFFS[6:0]	Lower bits of the Z accelerometer offset cancellation.
0	-	Reserved.

8.2.13 TIMEBASE_CORRECTION_PLL

Name: TIMEBASE_CORRECTION_PLL
Address: 40 (28h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	TBC_PLL[7:0]	System PLL clock period error (signed, [-10%, +10%]).

8.2.14 REG_BANK_SEL

Name: REG_BANK_SEL
Address: 127 (7Fh)
Type:
Bank: 1
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved.
5:4	USER_BANK[1:0]	Use the following values in this bit-field to select a USER BANK 0: Select USER BANK 0 1: Select USER BANK 1 2: Select USER BANK 2 3: Select USER BANK 3
3:0	-	Reserved.

8.3 USR BANK 2 REGISTER MAP

8.3.1 GYRO_SMPLRT_DIV

Name: GYRO_SMPLRT_DIV
Address: 0 (00h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_SMPLRT_DIV[7:0]	Gyro sample rate divider. Divides the internal sample rate to generate the sample rate that controls sensor data output rate, FIFO sample rate, and DMP sequence rate. **Note**: This register is only effective when FCHOICE = 1'b1 (FCHOICE_B register bit is 1'b0), and (0 < DLPF_CFG < 7). ODR is computed as follows: 1.1 kHz/(1+GYRO_SMPLRT_DIV[7:0])

8.3.2 GYRO_CONFIG_1

Name: GYRO_CONFIG_1
Address: 1 (01h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x01

BIT	NAME	FUNCTION
7:6	-	Reserved.
5:3	GYRO_DLPFCFG[2:0]	Gyro low pass filter configuration as shown in Table 15.
2:1	GYRO_FS_SEL[1:0]	Gyro Full Scale Select: 00 = ±500 dps 01= ±1000 dps 10 = ±2000 dps 11 = ±4000 dps
0	GYRO_FCHOICE	0 – Bypass gyro DLPF. 1 – Enable gyro DLPF.

The gyroscope DLPF is configured by GYRO_DLPFCFG, when GYRO_FCHOICE = 1. The gyroscope data is filtered according to the value of GYRO_DLPFCFG and GYRO_FCHOICE as shown in Table 15.

GYRO_FCHOICE	GYRO_DLPFCFG	Output		
		3dB BW [Hz]	NBW [Hz]	Rate [Hz]
0	x	12106	12316	9000
1	0	196.6	229.8	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	1	151.8	187.6	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	2	119.5	154.3	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	3	51.2	73.3	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	4	23.9	35.9	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	5	11.6	17.8	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	6	5.7	8.9	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	7	361.4	376.5	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255

Table 15. Configuration

8.3.3 GYRO_CONFIG_2

Name: GYRO_CONFIG_2
Address: 2 (02h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved.
5	XGYRO_CTEN	X Gyro self-test enable.
4	YGYRO_CTEN	Y Gyro self-test enable.
3	ZGYRO_CTEN	Z Gyro self-test enable.
2:0	GYRO_AVGCFG[2:0]	Averaging filter configuration settings for low-power mode. 0: 1x averaging 1: 2x averaging 2: 4x averaging 3: 8x averaging 4: 16x averaging 5: 32x averaging 6: 64x averaging 7: 128x averaging

Table 16 lists the gyroscope filter bandwidths available in the low-power mode of operation. In the low-power mode of operation, the gyroscope is duty-cycled.

	Averages	1x	2x	4x	8x	16x	32x	64x	128x
	GYRO_FCHOICE	1	1	1	1	1	1	1	1
	GYRO_AVGCFG	0	1	2	3	4	5	6	7
	Ton [ms]	1.15	1.59	2.48	4.26	7.82	14.93	29.15	57.59
	NBW [Hz]	773.5	469.8	257.8	134.8	68.9	34.8	17.5	8.8
	RMS Noise [dps-rms] TYP (based on gyroscope noise: 0.0175dps/√Hz)	0.49	0.38	0.28	0.20	0.15	0.10	0.07	0.05
GYRO_SMPLRT_DIV	ODR [Hz]	Current Consumption [mA] TYP							
255	4.4	1.04	1.05	1.05	1.06	1.09	1.14	1.24	1.45
64	17.3	1.07	1.08	1.10	1.15	1.25	1.45	1.85	N/A
63	17.6	1.07	1.08	1.11	1.16	1.26	1.46	1.87	
32	34.1	1.10	1.12	1.17	1.27	1.47	1.86	N/A	
31	35.2	1.10	1.13	1.18	1.28	1.48	1.89		
22	48.9	1.13	1.16	1.23	1.37	1.66	2.22		
16	66.2	1.16	1.21	1.30	1.49	1.88	N/A		
15	70.3	1.17	1.22	1.32	1.52	1.93			
10	102.3	1.23	1.30	1.45	1.74	2.34			
8	125.0	1.27	1.36	1.54	1.90	N/A			
7	140.6	1.30	1.40	1.60	2.01				
5	187.5	1.38	1.52	1.79	2.33				
4	225.0	1.45	1.62	1.94	N/A				
3	281.3	1.56	1.76	2.17					
2	375.0	1.74	2.00	N/A					
1	562.5	2.09	N/A						

Table 16. Gyroscope Filter Bandwidths (Low-Power Mode)

Note: Ton is the ON time for motion measurement when the gyroscope is in duty cycle mode.

8.3.4 XG_OFFS_USRH

Name: XG_OFFS_USRH
Address: 3 (03h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	X_OFFS_USER[15:8]	Upper byte of X gyro offset cancellation.

8.3.5 XG_OFFS_USRL

Name: XG_OFFS_USRL
Address: 4 (04h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	X_OFFS_USER[7:0]	Lower byte of X gyro offset cancellation.

8.3.6 YG_OFFS_USRH

Name: YG_OFFS_USRH
Address: 5 (05h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	Y_OFFS_USER[15:8]	Upper byte of Y gyro offset cancellation.

8.3.7 YG_OFFS_USRL

Name: YG_OFFS_USRL
Address: 6 (06h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	Y_OFFS_USER[7:0]	Lower byte of Y gyro offset cancellation.

8.3.8 ZG_OFFS_USRH

Name: ZG_OFFS_USRH
Address: 7 (07h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	Z_OFFS_USER[15:8]	Upper byte of Z gyro offset cancellation.

8.3.9 ZG_OFFS_USRL

Name: ZG_OFFS_USRL
Address: 8 (08h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	Z_OFFS_USER[7:0]	Lower byte of Z gyro offset cancellation.

8.3.10 ODR_ALIGN_EN

Name: ODR_ALIGN_EN
Address: 9 (09h)
Type: USR2
Bank: 2
OTP: No
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:1	-	Reserved.
0	ODR_ALIGN_EN	0: Disables ODR start-time alignment. 1: Enables ODR start-time alignment when any of the following registers is written (with the same value or with different values): GYRO_SMPLRT_DIV, ACCEL_SMPLRT_DIV_1, ACCEL_SMPLRT_DIV_2, I2C_MST_ODR_CONFIG

8.3.11 ACCEL_SMPLRT_DIV_1

Name: ACCEL_SMPLRT_DIV_1
Address: 16 (10h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved.
3:0	ACCEL_SMPLRT_DIV[11:8]	MSB for ACCEL sample rate div.

8.3.12 ACCEL_SMPLRT_DIV_2

Name: ACCEL_SMPLRT_DIV_2
Address: 17 (11h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_SMPLRT_DIV[7:0]	LSB for ACCEL sample rate div. ODR is computed as follows: 1.125 kHz/(1+ACCEL_SMPLRT_DIV[11:0])

8.3.13 ACCEL_INTEL_CTRL

Name: ACCEL_INTEL_CTRL
Address: 18 (12h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:2	-	Reserved.
1	ACCEL_INTEL_EN	Enable the WOM logic.
0	ACCEL_INTEL_MODE_INT	Selects WOM algorithm. 1- Compare the current sample with the previous sample. 0 - Initial sample is stored, all future samples are compared to the initial sample

8.3.14 ACCEL_WOM_THR

Name: ACCEL_WOM_THR
Address: 19 (13h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	WOM_THRESHOLD[7:0]	This register holds the threshold value for the Wake on Motion Interrupt for ACCEL x/y/z axes. LSB = 4 mg. Range is 0 mg to 1020 mg

8.3.15 ACCEL_CONFIG

Name: ACCEL_CONFIG
Address: 20 (14h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x01

BIT	NAME	FUNCTION
7:6	-	Reserved.
5:3	ACCEL_DLPFCFG[2:0]	Accelerometer low pass filter configuration as shown in Table 17.
2:1	ACCEL_FS_SEL[1:0]	Accelerometer Full Scale Select: 00: ±4*g* 01: ±8*g* 10: ±16*g* 11: ±30*g*
0	ACCEL_FCHOICE	0 - Bypass accel DLPF. 1 - Enable accel DLPF.

ACCEL_FCHOICE	ACCEL_DLPFCFG	Output		
		3dB BW [Hz]	NBW [Hz]	Rate [Hz]
0	x	1209	1248	4500
1	0	246.0	265.0	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…4095
1	1	246.0	265.0	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…4095
1	2	111.4	136.0	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…4095
1	3	50.4	68.8	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…4095
1	4	23.9	34.4	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…4095
1	5	11.5	17.0	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…4095
1	6	5.7	8.3	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…4095
1	7	473	499	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…4095

Table 17. Accelerometer Configuration

The data rate out of the DLPF filter block can be further reduced by a factor of 1.125 kHz/(1+ACCEL_SMPLRT_DIV[11:0]) where ACCEL_SMPLRT_DIV is a 12-bit integer.

8.3.16 ACCEL_CONFIG_2

Name: ACCEL_CONFIG_2
Address: 21 (15h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved.
4	AX_ST_EN_REG	X Accel self-test enable.
3	AY_ST_EN_REG	Y Accel self-test enable.
2	AZ_ST_EN_REG	Z Accel self-test enable.
1:0	DEC3_CFG[1:0]	Controls the number of samples averaged in the accelerometer decimator: 0: Average 1 or 4 samples depending on ACCEL_FCHOICE (see table below) 1 - Average 8 samples. 2 - Average 16 samples. 3 - Average 32 samples.

Table 18 lists the accelerometer filter bandwidths available in the low-power mode of operation. In the low-power mode of operation, the accelerometer is duty-cycled.

	Averages	1x	4x	8x	16x	32x
	ACCEL_FCHOICE	0	1	1	1	1
	ACCEL_DLPFCFG	x	7	7	7	7
	DEC3_CFG	0	0	1	2	3
	Ton (ms)	0.821	1.488	2.377	4.154	7.71
	NBW (Hz)	1237.5	496.8	264.8	136.5	69.2
	RMS Noise [mg-rms] TYP (based on accelerometer noise: 285µg/√Hz)	10.0	6.4	4.6	3.3	2.4
ACCEL_SMPLRT_DIV	ODR [Hz]	Current Consumption [µA] TYP				
4095	0.27	6.2	6.3	6.5	6.9	7.6
2044	0.55	6.3	6.6	7.0	7.7	9.2
1022	1.1	6.7	7.2	8.0	9.4	12.3
513	2.2	7.3	8.4	9.9	12.8	18.6
255	4.4	8.7	10.9	13.8	19.7	31.4
127	8.8	11.4	15.8	21.6	33.3	56.7
63	17.6	16.8	25.6	37.3	60.7	107.5
31	35.2	27.6	45.2	68.6	115.3	208.9
22	48.9	36.1	60.5	93.0	158.1	288.3
15	70.3	49.2	84.3	131.1	224.7	411.9
10	102.3	68.9	119.9	188.0	324.1	596.3
7	140.6	92.4	162.7	256.3	443.3	N/A
5	187.5	121.2	214.9			
3	281.3	178.9	319.3	N/A		
1	562.5	351.7	N/A			

Table 18. Accelerometer Configuration 2

Note: Ton is the ON time for motion measurement when the accelerometer is in duty cycle mode.

8.3.17 FSYNC_CONFIG

Name: FSYNC_CONFIG
Address: 82 (52h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	DELAY_TIME_EN	0 - Disables delay time measurement between FSYNC event and the first ODR event (after FSYNC event). 1 - Enables delay time measurement between FSYNC event and the first ODR event (after FSYNC event).
6	-	Reserved.
5	WOF_DEGLITCH_EN	Enables digital deglitching of FSYNC input for Wake on FSYNC.
4	WOF_EDGE_INT	0 - FSYNC is a level interrupt for Wake on FSYNC. 1 - FSYNC is an edge interrupt for Wake on FSYNC. ACTL_FSYNC is used to set the polarity of the interrupt.
3:0	EXT_SYNC_SET[3:0]	Enables the FSYNC pin data to be sampled. EXT_SYNC_SET FSYNC bit location. 0 - Function disabled 1 - TEMP_OUT_L[0] 2 - GYRO_XOUT_L[0] 3 - GYRO_YOUT_L[0] 4 - GYRO_ZOUT_L[0] 5 - ACCEL_XOUT_L[0] 6 - ACCEL_YOUT_L[0] 7 - ACCEL_ZOUT_L[0]

8.3.18 TEMP_CONFIG

Name: TEMP_CONFIG
Address: 83 (53h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
2:0	TEMP_DLPFCFG[2:0]	Low pass filter configuration for temperature sensor as shown in the table below:

TEMP_DLPCFG<2:0>	Temp Sensor	
	NBW (Hz)	Rate (kHz)
0	7932.0	9
1	217.9	1.125
2	123.5	1.125
3	65.9	1.125
4	34.1	1.125
5	17.3	1.125
6	8.8	Rate (kHz)
7	7932.0	9

8.3.19 MOD_CTRL_USR

Name: MOD_CTRL_USR
Address: 84 (54h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x03

BIT	NAME	FUNCTION
7:1	-	Reserved.
0	REG_LP_DMP_EN	Enable turning on DMP in Low Power Accelerometer mode.

8.3.20 REG_BANK_SEL

Name: REG_BANK_SEL
Address: 127 (7Fh)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved.
5:4	USER_BANK[1:0]	Use the following values in this bit-field to select a USER BANK. 0 - Select USER BANK 0 1 - Select USER BANK 1 2 - Select USER BANK 2 3 - Select USER BANK 3
3:0	-	Reserved.

8.4 USR BANK 3 REGISTER MAP

8.4.1 I2C_MST_ODR_CONFIG

Name: I2C_MST_ODR_CONFIG
Address: 0 (00h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved.
3:0	I2C_MST_ODR_CONFIG[3:0]	ODR configuration for external sensor when gyroscope and accelerometer are disabled. ODR is computed as follows: 1 -1 kHz/(2^((odr_config[3:0]))) When gyroscope is enabled, all sensors (including I2C_MASTER) use the gyroscope ODR. If gyroscope is disabled then all sensors (including I2C_MASTER) use the accelerometer ODR.

8.4.2 I2C_MST_CTRL

Name: I2C_MST_CTRL
Address: 1 (01h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	MULT_MST_EN	Enables multi-master capability. When disabled, clocking to the I2C_MST_IF can be disabled when not in use and the logic to detect lost arbitration is disabled.
6:5	-	Reserved.
4	I2C_MST_P_NSR	This bit controls the I^2C Master's transition from one slave read to the next slave read. 0 - There is a restart between reads. 1 - There is a stop between reads.
3:0	I2C_MST_CLK[3:0]	Sets I^2C master clock frequency as shown in Table 19.

8.4.3 I2C_MST_DELAY_CTRL

Name: I2C_MST_DELAY_CTRL
Address: 2 (02h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	DELAY_ES_SHADOW	Delays shadowing of external sensor data until all data is received.
6:5	-	Reserved.
4	I2C_SLV4_DELAY_EN	When enabled, slave 4 will only be accessed 1/(1+I2C_SLC4_DLY) samples as determined by I2C_MST_ODR_CONFIG.
3	I2C_SLV3_DELAY_EN	When enabled, slave 3 will only be accessed 1/(1+I2C_SLC4_DLY) samples as determined by I2C_MST_ODR_CONFIG.
2	I2C_SLV2_DELAY_EN	When enabled, slave 2 will only be accessed 1/(1+I2C_SLC4_DLY) samples as determined by I2C_MST_ODR_CONFIG.
1	I2C_SLV1_DELAY_EN	When enabled, slave 1 will only be accessed 1/(1+I2C_SLC4_DLY) samples as determined by I2C_MST_ODR_CONFIG.
0	I2C_SLV0_DELAY_EN	When enabled, slave 0 will only be accessed 1/(1+I2C_SLC4_DLY) samples as determined by I2C_MST_ODR_CONFIG.

8.4.4 I2C_SLV0_ADDR

Name: I2C_SLV0_ADDR
Address: 3 (03h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	I2C_SLV0_RNW	1 – Transfer is a read. 0 – Transfer is a write.
6:0	I2C_ID_0[6:0]	Physical address of I^2C slave 0.

8.4.5 I2C_SLV0_REG

Name: I2C_SLV0_REG
Address: 4 (04h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	I2C_SLV0_REG[7:0]	I^2C slave 0 register address from where to begin data transfer.

8.4.6 I2C_SLV0_CTRL

Name: I2C_SLV0_CTRL
Address: 5 (05h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	I2C_SLV0_EN	1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register, which is always EXT_SENS_DATA_00 for I^2C slave 0. 0 – Function is disabled for this slave.
6	I2C_SLV0_BYTE_SW	1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV0_REG[0] = 1, or if the last byte read has a register address LSB = 0. For example, if I2C_SLV0_REG = 0x1, and I2C_SLV0_LENG = 0x4: 1) The first byte read from address 0x1 will be stored at EXT_SENS_DATA_00, 2) The second and third bytes will be read and swapped, so the data read from address 0x2 will be stored at EXT_SENS_DATA_02, and the data read from address 0x3 will be stored at EXT_SENS_DATA_01, 3) The last byte read from address 0x4 will be stored at EXT_SENS_DATA_03 0 – No swapping occurs; bytes are written in order read.
5	I2C_SLV0_REG_DIS	When set, the transaction does not write a register value, it will only read data, or write data
4	I2C_SLV0_GRP	External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc.., or if the groups are address 1 and 2, 3 and 4, etc. 0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address.
3:0	I2C_SLV0_LENG[3:0]	Number of bytes to be read from I^2C slave 0.

8.4.7 I2C_SLV0_DO

Name: I2C_SLV0_DO
Address: 6 (06h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	I2C_SLV0_DO[7:0]	Data out when slave 0 is set to write.

8.4.8 I2C_SLV1_ADDR

Name: I2C_SLV1_ADDR
Address: 7 (07h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	I2C_SLV1_RNW	1 – Transfer is a read. 0 – Transfer is a write.
6:0	I2C_ID_1[6:0]	Physical address of I^2C slave 1.

8.4.9 I2C_SLV1_REG

Name: I2C_SLV1_REG
Address: 8 (08h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	I2C_SLV1_REG[7:0]	I^2C slave 1 register address from where to begin data transfer.

8.4.10 I2C_SLV1_CTRL

Name: I2C_SLV1_CTRL
Address: 9 (09h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	I2C_SLV1_EN	1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register as determined by I2C_SLV0_EN and I2C_SLV0_LENG. 0 – Function is disabled for this slave.
6	I2C_SLV1_BYTE_SW	1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV1_REG[0] = 1, or if the last byte read has a register address LSB = 0. For example, if I2C_SLV0_EN = 0x1, and I2C_SLV0_LENG = 0x3 (to show swap has to do with I²C slave address not EXT_SENS_DATA address), and if I2C_SLV1_REG = 0x1, and I2C_SLV1_LENG = 0x4: 1) The first byte read from address 0x1 will be stored at EXT_SENS_DATA_03 (slave 0's data will be in EXT_SENS_DATA_00, EXT_SENS_DATA_01, and EXT_SENS_DATA_02), 2) The second and third bytes will be read and swapped, so the data read from address 0x2 will be stored at EXT_SENS_DATA_04, and the data read from address 0x3 will be stored at EXT_SENS_DATA_05, 3) The last byte read from address 0x4 will be stored at EXT_SENS_DATA_06 0 – No swapping occurs; bytes are written in order read.
5	I2C_SLV1_REG_DIS	When set, the transaction does not write a register value, it will only read data, or write data
4	I2C_SLV1_GRP	External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc., or if the groups are address 1 and 2, 3 and 4, etc. 0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address.
3:0	I2C_SLV1_LENG[3:0]	Number of bytes to be read from I²C slave 1.

8.4.11 SLV1_DO

Name: I2C_SLV1_DO
Address: 10 (0Ah)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	I2C_SLV1_DO[7:0]	Data out when slave 1 is set to write.

8.4.12 I2C_SLV2_ADDR

Name: I2C_SLV2_ADDR
Address: 11 (0Bh)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	I2C_SLV2_RNW	1 – Transfer is a read. 0 – Transfer is a write.
6:0	I2C_ID_2[6:0]	Physical address of I^2C slave 2.

8.4.13 I2C_SLV2_REG

Name: I2C_SLV2_REG
Address: 12 (0Ch)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	I2C_SLV2_REG[7:0]	I^2C slave 2 register address from where to begin data transfer.

8.4.14 I2C_SLV2_CTRL

Name: I2C_SLV2_CTRL
Address: 13 (0Dh)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	I2C_SLV2_EN	1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register as determined by I2C_SLV0_EN, I2C_SLV0_LENG, I2C_SLV1_EN and I2C_SLV1_LENG. 0 – Function is disabled for this slave.
6	I2C_SLV2_BYTE_SW	1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV2_REG[0] = 1, or if the last byte read has a register address LSB = 0. See I2C_SLV1_CTRL for an example. 0 – No swapping occurs; bytes are written in order read.
5	I2C_SLV2_REG_DIS	When set, the transaction does not write a register value, it will only read data, or write data
4	I2C_SLV2_GRP	External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc.., or if the groups are address 1 and 2, 3 and 4, etc. 0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address.
3:0	I2C_SLV2_LENG[3:0]	Number of bytes to be read from I^2C slave 2.

8.4.15 I2C_SLV2_DO

Name: I2C_SLV2_DO
Address: 14 (0Eh)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	I2C_SLV2_DO[7:0]	Data out when slave 2 is set to write.

8.4.16 I2C_SLV3_ADDR

Name: I2C_SLV3_ADDR
Address: 15 (0Fh)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	I2C_SLV3_RNW	1 – Transfer is a read. 0 – Transfer is a write.
6:0	I2C_ID_3[6:0]	Physical address of I^2C slave 3.

8.4.17 I2C_SLV3_REG

Name: I2C_SLV3_REG
Address: 16 (10h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	I2C_SLV3_REG[7:0]	I^2C slave 3 register address from where to begin data transfer.

8.4.18 I2C_SLV3_CTRL

Name: I2C_SLV3_CTRL
Address: 17 (11h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	I2C_SLV3_EN	1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register as determined by I2C_SLV0_EN, I2C_SLV0_LENG, I2C_SLV1_EN, I2C_SLV1_LENG, I2C_SLV2_EN and I2C_SLV2_LENG. 0 – Function is disabled for this slave.
6	I2C_SLV3_BYTE_SW	1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV3_REG[0] = 1, or if the last byte read has a register address LSB = 0. See I2C_SLV1_CTRL for an example. 0 – No swapping occurs, bytes are written in order read.
5	I2C_SLV3_REG_DIS	When set, the transaction does not write a register value, it will only read data, or write data
4	I2C_SLV3_GRP	External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc., or if the groups are address 1 and 2, 3 and 4, etc. 0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address.
3:0	I2C_SLV3_LENG[3:0]	Number of bytes to be read from I^2C slave 3.

8.4.19 I2C_SLV3_DO

Name: I2C_SLV3_DO
Address: 18 (12h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	I2C_SLV3_DO[7:0]	Data out when slave 3 is set to write.

8.4.20 I2C_SLV4_ADDR

Name: I2C_SLV4_ADDR
Address: 19 (13h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	I2C_SLV4_RNW	1 – Transfer is a read. 0 – Transfer is a write.
6:0	I2C_ID_4[6:0]	Physical address of I^2C slave 4.

Note: The I^2C Slave 4 interface can be used to perform only single byte read and write transactions.

8.4.21 I2C_SLV4_REG

Name: I2C_SLV4_REG
Address: 20 (14h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	I2C_SLV4_REG[7:0]	I^2C slave 4 register address from where to begin data transfer.

8.4.22 I2C_SLV4_CTRL

Name: I2C_SLV4_CTRL
Address: 21 (15h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7	I2C_SLV4_EN	1 – Enable data transfer with this slave at the sample rate. If read command, store data in I2C_SLV4_DI register, if write command, write data stored in I2C_SLV4_DO register. Bit is cleared when a single transfer is complete. Be sure to write I2C_SLV4_DO first 0 – Function is disabled for this slave.
6	I2C_SLV4_INT_EN	1 – Enables the completion of the I^2C slave 4 data transfer to cause an interrupt. 0 – Completion of the I^2C slave 4 data transfer will not cause an interrupt.
5	I2C_SLV4_REG_DIS	When set, the transaction does not write a register value, it will only read data, or write data.
4:0	I2C_SLV4_DLY[4:0]	When enabled via the I2C_MST_DELAY_CTRL, those slaves will only be enabled every1/(1+I2C_SLV4_DLY) samples as determined by I2C_MST_ODR_CONFIG

8.4.23 I2C_SLV4_DO

Name: I2C_SLV4_DO
Address: 22 (16h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	I2C_SLV4_DO[7:0]	Data out when slave 4 is set to write.

8.4.24 I2C_SLV4_DI

Name: I2C_SLV4_DI
Address: 23 (17h)
Type: USR3
Bank: 3
Serial IF: R
Reset Value: 0x00

BIT	NAME	FUNCTION
7:0	I2C_SLV4_DI[7:0]	Data read from I^2C Slave 4.

8.4.25 REG_BANK_SEL

Name: REG_BANK_SEL
Address: 127 (7Fh)
Type:
Bank: 3
Serial IF: R/W
Reset Value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved.
5:4	USER_BANK[1:0]	Use the following values in this bit-field to select a USER BANK: 0 - Select USER BANK 0 1 - Select USER BANK 1 2 - Select USER BANK 2 3 - Select USER BANK 3
3:0	-	Reserved.