Braidyn Sheffield

Dr. Martins

ENCE 3501

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Lab 1: 5-Bit R-2R Ladder DAC

The objective of this lab is to build a 5 bit R-2R ladder DAC using Electric VLSI. The DAC was constructed with 10kΩ n-well resistors. This lab was broken into four parts: building the R-2R voltage divider, simulating the voltage divider, building the DAC, and simulating the DAC. For both building parts of the lab, the schematic was designed, an icon was created, and the layout was designed for that specific part of the lab. This lab provided a foundation in learning how the Electric VLSI software worked as well as an overview of how to use LT Spice for simulating the circuits.

For the first part, the lab, the voltage divider was designed using a schematic, icon, and layout. In Figure 1 below, the schematic can be found for the voltage divider. In the figure, three 10kΩ n-well resistors were used as well as three exports that will allow us to use this schematic in later parts of the lab. On the right side of the figure the icon that was created can be found.

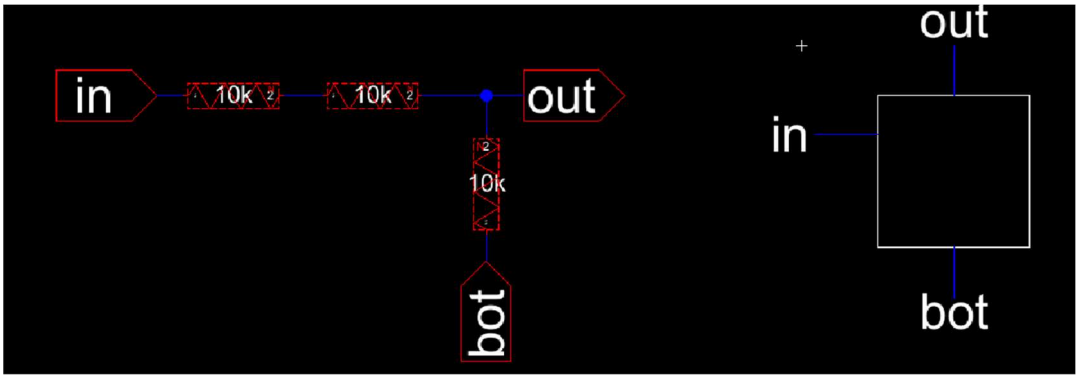

Figure 1: Schematic of Voltage Divider

The layout for the voltage divider was then created using three n-well resistors. To determine the size of each resistor, we used the equation:

$$R = R_{Square} * \frac{L}{W}$$

where the value for R_{Square} is a given value of 855 Ω/Square, the resistance is known as 10kΩ, and a chosen width of 14 was chosen. Using these values, the equation was rewritten and solved for W:

$$L = \frac{W * R}{R_{Square}} = \frac{14 * 10k}{855} = 159.1$$

We can determine the output of the resistance of the DAC by finding the Thevenin resistance. The Thevenin resistance in this case is just 2R//2R or 20kΩ//20kΩ which gives us a output resistance of 10kΩ. Now that the size of the resistor was found, the layout for the voltage divider was built. A photo of the layout can be found in Figure 2 below.

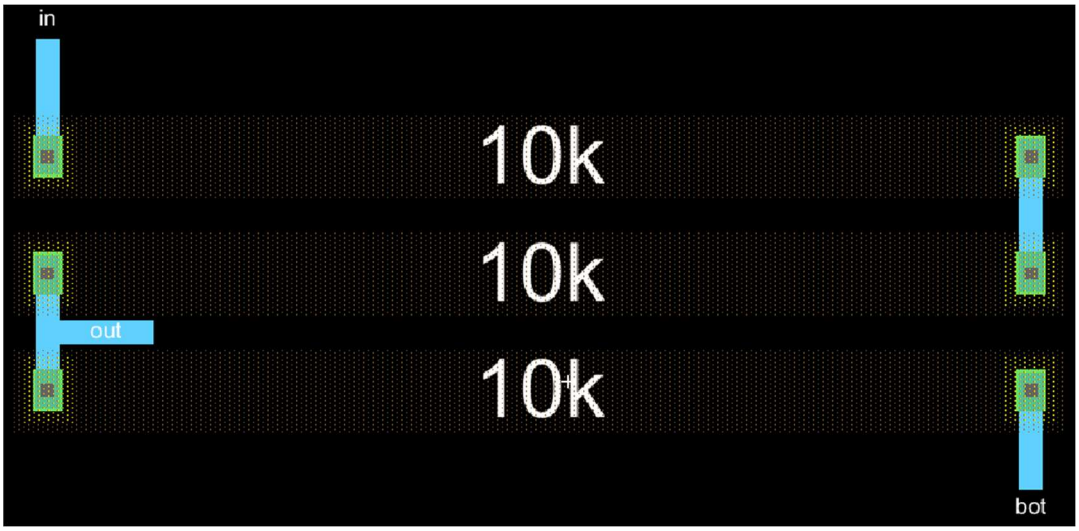

Figure 2: Layout of Voltage Divider

The schematic, icon and layout for the voltage divider were complete, and the designs could be simulated to verify functionality. In Figure 3 below the output of the schematic is shown. A voltage of 1V was applied to the input and the output was read at the "out" export.

```
       --- Operating Point ---

V(vin):         1              voltage
V(vout):        0.333333       voltage
I(vin):         -3.33333e-05   device_current
Ix(xr_divide@0:bot):           -3.33333e-05   subckt_current
Ix(xr_divide@0:in):            3.33333e-05    subckt_current
Ix(xr_divide@0:out):           0              subckt_current
```

Figure 3: Simulation of the Voltage Divider

The voltage was as expected for the schematic of the voltage divider. The next step was to simulate the layout of the voltage divider. The same results were returned as the first simulation of the voltage divider. A 3D rendering of the layout of the voltage divider can be found in Figure 4.

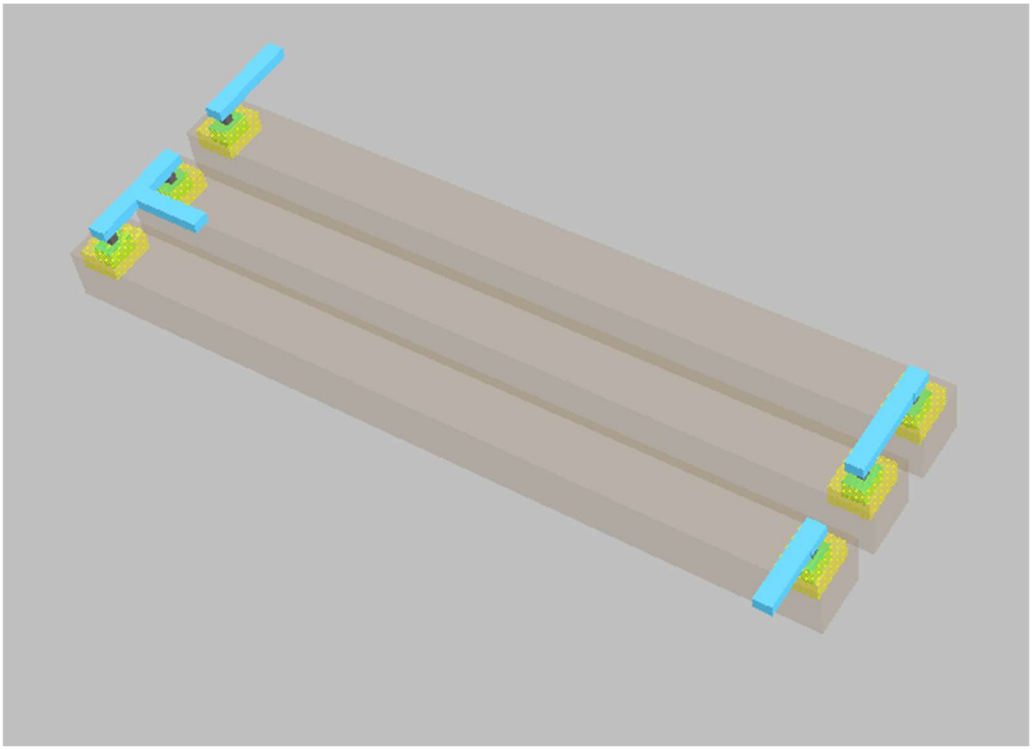

Figure 4: 3D Rendering of the Voltage Divider

The next part of the lab was designing the DAC. This was done by using the icon and schematic of the voltage divider which reduced the workload by allowing us to simply drag the icon onto the workspace and easily multiply the voltage dividers for the DAC. The schematic for the DAC was constructed first and can be found in Figure 5 below.

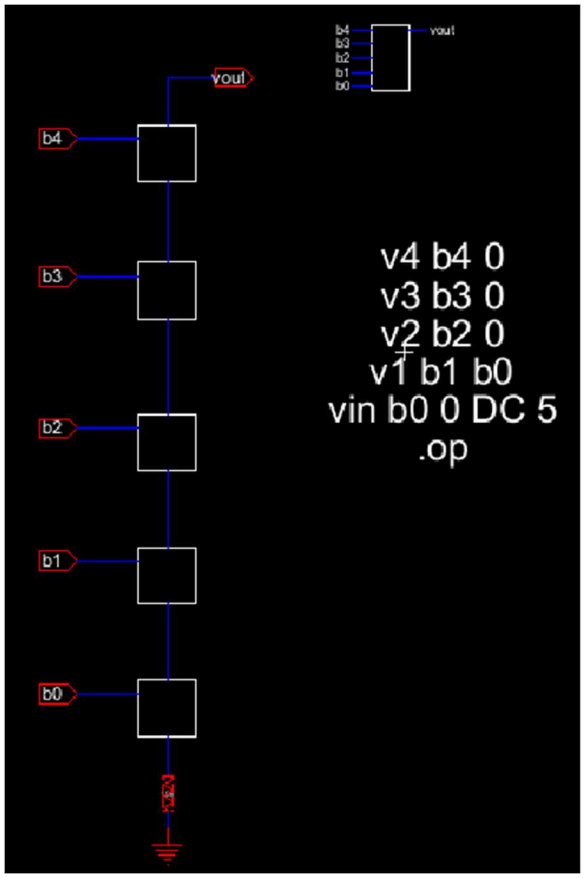

Figure 5: Schematic of the DAC

As seen in Figure 5, each of the white squares is a voltage divider that was designed in an earlier part of the lab. Also in Figure 5, the spice code used to simulate the DAC is on the right side of the figure. The icon that was created for the DAC is in the top right corner of the figure. Once the schematic was finished, the design of the layout was done. The layout of the DAC can be found in Figure 6 below.

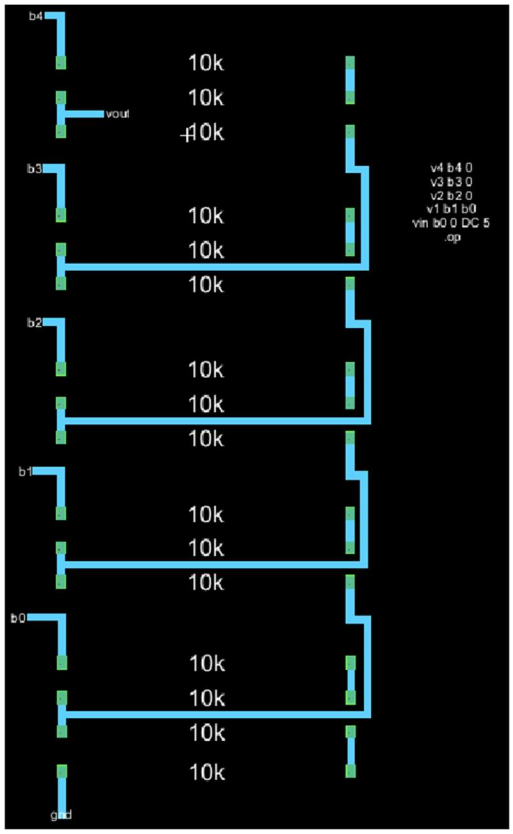

Figure 6: Layout of DAC

The schematic and layout of the DAC were designed and setup inside the software, the next step was to simulate and verify that they were functioning as intended. The simulation results of schematics can be found in Table 1 below. Different inputs to the DAC was used and the expected values were compared to the simulated values.

Table 1: DAC Simulation

DAC Input	Expected Vout (V)	Simulated Vout (V)
B4, B3, B2, B1 grounded with Vin and B0 at 5V	0.15625	0.15625
B4, B3, B2 grounded with Vin, B1 and B0 at 5V	0.46875	0.46875
B4, B3 grounded with Vin, B2, B1 and B0 at 5V	1.09375	1.09375
B4 grounded with Vin, B3, B2, B1 and B0 at 5V	2.34375	2.34375
All inputs and Vin at 5V	4.84375	4.84375

As expected, our hand calculations matched the simulated values for the DAC. The next step was to simulate a transient of the DAC by connecting a 10pF capacitor to the output. The hand calculation of the delay of the DAC was found by:

$$\tau = 0.7 * 10k\Omega * 10pF = 70ns$$

The schematic was the simulated to calculate the simulated delay. The output of the circuit and the delay can be found in Figure 7 below.

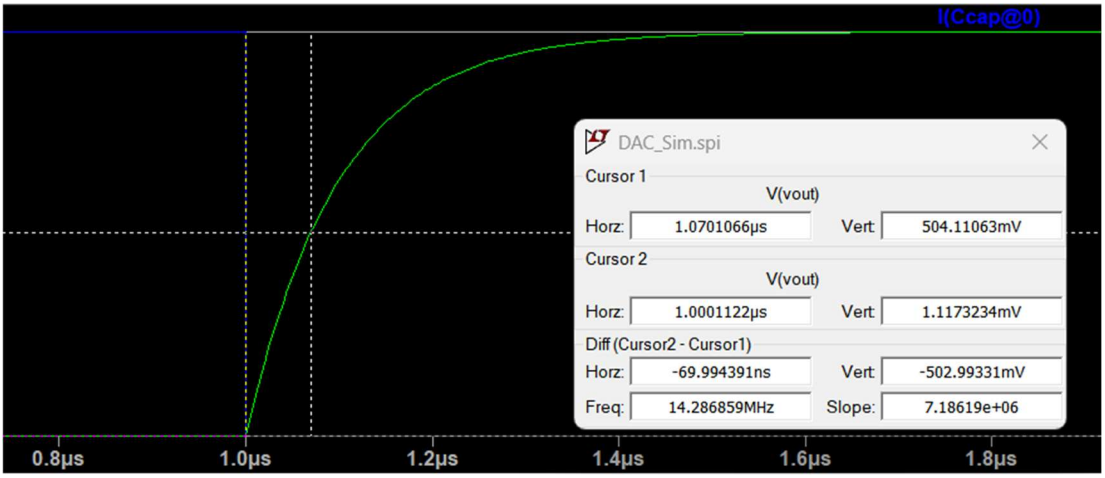

Figure 7: Transient Simulation of DAC

The delay was very close to the hand calculated value that we calculated. The next simulation that was done was connecting a 10kΩ load to the DAC. The simulation can be found in Figure 8 below.

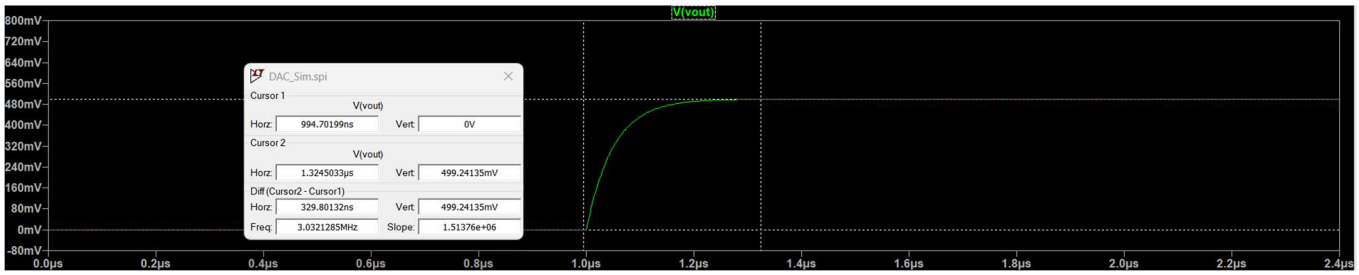

Figure 8: Transient Simulation of DAC with 10k Load

When the DAC drives a 10kΩ resistor, the delay increases to around 330 ns. Finally, a 3D rendering of the layout of the DAC can be found in Figure 9 below.

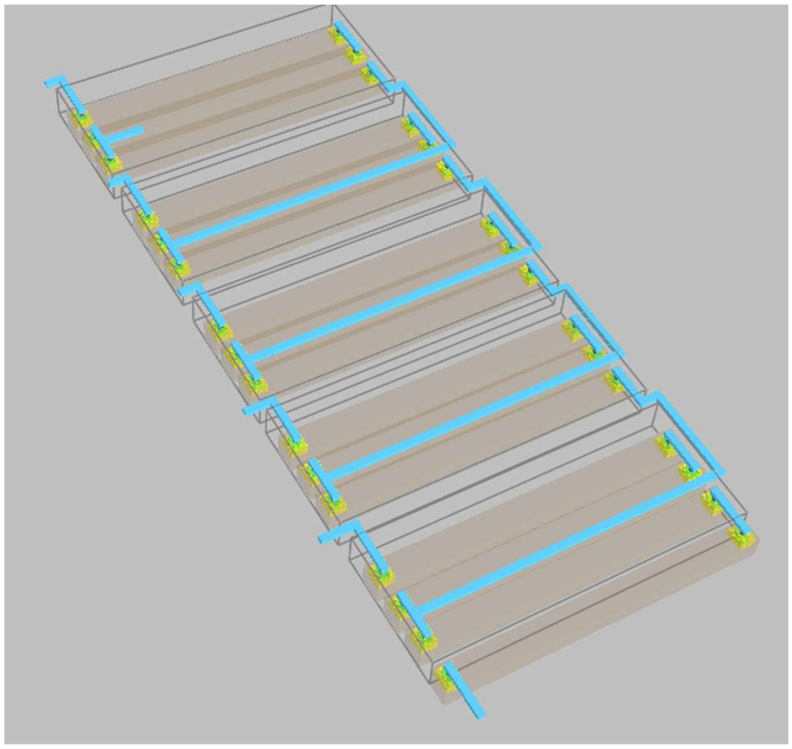

Figure 9: 3D Rendering of DAC

The final step of the lab is to verify that the DRC shows no errors for the DAC. A screenshot of the DRC results can be found in Figure 10 below.

```
================================15================================
Checking schematic cell 'R_Divider{sch}'
   No errors found
Checking schematic cell 'DAC{sch}'
   No errors found
Checking icon cell 'DAC{ic}'
   No errors found
Checking icon cell 'R_Divider{ic}'
   No errors found
0 errors and 0 warnings found (took 0.005 secs)
```

Figure 10: DRC Results

This lab gave a introductory foundation to using the Electric VLSI Software, as well as using LT Spice to simulate the created designs inside the software. For this lab, a 5-bit R-2R ladder DAC was successfully designed and verified. During each step of the lab simulations were ran to verify that the step of the lab was completed correctly and the design was functioning as intended. At the end of the lab, the final layout and schematic passed the DRC with no errors.