

4-Bit CMOS Arithmetic Logic Unit (ALU)

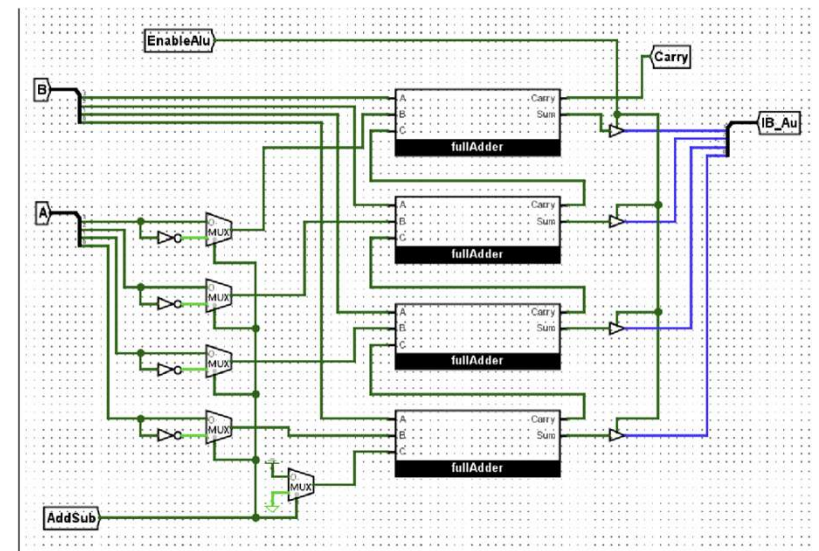
Braidyn Sheffield

Objective

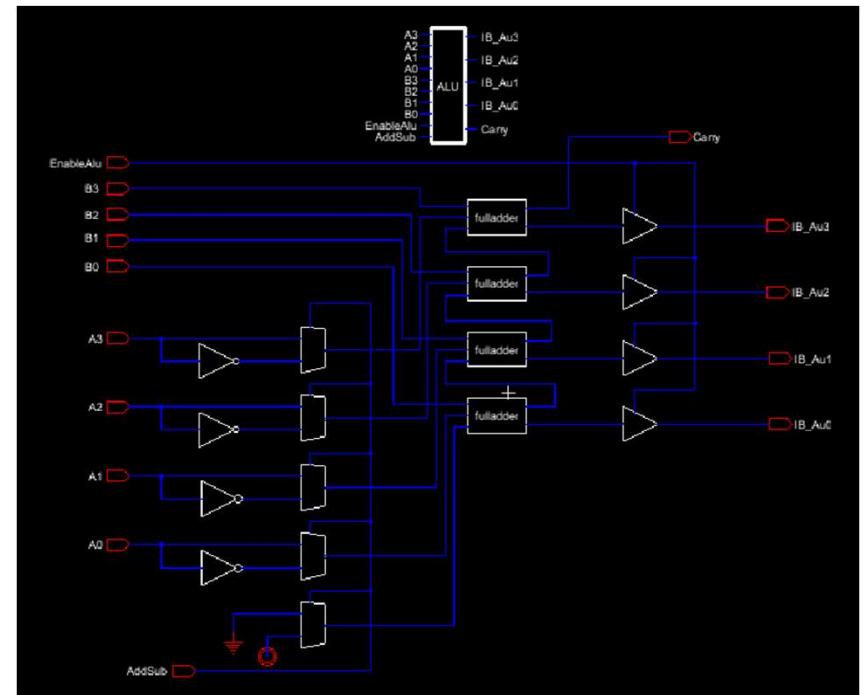
Design and simulate a 4-bit CMOS ALU that performs addition and subtraction using full adder and multiplexer logic.

Where I started

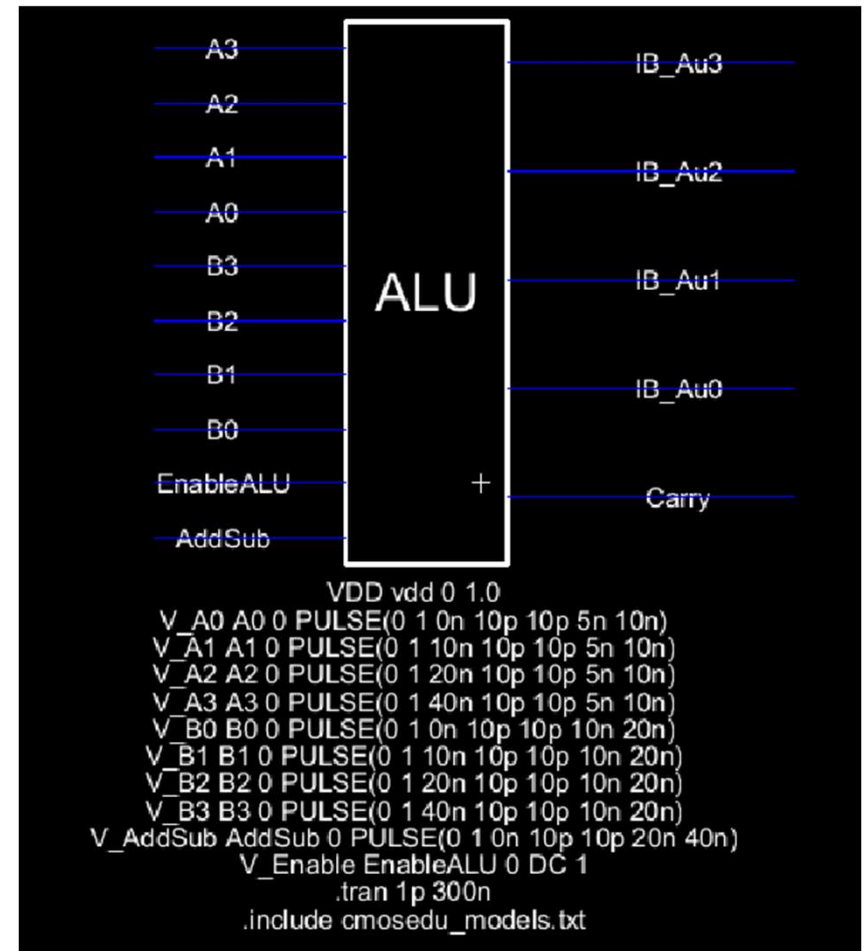
- The Logisim model defined the logical behavior of the ALU.
- It performed $A + B$ or $A - B$ based on the AddSub control.
- Output bits: [IB_Au3:0] and Carry.
- Served as the blueprint for transistor-level schematic design.



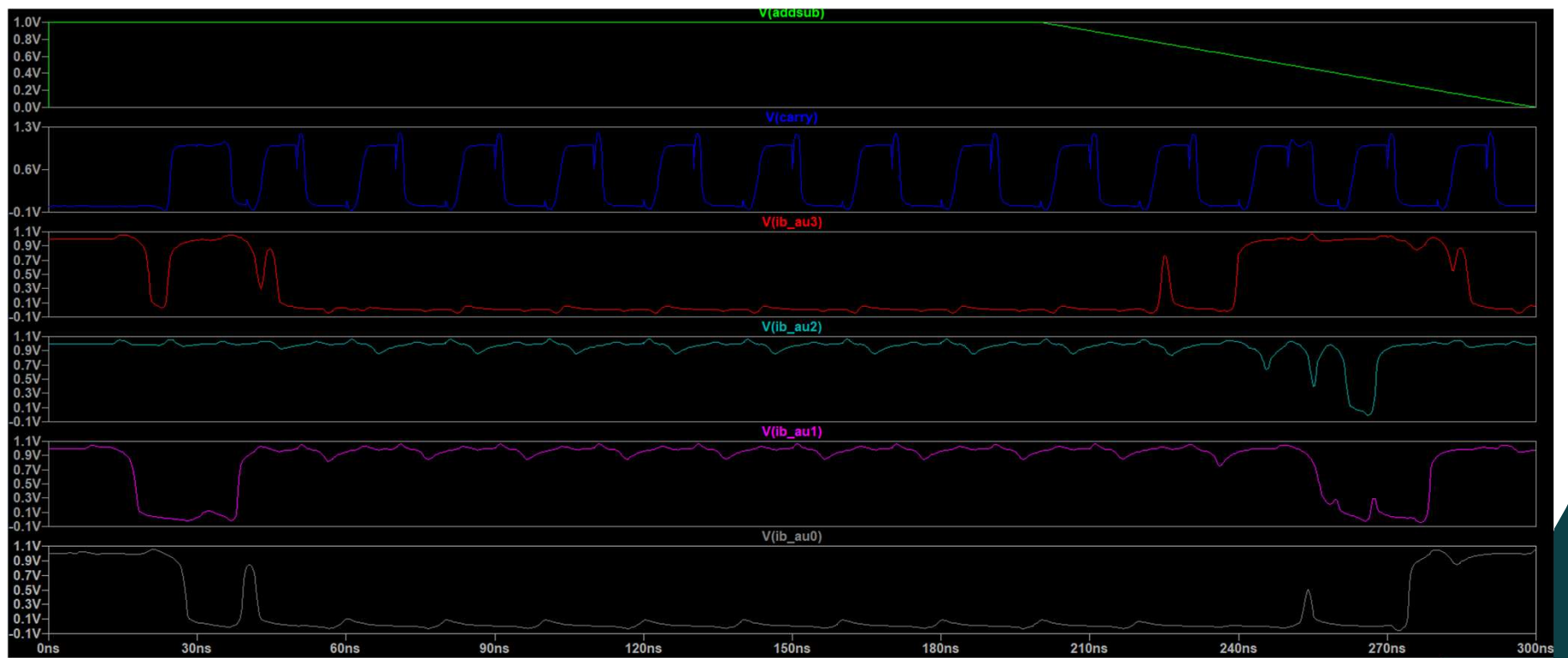
Building the Schematic



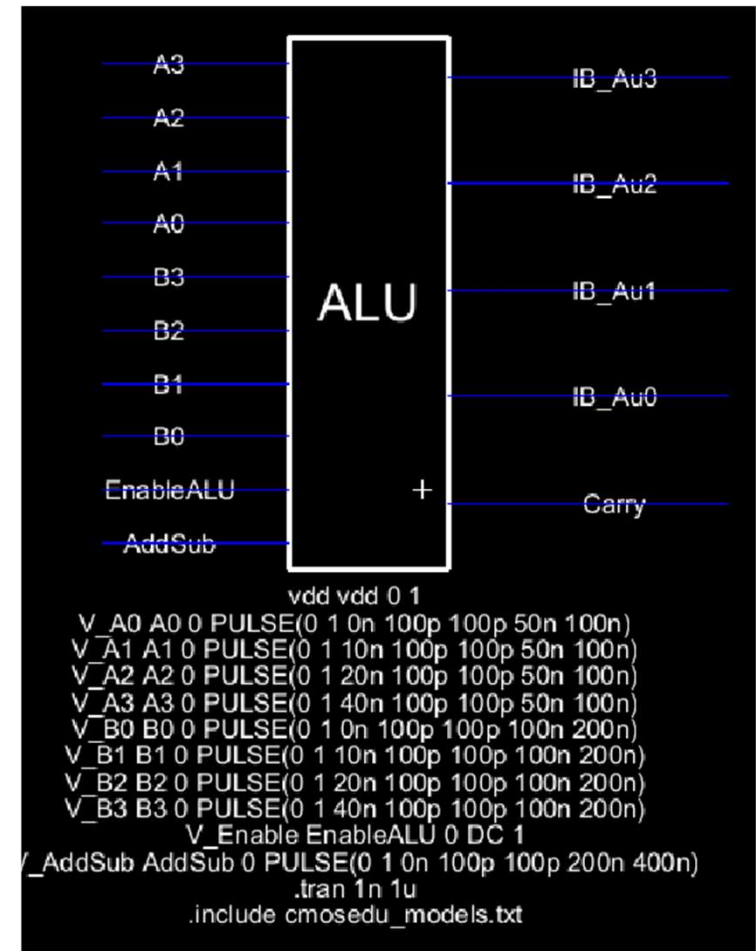
Simulating the Circuit



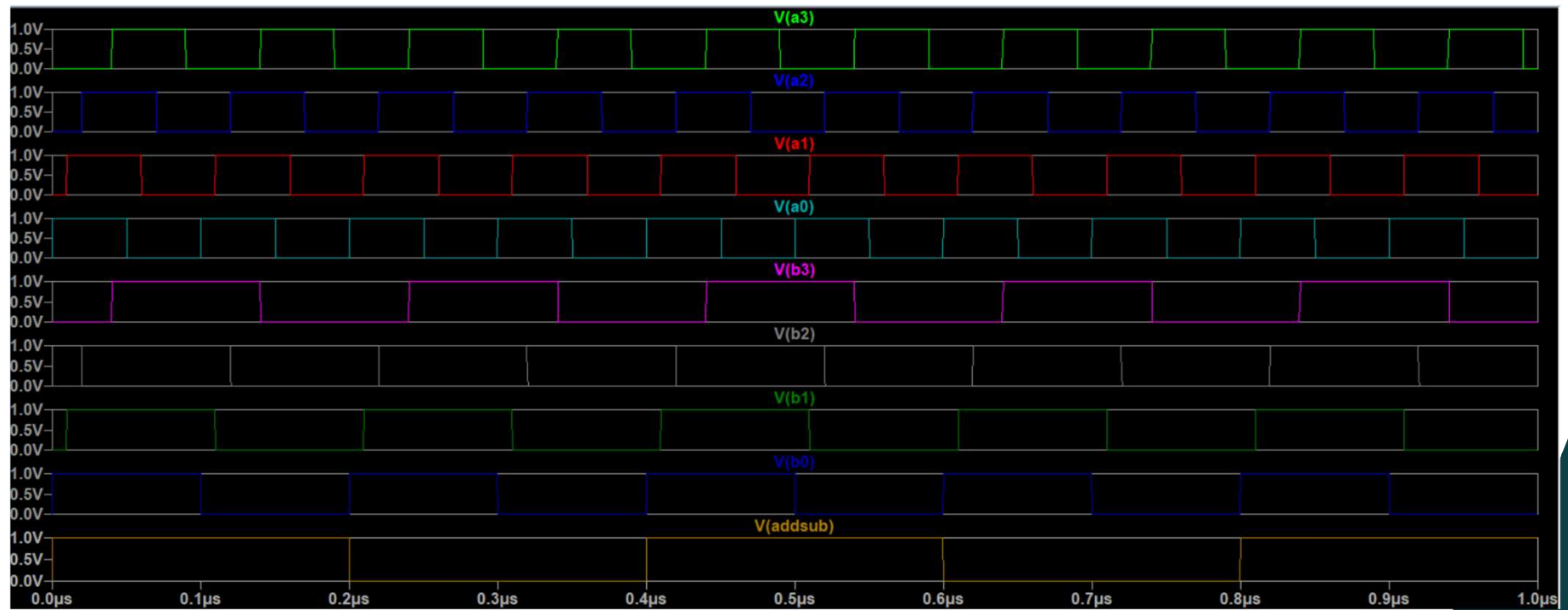
Simulating the Circuit



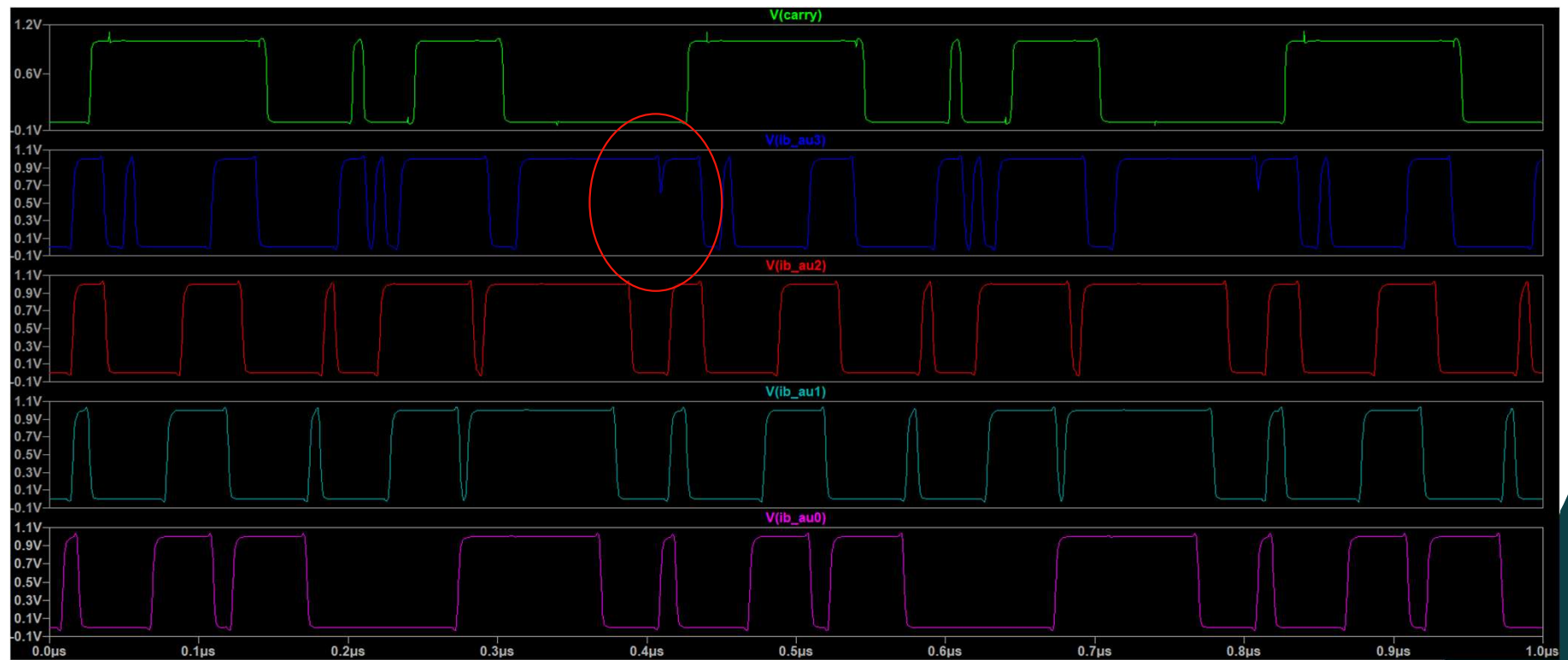
Simulating the Circuit



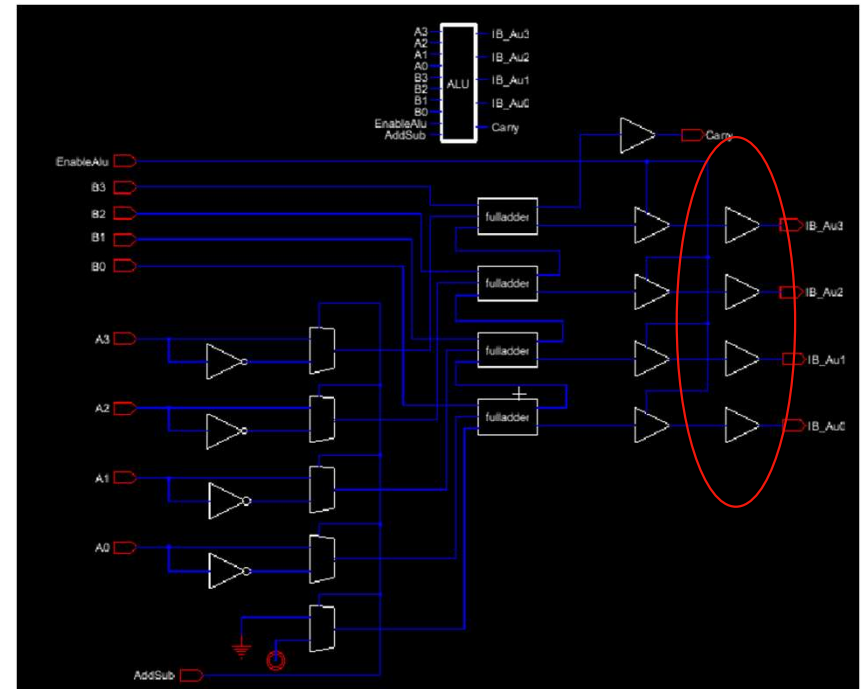
Simulating the Circuit



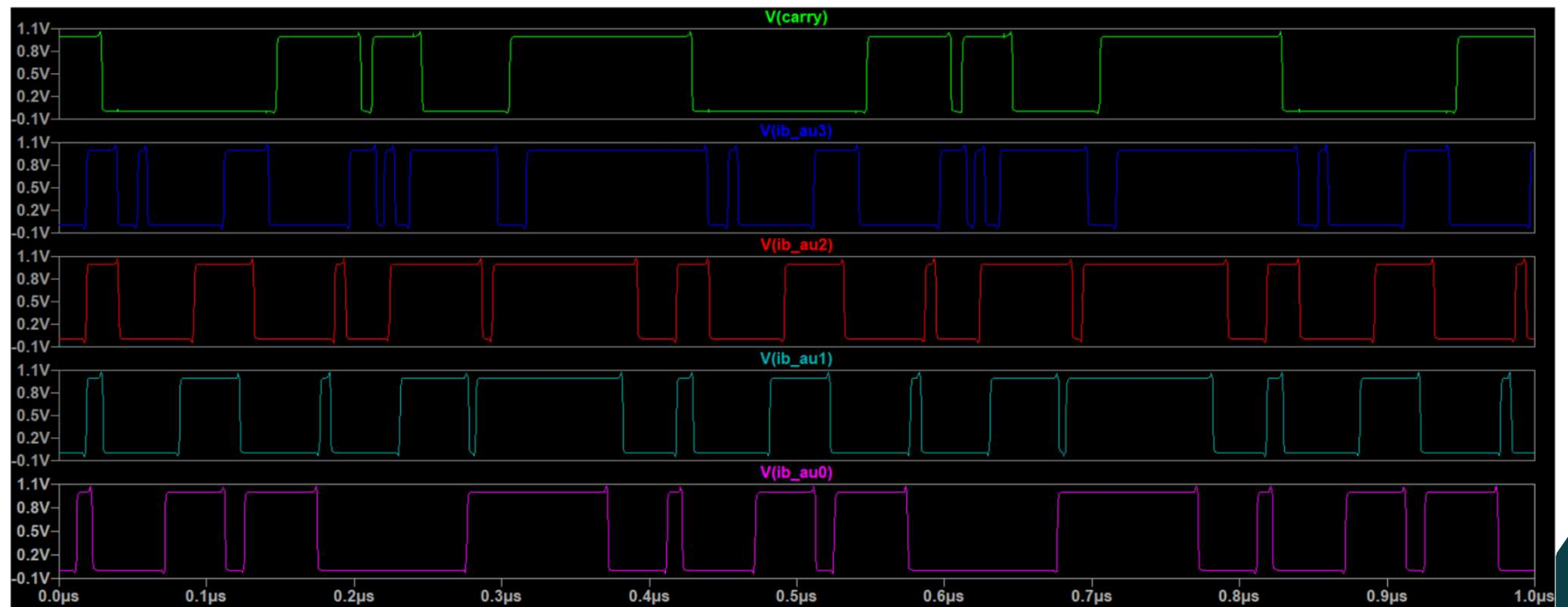
Simulating the Circuit



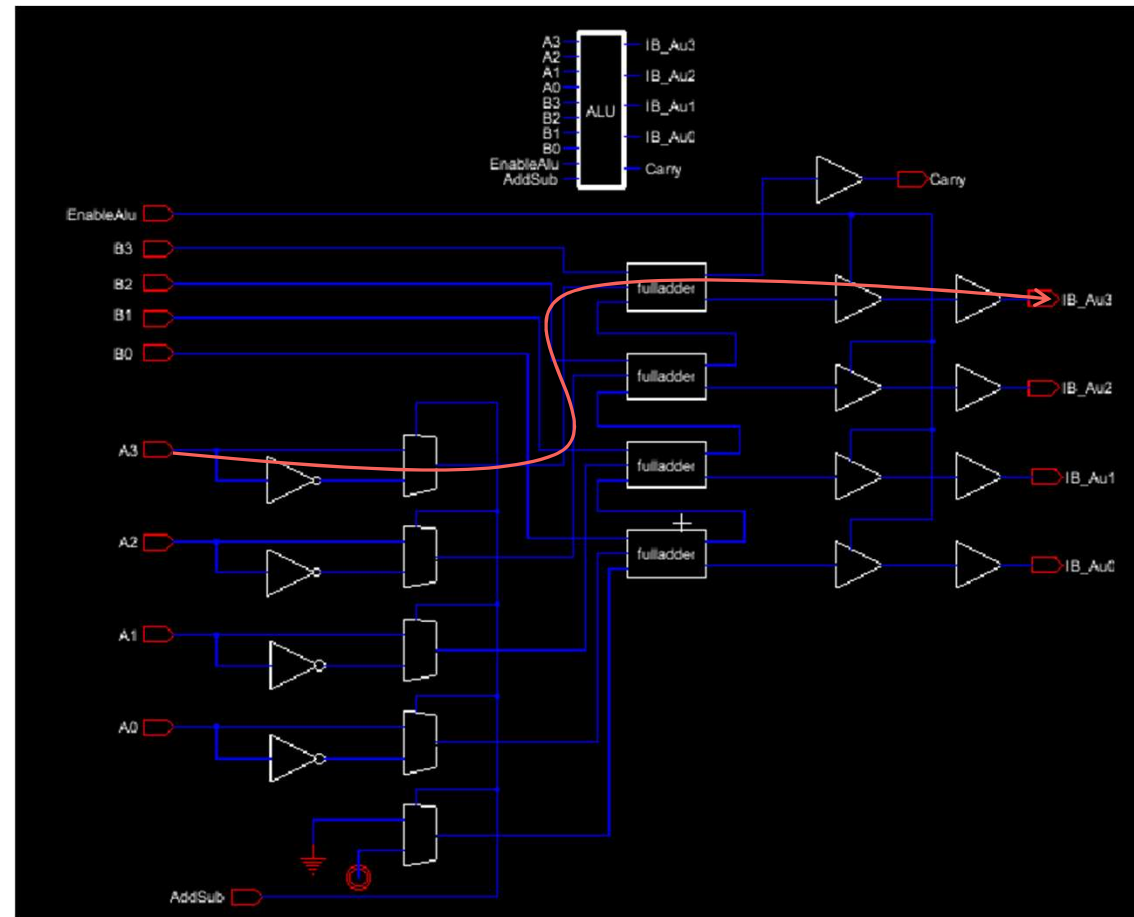
Adjusting the Schematic



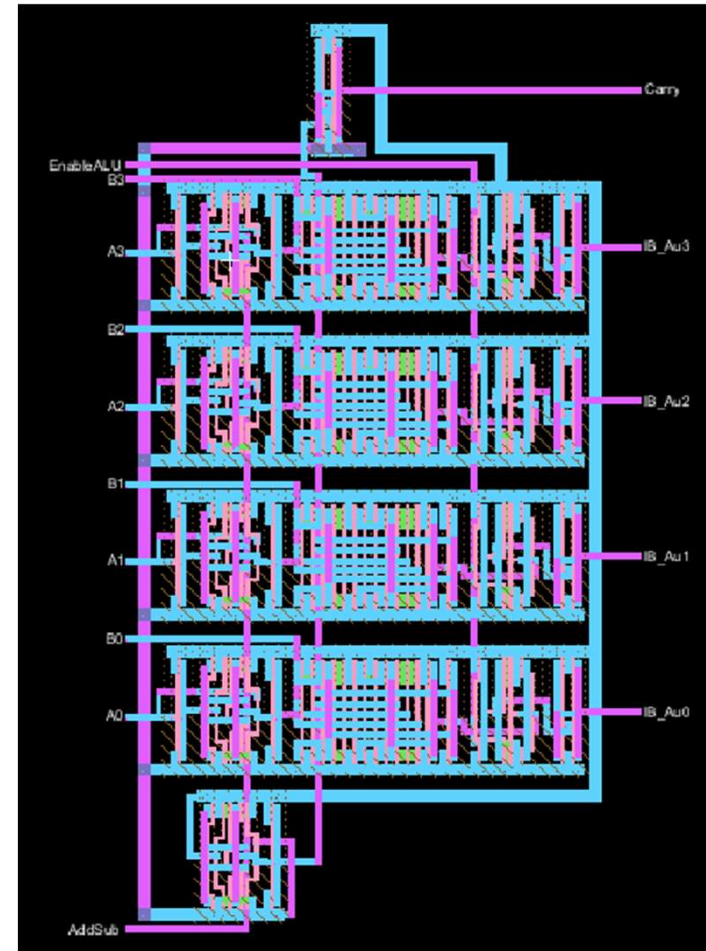
Simulating the Circuit



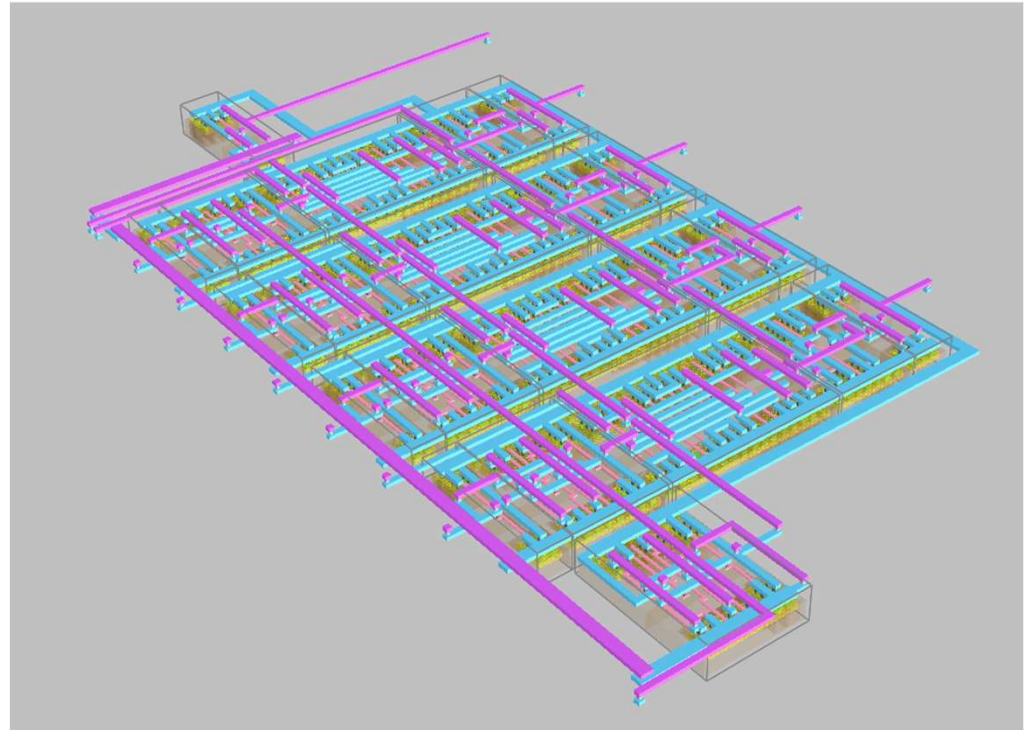
Building the Layout



Building the Layout



3D View of Layout



The background is a solid teal color. It features two large, overlapping circles of a slightly darker shade of teal. One circle is positioned on the left side, and the other is on the right side, with their edges intersecting in the center.

Thank you