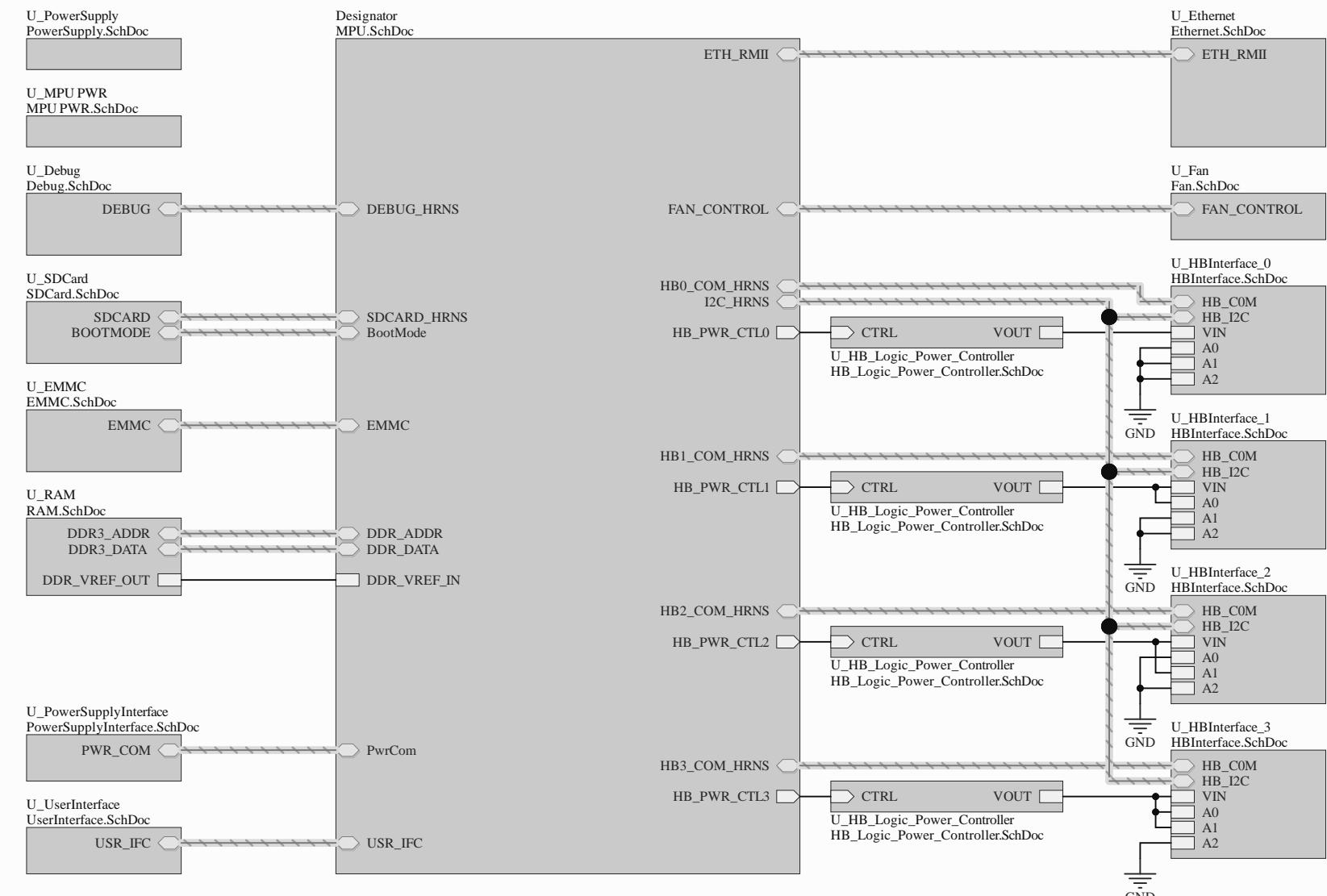


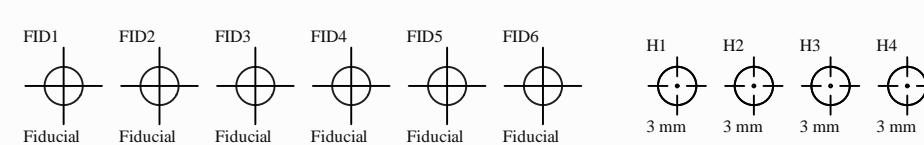
A



B

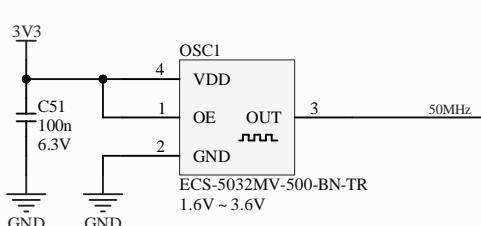
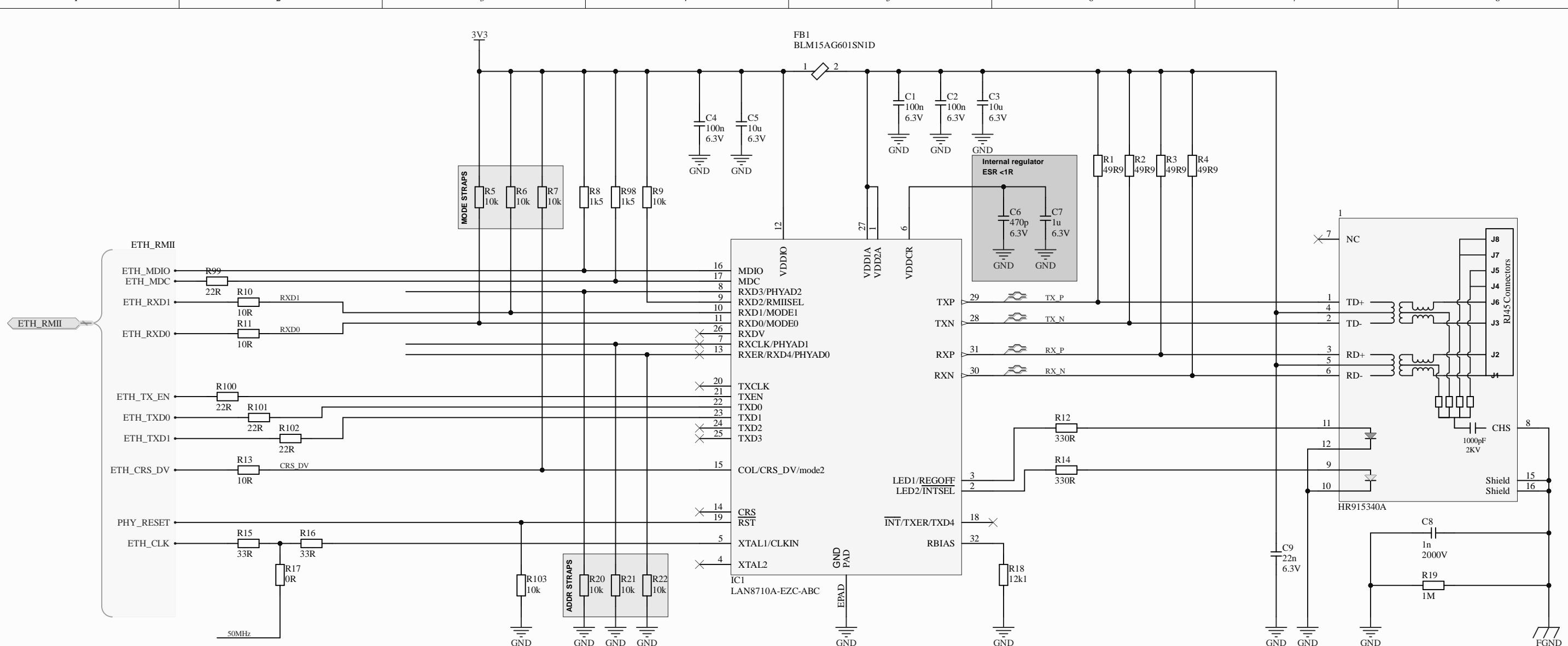
C

D



Project: BRR_CB_P03_REV_A1_1-STM32MP157.PjPcb	Revision: A1.1
Page Contents: System.SchDoc	
SCH Designer: JJU	Checked by: ---
PCB Designer: ---	Checked by: ---
Date: 25.3.2025	Sheet: 1 of 14

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△ 50 MHz clock source:
Generated by MAC (STM32MP15C):
R15, R16 - 0R
R17 - DNP
R116 - 0R (MPU.Schdoc)
R75 - DNP (MPU.Schdoc)

Generated by xtal:
R15, R16 - 33R
R17 - 0R
R116 - DNP (MPU.Schdoc)
R75 - 0R (MPU.Schdoc)

STRAPS:
MODE: 111
ADDR: 000

From:	Connects To:	
LAN8710 QFN	RMII MAC Device	Notes
RXD0 (pin 11)	RXD<0>	
RXD1 (pin 10)	RXD<1>	
RXD2 (pin 9)	RXD<2>	Not Used in RMII Mode
RXD3 (pin 8)	RXD<3>	Not Used in RMII Mode
RX DV (pin 26)	RX DV	Not Used in RMII Mode
RX_ER (pin 13)	RX_ER	This signal is optional in RMII Mode
RX_CLK (pin 7)	RX_CLK	Not Used in RMII Mode
TX_ER (pin 18)	TX_ER	Not Used in RMII Mode
TXD0 (pin 22)	TXD<0>	
TXD1 (pin 23)	TXD<1>	
TXD2 (pin 24)	TXD<2>	Not Used in RMII Mode; TXD2 Should be grounded
TXD3 (pin 25)	TXD<3>	Not Used in RMII Mode; TXD3 Should be grounded
TX_EN (pin 21)	TX_EN	
TX_CLK (pin 20)	TX_CLK	Not Used in RMII Mode
CRS_DV (pin 15)	CRS_DV	
CRS (pin 14)	CRS	Not Used in RMII Mode
COL (pin 15)	COL	
MDIO (pin 16)	MDIO	
MDC (pin 17)	MDC	

Project: BRR_CB_P03_REV_A1_1-STM32MP157.PjtPcb	Revision: A1.1
Page Contents: Ethernet.SchDoc	
SCH Designer: JJU	Checked by: ---
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Date: 25.3.2025	Sheet: 2 of 14

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A

A

B

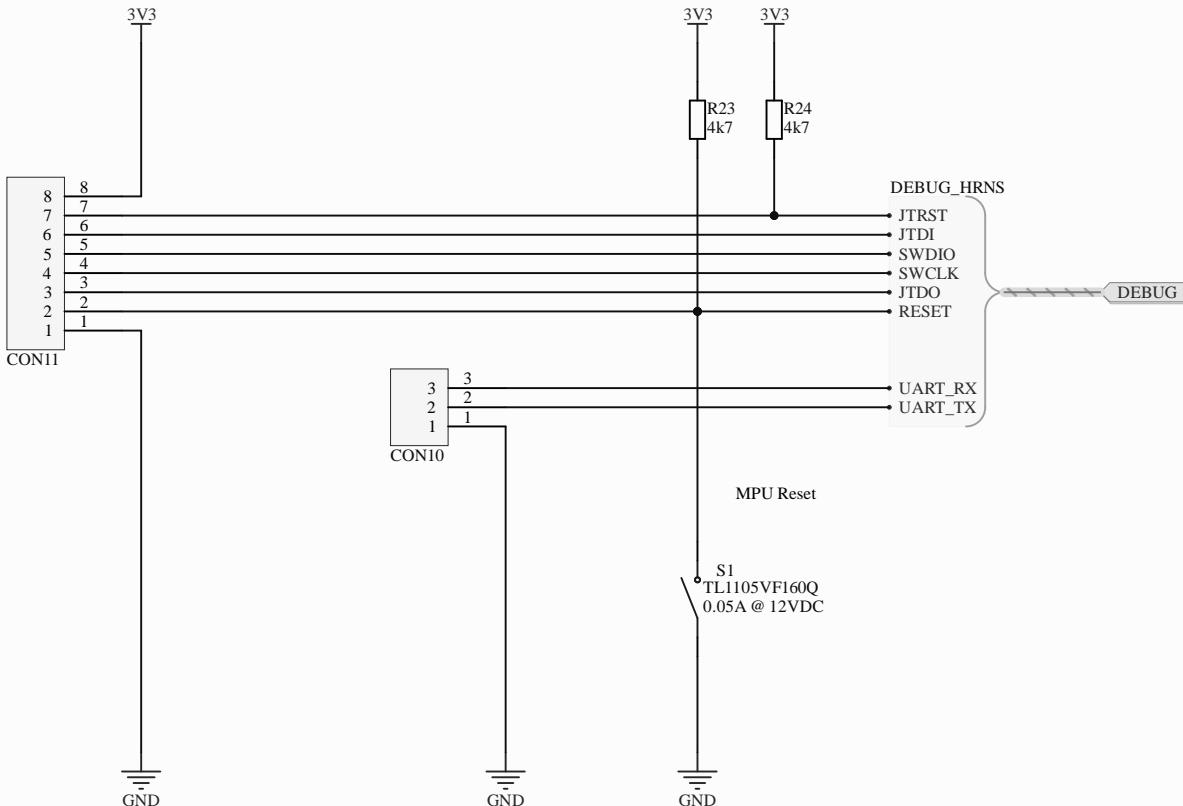
B

C

C

D

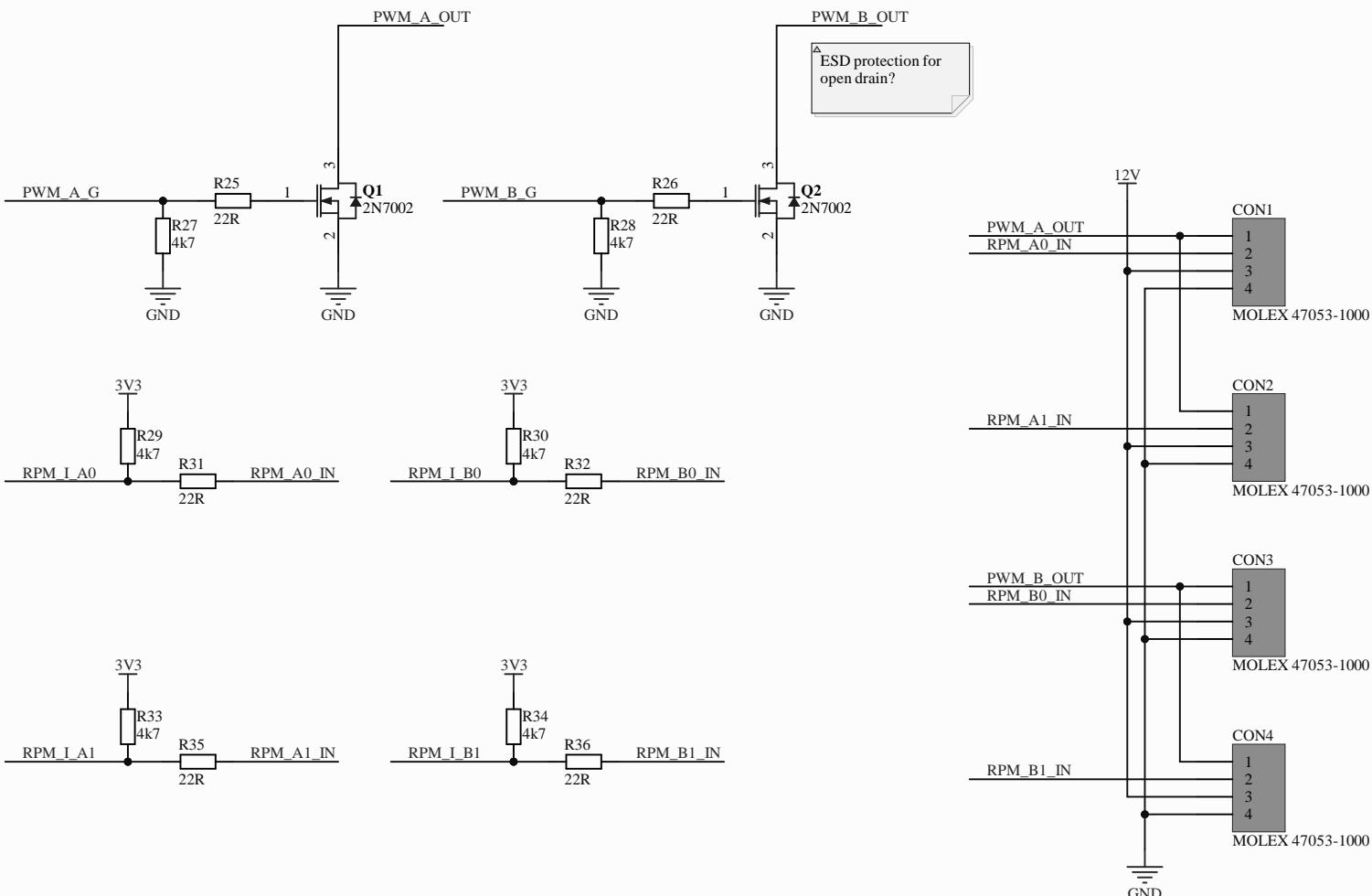
D



Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb	Revision: A1.1
Page Contents: Debug.SchDoc	
SCH Designer: JJU	Checked by: ---
PCB Designer: ---	Checked by: ---
Date: 25.3.2025	Sheet: 3 of 14

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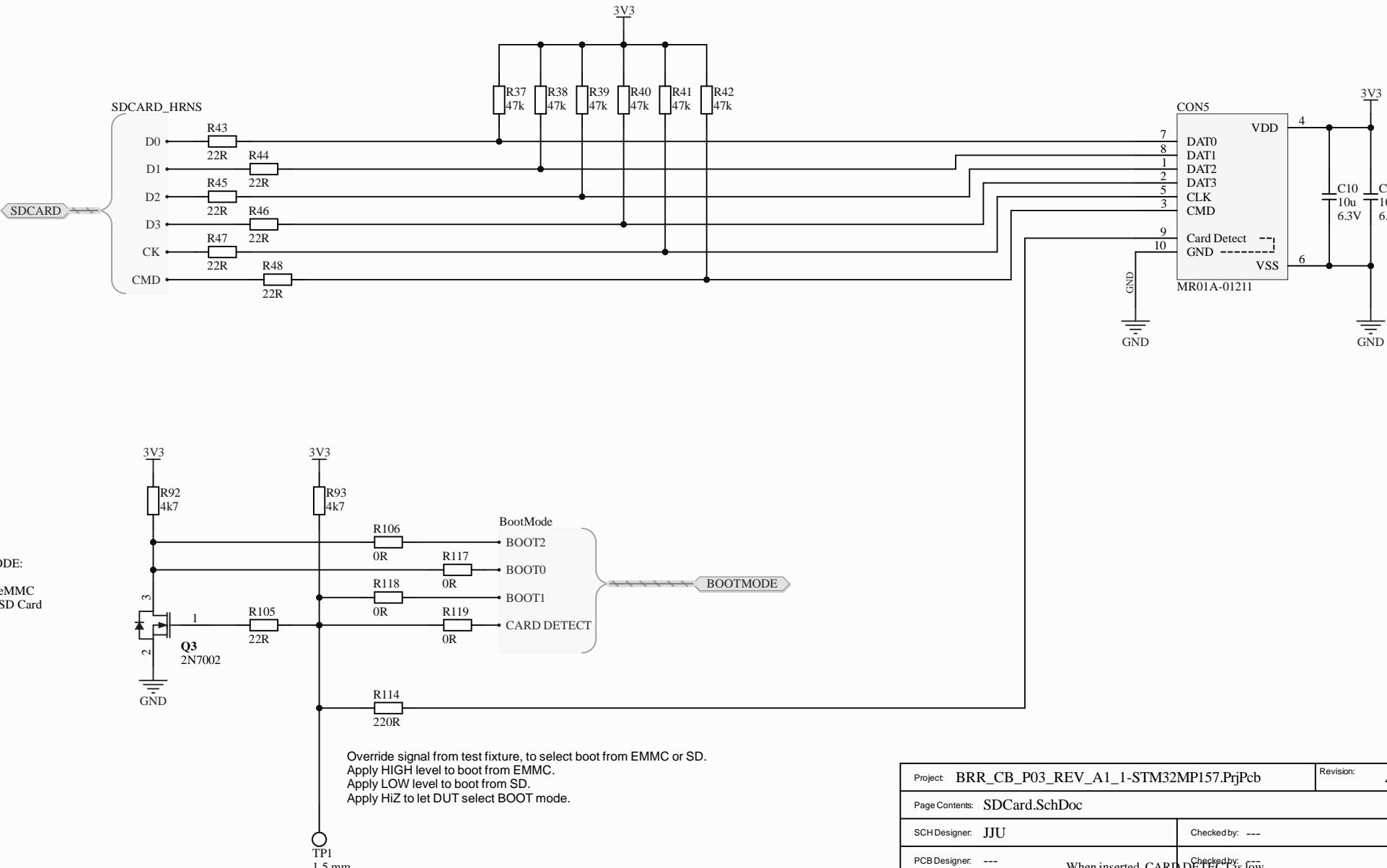
A



B

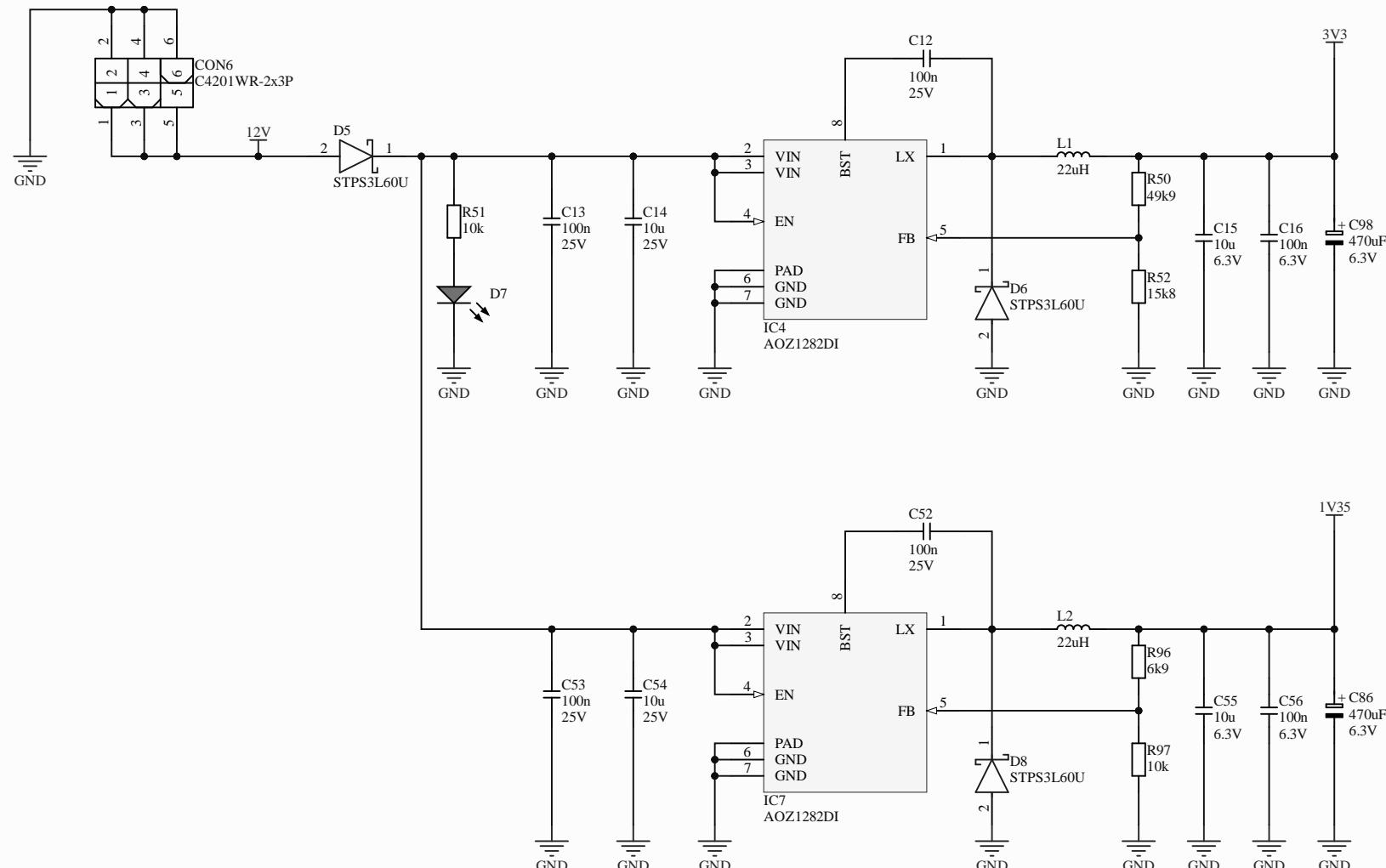
Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb	Revision: A1.1
Page Contents: Fan.SchDoc	
SCH Designer: JJU	Checked by: ---
PCB Designer: ---	Checked by: ---
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Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb	Revision: A1.1
Page Contents: SDCard.SchDoc	
SCH Designer: JJU	Checked by: ---
PCB Designer: ---	When inserted, CARD DETECT is low. otherwise floating.
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Power supply schemes

The circuit is powered by multiple power supplies:

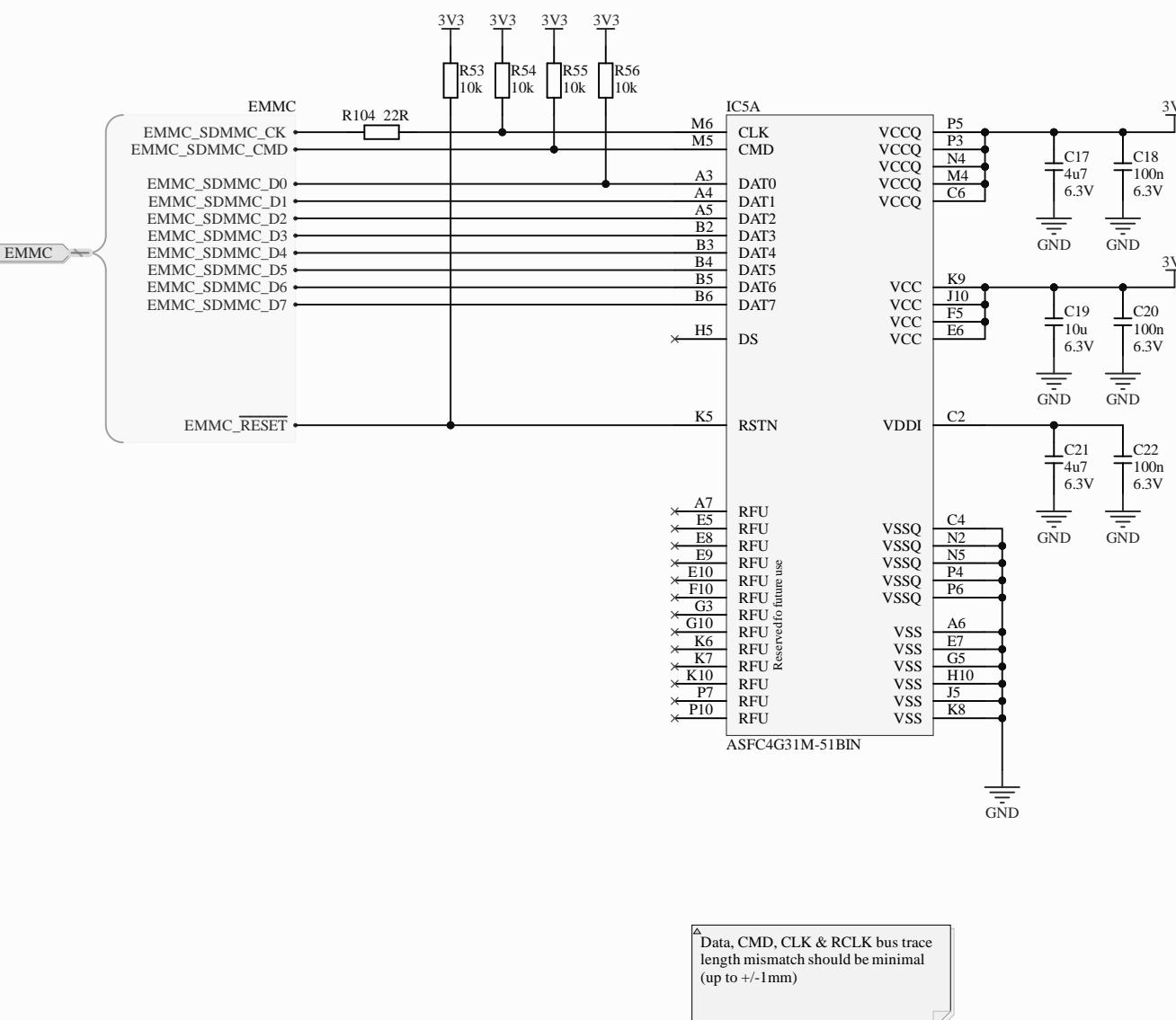
- The **V_{DD}** is the main supply for I/Os and internal part kept powered during the Standby mode. The useful voltage range is 1.71 V to 3.6 V (for example: 1.8 V, 2.5 V, 3.0 V or 3.3 V typical)
 - Those supplies must be connected to external decoupling capacitors (see Table 4).
 - V_{DD_{DSI}}, V_{DD_{PLL}} and V_{DD_{ANA}}** must be connected to **V_{DD}**.
- The **V_{DDCORE}** is the main digital voltage and shutdowns externally during the Standby mode. The voltage range during Run mode is 1.18 V to 1.25/1.38 V (1.2/1.34 V typical).
 - This supply must be connected to external decoupling capacitors (see Table 4).
 - V_{DDCORE}** is reduced further in specific Stop mode (LPLV_Stop). This involves either PWR_ON signal (for example with STPMIC1, external power management IC) or PWR_LP signal (with discrete SMPS components).
- The **V_{BAT}** pin can be connected to the external battery (1.2 V < V_{BAT} < 3.6 V).
 - If RETRAM is used, minimum V_{BAT} is 1.4 V
 - If the application does not support backup battery, it is recommended to connect this pin to **V_{DD}**.
 - If the application supports backup battery, it is recommended to add a 100 nF ceramic decoupling capacitor between V_{BAT} and V_{SS}.
 - If the application uses a supercapacitor on V_{BAT}, no additional decoupling is required.
- The **V_{DDA}** pin is the analog (ADC/DAC/VREFBUF) supply and must be connected to external decoupling capacitors (see Table 4).
- The **V_{REF+}** pin can be connected to the **V_{DDA}** external power supply. If a separate, internal or external, reference voltage is applied on **V_{REF+}**, a decoupling capacitor must be connected between this pin and **V_{REF-}** (see Table 4). Refer to Section 4.1.1. Additional precautions allow to filter analog noise:
 - V_{DDA}** can be connected to **V_{DD}** through an inductor based filter.
- V_{DDQ_DDR}** is the DDR I/O supply and must be connected to external decoupling capacitors (see Table 4).
 - Voltage range is 1.425 V to 1.575 V for interfacing DDR3 memories (1.5 V typical)
 - Voltage range is 1.283 V to 1.45 V for interfacing DDR3L memories (1.35 V typical)
 - Voltage range is 1.14 V to 1.3 V for interfacing LPDDR2 or LPDDR3 memories (1.2 V typical)

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A

A



Parameter	Symbol	Unit	Value
VDDI	C1 + C2	uF	4.7 + 0.1
VCCQ	C3 + C4	uF	4.7 + 0.1
VCC	C5 + C6	uF	10 + 0.1

[△] Recommended types described in datasheet.

▪ Operating Power Supply

- VCC : 2.7V ~ 3.6V (for NAND Flash Memory)
- VCCQ : 1.7V ~ 1.95V or 2.7V ~ 3.6V (for Interface)

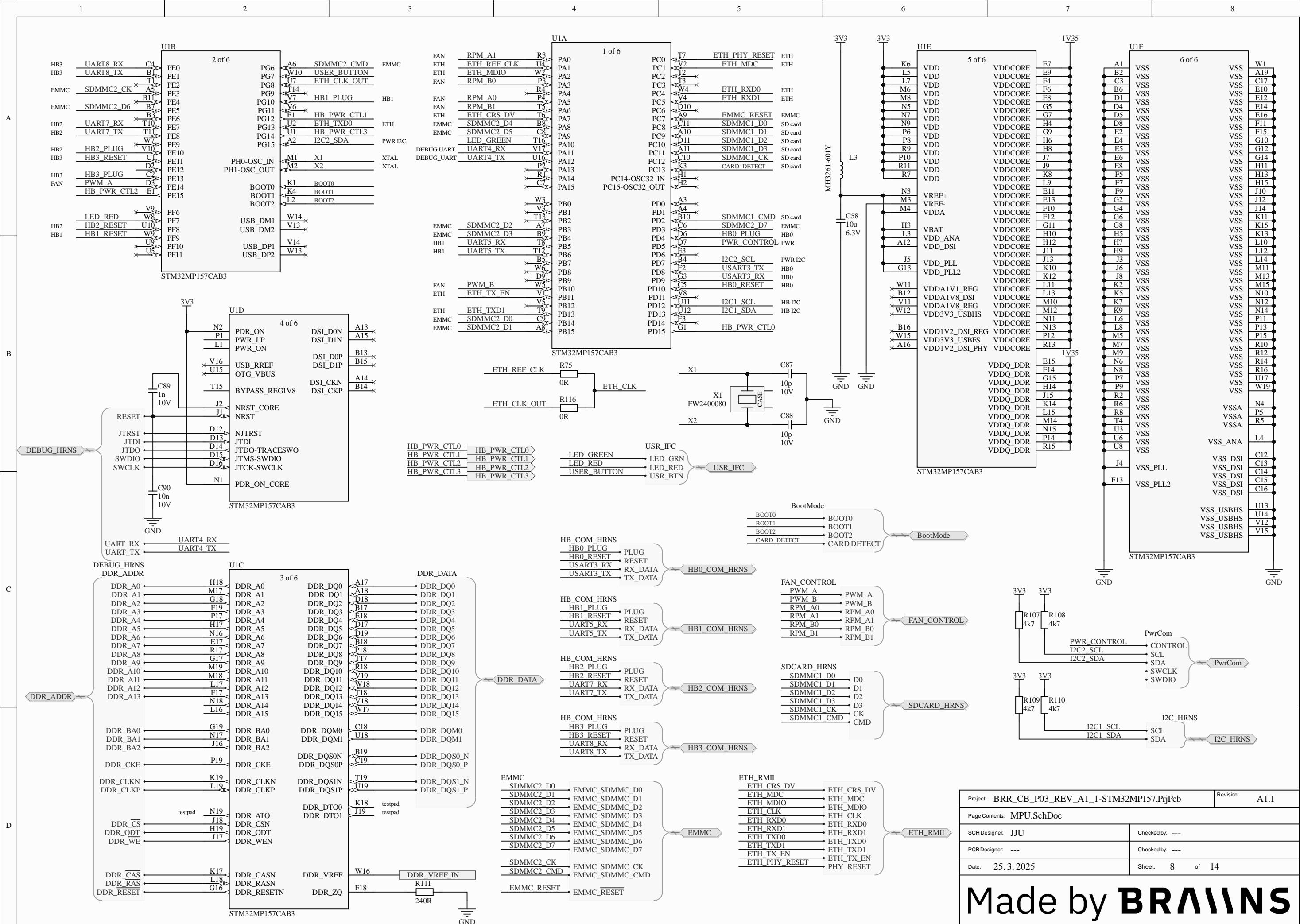
IC5B	
x A1	NC H1
x A2	NC H2
x A8	NC H3
x A9	NC H12
x A10	NC H13
x A11	NC H14
x A12	NC J1
x A13	NC J2
x A14	NC J3
x B1	NC J12
x B7	NC J13
x B8	NC J14
x B9	NC K1
x B10	NC K2
x B11	NC K3
x B12	NC K12
x B13	NC K13
x B14	NC K14
x C1	NC L1
x C3	NC L2
x C5	NC L3
x C7	NC L12
x C8	NC L13
x C9	NC L14
x C10	NC M1
x C11	NC M2
x C12	NC M3
x C13	NC M7
x C14	NC M8
x D1	NC M9
x D2	NC M10
x D3	NC M11
x D4	NC M12
x D12	NC M13
x D13	NC M14
x D14	NC N1
x E1	NC N3
x E2	NC N6
x E3	NC N7
x E12	NC N8
x E13	NC N9
x E14	NC N10
x F1	NC N11
x F2	NC N12
x F3	NC N13
x F12	NC N14
x F13	NC P1
x F14	NC P2
x G1	NC P8
x G2	NC P9
x G12	NC P11
x G13	NC P12
x G14	NC P13
	NC P14

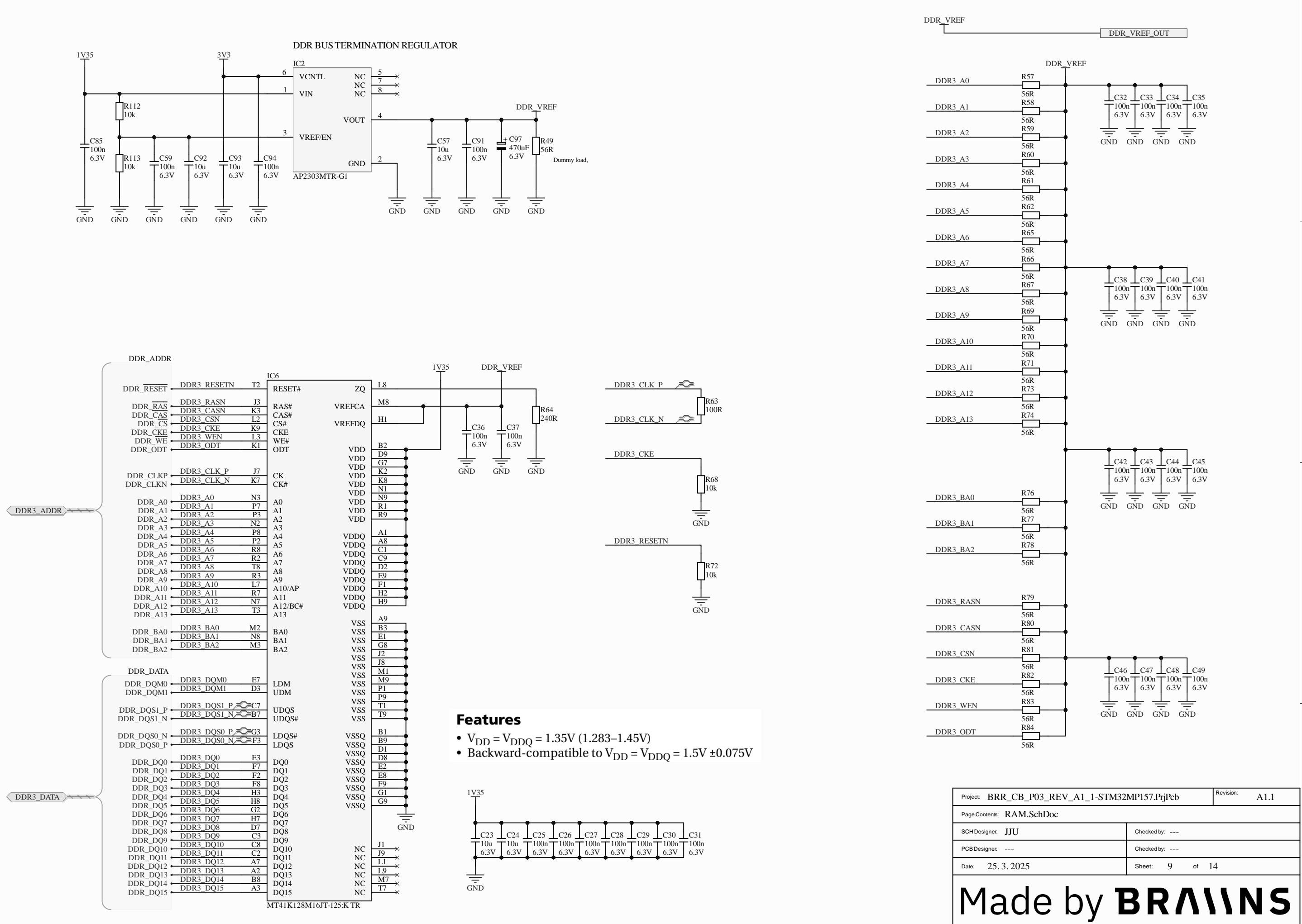
ASFC4G31M-51BIN

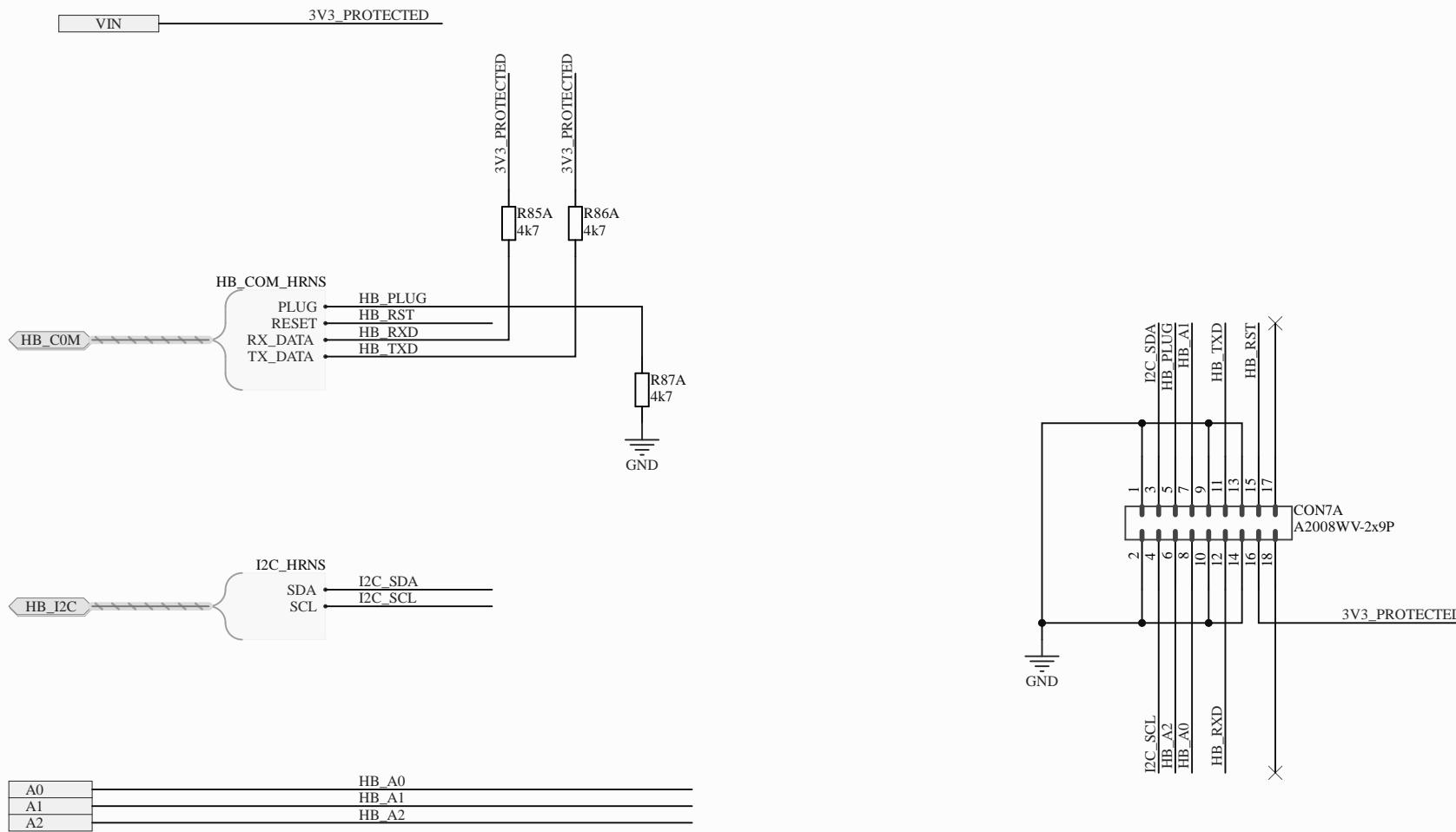
Project: BRR_CB_P03_REV_A1_1-STM32MP157.PjPcb	Revision: A1.1
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SCH Designer: JJU	Checked by: ---
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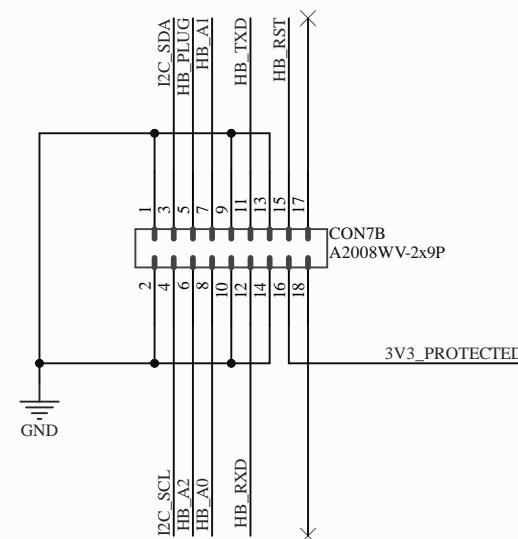
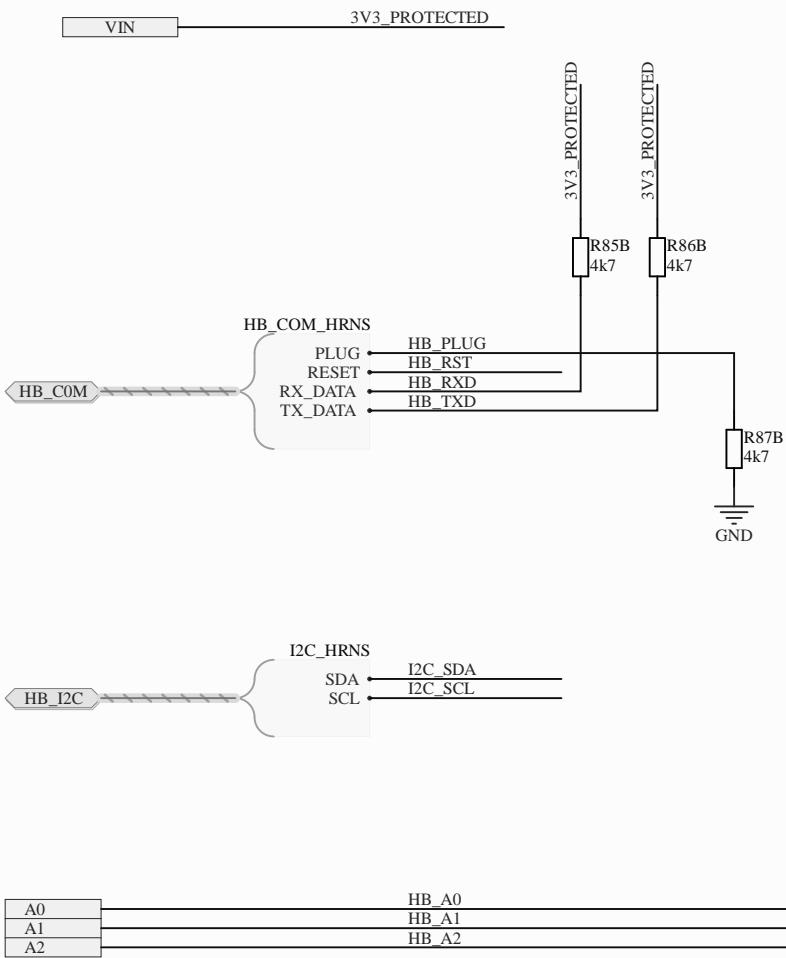






Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb		Revision: A1.1
Page Contents: HBInterface.SchDoc		
SCH Designer: JJU	Checked by:	---
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Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb

Revision: A1.1

Page Contents: HBInterface.SchDoc

SCH Designer: JJU

Checked by: ---

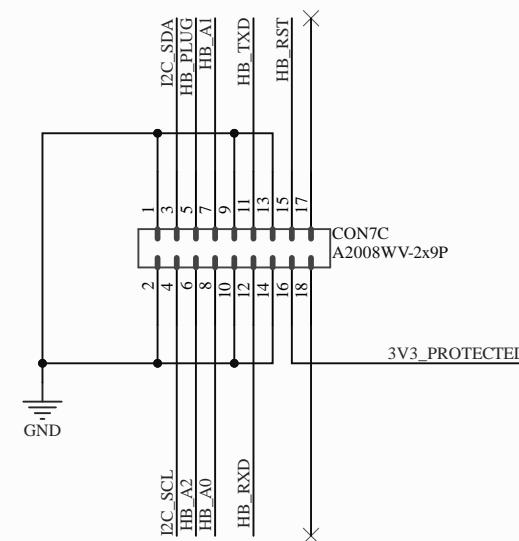
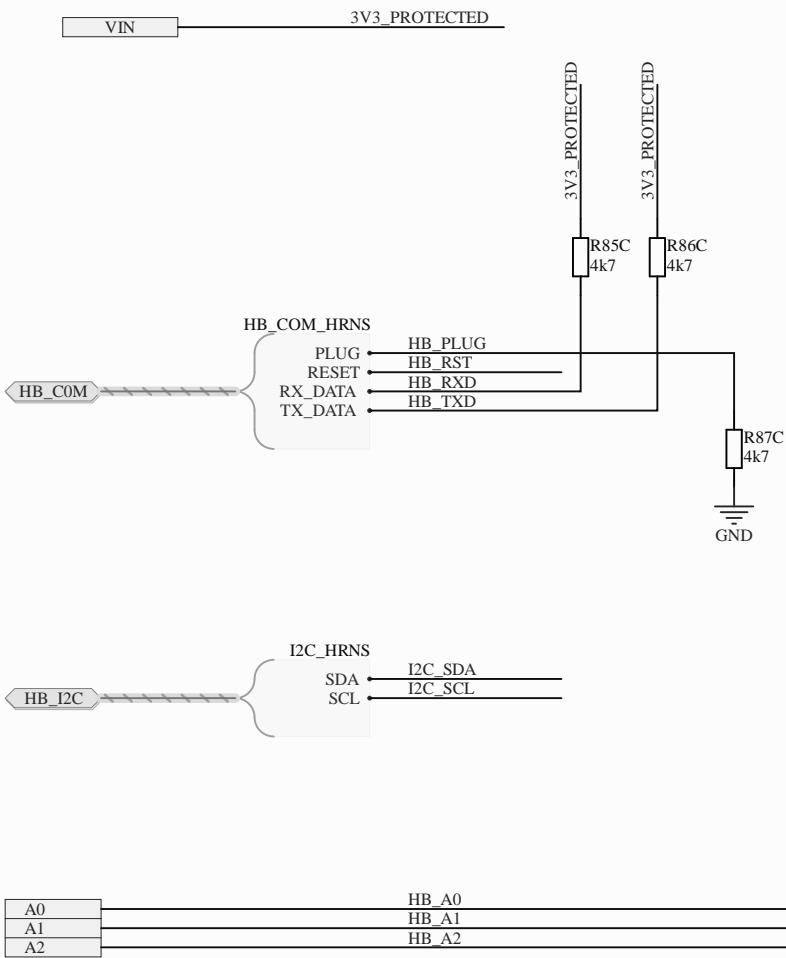
PCB Designer: ---

Checked by: ---

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Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb

Revision: A1.1

Page Contents: HBInterface.SchDoc

SCH Designer: JJU

Checked by: ---

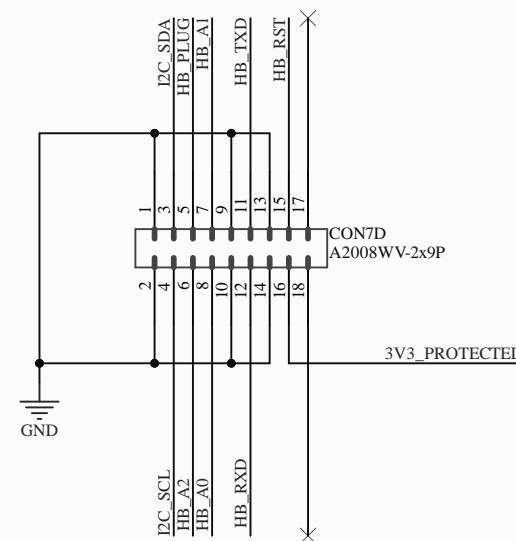
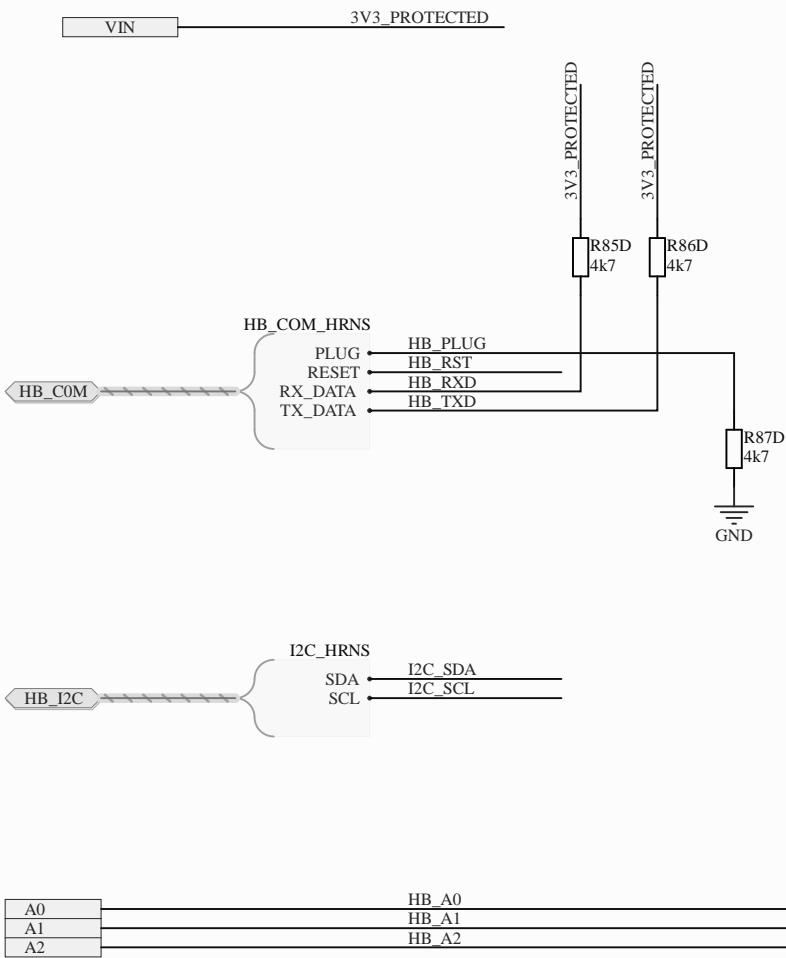
PCB Designer: ---

Checked by: ---

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Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb

Revision: A1.1

Page Contents: HBInterface.SchDoc

SCH Designer: JJU

Checked by: ---

PCB Designer: ---

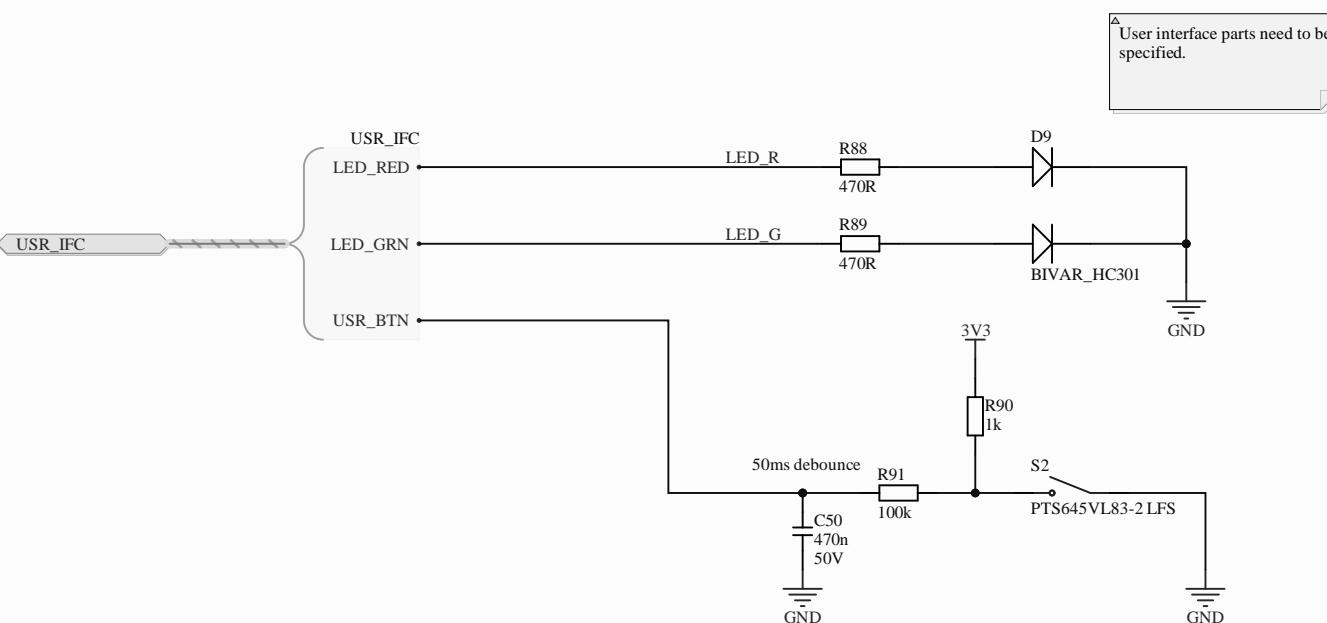
Checked by: ---

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A



Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb	Revision: A1.1
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PCB Designer: ---	Checked by: ---
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A

A

B

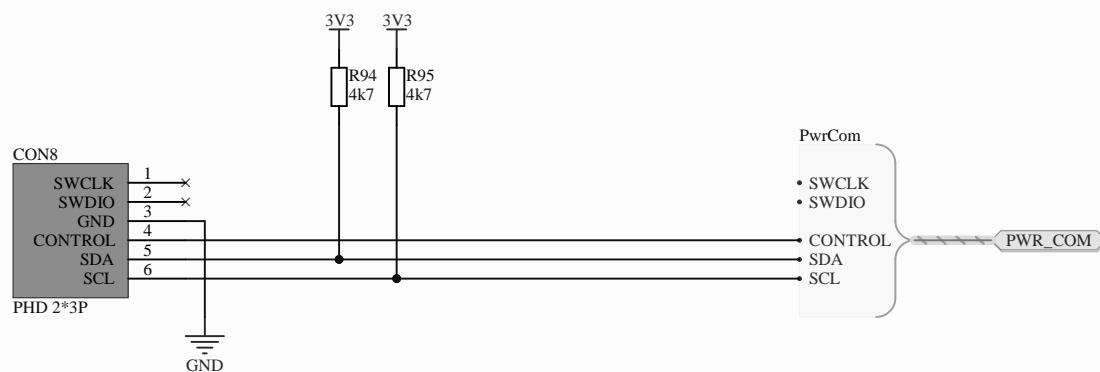
B

C

C

D

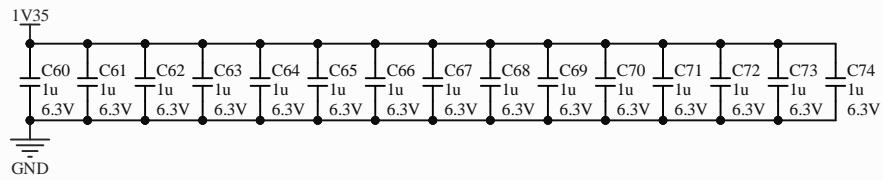
D



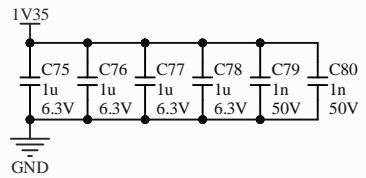
Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb	Revision: A1.1
Page Contents: PowerSupplyInterface.SchDoc	
SCH Designer: JJJ	Checked by: ---
PCB Designer: ---	Checked by: ---
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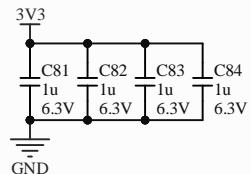
VDDCORE - 15x 1uF



VDDQ_DDR - 2x1nF, 4x 1uF



VDD - 4x 1uF



Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb	Revision: A1.1
Page Contents: MPU PWR.SchDoc	
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A

A

8.4 Device Functional Modes

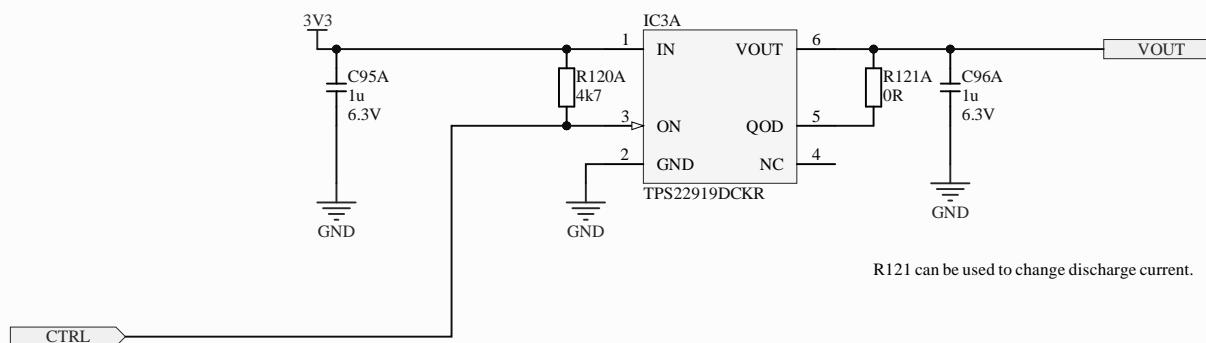
Table 2 describes the connection of the VOUT pin depending on the state of the ON pin as well as the various QOD pin configurations.

Table 2. VOUT Connection

ON	QOD CONFIGURATION	TPS22919 VOUT
L	QOD pin connected to VOUT with R_{QOD}	GND ($R_{PD_QOD} + R_{QOD}$)
L	QOD pin tied to VOUT directly	GND (R_{PD_QOD})
L	QOD pin left open	Floating
H	N/A	VIN

B

B



C

C

Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb	Revision: A1.1
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PCB Designer: ---	Checked by: ---
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A

A

8.4 Device Functional Modes

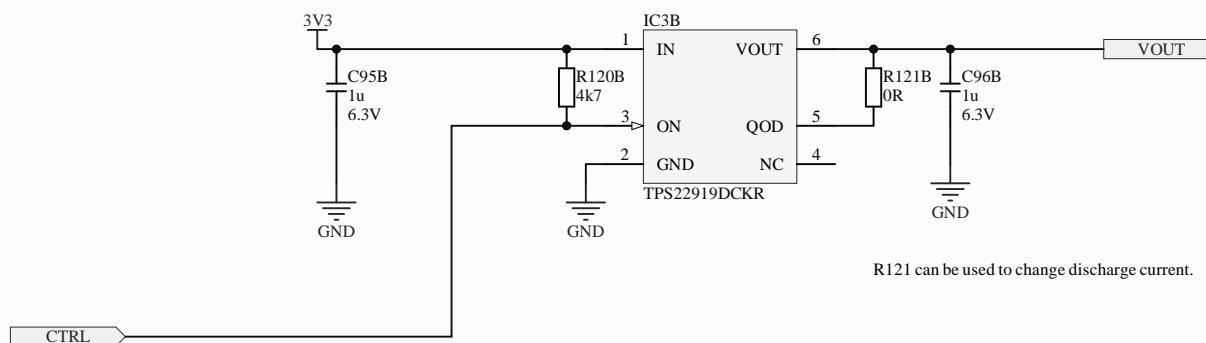
Table 2 describes the connection of the VOUT pin depending on the state of the ON pin as well as the various QOD pin configurations.

Table 2. VOUT Connection

ON	QOD CONFIGURATION	TPS22919 VOUT
L	QOD pin connected to VOUT with R_{QOD}	GND ($R_{PD_QOD} + R_{QOD}$)
L	QOD pin tied to VOUT directly	GND (R_{PD_QOD})
L	QOD pin left open	Floating
H	N/A	VIN

B

B



R121 can be used to change discharge current.

C

C

Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb	Revision: A1.1
Page Contents: HB_Logic_Power_Controller.SchDoc	
SCH Designer: JJJ	Checked by: ---
PCB Designer: ---	Checked by: ---
Date: 25.3.2025	Sheet: 14 of 14

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D

D

A

A

8.4 Device Functional Modes

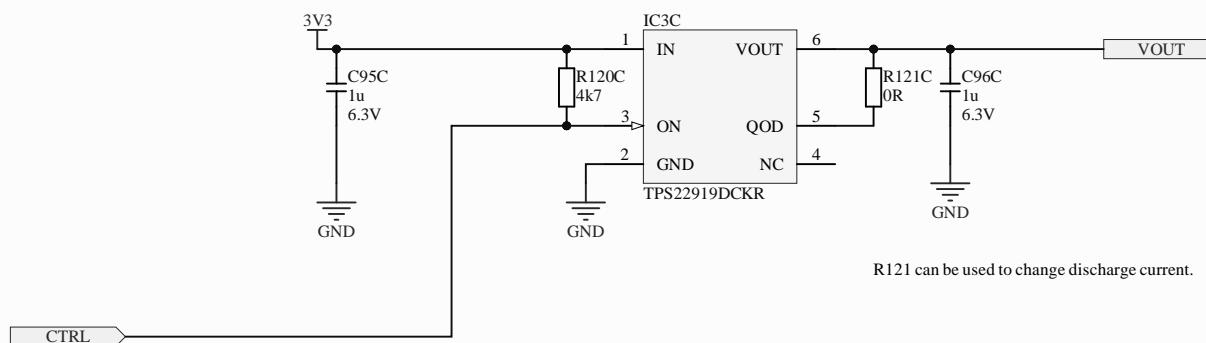
Table 2 describes the connection of the VOUT pin depending on the state of the ON pin as well as the various QOD pin configurations.

Table 2. VOUT Connection

ON	QOD CONFIGURATION	TPS22919 VOUT
L	QOD pin connected to VOUT with R_{QOD}	GND ($R_{PD_QOD} + R_{QOD}$)
L	QOD pin tied to VOUT directly	GND (R_{PD_QOD})
L	QOD pin left open	Floating
H	N/A	VIN

B

B



R121 can be used to change discharge current.

Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb	Revision: A1.1
Page Contents: HB_Logic_Power_Controller.SchDoc	
SCH Designer: JJJ	Checked by: ---
PCB Designer: ---	Checked by: ---
Date: 25.3.2025	Sheet: 14 of 14

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A

A

8.4 Device Functional Modes

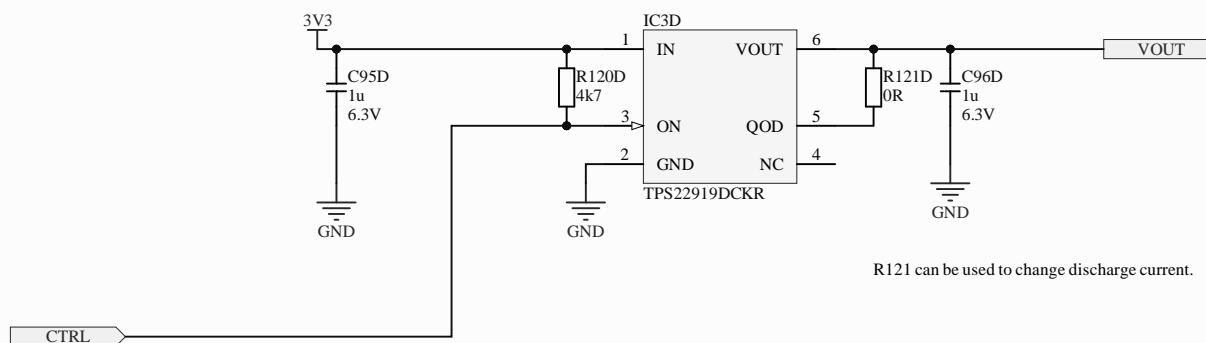
Table 2 describes the connection of the VOUT pin depending on the state of the ON pin as well as the various QOD pin configurations.

Table 2. VOUT Connection

ON	QOD CONFIGURATION	TPS22919 VOUT
L	QOD pin connected to VOUT with R_{QOD}	GND ($R_{PD_QOD} + R_{QOD}$)
L	QOD pin tied to VOUT directly	GND (R_{PD_QOD})
L	QOD pin left open	Floating
H	N/A	VIN

B

B



C

C

Project: BRR_CB_P03_REV_A1_1-STM32MP157.PrjPcb	Revision: A1.1
Page Contents: HB_Logic_Power_Controller.SchDoc	
SCH Designer: JJJ	Checked by: ---
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