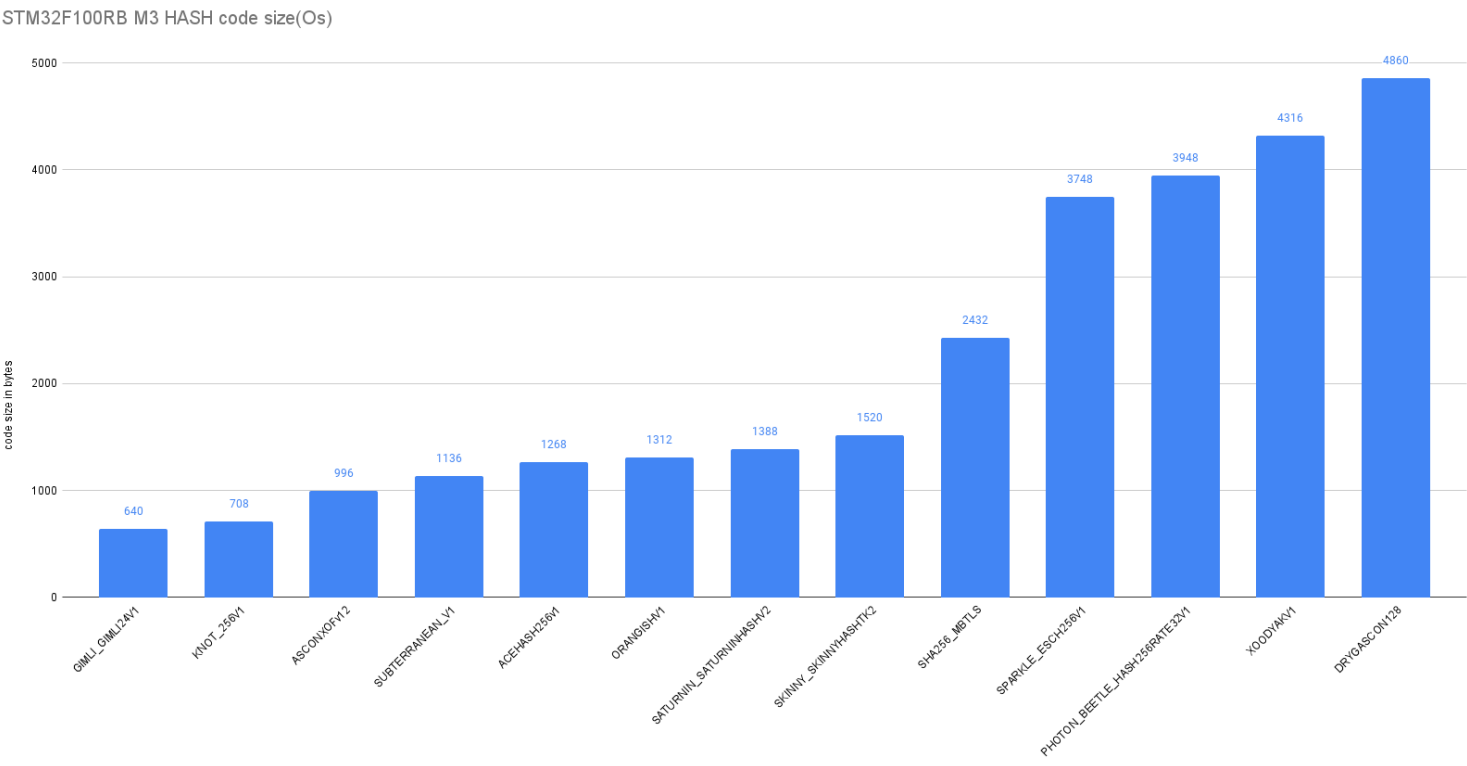
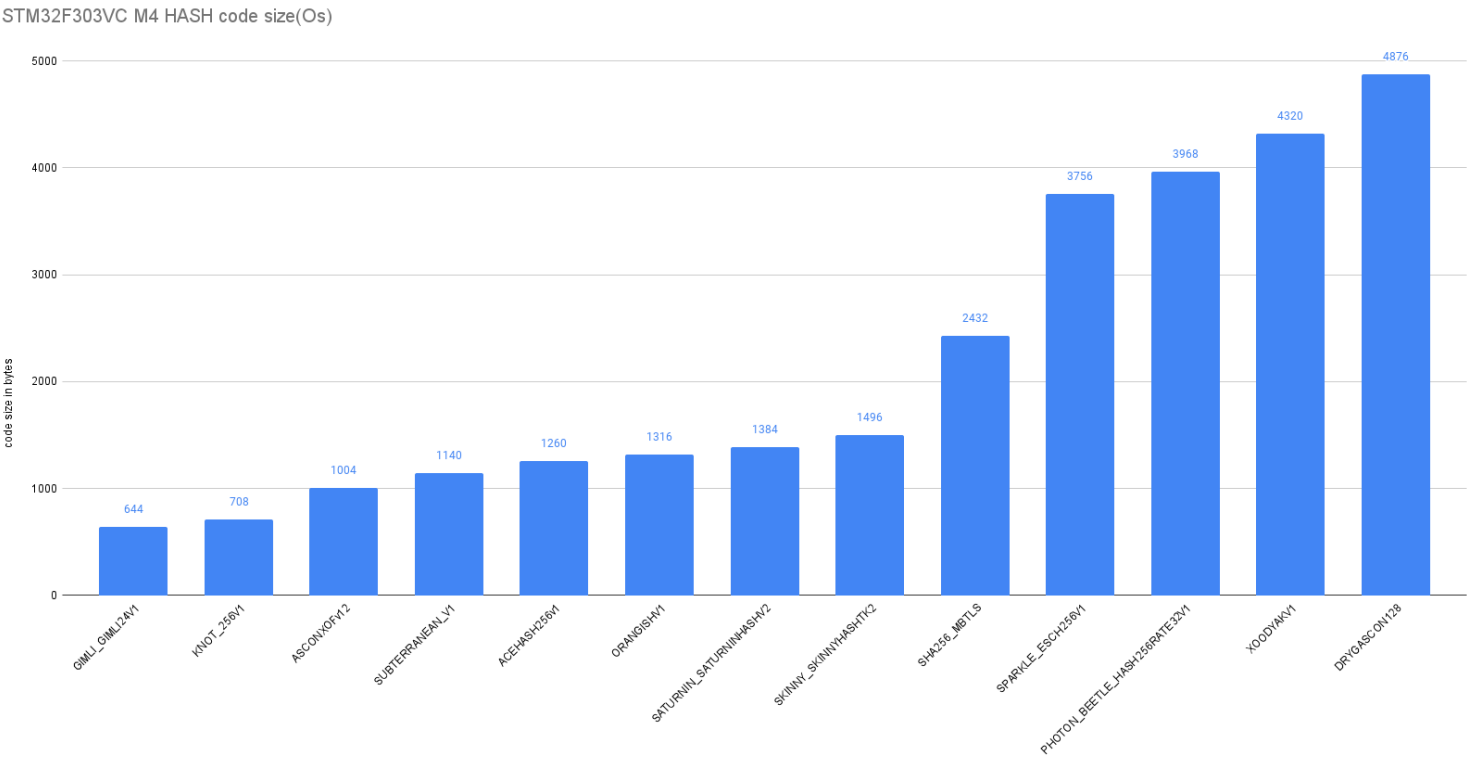
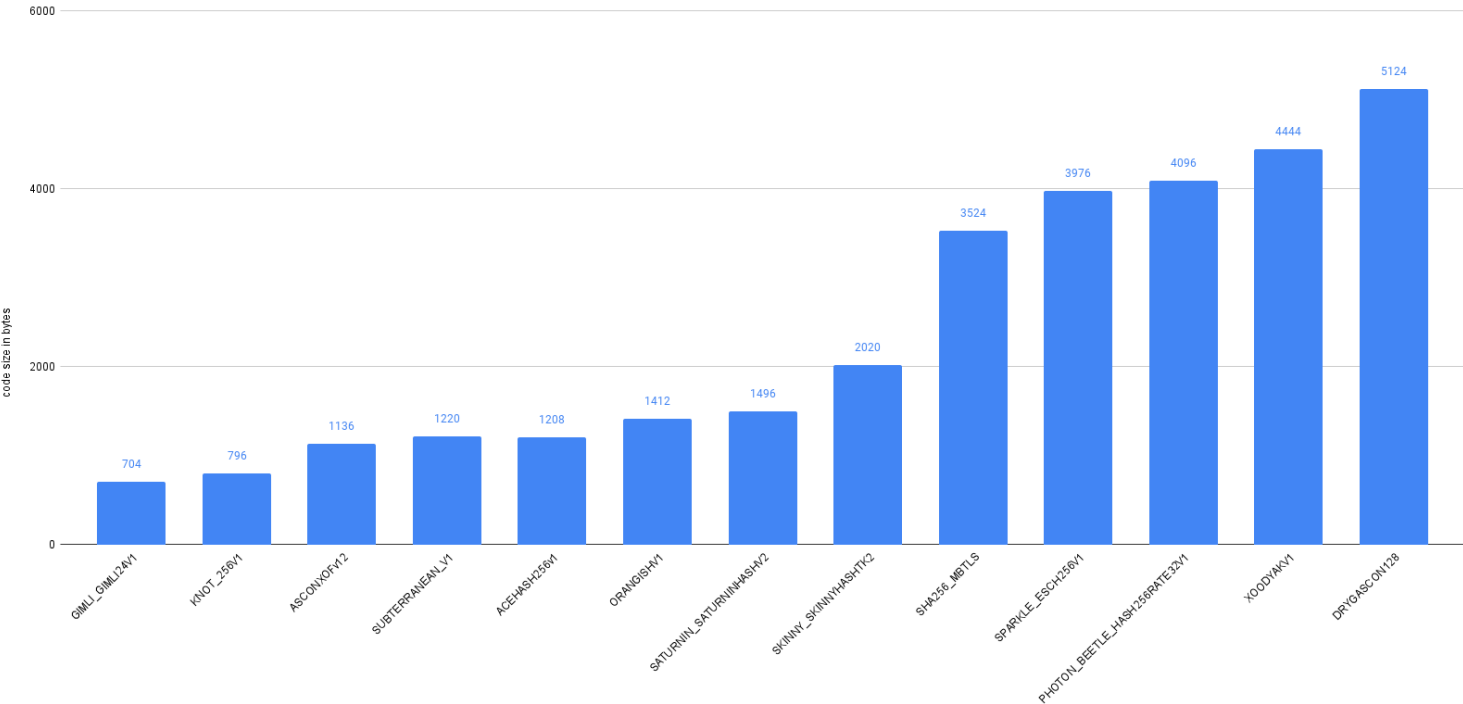


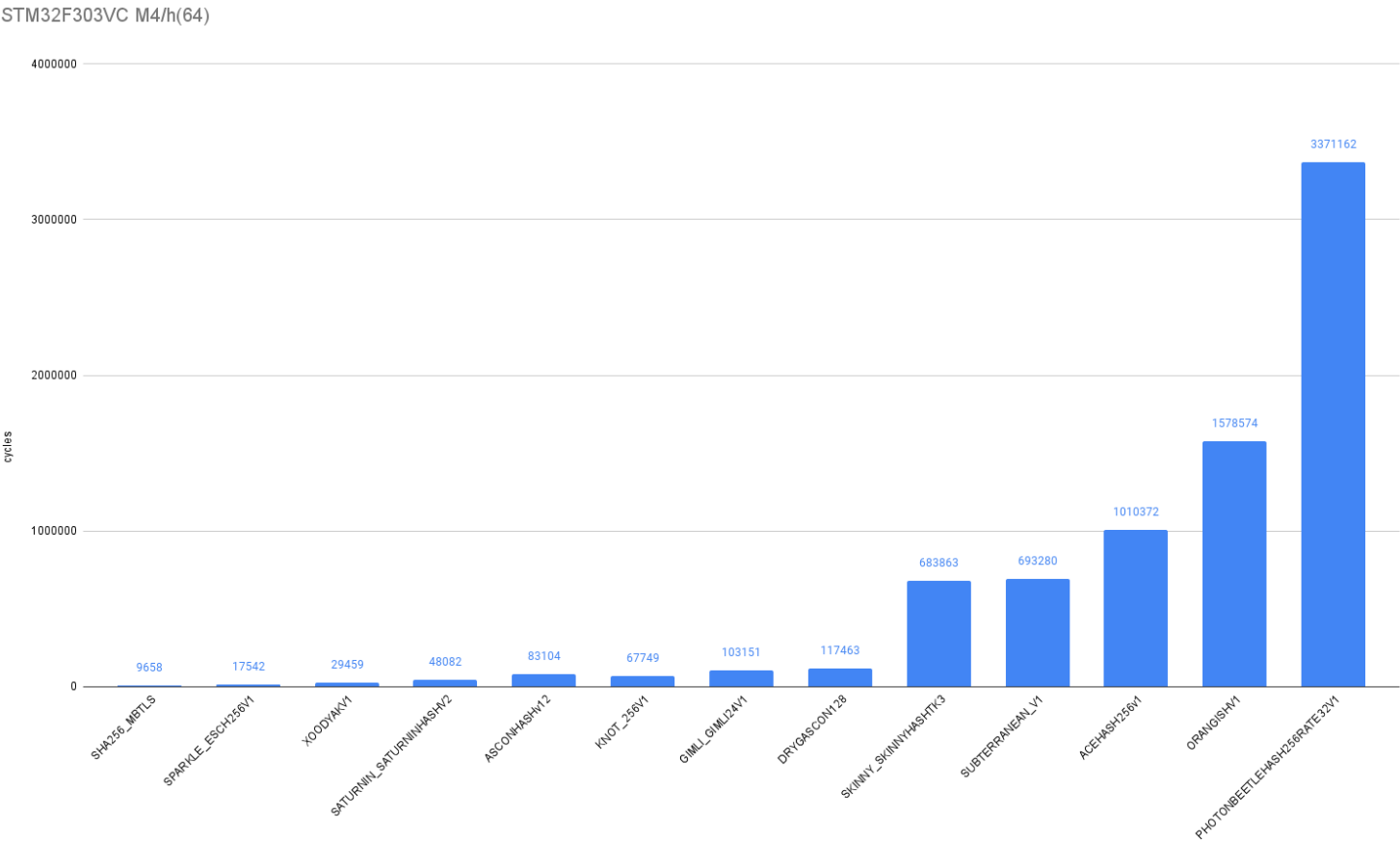
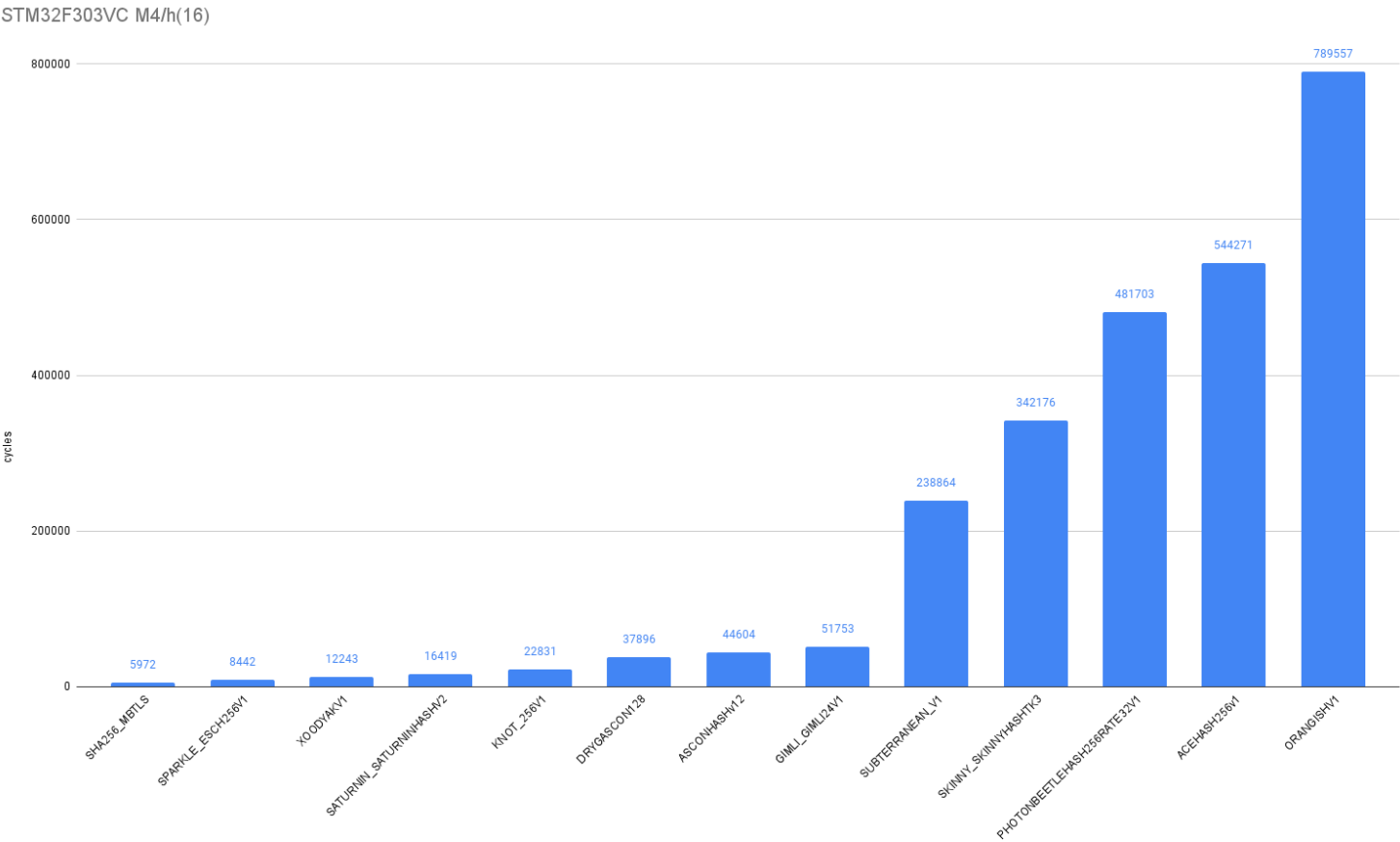
Code size of different HASH algorithms on Cortex-M0, Cortex-M3 and Cortex-M4 Platforms



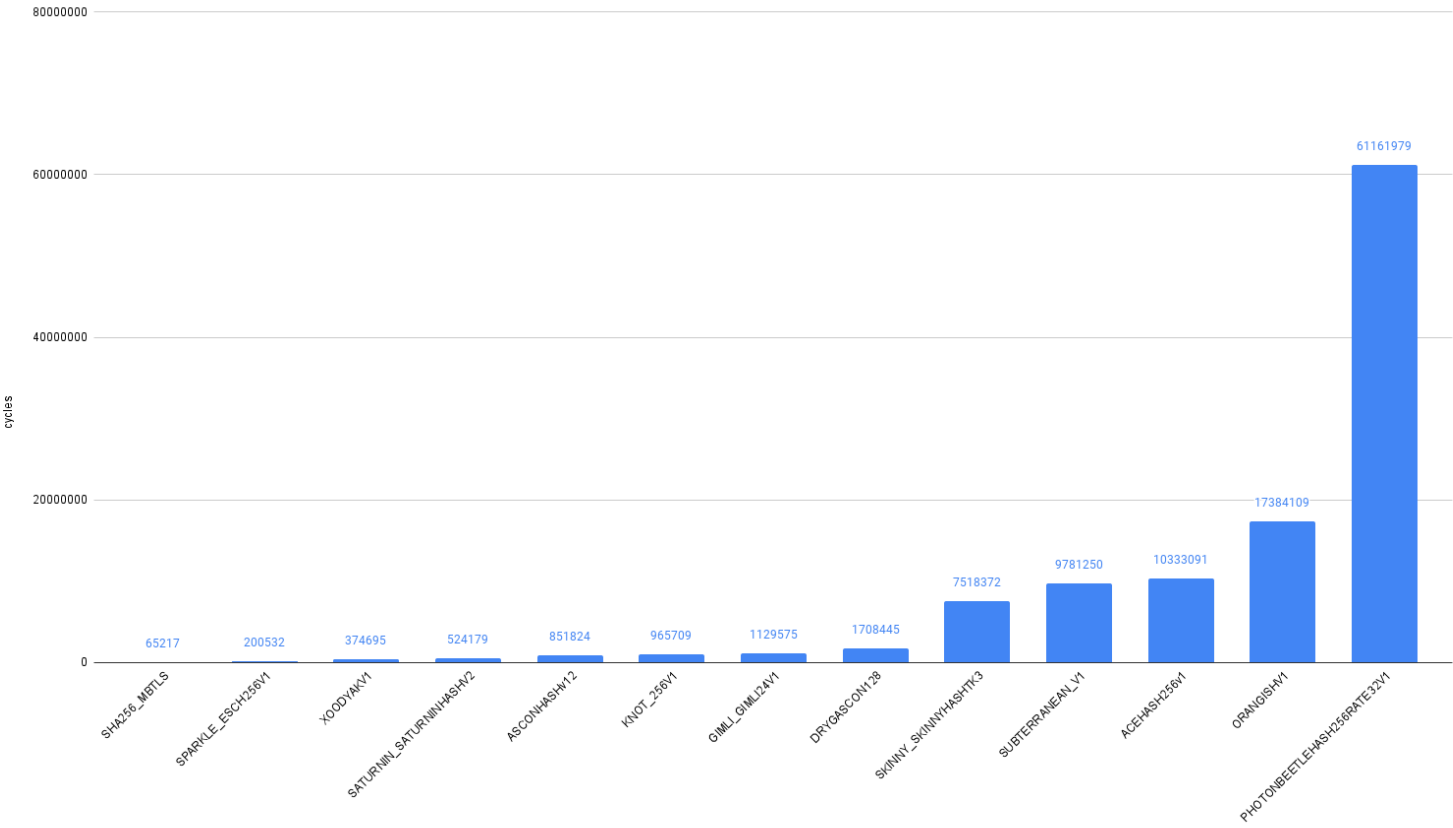
STM32F051R8 M0 HASH code size(0s)



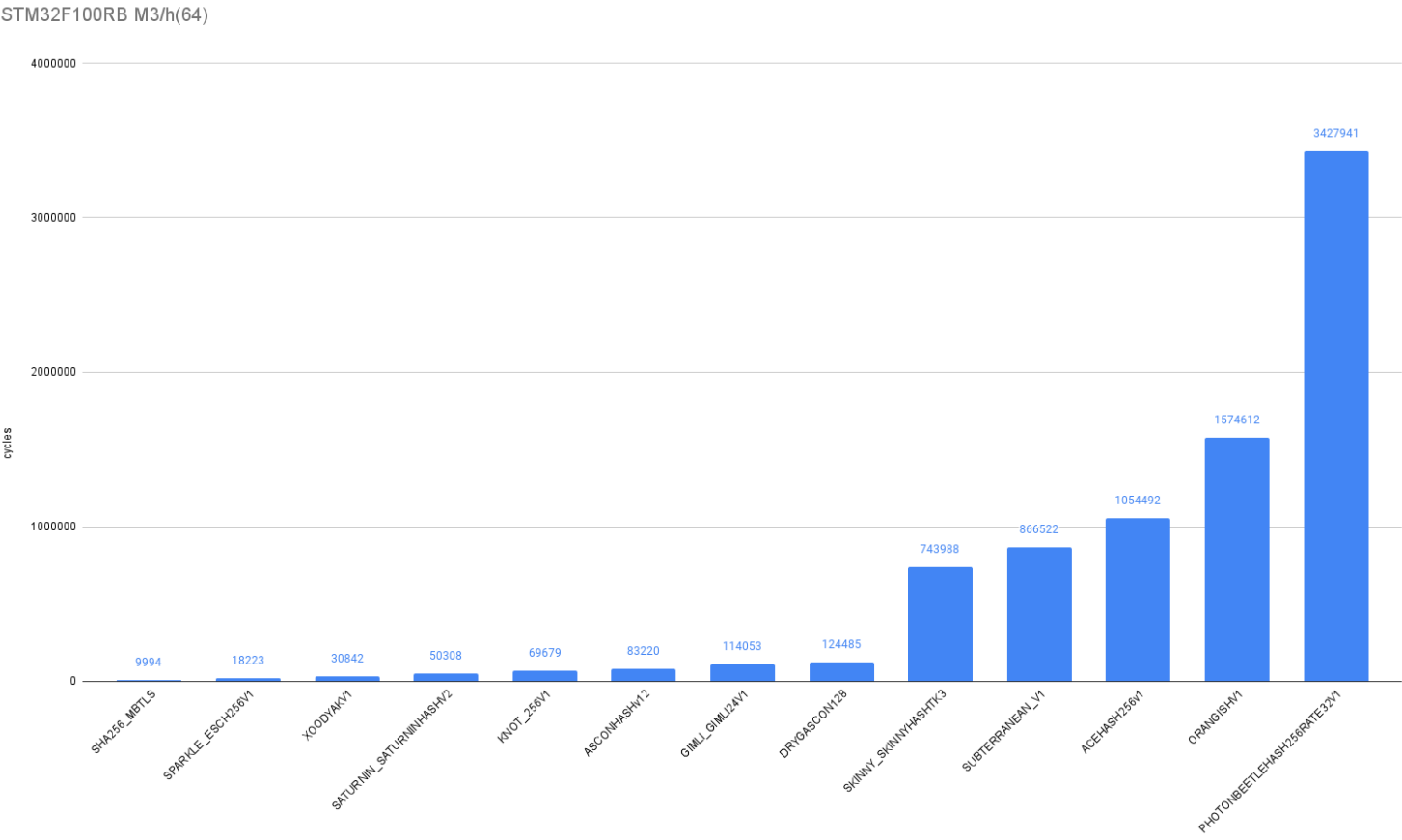
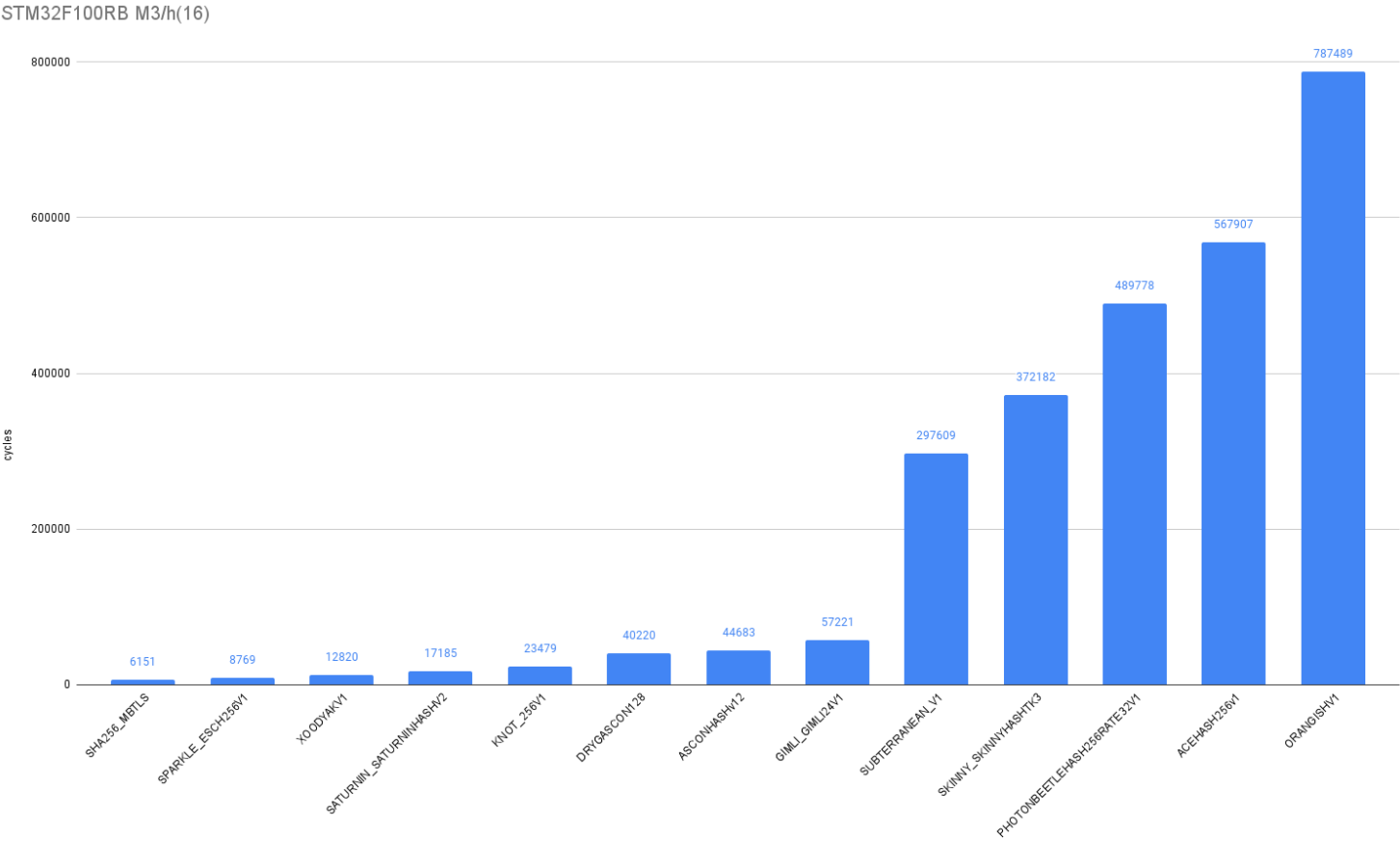
Execution cycles of different HASH algorithms on Cortex-M4



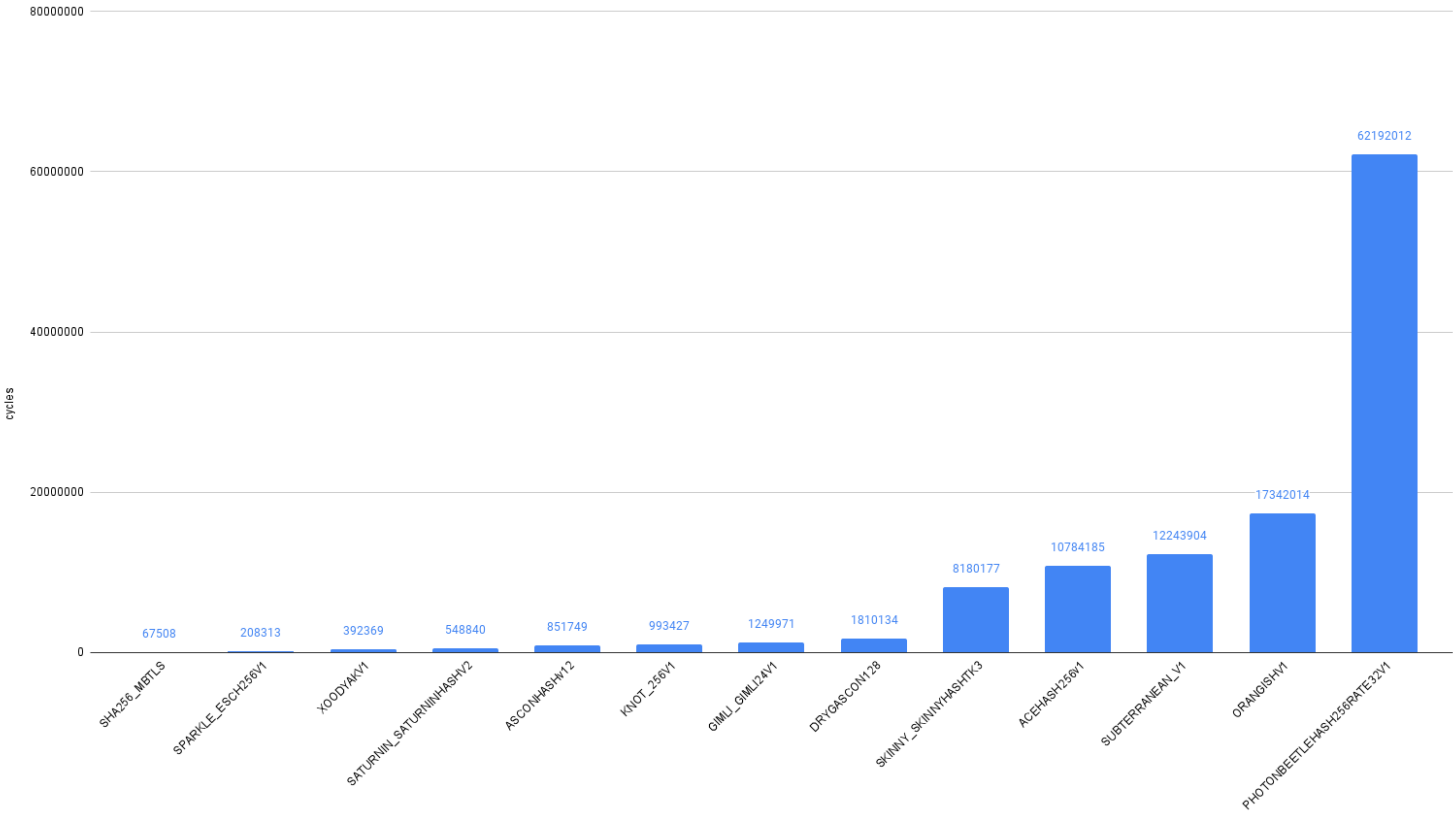
STM32F303VC M4/h(1024)



Execution cycles of different HASH algorithms on Cortex-M3

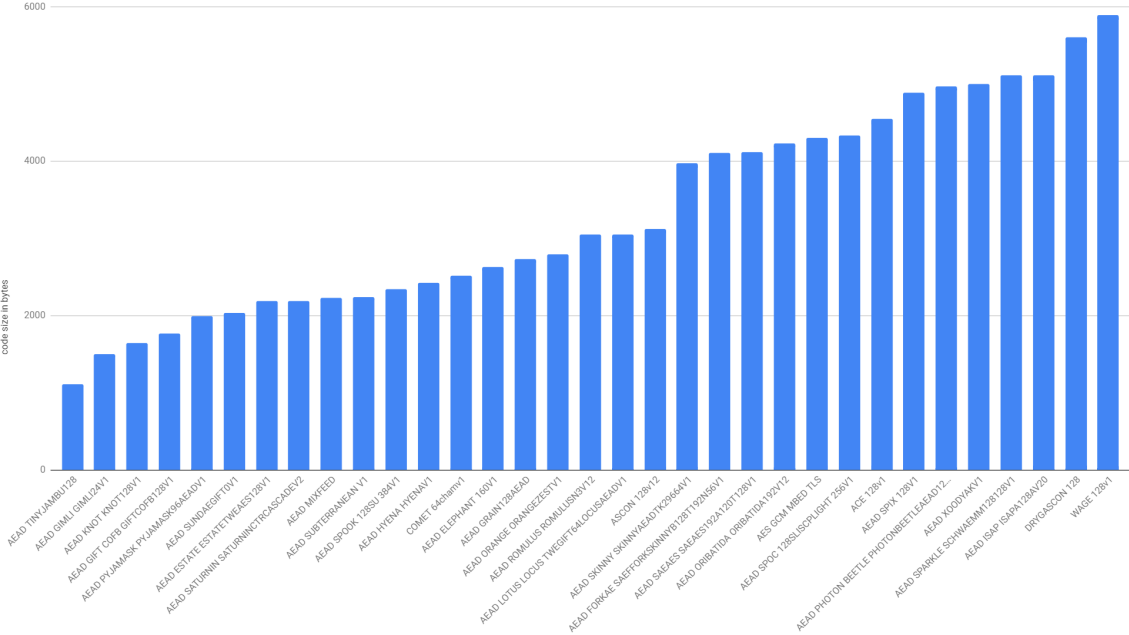


STM32F100RB M3/h(1024)

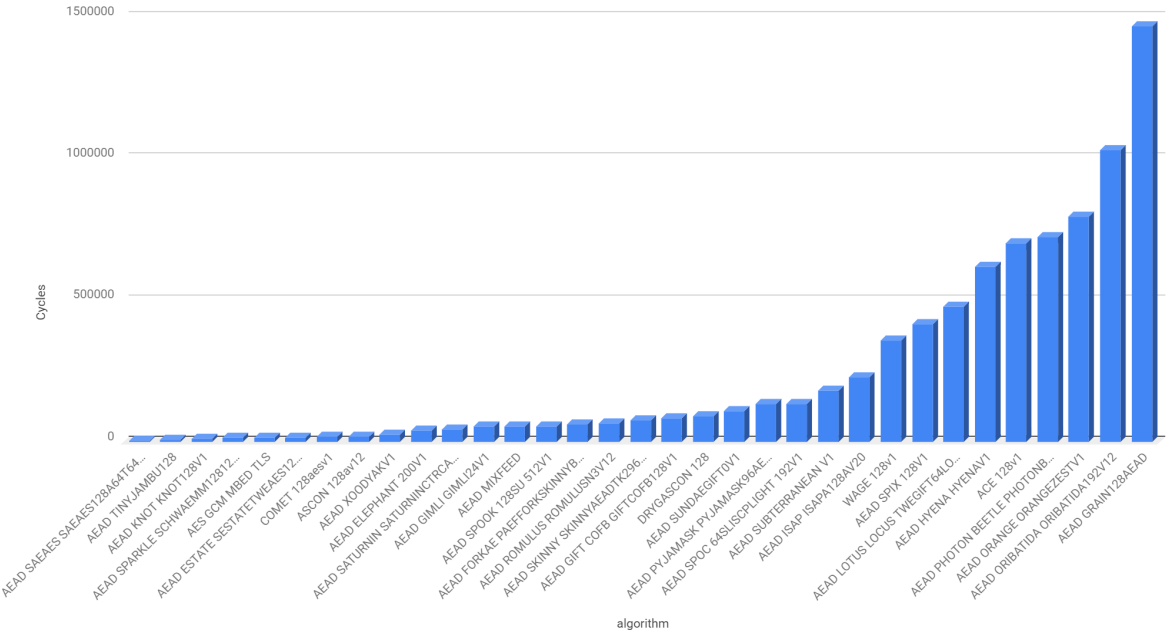


Execution cycles of different HASH algorithms on Cortex-M0

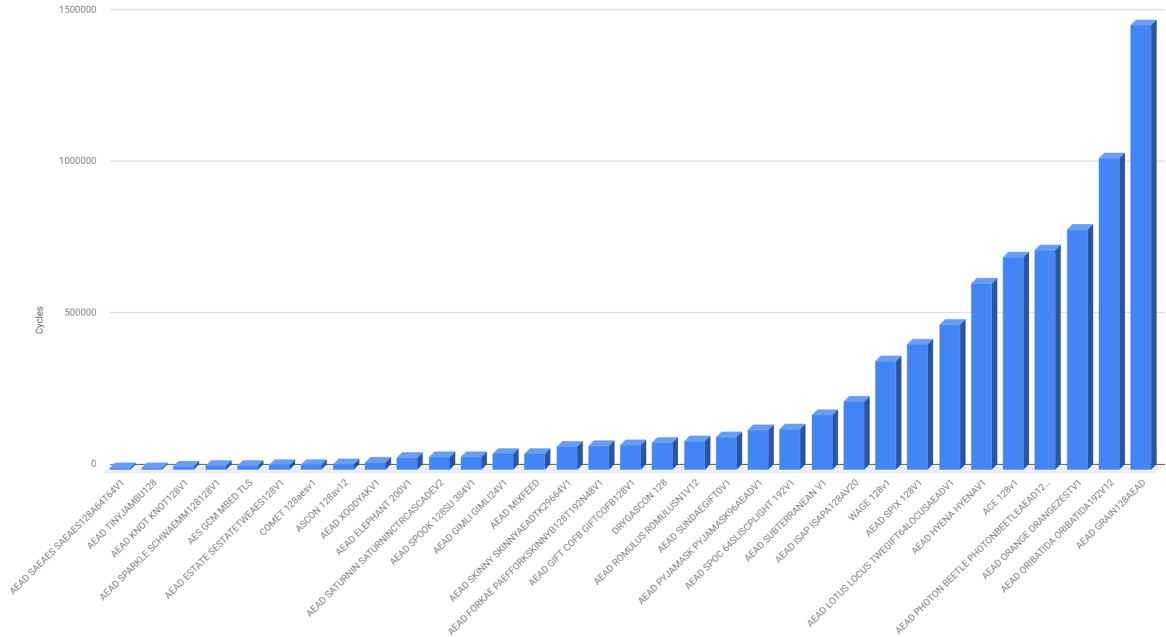
STM32F303VC M4 AEAD code size(0s)



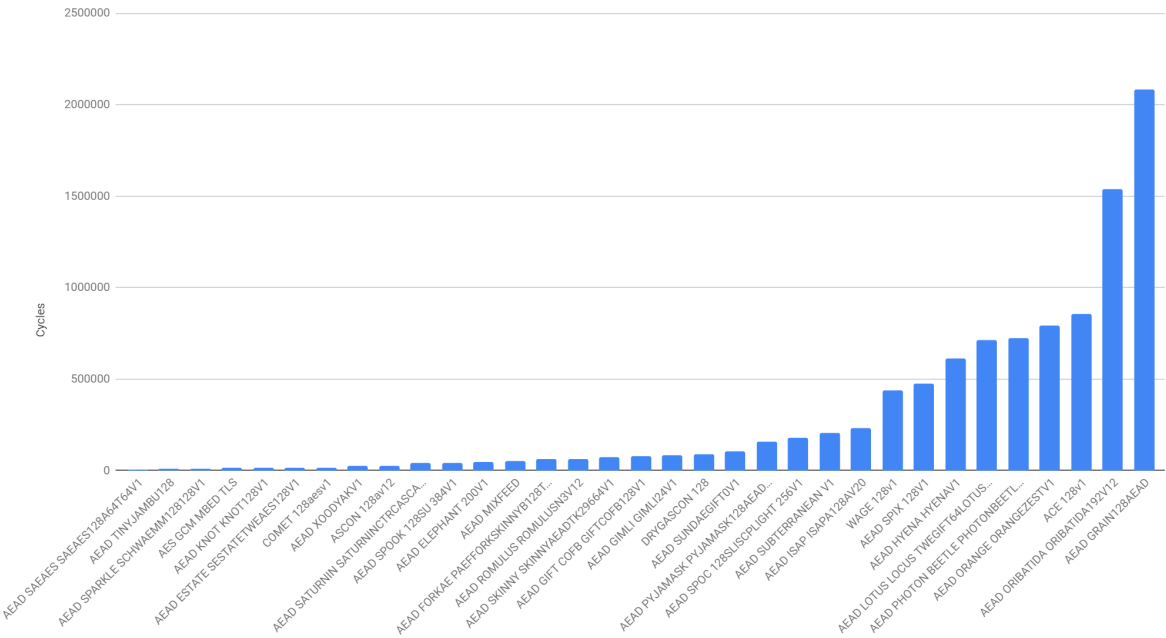
STM32F303VC M4 AEAD / enc(8.8)



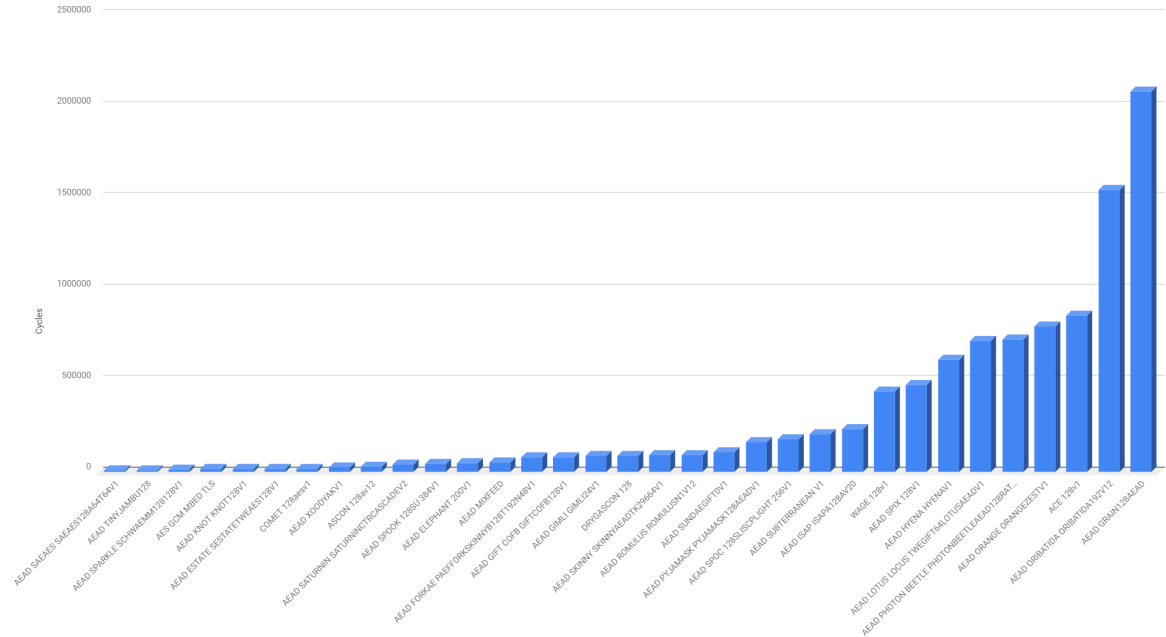
STM32F303VC M4 AEAD / dec(8.8)



STM32F303VC M4 AEAD / enc(16,16)

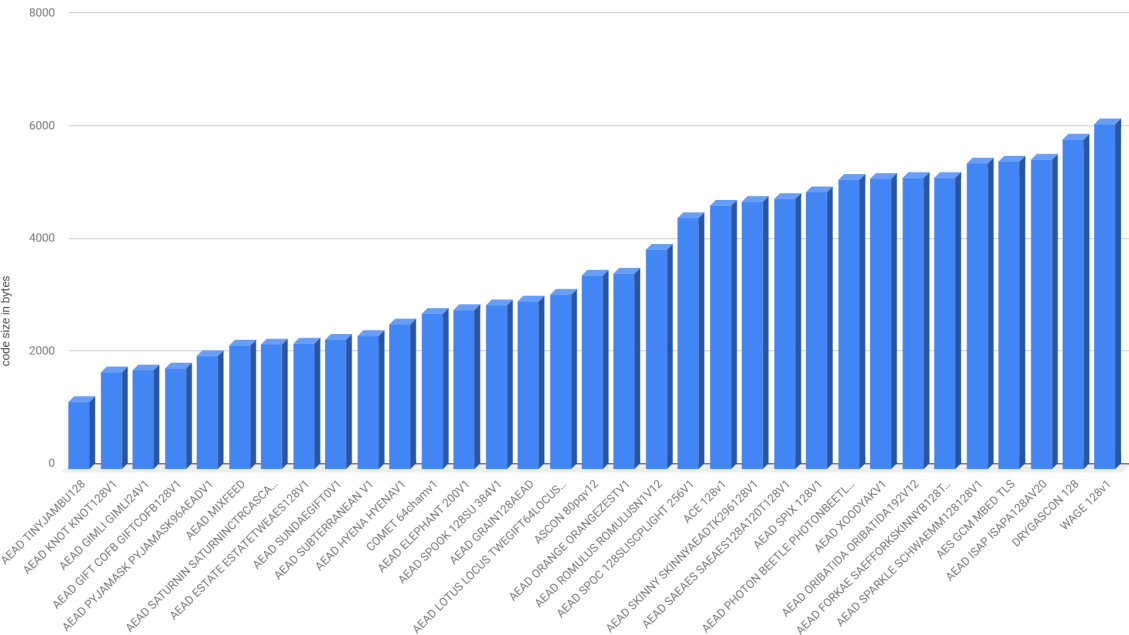


STM32F303VC M4 AEAD / dec(16,16)

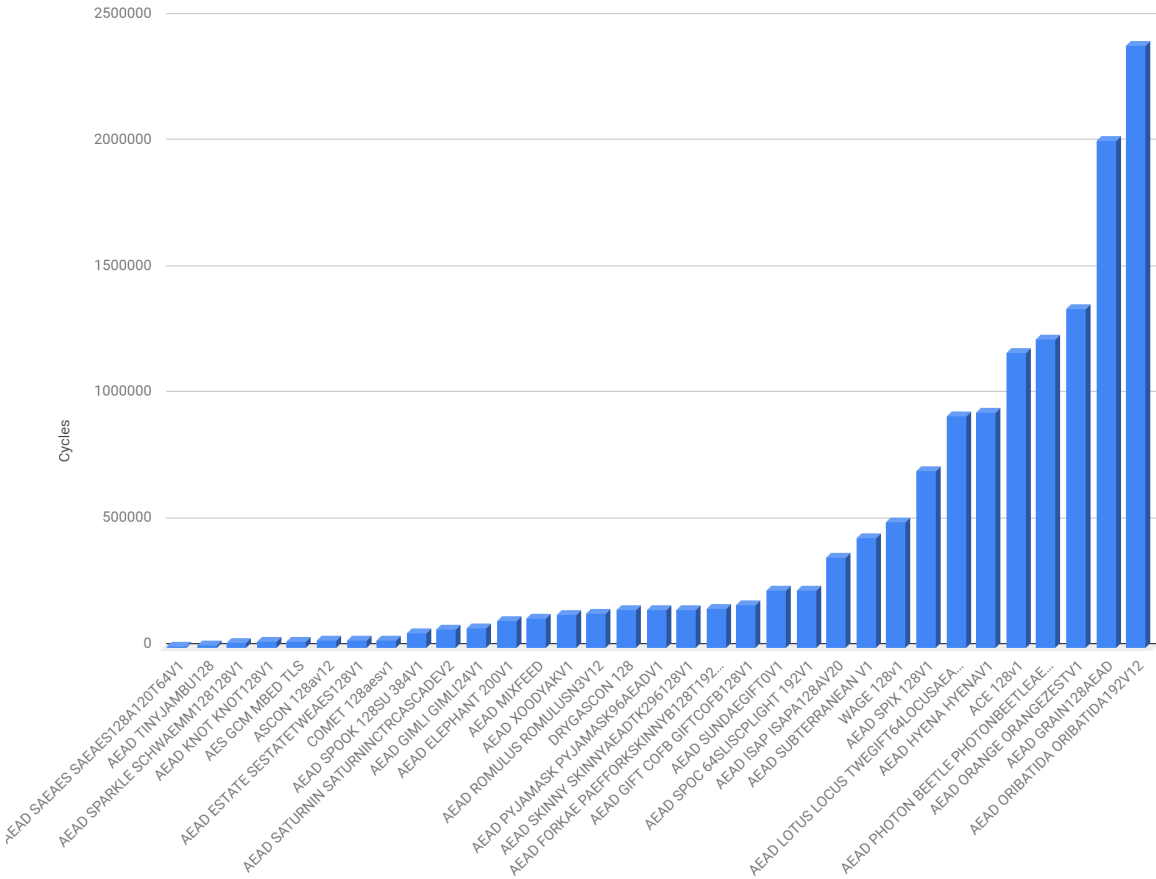


[illegible][illegible]

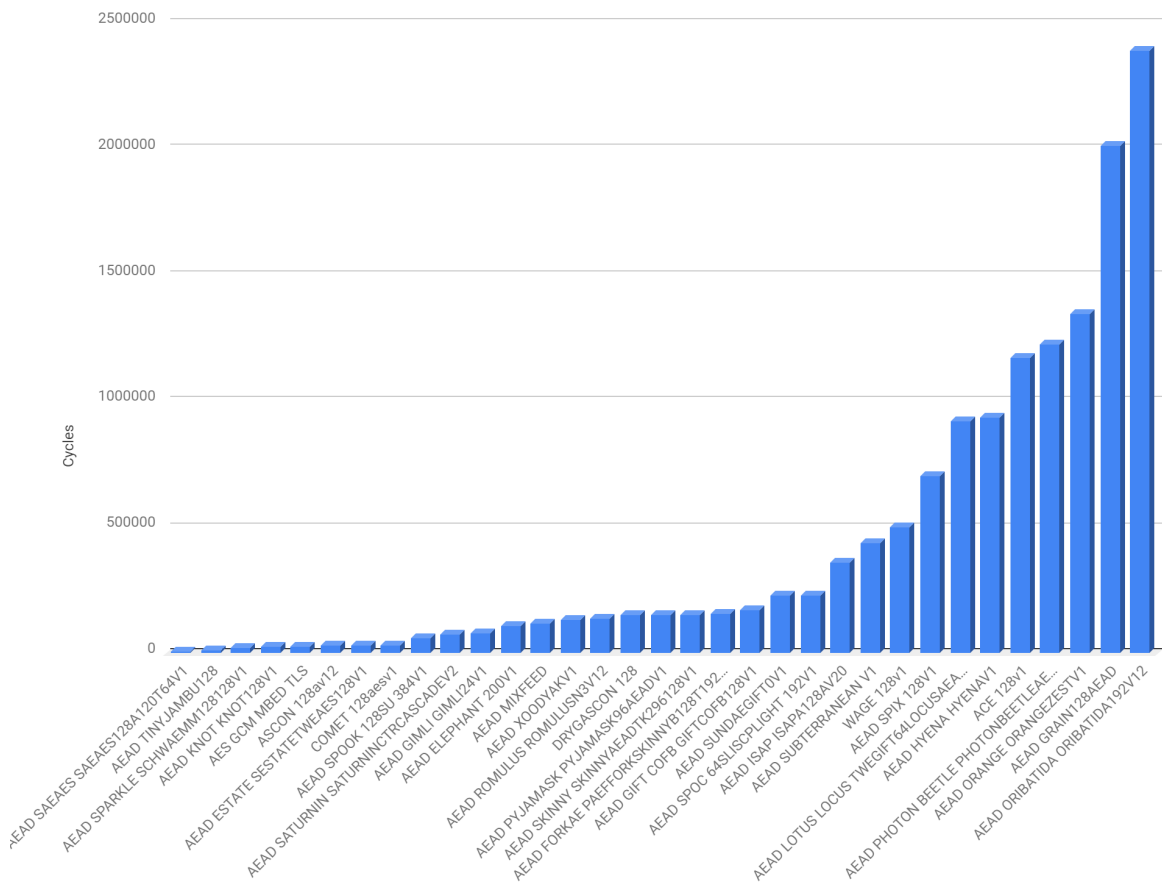
STM32F051R8 M0 AEAD code size(0s)



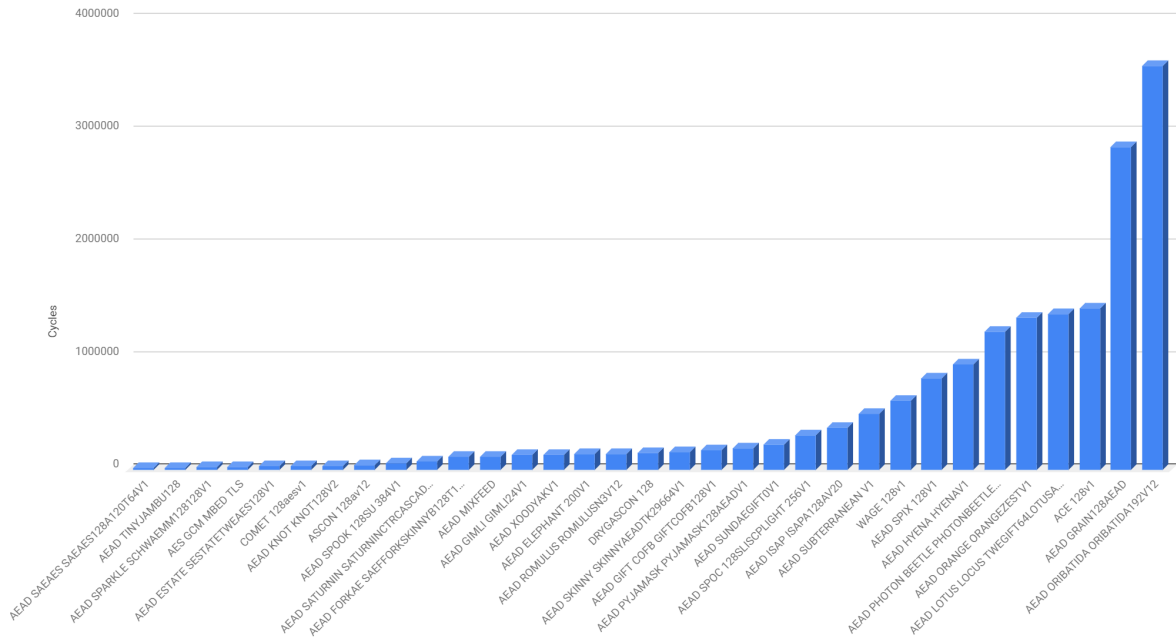
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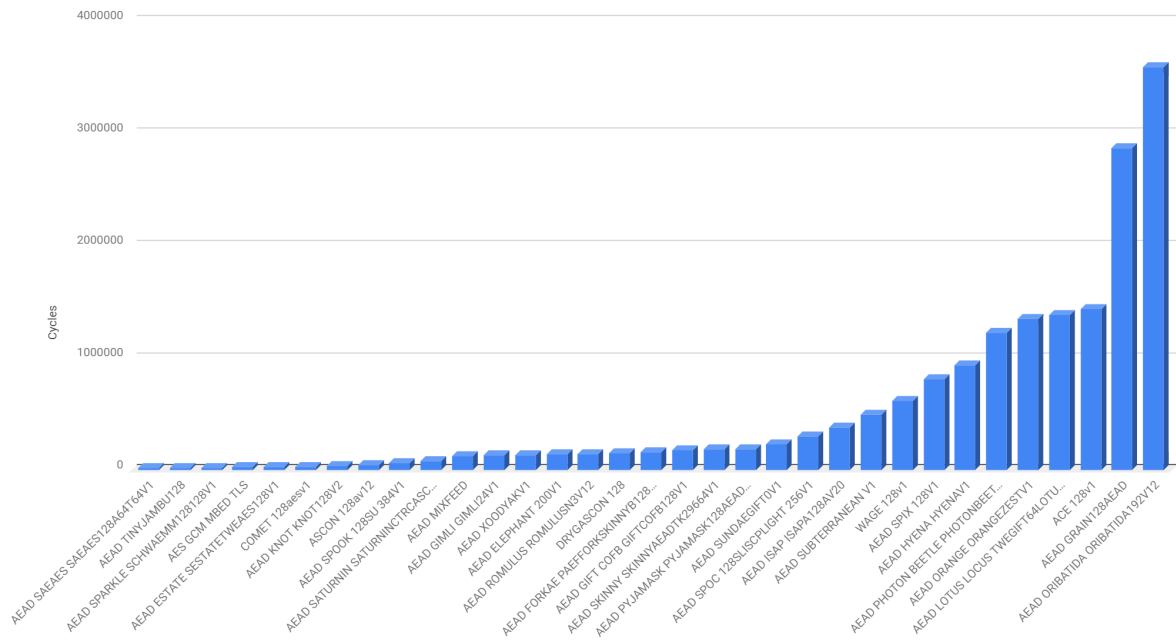
STM32F051R8 M0 AEAD / dec(8,8)



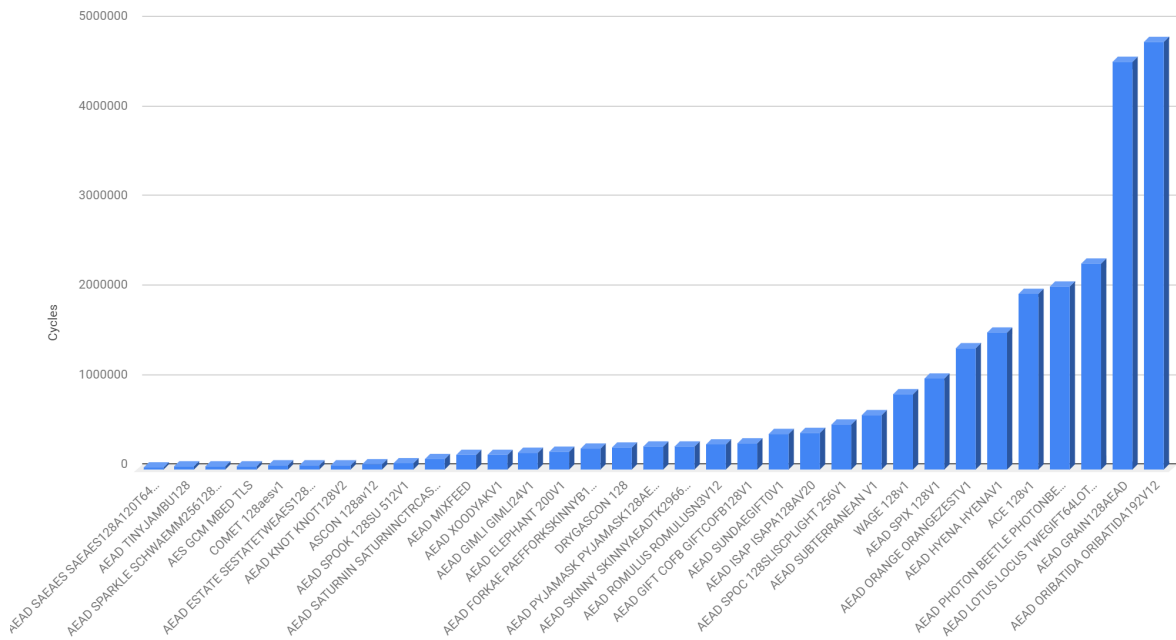
STM32F051R8 M0 AEAD / enc(16,16)



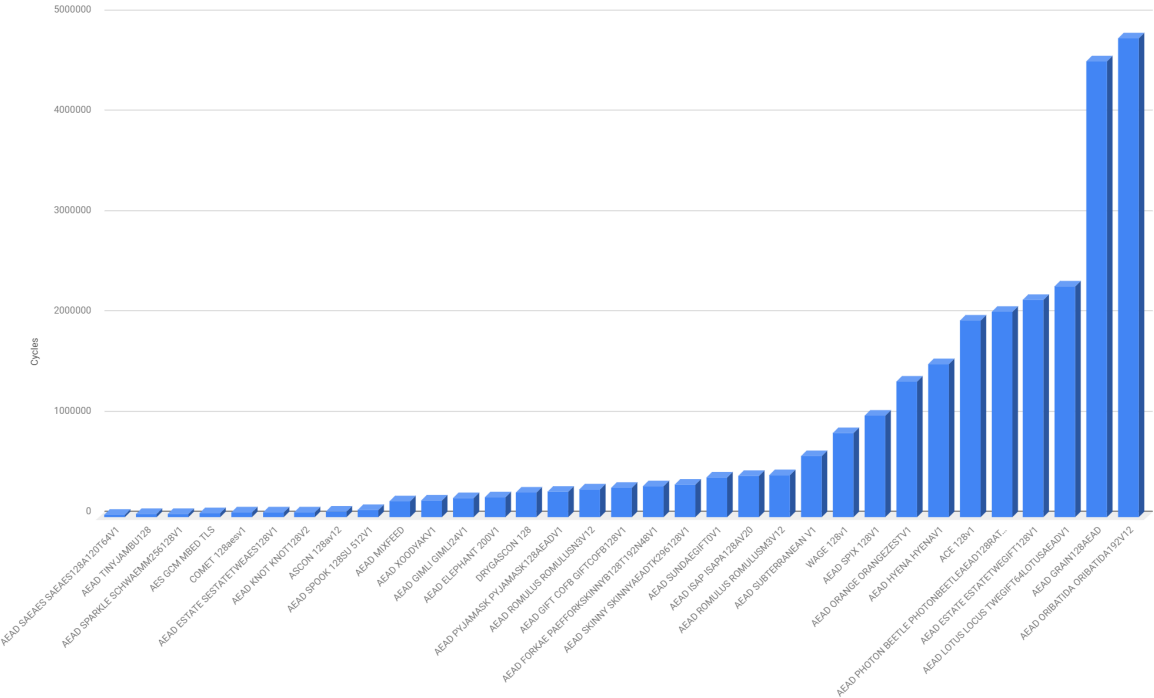
STM32F051R8 M0 AEAD / dec(16,16)



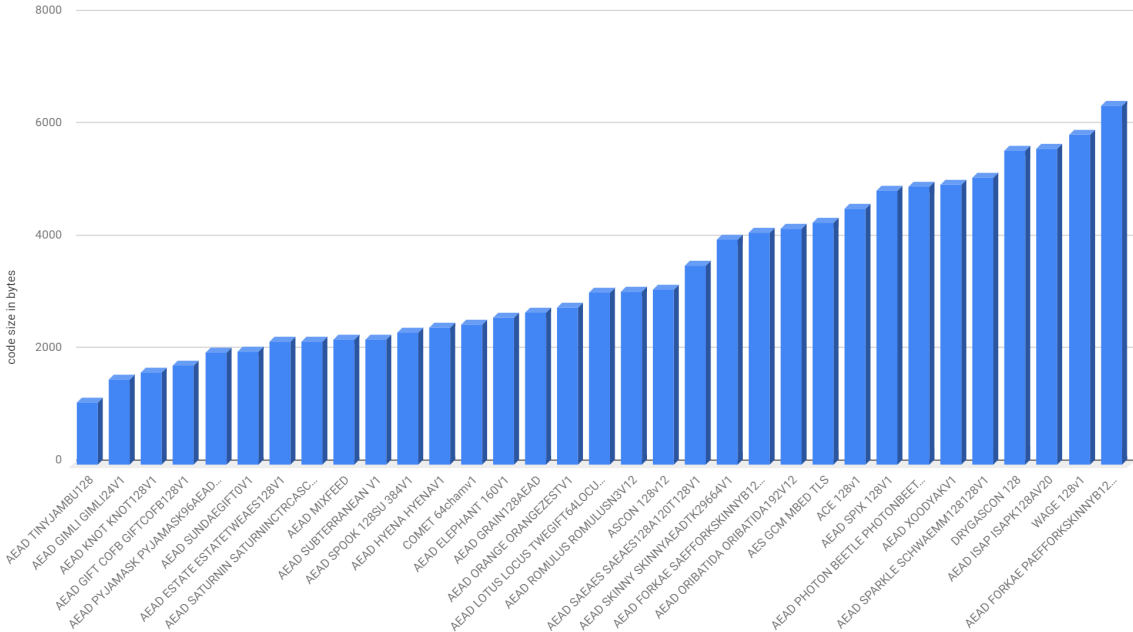
STM32F051R8 M0 AEAD / enc(32,32)



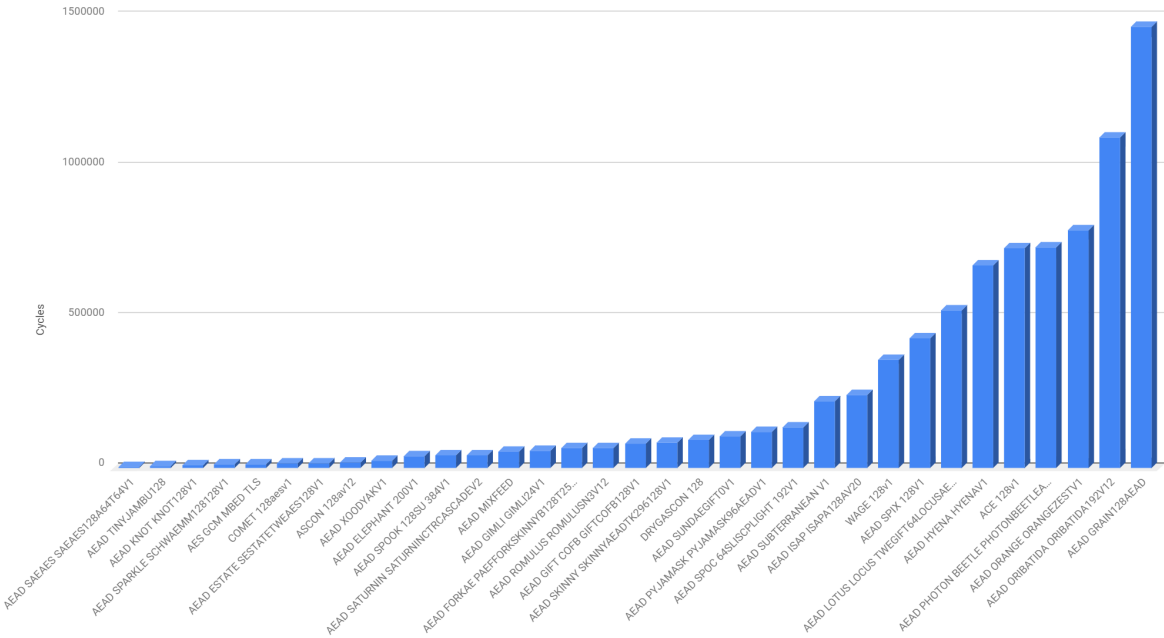
STM32F051R8 M0 AEAD / dec(32,32)



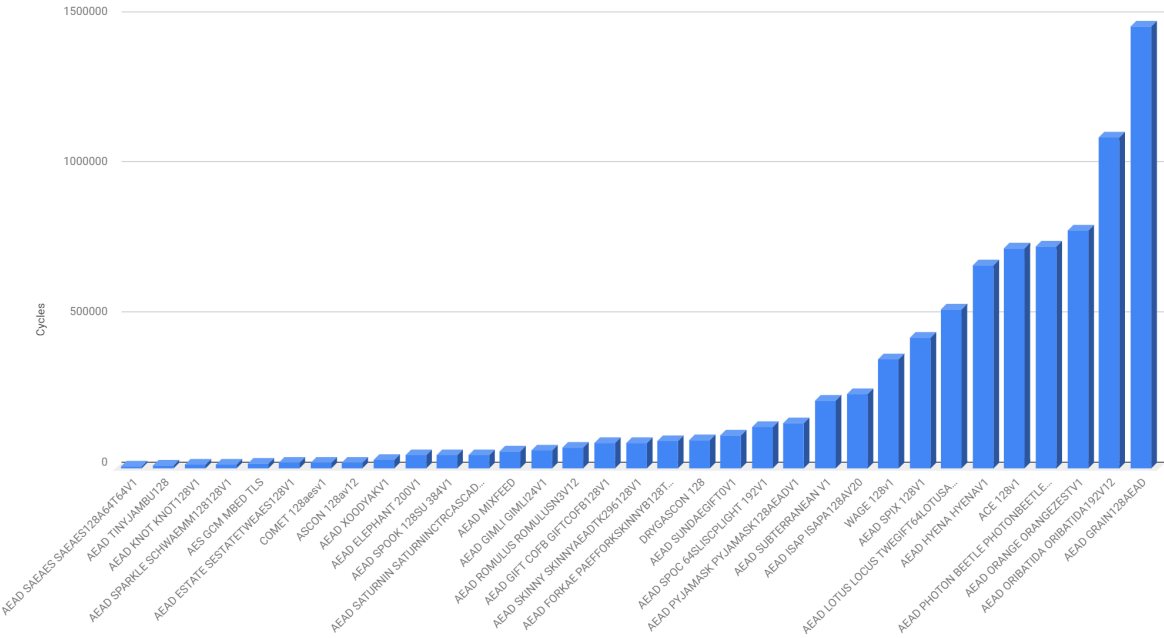
STM32f100RB M3 AEAD code size(0s)



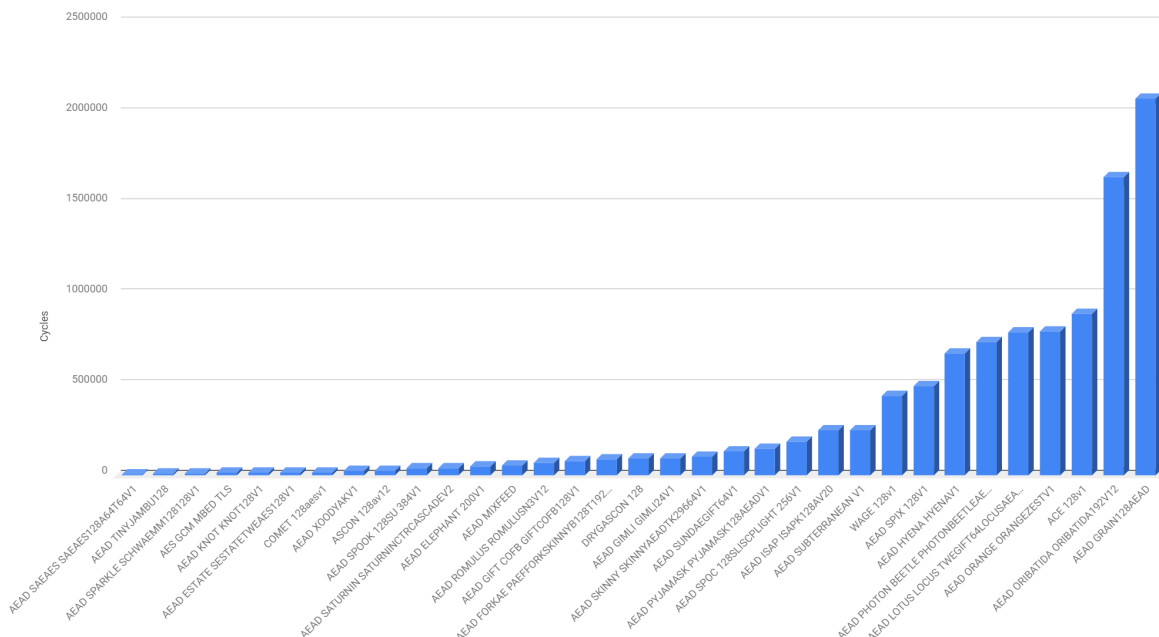
STM32f100RB M3 AEAD / enc(8,8)



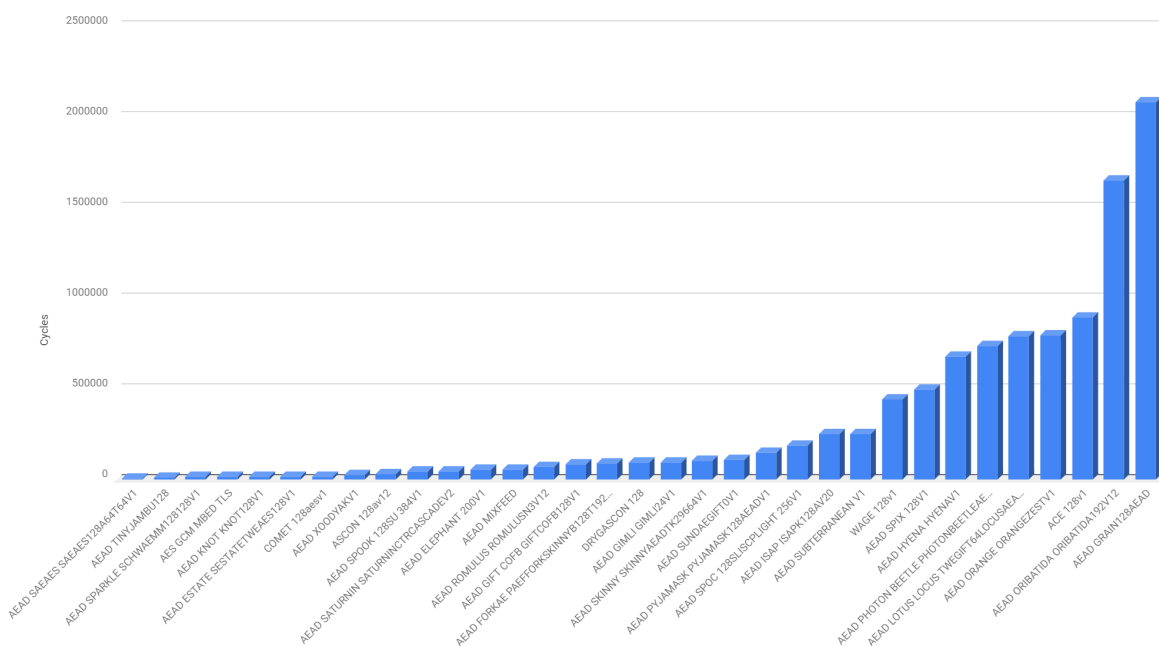
STM32f100RB M3 AEAD / dec(8,8)



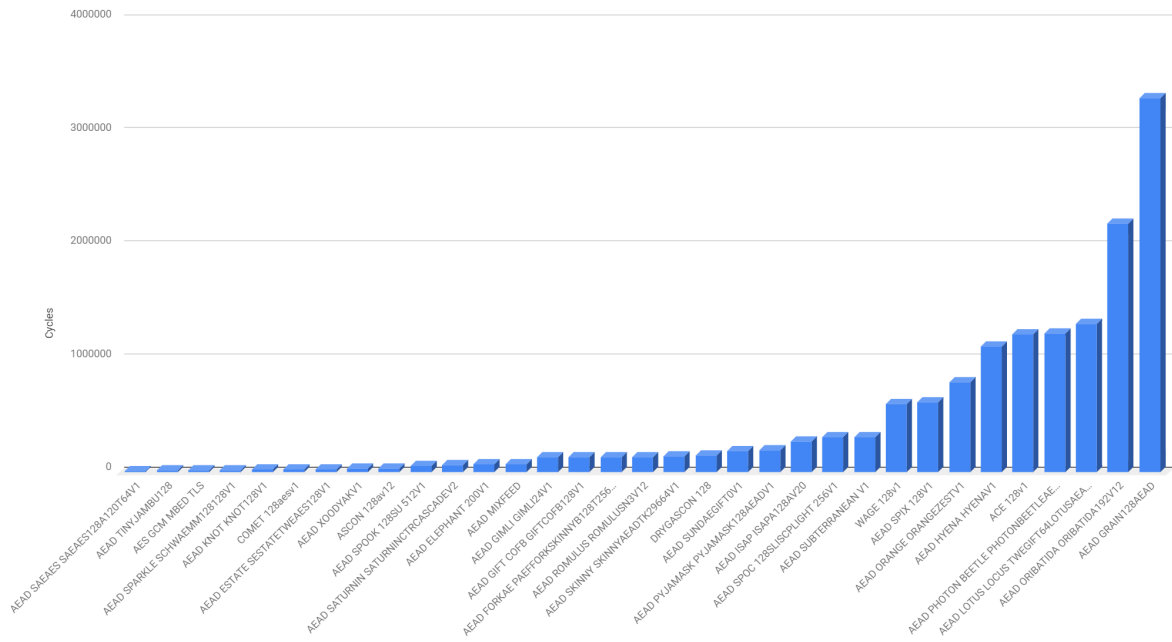
STM32f100RB M3 AEAD / enc(16,16)



STM32f100RB M3 AEAD / dec(16,16)



STM32f100RB M3 AEAD / enc(32,32)



STM32f100RB M3 AEAD / dec(32,32)

