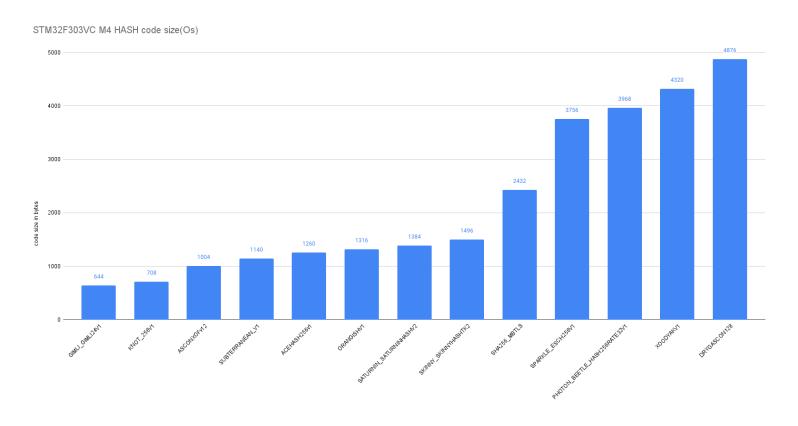
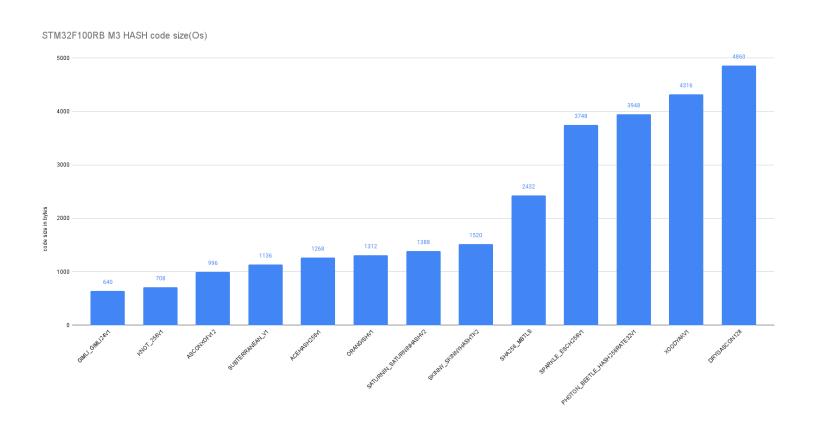
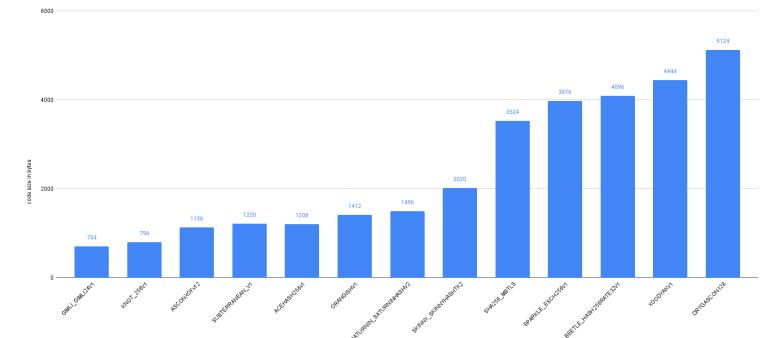
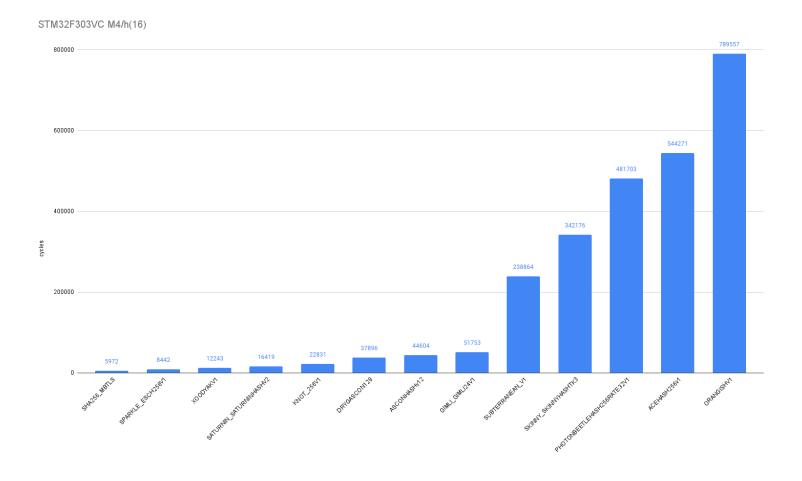
Code size of different HASH algorithms on Cortex-M0, Cortex-M3 and Cortex-M4 Platforms

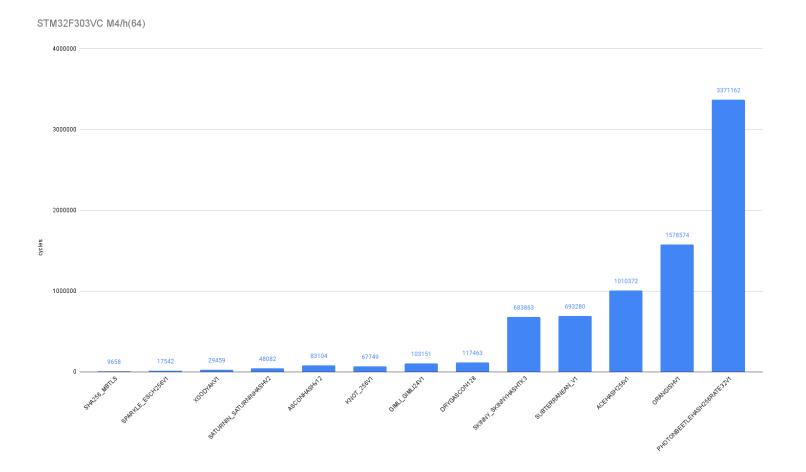


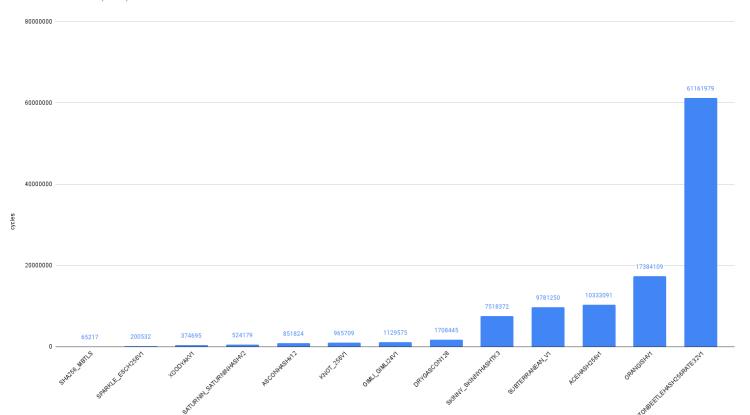




Execution cycles of different HASH algorithms on Cortex-M4

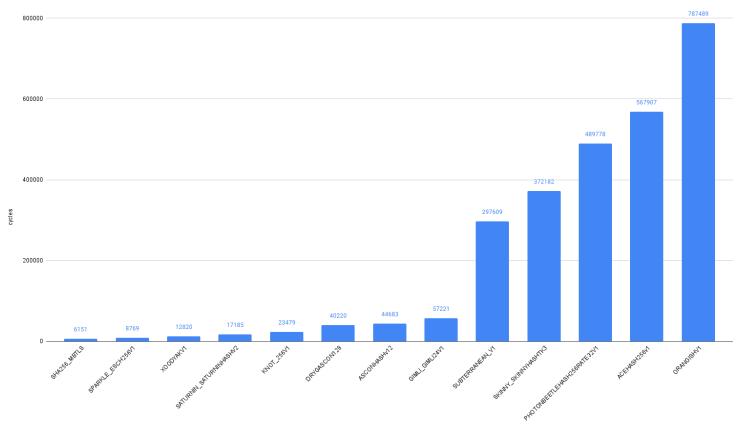




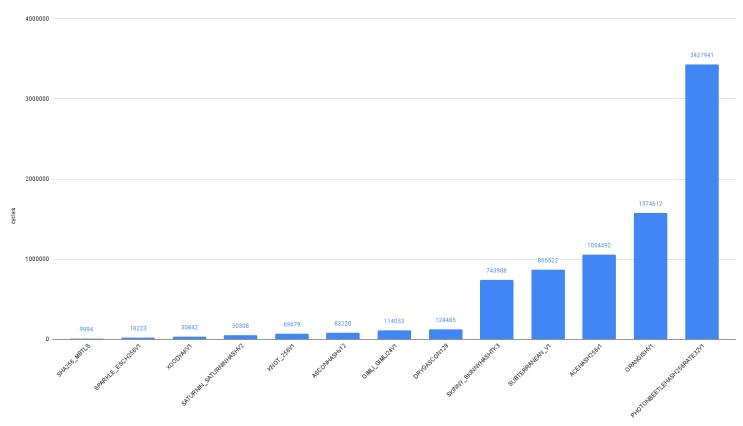


Execution cycles of different HASH algorithms on Cortex-M3



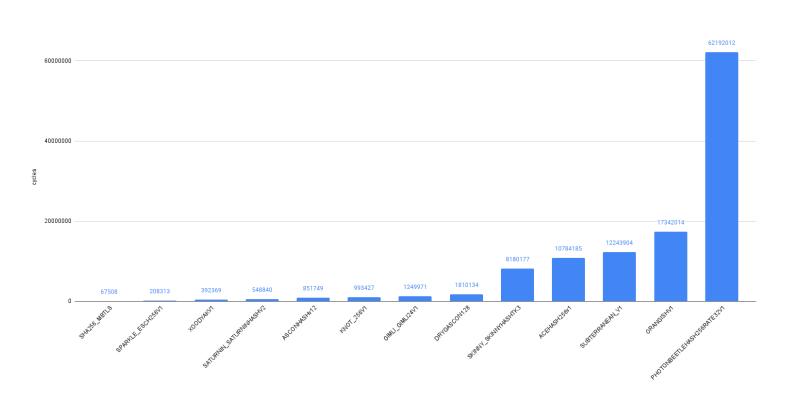


STM32F100RB M3/h(64)



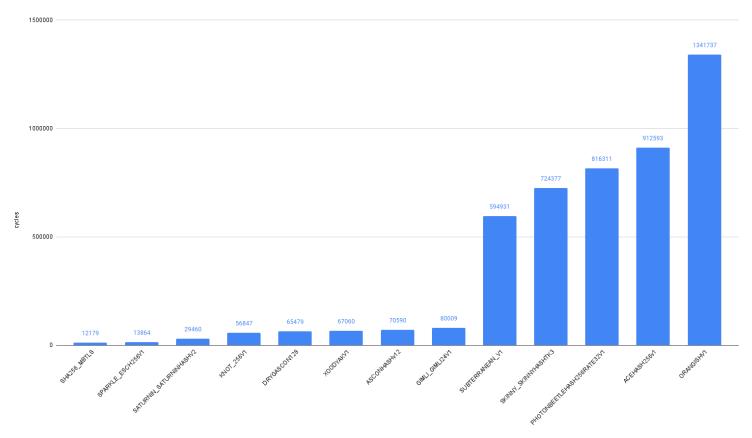




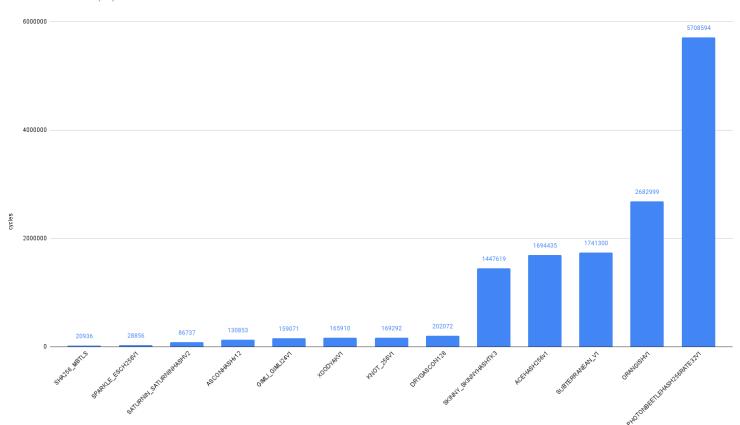


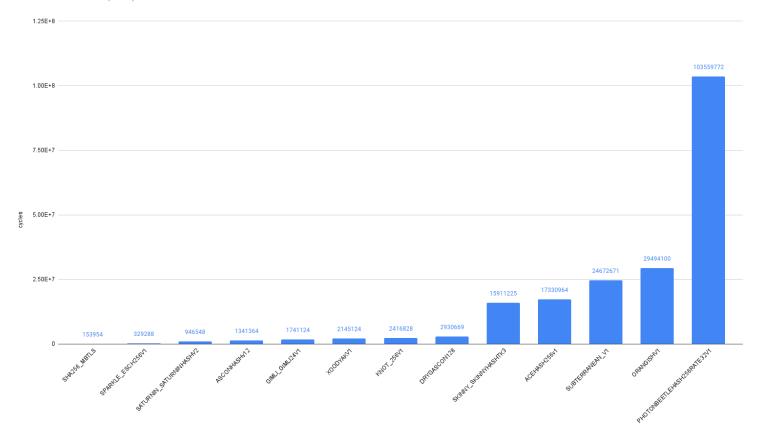
Execution cycles of different HASH algorithms on Cortex-M0

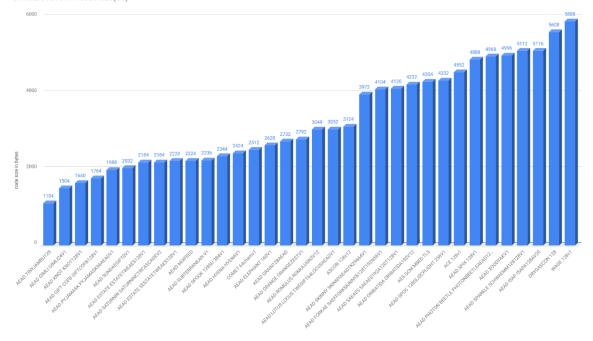




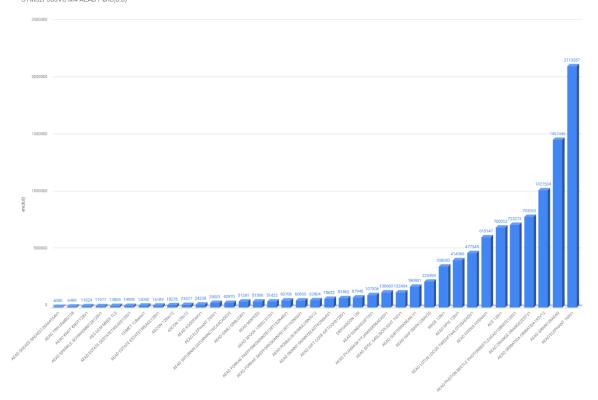
STM32F030R8 M0/h(64)

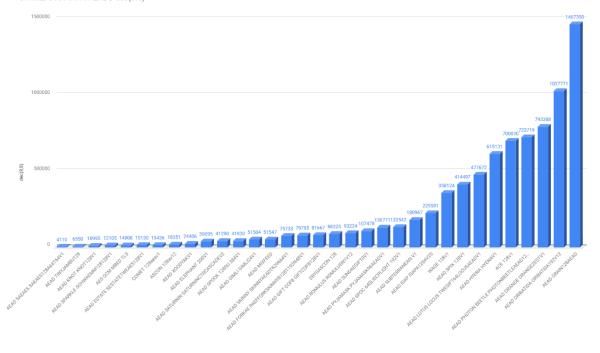




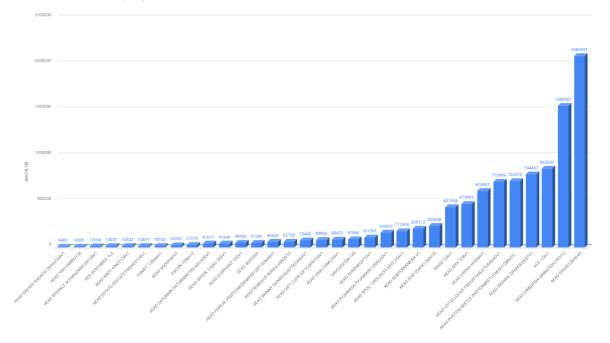




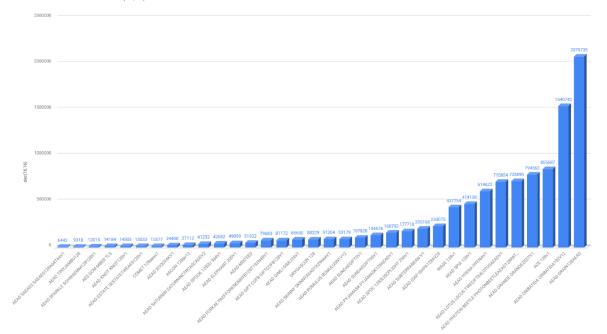




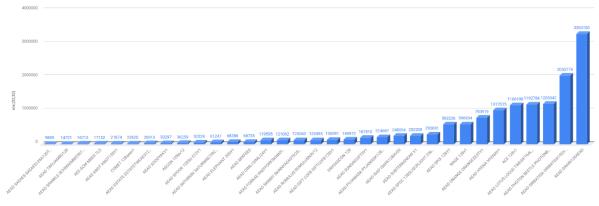




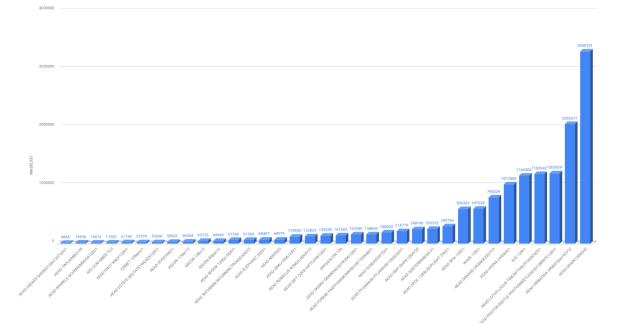




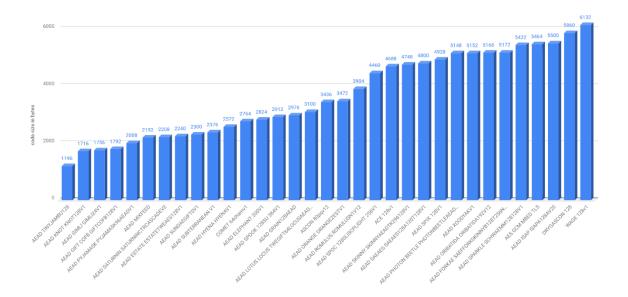
STM32F303VC M4 AEAD / enc(32,32)



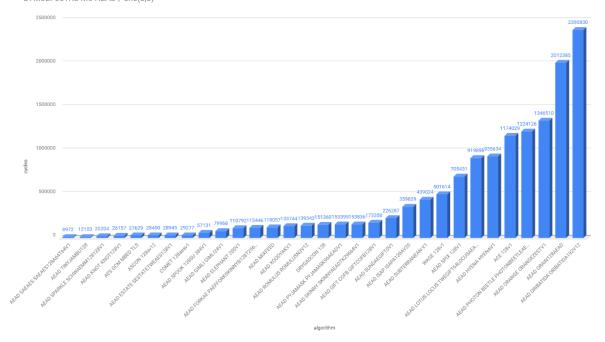
STM32F303VC M4 AEAD / dec(32,32)



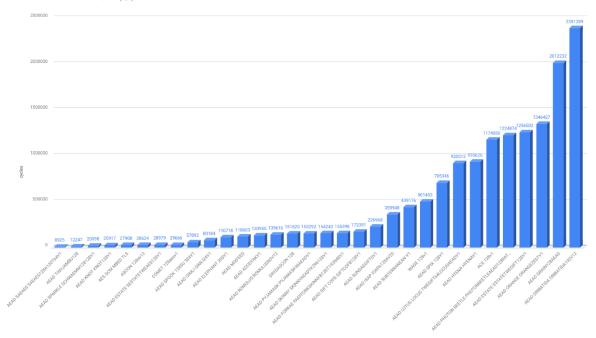




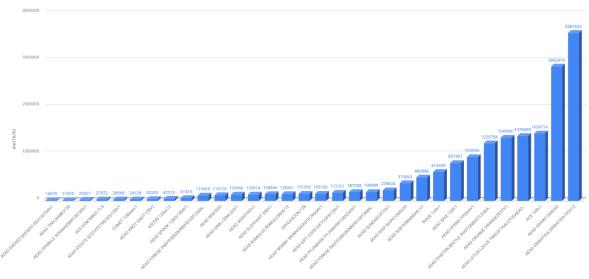
STM32F051R8 M0 AEAD / enc(8,8)



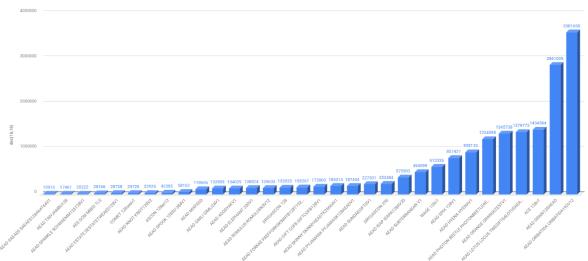
STM32F051R8 M0 AEAD / dec(8,8)



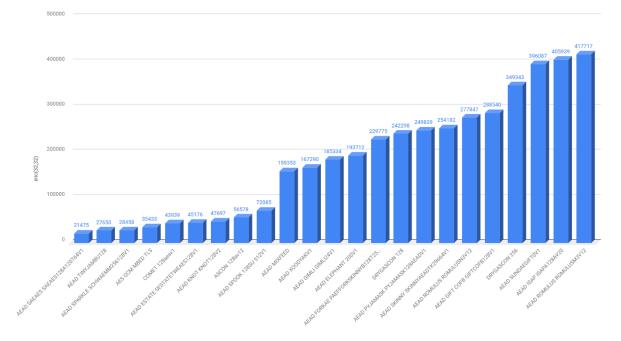
STM32F051R8 M0 AEAD / enc(16,16)



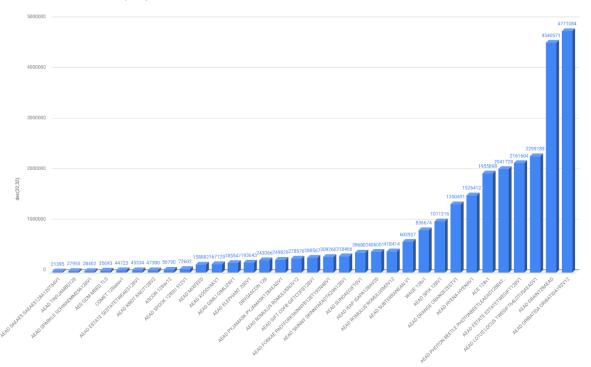
STM32F051R8 M0 AEAD / dec(16,16)



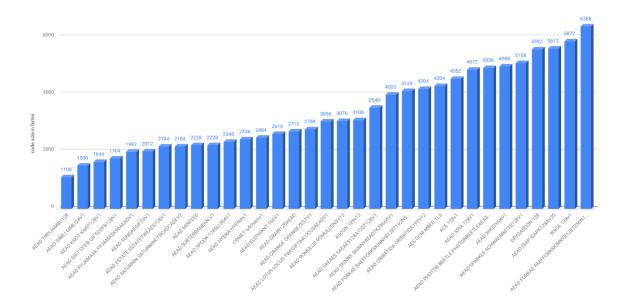
STM32F051R8 M0 AEAD / enc(32,32)



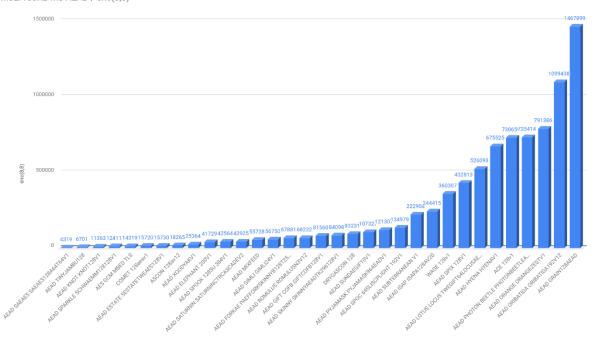
STM32F051R8 M0 AEAD / dec(32,32)



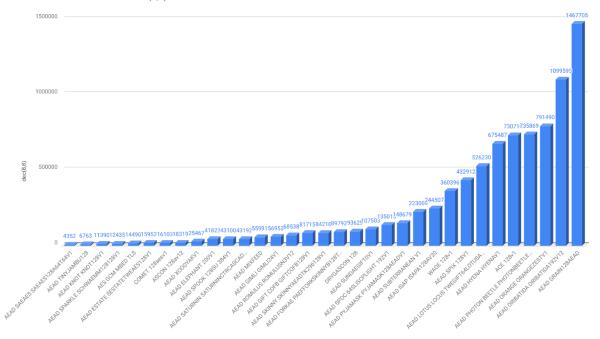




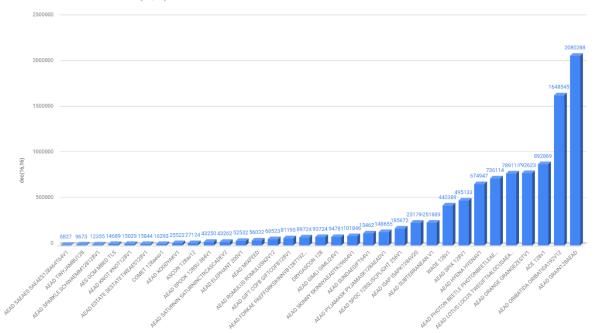
M32f100RB M3 AEAD / enc(8,8)

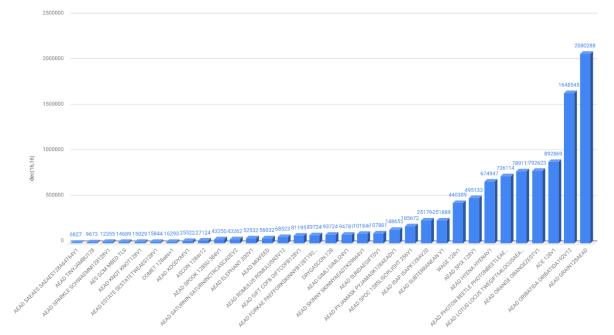


STM32f100RB M3 AEAD / dec(8,8)

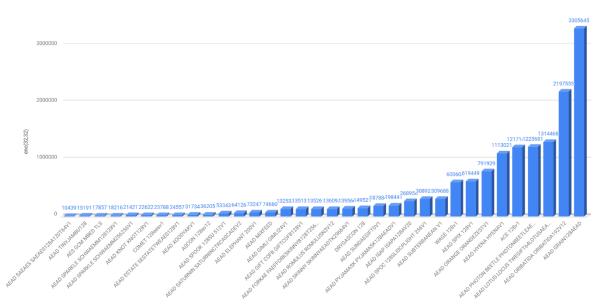


STM32f100RB M3 AEAD / enc(16,16)









STM32f100RB M3 AEAD / dec(32,32)

