Rassul Bairamkulov

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Experience

Postdoctoral scholar — August 2022 – Present
EPFL — *Lausanne, Vaud, Switzerland*

- Developing logic synthesis tools for emerging computing technologies

Intern (Design Automation) — May 2020 – August 2020
Qualcomm Inc. — *Remote – Rochester, New York, USA*

- Automated PCB-level power delivery network layout synthesis in low-power high-performance systems
- Enabled fast PCB prototype generation and comprehensive early power delivery exploration

Intern (Power Integrity) — May 2018 – August 2018
Qualcomm Inc. — *San Diego, California, USA*

- Developed software to optimize power delivery network parameters based on PPA specifications
- Efficient design space exploration for power delivery in high-performance integrated circuits

Research Assistant — June 2017 – June 2022
University of Rochester — *Rochester, New York, USA*

- Developed EDA methodologies and software for VLSI power delivery network design, early system-level exploration, and layout synthesis (funded by Qualcomm)
- Developed algorithms and software for clock distribution network synthesis for Superconductive Rapid Single Flux Quantum integrated circuits (funded by Synopsys)
- Developed Infinity Mirror Technique for fast and accurate analysis of voltage drop within large grids (funded by National Science Foundation)

Teaching Assistant — Fall 2017 – Fall 2022
University of Rochester — *Rochester, New York, USA*

- Graduate-level course `ECE461 "Introduction to VLSI"`

Undergraduate Research Assistant — November 2014 – May 2016
Nazarbayev University — *Astana, Kazakhstan*

- Developed software for minimizing the total harmonic distortion (THD) in multilevel voltage converters

Education

University of Rochester — June 2016 – June 2022
M.S./Ph.D. in Electrical and Computer Engineering — *Rochester, New York, USA*

- Thesis title: *Graph Algorithms for VLSI Power and Clock Networks*

Nazarbayev University — August 2012 – May 2016
B.Eng. in Electrical and Electronic Engineering — *Astana, Kazakhstan*

- Thesis title: *Analysis of Natural Voltage Balancing in Single-Phase Multilevel Power Converters*

Awards

Best Paper Award — October, 2023
IFIP/IEEE Conference on Very Large Scale Integration — *Sharjah, UAE*

- Paper: *Synthesis of SFQ Circuits with Compound Gates* by R. Bairamkulov, A. Tempia Calvino, and G. De Micheli

Best Paper Award Nominee — January, 2024
ACM/IEEE Asia and South Pacific Design Automation Conference — *Incheon, South Korea*

- Paper: *Towards Multiphase Clocking in Single-Flux Quantum Systems* by R. Bairamkulov and G. De Micheli

Service

Technical Program Committee — February-June 2024
ACM/IEEE Design Automation Conference — *San Francisco, CA*

Technical Program Committee — January-March 2024
IEEE Panhellenic Conference on Electronics and Telecommunications — *Thessaloniki, Greece*

Best Paper Award Committee — June 2023
ACM Great Lakes Symposium on VLSI — *Knoxville, TN, USA*

Session Chair — June 2023
ACM Great Lakes Symposium on VLSI — *Knoxville, TN, USA*

Publications

Authored Book

R. Bairamkulov and E. G. Friedman. *Graphs in VLSI*. Springer Nature, Cham, Switzerland, 2023. DOI: 10.1007/978-3-031-11047-4.

Journal Articles

R. Bairamkulov and E. G. Friedman. "Power Aware Placement of On-Chip Voltage Regulators". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2024).

N. Zhuldassov, **R. Bairamkulov**, and E. G. Friedman. "Thermal Optimization of Hybrid Cryogenic Computing Systems". In: *IEEE Transactions on Very Large Scale Integration Systems (in press)* (2024). DOI: 10.1109/TVLSI.2023.3271898.

R. Bairamkulov, A. Roy, M. Nagarajan, V. Srinivas, and E. G. Friedman. "SPROUT—Smart Power Routing Tool for Board-Level Exploration and Prototyping". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 41.7 (July 2022), pp. 2263–2275. DOI: 10.1109/TCAD.2021.3101411.

R. Bairamkulov, T. Jabbari, and E. G. Friedman. "QuCTS -— Single-Flux Quantum Clock Tree Synthesis". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 41.10 (Oct. 2021), pp. 3346–3358. DOI: 10.1109/TCAD.2021.3123141.

R. Bairamkulov and E. G. Friedman. "Effective Resistance of Finite Two-Dimensional Grids Based on Infinity Mirror Technique". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 67.9 (Sept. 2020), pp. 3224–3233. DOI: 10.1109/TCSI.2020.2985652.

R. Bairamkulov and E. G. Friedman. "Effective Resistance of Two-Dimensional Truncated Infinite Mesh Structures". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 66.11 (Nov. 2019), pp. 4368–4376. DOI: 10.1109/TCSI.2019.2933749.

R. Bairamkulov, K. Xu, M. Popovich, J. S. Ochoa, V. Srinivas, and E. G. Friedman. "Power Delivery Exploration Methodology Based on Constrained Optimization". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 39.9 (Sept. 2019), pp. 1916–1924. DOI: 10.1109/TCAD.2019.2925397.

Conference Proceedings

R. Bairamkulov, M. Yu, and G. De Micheli. "Unleashing the Power of T1-cells in SFQ Arithmetic Circuits". In: *Proceedings of the ACM/IEEE Design, Automation and Test in Europe Conference and Exhibition, Valencia, Spain*. Mar. 2024.

N. Zhuldassov, **R. Bairamkulov**, and E. G. Friedman. "Thermal Optimization of Hybrid Cryogenic Computing Systems". In: *Government Microcircuit Applications & Critical Technology Conference (GOMACTech), Charleston, SC*. Mar. 2024.

R. Bairamkulov and G. De Micheli. "Towards Multiphase Clocking in Single-Flux Quantum Systems". In: *Proceedings of the ACM/IEEE Asia South Pacific Design Automation Conference, Incheon, South Korea*. Jan. 2024.

R. Bairamkulov, A. Tempia Calvino, and G. De Micheli. "Synthesis of SFQ Circuits with Compound Gates". In: *Proceedings of the IEEE/IFIP VLSI-SoC Conference*. Oct. 2023.

R. Bairamkulov and G. De Micheli. "Compound Logic Gates for Pipeline Depth Minimization in Single Flux Quantum Integrated Systems". In: *Proceedings of the ACM Great Lakes Symposium on VLSI*. June 2023, pp. 421–425. DOI: 10.1145/3583781.3590287.

R. Bairamkulov, A. Roy, M. Nagarajan, V. Srinivas, and E. G. Friedman. "SPROUT—Smart Power Routing Tool for Board-Level Exploration and Prototyping". In: *Proceedings of the ACM/IEEE Design Automation Conference*. Dec. 2021, pp. 283–288. DOI: 10.1109/DAC18074.2021.9586128.

R. Bairamkulov, E. G. Friedman, A. Roy, M. Nagarajan, and V. Srinivas. "Graph-Based Power Network Routing for Board-Level High Performance Systems". In: *Proceedings of the IEEE International Symposium on Circuits and Systems*. Oct. 2020. DOI: 10.1109/ISCAS45731.2020.9181140.

R. Bairamkulov, K. Xu, E. G. Friedman, M. Popovich, J. S. Ochoa, and V. Srinivas. "Versatile Framework for Power Delivery Exploration". In: *Proceedings of the IEEE International Symposium on Circuits and Systems*. May 2018. DOI: 10.1109/ISCAS.2018.8351478.

R. Bairamkulov, A. Ruderman, and Y. L. Familiant. "Time Domain Optimization of Voltage and Current THD for a Three-Phase Cascaded H-Bridge Inverter". In: *Proceedings of the IEEE International Power Electronics and Motion Control Conference*. Sept. 2016, pp. 227–232. DOI: 10.1109/EPEPEMC.2016.7752002.

Doctoral Dissertation

R. Bairamkulov. "Graph Algorithms for VLSI Power and Clock Networks". PhD thesis. University of Rochester, 2022.