

# Hopping-Transport Mechanism for Reconfigurable Logic in Disordered Dopant Networks

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We present an atomic-scale mechanism based on variable-range hopping of interacting charges enabling reconfigurable logic in dopant network processing units. Kinetic Monte Carlo simulations of the hopping process show temperature-dependent current-voltage characteristics and artificially evolved basic Boolean logic gates in very good agreement with experiment. The simulations provide unique insights into the local electrostatic potential and current flow in the dopant network, showing subtle changes induced by control voltages that set the conditions for the logic operation. These insights will be crucial in the systematic further development of this burgeoning technology for unconventional computing. The establishment of the principles underlying the logic functionality of these devices encourages the exploration and utilization of the same principles in other materials and device geometries.

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## I. INTRODUCTION

Reconfigurable logic [1] exploiting intrinsic complexity and nonlinear behavior of a material system [2–4] offers revolutionary concepts for unconventional computing by “intelligent matter” [5]. Recently, we explored such a concept in dopant network processing units (DNPUs) made by implantation of boron (B) dopants in silicon (Si), where surrounding electrodes define an active region at the Si surface for current flow in between the electrodes. An individual DNPUs can be configured to execute a specific logic task by choosing one or more electrodes as output and other electrodes as inputs or controls. Boolean logic can be realized by applying voltages corresponding to logic levels “0” and “1” to two input electrodes, giving rise to a low (“0”) or high (“1”) current at an output electrode. Voltages applied at control electrodes are adjusted to obtain an optimal Boolean gate fitness, allowing high-fitness configuration of any of the six basic logic gates (AND, OR, NOR, NAND, XOR, XNOR) in one and the same device. The devices can compete with CMOS-based logic on energy efficiency

and footprint, while competitiveness on speed could be achievable. They operate reliably at liquid-nitrogen temperature (77 K) and even operation at room temperature using a backgating technique was shown [6]. Efficient neural network-type computing can be achieved by coupling DNPs in hierarchical structures [7].

The control voltages for realizing a specific logic gate are different for each device and supposedly depend on the specific dopant configuration in the active region. From the estimated B concentration at the Si surface of the order of  $5 \times 10^{17} \text{ cm}^{-3}$  and the implantation penetration depth of about 20 nm [6], we estimate that a few hundred dopant atoms are present in the active area of about 300 nm in diameter. Functionality can be realized by artificial evolution, where the control voltages are treated as “genes” that evolve by mutation and cross-breeding in an evolutionary process to optimize fitness for the desired functionality [6,8]. Alternatively, a deep neural network can be trained to accurately emulate the complex multidimensional input-output relationship of a device, after which a desired functionality is established by gradient descent [9]. Both approaches are physics agnostic, i.e., they do not assume a specific physical mechanism for the device operation and therefore cannot shed light on the underlying

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mechanism. To understand the reconfigurable logic operation of DNPUs and pave the way for its further deployment, we explore in this work the atomic-scale mechanism underlying the operation.

In Sec. II we describe the atomic-scale kinetic Monte Carlo method used to simulate the operation of the DNPUs. In Sec. III we show that simulated current-voltage characteristics of the DNPUs are very similar to measured characteristics, using reasonable simulation parameters. In Sec. IV we demonstrate the artificial evolution of Boolean logic in the simulated DNPUs in a similar way as in experiment. In Sec. V we show the current and voltage distributions inside the simulated DNPUs, which provide the basis of an analysis of their operational principles. We end in Sec. VI with a detailed analysis of these operational principles, followed by a summary and conclusions.

## II. SIMULATION METHOD

The suggested atomic-scale mechanism for the operation of the DNPUs is based on variable-range hopping (VRH) of electrons in between the dopants, which can occur in the neutral ( $B^0$ ) or ionized ( $B^-$ ) state. The applicable rate for phonon-assisted electron hopping between two dopants  $i$  and  $j$  at a mutual distance  $r_{ij}$  is the Miller-Abrahams (MA) rate  $\Gamma_{ij} = v_0 \exp(-2r_{ij}/a) \min[1, \exp(-\Delta E_{ij}/k_B T)]$ , where  $\Delta E_{ij}$  is the total energy change when the electron hops and  $k_B T$  is the thermal energy [10]. For the hopping prefactor, we take a typical phonon frequency  $v_0 = 10^{12} \text{ s}^{-1}$ , determining the absolute current scale. For the wave function decay length, we take  $a = 5 \text{ nm}$ , the approximate Bohr radius of a  $p$ -type dopant like B in Si. The hopping process is simulated by a standard rejection-free kinetic Monte Carlo (KMC) algorithm that considers at each step all possible electron hops. All Coulomb interactions between charges are taken into account. Simulation of frequent back-and-forth hops of electrons between nearby dopants (“rattling”) consumes CPU time while such hops do not contribute to the current. We therefore excluded hops with  $r_{ij} < 1.5$  and checked that this has no relevant influence on the results.

The upper inset of Fig. 1 shows the geometry of a representative simulated device with eight electrodes. The dots indicate 200 randomly placed B dopants. We replace the tip-shaped electrodes in the experiment [6] by circular segments. This avoids singularities in the electrostatic potential. The functionality of a device is a joint effect of the voltages applied to all electrodes, governed by processes taking place in an effective region in the interior of the device and not close to the electrodes. We therefore expect the particular way in which the electrodes are modeled to be of minor importance. We take 150 nm for the diameter of the effective region (half the diameter of the active region in the experiment). In this way we also keep the number of dopants feasible for the simulations.

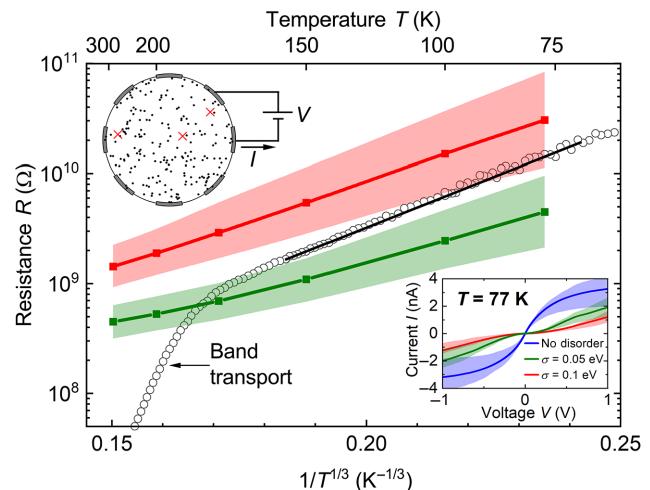


FIG. 1. Upper inset: geometry of a simulated device with segmented electrodes and 200 randomly positioned dopants (dots) and three counterdopants (red crosses). Lower inset: simulated current  $I$  as a function of voltage  $V$  at  $T = 77 \text{ K}$  averaged over eight adjacent electrode combinations of 30 devices, without energy disorder (blue) and with energy disorder strengths  $\sigma = 0.05$  (green) and  $0.1 \text{ eV}$  (red). Half of the  $I$ - $V$  characteristics fall in the shaded regions. Main panel: geometrically averaged resistances  $R$  for  $\sigma = 0.05$  and  $0.1 \text{ eV}$  as a function of  $1/T^{1/3}$ , obtained from the linear parts of the  $I$ - $V$  characteristics in the lower inset around  $V = 0$ . Half of the resistances fall in the shaded regions. The circles denote measured resistances [6]; the line denotes the linear fit to the experimental results in the region 70–160 K.

We randomly place three counterdopants (red crosses) in the effective region, corresponding to a typical background doping of about  $10^{16} \text{ cm}^{-3}$  in the experimentally used Si wafers. We assume that the counterdopants are ionized and thus positively charged.

The ionization energy of a B dopant depends on its random distance to the Si surface and possibly other random fluctuations in its environment. We model these fluctuations by a Gaussian energy disorder in the dopant ionization energy with standard deviation  $\sigma$ . For specified voltages applied to the eight electrodes, we solve the Laplace equation for the electrostatic potential with a finite-element method [11]. We use a relative dielectric constant  $\epsilon_r = 12$  in the Coulomb interactions between the charges, which is close to the value of 11.7 for silicon. Altogether this fixes  $\Delta E_{ij}$  in the MA rate. For hops in between dopants and electrodes, we also use the MA rate, where  $r_{ij}$  is then taken to be the distance between a dopant and the middle of a circular segment. The voltages applied to the electrodes are accounted for in  $\Delta E_{ij}$ . Starting from a neutral system where the number of mobile electrons in the system is equal to the number of counterdopants,  $10^4$  KMC steps are sufficient to reach a steady-state current for all considered voltage combinations. Unless stated otherwise,

we determine the current from a certain (arbitrarily) chosen output electrode to ground in a time interval corresponding to  $10^7$  KMC steps and the statistical uncertainty from the current fluctuations in 100 equally long subintervals.

### III. CURRENT-VOLTAGE CHARACTERISTICS

The curves in the lower inset of Fig. 1 are the averaged simulated currents  $I$  at a temperature  $T = 77$  K of the device displayed in the upper inset and 29 other devices with different positions of the (counter)dopants, when applying a voltage  $V$  between two adjacent electrodes. The average includes the eight possible adjacent electrode combinations for each device. The results can be compared to the device characterization measurements in Ref. [6]. For the case without energy disorder (blue), the current saturates with growing voltage, leading to sublinear instead of the experimentally observed superlinear  $I$ - $V$  curves. The reason for the saturation is that, for energetically downward hops, which dominate the transport at high electric field, the MA rate has no energy dependence. Introducing energy disorder yields the observed superlinear curves on a voltage and current scale comparable to the experiment. We show results for  $\sigma = 0.05$  eV (green) and 0.1 eV (red). Half of the simulated 240  $I$ - $V$  characteristics fall in the shaded regions, which quantifies the device-to-device variability. Since different Si wafers may have different background doping concentrations, we checked the effect of a change in the number of counterdopants. An increase in this number leads to only a small increase in the current because the number of mobile charges present in the system is mostly determined by injection from the electrodes and not by the number of counterdopants; see Fig. 5 in Appendix A. In the main panel of Fig. 1 we plot for  $\sigma = 0.05$  and 0.1 eV the geometric average [12] of the resistances  $R$ , extracted from the linear parts of the simulated  $I$ - $V$  characteristics around  $V = 0$ , versus  $T^{-1/3}$ . The almost straight lines in the semilogarithmic plots suggest the applicability of VRH in  $d = 2$  dimensions, yielding  $R(T) = R_0 \exp[(T_0/T)^{1/(1+d)}]$  [13]. Also plotted (circles) is the  $T$ -dependent resistance in the measurements of Ref. [6] for an adjacent electrode combination of one device. Above about 160 K, the experimental resistance starts to deviate from VRH behavior, which is attributed to the onset of band conduction due to thermal dopant ionization [6], not taken into account in the simulations. We note that the studied temperature window is too small to distinguish the temperature dependence from Coulomb gap behavior  $R(T) = R_0 \exp[(T_0/T)^{1/2}]$  [14], but irrespective of the correct theoretical description we conclude that the simulated results are in reassuring agreement with experiment.

The temperature at which the experimentally observed transition from hopping to band transport occurs yields an estimated effective ionization energy of 130 meV [6], instead of the 45 meV ionization energy of B in bulk Si

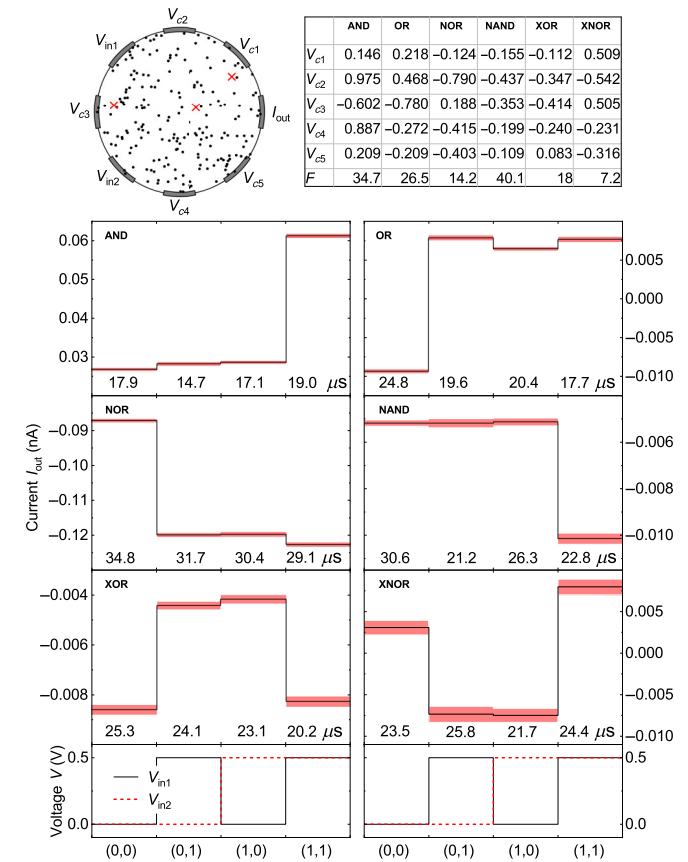


FIG. 2. Top left: simulated device (same as in Fig. 1) with input voltages  $V_{\text{in}1}$  and  $V_{\text{in}2}$ , control voltages  $V_{c1}$ – $V_{c5}$ , and output current  $I_{\text{out}}$ . Middle panels:  $I_{\text{out}}$ , uncertainties (shaded regions), and time intervals for which these are determined, for the six basic Boolean logic gates found with artificial evolution at 77 K, with  $V_{\text{in}1}$ ,  $V_{\text{in}2}$  given in the bottom panels and  $V_{c1}$ – $V_{c5}$  and fitnesses  $F$  in the table at the top right.

[15,16]. The difference is attributed to the reduced dielectric screening of the Coulomb interaction at the Si surface. Since the distance of the B dopants to the Si surface will vary between dopants, so will their ionization energy. Disorder strengths of the order of the difference between the experimentally estimated and bulk ionization energy are therefore expected, which holds for the two considered disorder strengths. We henceforth take  $\sigma = 0.1$  eV as a realistic estimate of the disorder strength, because the slope of the corresponding resistance results (red line in the main panel of Fig. 1) agrees better with experiment than for  $\sigma = 0.05$  eV (green line). Multiplying the only approximately known hopping prefactor  $v_0$  by a factor 2 would lead for  $\sigma = 0.1$  eV to an almost perfect agreement with experiment below 160 K.

### IV. BOOLEAN FUNCTIONALITY

As in the experiment, we obtain Boolean functionality at 77 K by optimizing a fitness function  $F$  for each logic

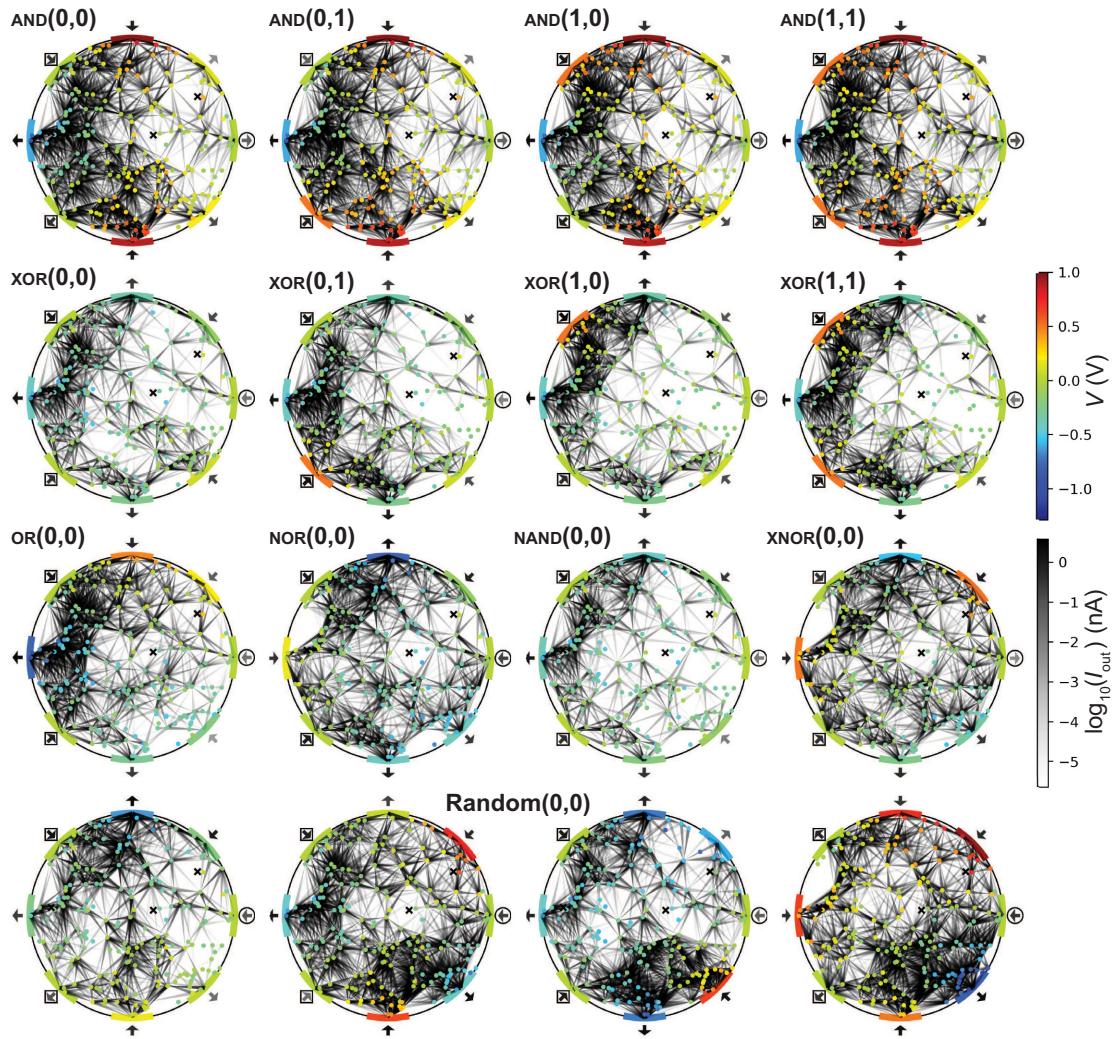


FIG. 3. Time-averaged voltages (linear color scale) and currents (logarithmic gray scale, current direction from wide to narrow) in the device, for the simulations in Fig. 2. Arrows with different gray scale denote currents flowing into or out of the electrodes. Squares denote input electrodes. The circle denotes the output electrode. First row: AND gate for the four different logic input combinations. Second row: XOR gate. Third row: OR, NOR, NAND, and XNOR gates for logic input (0, 0). Fourth row: four random control voltages in the interval  $[-1, 1]$  V for logic input (0, 0).

gate, where two voltages  $V_{\text{in}1}$  and  $V_{\text{in}2}$  can take on the values 0 V (logic “0”) and 0.5 V (logic “1”), and the current  $I_{\text{out}}$  to ground (0 V) is measured at an output electrode. Motivated by the application perspective, the used fitness function is only sensitive to relative current differences and not to the absolute current scale. The optimization occurs by artificial evolution of the control voltages  $V_{c1}-V_{c5}$  of the five remaining electrodes using an evolutionary algorithm comparable to that in Ref. [6]; see Appendix B. The control voltages are referred to as the “genes” and are restricted to lie in the interval  $[-1, 1]$  V. At the top left of Fig. 2 the model device shown in Fig. 1 is reproduced, indicating the input, output, and control electrodes. Examples of artificially evolved control voltages for the six basic Boolean logic gates and their gate fitnesses  $F$  are given in the table at the top right. The panels underneath show  $I_{\text{out}}$  for the

different logic input combinations, displayed in the bottom panels. The shaded regions indicate the uncertainty in  $I_{\text{out}}$ . We find very good global agreement with the gates reported in the experiment [6]. This holds for the quality (fitness) of the gates as well as the approximate magnitude of the currents, with in both cases maximum values of the order of 0.1 nA.

We note that it is to a large extent arbitrary which electrodes are used for input, output, and control. It may be advantageous when the input electrodes are not adjacent to the output electrode or each other, because the control voltages can then more effectively influence the output current differences for the different inputs. This is the case for the electrode choices in Fig. 2. We also note that there is nothing special or specifically suitable to the device of Fig. 2. Figure 6 in Appendix C shows the realization of

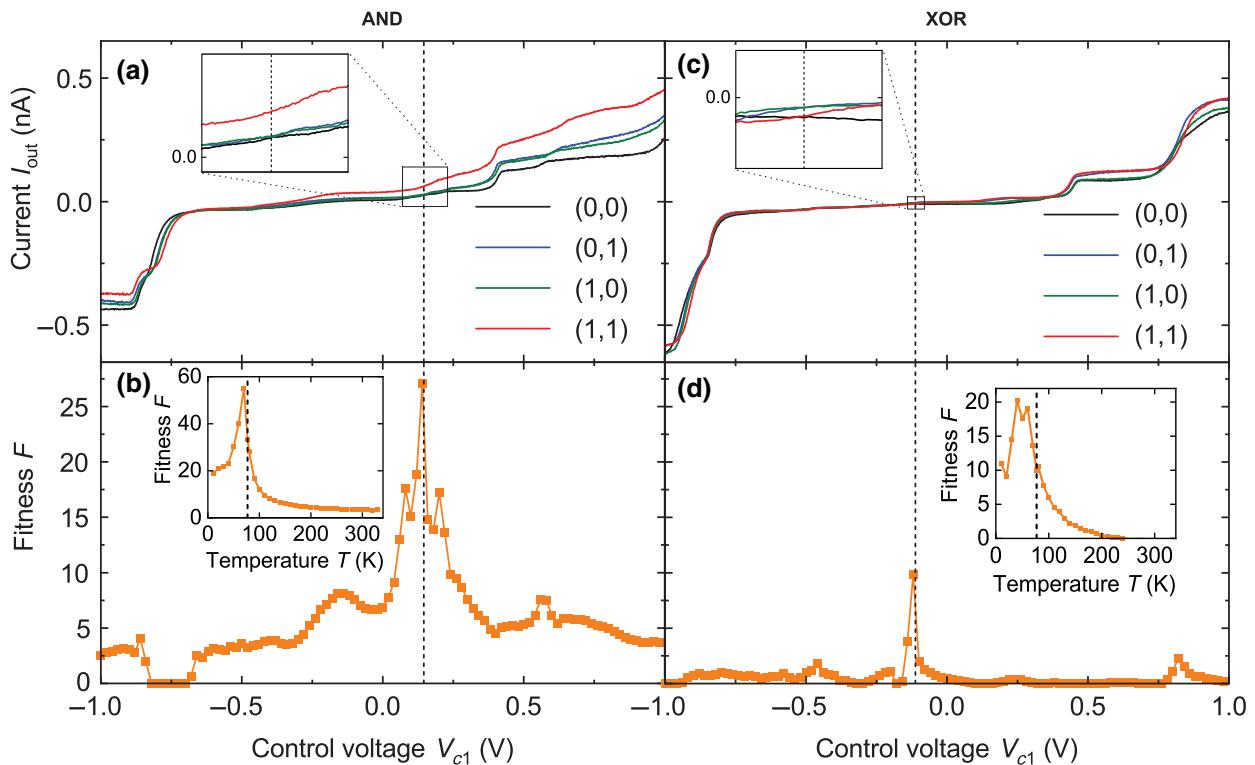


FIG. 4. (a) Output currents  $I_{\text{out}}$  for the four logic input combinations and (b) fitness  $F$  of the AND gate of Fig. 2 as a function of the control voltage  $V_{c1}$ . Vertical dashed lines in (a) and (b) denote the values of  $V_{c1}$  found by artificial evolution. Inset in (a): magnification of indicated area. Inset in (b): temperature dependence of  $F$  for the control voltages found by artificial evolution at 77 K (vertical dashed line). Panels (c) and (d) are the same as (a) and (b), but for the XOR gate.

the six basic logic gates in a device with other random positions of the (counter)dopants. Gates with good fitness can in principle be evolved for any device, as also found experimentally [6].

The  $10^7$  KMC steps used to obtain the results in Fig. 2 correspond to time intervals in the range 15–35  $\mu\text{s}$  (the precise values are indicated in Fig. 2). This is more than 4 orders of magnitude shorter than the 0.5 s used in the experiment [6]. In the simulations, the uncertainty in the current is the cumulative effect of stochastic hopping events of single electrons. During the measurement time of 0.5 s considerable fluctuations in the experimental current are observed, which are much larger than the fluctuations in the KMC simulations on this time scale. This indicates that in the experiment the noise in the current is not the intrinsic noise due to individual hopping events but extrinsic noise of the measurement equipment. If the noise can be suppressed to the intrinsic noise level, much shorter experimental measurement times should be possible. We verified (see Fig. 7 in Appendix D) that the uncertainty in the simulated current scales as  $1/\sqrt{N}$  with the number  $N$  of KMC steps for time scales exceeding the used equilibration time ( $10^4$  KMC steps), which demonstrates that the intrinsic noise is uncorrelated at these time scales. Obviously, if the statistical uncertainty becomes too large,

it will become impossible to distinguish the different logical current levels. In the case of the XNOR gate in Fig. 2, for which the uncertainty in the current is largest, it will become impossible to distinguish the different current levels if the uncertainty is increased by approximately a factor 5. Dividing the corresponding time intervals in Fig. 2 by a factor  $5^2 = 25$ , we obtain time intervals of the order of 1  $\mu\text{s}$  for which the current levels will no longer be distinguishable. This corresponds to a maximum DNPUs operational frequency of approximately 1 MHz, relevant when DNPUs are combined with optimized peripheral electronics introducing negligible extrinsic noise.

## V. CURRENT AND VOLTAGE DISTRIBUTIONS

The simulations provide unique microscopic information about the local potential and current flow within the device that is impossible to obtain experimentally. Figure 3 shows, for the same device and Boolean gate realizations as in Fig. 2, the voltages applied at the electrodes and the time-averaged voltages and currents in the dopant network. The total currents flowing into or out of the electrodes are also shown. The first and second rows show results for the AND and XOR gates, as respective examples of gates solving linearly separable problems (the others are OR, NOR

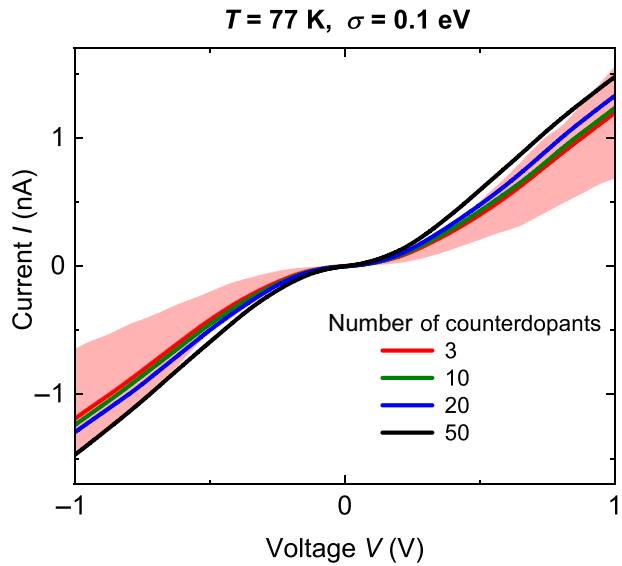


FIG. 5. Simulated  $I$ - $V$  characteristics at 77 K and energy disorder strength  $\sigma = 0.1$  eV, averaged over the eight neighboring electrode combinations of 30 devices with different numbers of counterdopants. The result for three counterdopants is the same as in Fig. 1 (lower inset), where half of the 240  $I$ - $V$  characteristics fall in the shaded red region.

and NAND gates) and inseparable problems (the other is the XNOR gate) [3,4,17]. Results are given for the logic input combinations  $(0, 0)$ ,  $(0, 1)$ ,  $(1, 0)$ , and  $(1, 1)$ . We observe that the differences in the voltage and current distributions between the four different input combinations are for both gates remarkably small, while the differences in between the AND and XOR gates are comparatively large. The third row shows results for the OR, NOR, NAND, and XNOR gates; in these cases only for the  $(0, 0)$  input. We also verified that for these gates the differences in the voltage and current distributions between different input combinations are small. The fourth row shows results for four randomly chosen control voltages in the interval  $[-1, 1]$  V for  $(0, 0)$  input. Results for 16 other randomly chosen control voltages are given in Fig. 8 in Appendix E. We observe that, in general, the output currents for the control voltages found for the Boolean gates are smaller than those for random control voltages. For example, the average of  $|I_{\text{out}}|$  for the logic gates in Fig. 3 is 0.023 nA for  $(0, 0)$  input, while the average is 0.174 nA for the random control voltages.

## VI. ANALYSIS, SUMMARY, AND CONCLUSIONS

These observations suggest an explanation for the realization of Boolean functionality by the evolutionary algorithm that has two ingredients. (1) The evolutionary algorithm tends to tune the control voltages such that the output current is small for all input combinations, thus creating for all gates a strong dependence of the fitness  $F$  on the control voltages. (2) For the specific gate found by the

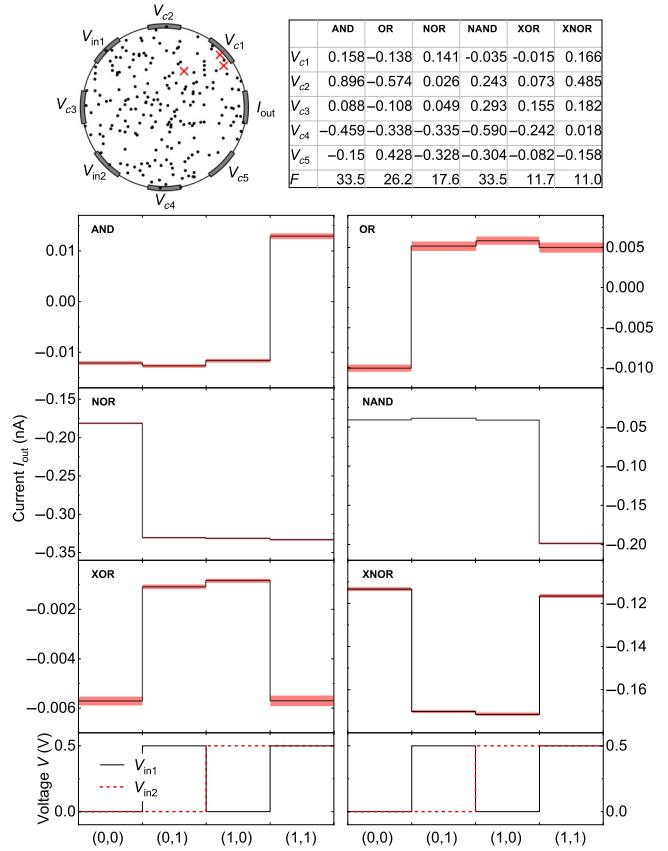


FIG. 6. Boolean functionality at 77 K as found by artificial evolution in the device shown at the top left, which is different from that in Fig. 2. The control voltages  $V_{c1}$ – $V_{c5}$  and fitnesses  $F$  are given in the table at the top right.

evolutionary algorithm, this strong dependence happens to be such that a particularly high  $F$  is realized by subtly tuned control voltages. The nonlinearity, complexity, and flexibility of the DNPUs allow a high-fitness realization of all Boolean logic gates in one and the same device. Interestingly, there is no obvious correlation between a particular gate and its voltage and current distribution, as shown by the completely different voltage and current distributions for another device in Fig. 9 in Appendix F. Also, for the hopping dynamics in other disordered systems, it has been found that the total current in the nonlinear regime does not need to be related to some obvious pattern of the current distribution [18].

The explanation suggested above is corroborated by a study of the output currents  $I_{\text{out}}$  for the four logic input combinations and the resulting gate fitness  $F$  when changing a control voltage from the value found by artificial evolution. In Fig. 4  $I_{\text{out}}$  is shown for the AND and XOR gates when changing the control voltage  $V_{c1}$  while keeping the other control voltages fixed. At the values of  $V_{c1}$  found by the evolutionary algorithm (vertical dashed lines; values as in Fig. 2) all four output currents are small, as is clear from

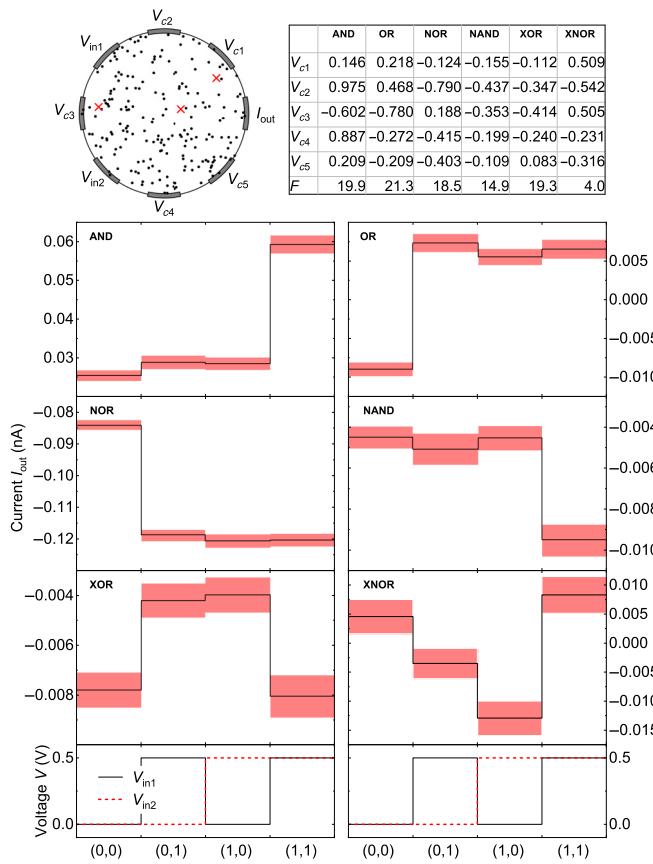


FIG. 7. Same as in Fig. 2, but with currents and uncertainties determined for  $10^6$  instead of  $10^7$  KMC steps. The control voltages  $V_{c1}\text{--}V_{c5}$  are unchanged.

Figs. 4(a) and 4(c). As a result, changes in the voltages of the input electrodes can have a large relative influence on the output current, despite the fact that these electrodes are further away from the output electrode than the adjacent electrode to which  $V_{c1}$  is applied. The strong correlation in the output currents for the four logic input combinations observed in Figs. 4(a) and 4(c) is a general feature that is confirmed in Fig. 10 in Appendix G for random control voltages. Tuning  $I_{\text{out}}$  to be small is therefore crucial for high gate fitness.

By comparing the heights as well as the widths of the peaks in Figs. 4(b) and 4(d) we conclude that it is much easier to realize a good AND gate than a good XOR gate. This is understandable, because the negative differential resistance (NDR) required for the XOR gate to obtain a decreasing current when switching from the logic input  $(0, 1)$  or  $(1, 0)$  to the logic input  $(1, 1)$  is a subtle feature. By contrast, the AND gate does not require NDR. We note that stochastic fluctuations in the current lead to fluctuations in the fitness values, which are most clearly visible around the peak in Fig. 4(b). Figure 11 in Appendix H shows results equivalent to Fig. 4 for the output currents

for the four logic input combinations and the resulting AND and XOR gate fitnesses when changing  $V_{c2}$  or  $V_{c3}$ . Because the corresponding electrodes are further away from the output electrode than the electrode of  $V_{c1}$ , the output currents are in that case less influenced by the control voltage. Results for changing  $V_{c4}$  ( $V_{c5}$ ) are qualitatively similar to those for changing  $V_{c2}$  ( $V_{c1}$ ) because of symmetry (see the electrode labeling of the device at the top left in Fig. 2).

The insets in Figs. 4(b) and 4(d) show the  $T$  dependence of the fitness of the AND and XOR gates, respectively, when the control voltages  $V_{c1}\text{--}V_{c5}$  are fixed to their values found by artificial evolution at  $T = 77$  K. The results are qualitatively similar to those in Ref. [6] (in that case for a NAND gate):  $F$  first slightly increases with decreasing  $T$  and then decreases, while with increasing temperature  $F$  decreases monotonically. We rationalize this as follows. A large positive or negative change in  $T$  substantially modifies the relative hopping rates and thus the system response. The high fitness of a gate realized at 77 K is then expected to decrease substantially (adapted control voltages would be required to reestablish the high fitness). With increasing  $T$ , the nonlinearity and therefore the ability of the device to perform logic gradually disappears. With decreasing  $T$ , however, the nonlinearity increases, counteracting the concomitant loss in fitness, which can lead to an initial increase of fitness before a final decrease.

In summary, we have presented and simulated an atomic-scale mechanism for reconfigurable logic in DNPUs in silicon that is based on variable-range hopping of interacting charge carriers. We demonstrated artificial evolution of the six basic logic Boolean gates in very good agreement with experiment. The simulations provide a unique visualization of the voltage and current distributions in the devices, revealing an intricate operation mechanism where subtle changes induced by control voltages set the conditions for the logic operation. Our findings are crucial for a rational improvement of DNPUs and the revealed operation mechanism could also help exploit complex behavior in other disordered material systems for realizing functionality.

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## APPENDIX A: INFLUENCE OF THE NUMBER OF COUNTERDOPANTS

Figure 5 shows averaged current-voltage ( $I\text{-}V$ ) characteristics comparable to the lower inset of Fig. 1 for  $\sigma = 0.1$  eV, but for larger numbers of counterdopants. The

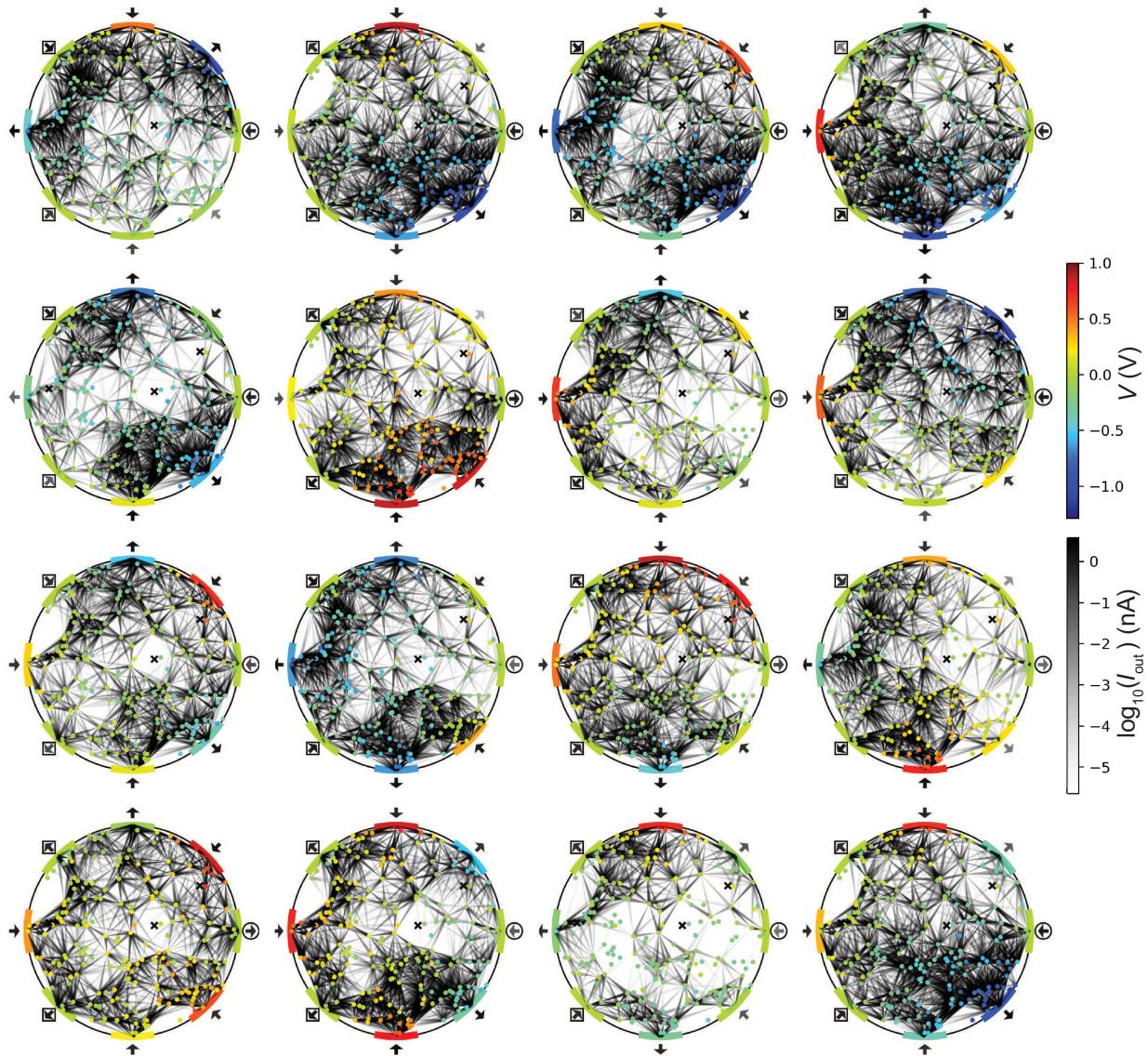


FIG. 8. Voltages and currents for the device of Fig. 2 with 16 random control voltage combinations in the interval  $[-1, 1]$  V and  $(0, 0)$  input.

result for three counterdopants from Fig. 1 is reproduced. The averaged  $I$ - $V$  characteristic for 50 counterdopants (black line) still falls in the shaded region for three counterdopants. We conclude from this that the dependence of the  $I$ - $V$  characteristics on the number of counterdopants is relatively weak. Analysis shows that the number of mobile charge carriers is predominantly determined by the charge carriers injected from the electrodes and not by the number of counterdopants.

## APPENDIX B: ARTIFICIAL EVOLUTION OF BOOLEAN GATES

The six basic Boolean gates in Fig. 2 are found by artificial evolution, where the control voltages  $V_{c1}$ – $V_{c5}$  are the “genes” that are evolved to optimize a fitness  $\tilde{F}$  =

$$F_0 - 2u_F,$$

$$F_0 = 1 - \frac{1}{4} \sum_{V_{in1}, V_{in2}} \left| G(V_{in1}, V_{in2}) - \frac{I_{out}(V_{in1}, V_{in2}) - I_{out}^{\min}}{I_{out}^{\max} - I_{out}^{\min}} \right| + 0.05 \frac{I_{out}^{\max} - I_{out}^{\min}}{\max(|I_{out}^{\max}|, |I_{out}^{\min}|)} \quad (B1)$$

with

$$\begin{aligned} I_{out}^{\max} &\equiv \max_{V_{in1}, V_{in2}} I_{out}(V_{in1}, V_{in2}), \\ I_{out}^{\min} &\equiv \min_{V_{in1}, V_{in2}} I_{out}(V_{in1}, V_{in2}). \end{aligned} \quad (B2)$$

Here,  $G(V_{in1}, V_{in2}) \in \{0, 1\}$  is the output of the logic gate searched for and  $u_F$  is the statistical uncertainty in  $F_0$ ,

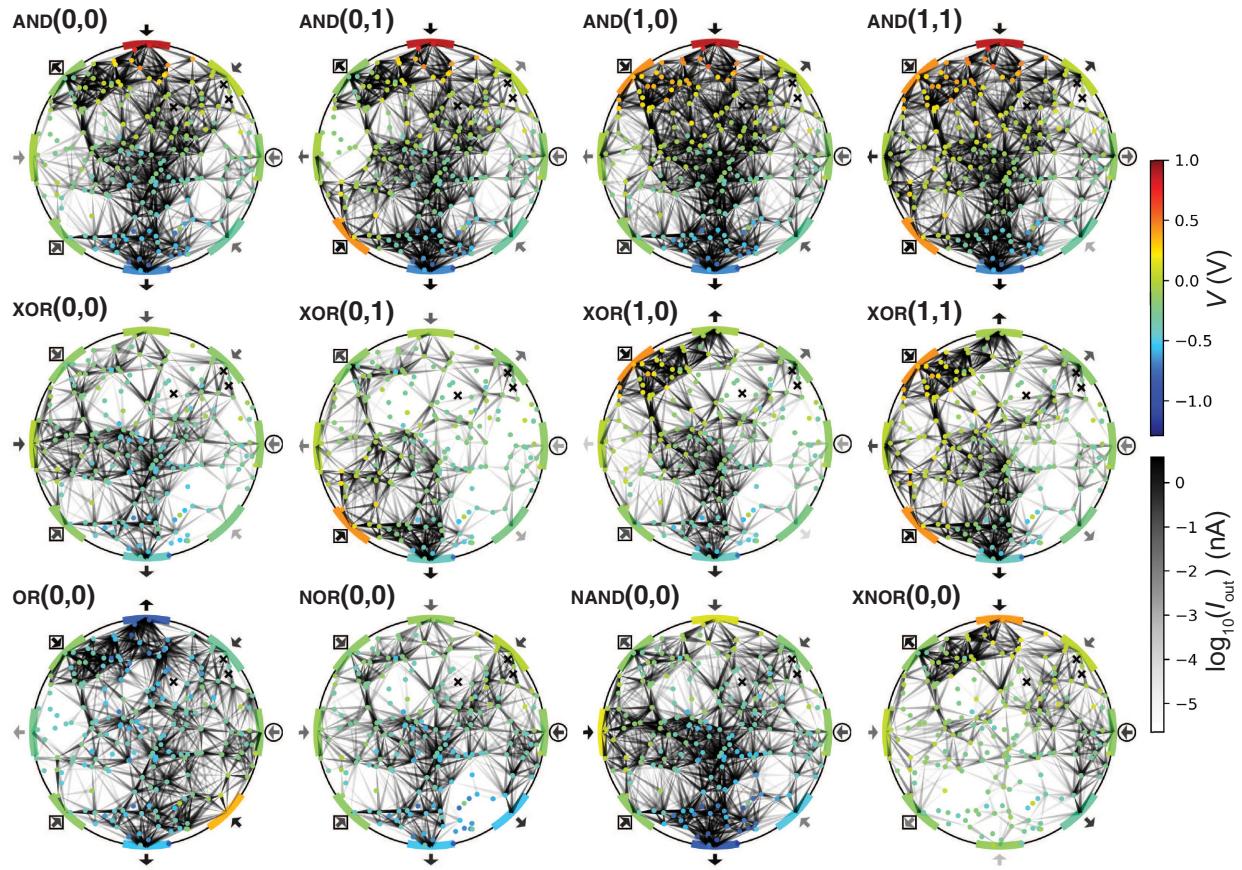


FIG. 9. Voltages and currents for the device of Fig. 6. First row: AND gate for the four logic input combinations. Second row: XOR gate. Third row: OR, NOR, NAND, and XNOR gates with (0, 0) input.

which follows from the individual statistical uncertainties in the four currents  $I_{\text{out}}(V_{\text{in}1}, V_{\text{in}2})$ , where  $V_{\text{in}1}$  and  $V_{\text{in}2}$  can be either 0 or 0.5 V. By subtracting  $2u_F$  from  $F_0$  we avoid spurious high fitnesses occurring as a result of statistical fluctuations in the current. The following genetic algorithm is used in the artificial evolution of each gate.

1. *Initial generation.* The initial generation of “genomes” consists of 25 control voltage combinations  $V_{c1}\text{--}V_{c5}$ , randomly generated from a uniform distribution on the interval  $[-1, 1]$  V.

2. *Evaluate fitness.* For each genome and each input voltage combination, the four currents and their uncertainties are obtained from KMC simulations with a variable number of steps (see below), after an equilibration of  $10^4$  KMC steps. The fitness  $\tilde{F} = F_0 - 2u_F$  is evaluated for each genome. The genomes  $G_k^l$  ( $k = 1, \dots, 25$ ) of a generation  $l$  are ordered according to decreasing fitness.

3. *Next generation.* A new generation of 25 genomes  $G_k^{l+1}$  is generated in the following way.

(a) *Genomes 1–5:* the five fittest genomes of the previous generation,  $G_1^{l+1} = G_1^l, \dots, G_5^{l+1} = G_5^l$ .

(b) *Genomes 6–10:* the five fittest genomes of the previous generation, with slightly adjusted control voltages

(genes), randomly chosen from the interval  $[V_{ci}(G_k^l) - 0.05V, V_{ci}(G_k^l) + 0.05V]$ , where  $V_{ci}(G_k^l)$  is the previous control voltage (gene). This allows random exploration in the vicinity of the current elite genomes.

(c) *Genomes 11–15:* the next five genomes are generated by performing crossover between the fittest and next fittest genome with a 50% chance. If the control voltages of  $G_1^l$  are  $V_{c1}(G_1^l), \dots, V_{c5}(G_1^l)$  then  $V_{ci}(G_{11}^{l+1})$  is either  $V_{ci}(G_1^l)$  or  $V_{ci}(G_2^l)$ , both with 50% probability. Similarly,  $V_{ci}(G_{12}^{l+1})$  is either  $V_{ci}(G_2^l)$  or  $V_{ci}(G_3^l)$ , both with 50% probability, etc.

(d) *Genomes 16–20:* the next five genomes are generated by performing crossover between the five fittest five genomes and five random genomes. So,  $G_{16}^{l+1}$ , for instance, is a crossover between  $G_1^l$  and a random genome.

(e) *Genomes 21–25:* the last five genomes are completely randomly generated.

Additionally, each gene (control voltage) has a 10% chance of mutating. If a gene mutates, its new value is drawn from a triangular distribution between  $-1$  and  $1$  V around its old value.

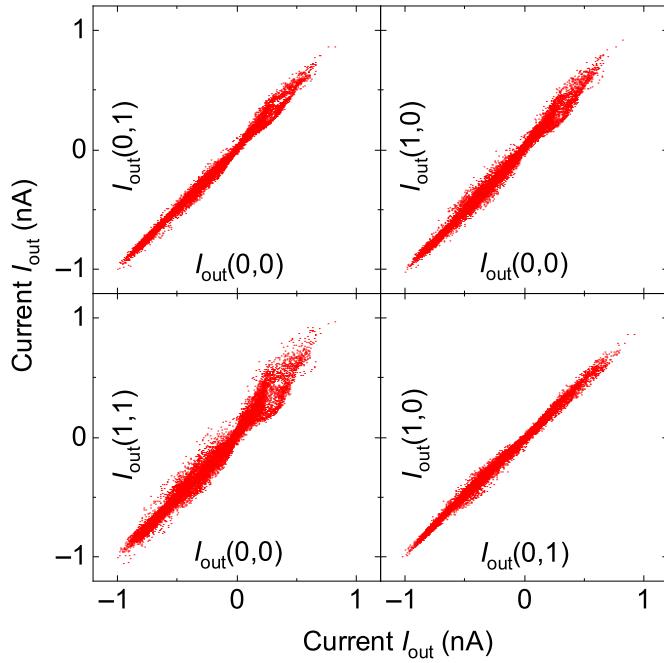


FIG. 10. Correlations between current outputs of the device of Fig. 2 for logic inputs  $(0, 0)$ ,  $(1, 0)$ ,  $(0, 1)$ , and  $(1, 1)$ , and about 20 000 random combinations of the control voltages  $V_{c1}–V_{c5}$  in the interval  $[-1, 1]$  V.

4. *Iterate until convergence.* Repeat steps 2 and 3 until a sufficiently high fitness value is obtained.

For a randomly chosen initial generation and for a given gate, the genetic algorithm is run for a fixed CPU time (of the order of one week on eight threads). Initially, the current is determined from  $10^5$  KMC steps. To reduce the statistical uncertainty in the current, the number of KMC steps is doubled as soon as  $F_0 + u_F > 1$  for the best gate during the artificial evolution. This doubling is applied for a maximum of 10 times. Each run is repeated 20 times with different initial conditions. Finally, based on these runs for each gate the realization of control voltages, yielding a particular high fitness value, is selected for Fig. 2. To obtain the actually shown currents and uncertainties in Fig. 2 for these control voltages, an additional KMC simulation with  $10^7$  steps is performed after an equilibration of  $10^4$  steps. Figure 2 shows the currents for the best gates found after the 20 runs of the genetic algorithm.

The fitness function  $F$  used in the final analysis of the results is similar to that of Refs. [6] and [8], and is defined as

$$F = \frac{m}{\sqrt{r_{ss}} + k|C|}, \quad (B3)$$

where  $m$  and  $C$  are fit parameters of a linear fit  $I_{\text{out}}(V_{\text{in}1}, V_{\text{in}2}) = mG(V_{\text{in}1}, V_{\text{in}2}) + C$ . Here,  $r_{ss}$  is the mean squared error of the linear regression. The constant  $k$  is

set to 0.01, as in the experiments [6,8]. A finite value of  $k$  awards a large relative separation of the high and the low current levels, which is relevant for the experimental separation of these levels. This is achieved when the ratio of  $m$  and  $|C|$  is large.

### APPENDIX C: ARTIFICIAL EVOLUTION OF BOOLEAN LOGIC IN A SECOND DEVICE

Figure 6 shows results comparable to Fig. 2, but for a device with different positions of the (counter)dopants.

### APPENDIX D: BOOLEAN LOGIC WITH SHORTER SIMULATION TIMES

Figure 7 shows results comparable to Fig. 2, but for 10 times less KMC steps. The time intervals are about a factor 10 smaller and the uncertainties in the current are about a factor  $\sqrt{10} \approx 3.16$  larger than in Fig. 2.

### APPENDIX E: VOLTAGE AND CURRENT DISTRIBUTIONS FOR RANDOM CONTROL VOLTAGES

Figure 8 shows results comparable to Fig. 3 for the device of Fig. 2, using random control voltages.

### APPENDIX F: VOLTAGE AND CURRENT DISTRIBUTIONS FOR BOOLEAN GATES IN A SECOND DEVICE

Figure 9 shows results comparable to the first three rows of Fig. 3 for the device of Fig. 6.

### APPENDIX G: CORRELATIONS IN OUTPUT CURRENT FOR DIFFERENT LOGIC INPUTS

Figure 10 shows the correlations between the output current of the device of Fig. 2 for the different logic inputs.

### APPENDIX H: SENSITIVITY OF AND AND XOR GATES TO $V_{c2}$ AND $V_{c3}$

Figure 11 shows results comparable to Fig. 4 for the fitnesses  $F$  of the AND and XOR gates of Fig. 2 when changing  $V_{c2}$  and  $V_{c3}$  from their values found by artificial evolution, given in the table at the top right of Fig. 2.

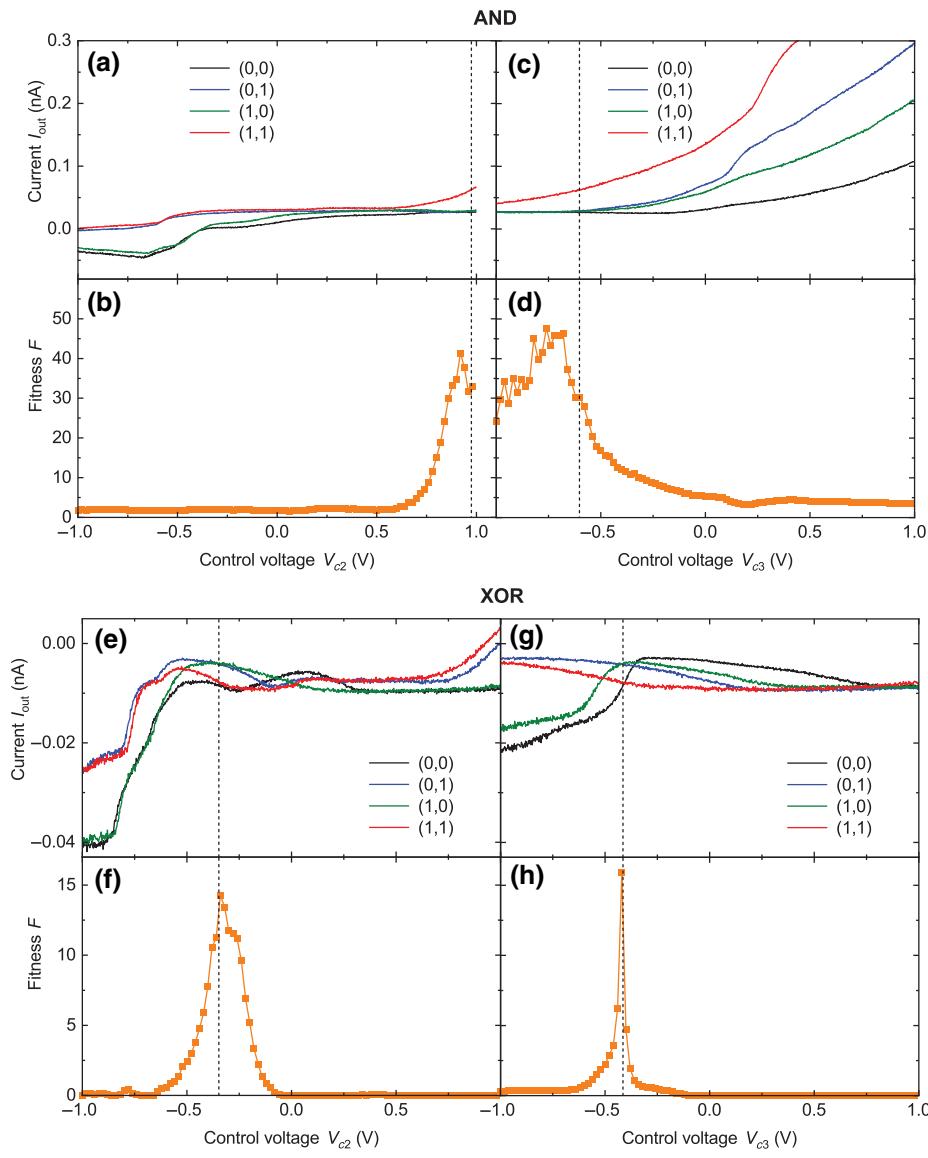


FIG. 11. (a) Output currents  $I_{\text{out}}$  for the four logic input combinations and (b) fitness  $F$  of the AND gate of Fig. 2 as a function of control voltage  $V_{c2}$ . Vertical dashed lines in (a) and (b) denote the values of  $V_{c2}$  found by artificial evolution. Panels (c) and (d) are the same as (a) and (b), but for  $V_{c3}$ . The evolutionary algorithm did not find before stopping the somewhat higher fitnesses of  $F$  in (b) and (d) at other values of  $V_{c2}$  and  $V_{c3}$ . Panels (e)–(h) are the same as (a)–(d), but for the XOR gate.

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