CSCI 1510 Lab 2

Purpose

This lab is designed to provide you to demonstrate and validate your understaning on logic gates and logic theorems by developing and simulating some basic and important logics using LogiSim tool you learned in Lab 1.

You are asked to design and simulate following 3 simple logic circuits

1. **Distribuity Postulate**
2. **DeMorgan's Theorem**
3. **Duality Law**

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1. Setting up your lab work environment (From Lab 0)

For this lab work, we expect you have fishinshed Lab 0 and Lab 1 completely and your lab environment is ready for this lab 2 assignment. If you haven't, please refer to the Section 2 of Lab 0 instructions. Again, you are allowed to use any working lab environment and in fact, you may store your latest work in a second storage or cloud so that you can work from the latest copy from either envrionment at your convenience.

2. Lab 2 Assignment

2.1 Part 1: Validating Distribuity Postulate

1. Start a new project and draw a new logic diagram on the canvas to prove the following logic expressions are equal. You may draw the both in the same project

Left Hand Side	Right Hand Side
x(y+z)	xy + xz
x + yz	(x+y)(x+z)

2. To add a gate to your canvas, simply click on the gate you want to work on and drag your mouse to the Canvas (work area).
3. You should see that the ***Attribute*** Table for each gate you added. If you do not, just click on your gate and the table will appear. Update the values as needed per specification. Make sure you don't need to leave excessive inputs and label each gate with approprate name.
4. Extend from the same inputs (x, y, z) to feed to both LH and RH side logic circuits.
5. Set the "Data Bits" for inputs, all the logic gates, and output to "***n***" number bits. What should be the best number for "***n***" for 3-variable logic circuit? Using the "poke" tool, make sure that all the possible combinations of inputs are passed to the logic circuit.
6. You may add your design descriptions using "Text" tool (***A*** icon on the tool bar).
7. Compare the output from both side logic circuits and the outputs should be the same for all the input combinations

2.2 Part 2: Validating DeMorgan's Theorem

1. Read Extension of Multiple Inputs (pg 62), if you haven't already. This reading will help you with the rest of the lab.
2. In the canvas of the same Lab 2 project, design and simulate both sides of the following functions. Use only 2-INPUT (***No*** 3-INPUT) GATES AT THIS TIME. The reading in step 1 will tell you how to create a 3-input gate from 2-input gates.

Left Hand Side	Right Hand Side
(x + y + z)'	x'y'z'
x' + y' + z'	(xyz)'

3. Again, you may put the left hand side and right hand side for each row in the table on the same page.
4. Follow the same steps 4 - 7 instructions from Part1

2.3 Part 3: Validating Duality Principle

Now, let's do the same for the Duality Law. Follow the same steps from Part 1 and Part 2 for validating the following Daulity Principle.

If (x' + y') + xy = 1, then (x'y')(x + y) = 0

3. Deliverables

1. **Part 1, Part 2, Part 3:**
   - One PDF file containing the logic circuit drawing of all three parts.
   - Lab 2 LogiSim design file (*.circ) for validation purpose
2. Then submit both files on Canvas lab 2 assignment.