| clk=0 leds[4:0]=00 00 mem_addr[31:0]=00000060 mem_rdata[31:0]=00008067 mem_rstrb=0 mem_wdata[31:0]=00000000 mem_wdata[31:0]=00000000 mem_wstrb[3:0]=0 processor_rdata[31:0]=00008067 rdata_gpio[31:0]=00000000 [0000000]   | Time                           | 1000     | 1 sec 2000 sec | 31010 sec | 4000 sec 5000 | 0 sec 6000 | 0 sec 7000 s | ec 81010 : | sec 9000 s | ec 11010    | 0 sec 11000 : | séc 12000 s | sc 131010 s | c 14000 sec | 150000 sec | 160000 sec | 17000 sec | 181000 sec | 19000 sec | 210000 sec |
|--|--------------------------------|----------|----------------|-----------|---------------|------------|--------------|------------|------------|-------------|---------------|-------------|-------------|-------------|------------|------------|-----------|------------|-----------|------------|
| men_addr(31:0)=00000060 men_xdata(31:0)=00000067 men_xstrf=0 men_wstrf=0 men_wstrf(30)=0 0 men_wstrf(30)=0 0 processor_rdata(31:0)=00000067 rdata_gpio(31:0)=00000007 rdata_ausrt[31:0]=00000000 processor_rdata[31:0]=00000000 processor_rdata(31:0)=00000000 processor_rdata(31:0)=000000000 processor_rdata(31:0)=000000000 processor_rdata(31:0)=000000000 processor_rdata(31:0) | clk=0                          |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| mem_rdata[31:0]=00000007 mem_vstrb=0 mem_wstrb[3:0]=00000000 mem_wstrb[3:0]=0 processor_rdata[31:0]=0000000 rdata_usrt[31:0]=00000000 processor_rdata[31:0]=00000000 processor_rdata[31:0]=00000000 processor_rdata_usrt[31:0]=00000000 processor_rdata_usrt[31:0]=00000000 processor_rdata_usrt[31:0]=00000000 processor_rdata_usrt[31:0]=00000000 processor_rdata_usrt[31:0]=00000000 processor_rdata_usrt[31:0]=00000000 processor_rdata_usrt[31:0]=000000000 processor_rdata_usrt[31:0]=00000000 processor_rdata_usrt[31:0]=00000000 processor_rdata_usrt[31:0]=000000000 processor_rdata_usrt[31:0]=000000000 processor_rdata_usrt[31:0]=000000000 processor_rdata_usrt[31:0]=000000000 processor_rdata_usrt[31:0]=00000000000 processor_rdata_usrt[31:0]=000000000 processor_rdata_usrt[31:0]=00000000000000000000000000000000000  |                                | 00       |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| mem_wdata[31:0]=00000000 mem_wstrb[3:0]=0 processor_rdata[31:0]=00000007 rdata_uart[31:0]=00000000 processor_rdata[31:0]=00000000 processor_rdata[31:0]=0000000000 processor_rdata[31:0]=00000000 processor_rdata[31:0]=0 | mem_addr[31:0]=00000060        |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| mem_wdata[31:0]=00000000 mem_wstrb[3:0]=0 processor_rdata[31:0]=00000007 rdata_gpio[31:0]=00000000 g000000 rdata_uart[31:0]=00000000 processor_rdata[31:0]=00000000 g000000 processor_rdata[31:0]=00000000 g000000 processor_rdata[31:0]=00000000 g000000 processor_rdata[31:0]=00000000 g000000 processor_rdata[31:0]=00000000 g000000 g000000 g000000 g000000  | mem_rdata[31:0]=00008067       |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| mem_wstrb[3:0]=0   | mem_rstrb=0                    |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| processor_rdata[31:0]=00000000   | mem_wdata[31:0]=00000000       |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| rdata_gpio[31:0]=00000000  | mem_wstrb[3:0]=0               | 0        |                |           |               |            |              |            |            | <b>X</b> 0  |               |             |             |             |            |            |           |            |           | <b>X</b> 0 |
| rdata_uart[31:0]=00000000  | processor_rdata[31:0]=00008067 |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| reset_n=1 s0_sel_mem=1 s1_sel_gpio=0 s2_sel_uart=0 uart_tx=0 i_clk=0 i_data[7:0]=F i_rsst=0 i_valid=0 i_valid=0 i_cready=0   | rdata_gpio[31:0]=00000000      | 00000000 |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| s0_sel_mem=1         s1_sel_gpio=0         s2_sel_uart=0         uart_tx=0         i_clk=0         i_data[7:0]=F       F         i_rst=0                 i_valid=0                 0_ready=0   | rdata_uart[31:0]=00000000      | 00000000 |                |           |               |            |              |            |            | <b>X</b> 00 | 1000000       |             |             |             |            |            |           |            |           | (0000000)  |
| sl_sel_gpio=0  s2_sel_uart=0  uart_tx=0  i_clk=0  i_data[7:0]=F  i_rst=0  i_valid=0  o_ready=0   | reset_n=1                      |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| s2_sel_uart=0  | s0_sel_mem=1                   |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| uart_tx=0         i_clk=0         i_data[7:0]=F       )F         i_rst=0       )c         i_valid=0                 o_ready=0  | s1_sel_gpio=0                  |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| i_clk=0 i_data[7:0]=F  | s2_sel_uart=0                  |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| i_data[7:0]=F  | uart_tx=0                      |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| i_data[7:0]=F  |                                |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| i_data[7:0]=F  |                                |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| i_data[7:0]=F  |                                |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| i_rst=0 i_valid=0 o_ready=0  | i_clk=0                        |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| i_valid=0  | i_data[7:0]=F                  | (XF      |                |           |               |            |              |            |            | χr          |               |             |             |             |            |            |           |            |           | Xe Xe      |
| o_ready=0  | i_rst=0                        |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
|  | i_valid=0                      |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
| o_uart_tx=0  | o_ready=0                      |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           | I          |
|  | o_uart_tx=0                    |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
|  |                                |          |                |           | -             |            |              |            |            |             | -             |             |             |             |            | 1          |           |            |           |            |
|  |                                |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
|  |                                |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
|  |                                |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
|  |                                |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
|  |                                |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
|  |                                |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
|  |                                |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |
|  |                                |          |                |           |               |            |              |            |            |             |               |             |             |             |            |            |           |            |           |            |