

# IC Fabrication Review Notes

## IC Manufacturing Technology

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# 1 Chapter 4 pattern transfer

## 1.1 Photolithography

### 1.1.1 Process Step and Purpose

#### Standard Sequence

Surface Prime → Spin Coat → Soft Bake → Alignment & Exposure → Post Exposure Bake (PEB) → Develop → Hard Bake.

#### Purpose

Surface prime: Removes surface moisture

Coat: (thickness of resist,  $t$  和转速  $w$  成反比)

Soft bake: 1. remove solvent 2. Improves resist adhesion

- equipment: Oven and hot plate
- excessive bake: decrease photosensitivity
- insufficient bake: decrease develop selectivity

Post exposure bake: to make sure the photoinduced chemical reaction in the PR.

Develop: dissolve the exposed resist.

- Different dissolution: (a) Positive resist: alkaline solution. (b) Negative resist: organic solution.
- Equipment: (a) Batch: Immersion with agitation/Spray. (b) Single wafer: Puddle. (批量或者单独显影, 室温下进行)

Hard baking: 1. removes residual solvent 2. improve adhesion 3. increase etch resistance (equipment: Oven and hot plate)

### 1.1.2 Photoresist

Consists of three components: 1. resin (mechanical properties) 2. sensitizer (photoactive compound) 3. solvent (keep in a liquid form and for coating)

#### Positive and Negative

Positive:

Mechanism: exposure increases solubility.

Result: Exposed areas are removed after development.

Pattern: Same as the mask.

Feature: Better resolution, used in IC manufacturing.

Negative: opposite from positive.

#### Resist Contrast (光刻胶对比度)

Developed thickness - Exposure dose curve, slope is resist contrast (斜率越大越好). 正胶负斜率, 负胶正斜率.

#### Real Exposure vs. Real Resist

Due to light diffraction, real exposure is not a perfect square wave but has a gradual slope, resulting in sloped resist profile.

### 1.1.3 Alignment and Exposure

#### Printing Methods for Exposure (Aligners)

Contact printing: mask on the resist.

Proximity printing: a gap between mask and resist.

Projection printing: an optical system between mask and resist.

#### Comparison

Contact: high resolution, high defects (dirty), full wafer exposure.

Proximity: low resolution (diffraction), low defects, full wafer exposure.

Projection: high resolution, low defects, uses reticle (not full wafer exposure).

#### Projection Photolithography

Evolution: step-and-repeat → step-and-scan (工业主流, 衍射小).

Wavelength trend: G-line (436nm) → I-line (365nm) → KrF (248nm) → ArF (193nm) → EUV (13.5nm).

Optical resolution:  $R = k_1 \frac{\lambda}{NA}$  (lower better; NA = numerical aperture,  $k_1$  depends on process).

Depth of focus (DOF):  $DOF = k_2 \frac{\lambda}{NA^2}$  (larger better).

### 1.1.4 Resolution Enhancement

Double patterning lithography: double litho + double etch.

Off-axis illumination.

Optical proximity correction (OPC): moving edges or adding extra polygons.

Phase shift mask (PSM): uses interference to reduce  $k_1$ .

### 1.1.5 Advanced Lithography Techniques

E-beam lithography (EBL): maskless, high resolution, low throughput.

Nanoimprint lithography (NIL): highest resolution, no diffraction limit, mold making difficult.

X-ray, ion-beam: high resolution but mask issues.

## 1.2 Etching

### 1.2.1 Classification: Wet vs. Dry

Wet etch: chemical (liquid), isotropic(result in undercut), highly selective, less used in VLSI.

Dry etch: physical (ions, momentum transfer), anisotropic, low selectivity, used for small features.

Combination: RIE (best directionality + selectivity).

*Note: Masks classified as photoresist (soft mask) and  $\text{SiO}_2/\text{Si}_3\text{N}_4$  (hard mask; usually defined by PR first, more robust).*

### 1.2.2 Properties of Etching

Uniformity, rate, selectivity, anisotropy, byproducts.

### 1.2.3 Isotropic and Anisotropic Etching

#### Degree of Anisotropy

$A_f$  (0–1): 0 = isotropic, 1 = anisotropic.

#### Selectivity

Selectivity = etch rate of target / etch rate of mask.

### 1.2.4 Wet Etching

#### Describe Briefly

Uses liquid chemical solutions to remove film materials (not masked areas).

#### Chemical Etchants

$\text{SiO}_2$ : HF

Si:  $\text{HNO}_3 + \text{HF}$

$\text{Si}_3\text{N}_4$ : hot  $\text{H}_3\text{PO}_4$

#### Calculation!

Selectivity  $S = r_1/r_2$ , mask erosion ( $I_{etch}$ ,  $A_{etch}$ ).

## Drawbacks

Lack of anisotropy, poor control, particulate contamination → used only for non-critical features.

### 1.2.5 Dry Etching (主要用 RIE 做对比)

#### Describe Briefly

Uses reactive gases in plasma; mechanism = physical + chemical etching.

#### Plasma Generation

CCP: capacitively coupled plasma.

ICP: inductively coupled plasma.

ECR: electron cyclotron resonance.

#### Dry Etching Techniques Summary

Sputter etch / ion milling / IBE (pure physical).

Plasma etch (pure chemical).

Barrel etcher (chemical-dominant).

HDPE & RIE: high selectivity + high anisotropy.

#### Dry Etching Methods (Must Form Volatile Byproducts)

SiO<sub>2</sub>: CF<sub>4</sub> (high selectivity to Si, C protects Si); CHF<sub>3</sub>/C<sub>4</sub>F<sub>8</sub> for better anisotropy.

Si<sub>3</sub>N<sub>4</sub>: similar to oxide (CF<sub>4</sub> etc.).

Al: Cl<sub>2</sub> (AlCl<sub>3</sub> volatile; avoid F → AlF<sub>3</sub> solid).

## 2 Chapter 3 Thin Film Technology

### 2.1 Vacuum Technology

#### 2.1.1 why vacuum technology?

Oxidation, Ion implantation, CVD, PVD are all processed in vacuum or controlled environment.

#### 2.1.2 Vacuum basics

##### mean free path

$\lambda = \frac{\sqrt{2}k_B T}{2\pi d^2 p}$ , 跟 p 成反比。(撞到下一个气体分子前平均移动距离)

##### Knudsen number

$\frac{\lambda}{L}$ , <1 flow is viscous. >1 flow is ballistic. (L 是腔体的特征尺寸)

##### vacuum pump

(removed from): mechanical, turbo molecular. (buried in a layer): cryo pump (最干净, 需要前级 pump)

## **vacuum regions**

PVD and CVD all need High vacuum( $-6$  - $9$  次方 pa)

## **2.2 Chemical Vapor Deposition (CVD)**

CVD is film growth from vapor/gas phase via chemical reaction at substrate.

### **2.2.1 CVD process**

- 1.introduction of gas/vapor species
- 2.species travel to surface of substrate.
- 3.species adsorb on surface
- 4.surface diffusion/chemical decomposition
- 5.chemical reaction of reactive species
- 6.desorption of by-products
- 7.surface diffusion
- 8.bulk transport of by-products.

(prefer **heterogeneous reaction**(reaction at the interface between two different phase) avoid **homogeneous reaction**(reaction in the same phase)

Atomic-scale: bulk transport, transport across boundary layer, adsorption, decomposition, reaction with film, desorption, diffusion of byproduct, bulk transport.

### **2.2.2 CVD film growth: transport limited and reaction limited**

画两张图!  $\ln(v)$ - $1/T$  曲线和  $\ln(v)$ - $\sqrt{u_0}$  曲线 (arrhenius-like)

high-T small slope(transport limited), low-T high slope(reaction limited).

#### **Describe briefly**

Transport limited: reaction is fast, limited by gas diffusion velocity  $D$ .  $D$  has low temperature dependence.(跟平均自由程成正比, 跟气压反比, 需要低压, APCVD 会出现 transport limited.)

Reaction limited: gas supply is sufficient, but reaction is low. reaction has high temperature dependence. (LPCVD 会出现 reaction limited. 低压, 扩散率够, 温度是敏感点。可以用来 deposit amorphous film)

### **2.2.3 CVD systems**

APCVD: atmospheric pressure. 常压

LPCVD: low pressure. 低压, 抽真空, 扩散率  $D$  大

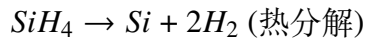
PECVD: plasma enhanced. 温度不用 lpcvd 那么高, 通过离子撞击, 跟 etch 相反, 是生长

材料，用的还原性气体，使用 CCP 生成。

HDPCVD: ICP 生成，plasma 密度更高。

## 2.2.4 How to grow $Si$ , $SiO_2$ , $SiN$ , *metal* and chemical reactions

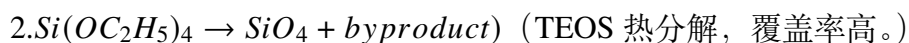
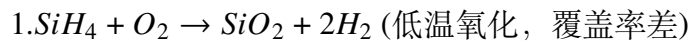
### polysilicon:



doping 用来 reduce resistance

application: 1.MOS gate electrode 2.bipolar emitter 3.register SRAM

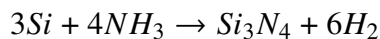
### silicon oxide:



3.Doping: 1.PSG(catch electron) 2.BSG(make silicon flow, lower melting point) 3.BPSG purpose: to make silicon flow, planarize and catch electrons prevent pollution.

4.application: 1.ILD(interlevel dielectric) 2.side wall spacer

### silicon nitride:



application: 1.oxidation mask 2.final passivation 3.diffusion barrier.

**Tungsten(钨):** 1.silicon reduction:  $2WF_6 + 3Si \rightarrow 2W + 3SiCl_4$  2.hydrogen reduction:  $WF_6 + 3H_2 \rightarrow W + 6HF$  (还原性，可以用作填孔并且好在 selective)

## 2.3 Physical Vapor Deposition (PVD)

two kinds of PVD techniques, Sputtering and Evaporation.

### 2.3.1 Plasma

the bulk of plasma contains equal concentrations of ions and electrons.

#### how to generate plasma, necessary conditions

1.Pressures:  $\frac{\lambda}{L} < 1$  (viscous flow)(10mT 100mT (太低分子数不够，太高不够加速的))

2.Energy:  $E_k > \text{ionization potential of } Ar^+ (E_k = Eq\lambda)$  (不断电离，维持 plasma 产生)

### 2.3.2 Sputter

sputter rate depends on 1.angle of incidence 2.relative masses 3.kinetic energy.

#### sputtering deposition process(腔内有气体氩气)

1. $Ar^+$  accelerated to cathode

2.Neutral target species kicked off (Al).

3.Some  $Ar$ ,  $Ar^+$ ,  $e^-$  also

4.  $e^-$  may ionize impurities
5. deposition at anode (Al and impurities).
6. some physical resputtering of film by Ar

#### **five different sputtering:**

1. DC sputter deposition: only for conducting materials.
2. RF plasma sputtering: (射频电源, 13.56MHz)
3. RF bias sputtering: 衬底加偏压, 轰击衬底膜, 改善台阶覆盖性
4. Magnetron sputtering: + 磁场
5. Reactive sputter deposition: 通入反应气体

#### **materials commonly sputtered**

Pure: Al, Cu, Ti, W

Alloy: Al-Si, Al-Cu (composite target 很好的保持比例)

Compound: TiN, Silicides

### **2.3.3 Evaporation**

#### **Requirement of PVD-evaporation**

##### **1. median to high Vacuum required**

1. to avoid atom scattering
2. to reduce contamination

##### **2. evaporation heating techniques (source)**

1. resistive heater (heating temperature is low and have contamination)
2. RF-induction heater
3. e-beam (high temperature and no contamination but have X-ray may have radiation damage)
4. flash heating.

#### **Process and vapour pressure**

1. Heating
2. Vaporization
3. Transport
4. Condensation (撞到冷的晶圆, 冷凝成固体薄膜)

(vapor pressure  $P$ , 和温度呈指数关系。材料想要变成气体的程度; evaporation rate 也跟 T 有关)

#### **constraints**

1. step coverage is poor (because has shadow effects—solve: 1. substrate heating 2. target holder with planetary rotation)
2. alloy is not suitable for evaporation. (different elements have different melting point. result in film will not have same composition as the source material.)

### 2.3.4 Sputtering compared with evaporation

#### Pros

- 1.allow use of large area target.
- 2.better control of alloy composition.
- 3.better rate control (film thickness)
- 4.substrate sputter: in-situ clean(溅射衬底来清洁)
- 5.no x-ray generation.

#### Cons

- 1.higher cost.
- 2.higher process pressure(中低真空 pressure high)- contamination
- 3.potential bombardment damage.

### 2.3.5 PVD application

#### self-aligned silicide

Process: 1.Sputter Ti 2.1st heat treatment in  $N_2$  (si 上生成  $TiSi_2$  想要, 二氧化物上生成  $TiN$  不想要, 因为其导电) 3.wet etch to remove  $TiN$  4.2nd heat treatment (降低电阻, 提高导电能力)

#### Via metallization (metal-metal)

Preocess: 1. sputter  $TiN$  glue layer 2.conformal CVD W 3.W etch back for planarized via(溅射不干净, 用 CVD 可以, 先搞一层 glue layer)

Cons of sputter: 1.poor step coverage 2.high resistance(侧壁无法被 sputter 到)

#### Contact metallization (metal-silicon)

Cons: 1.junction spiking(铝渗入硅) 2.Native oxide result in high contact resistance

Remedy:

- 1.saturate Al with Si (Al-Si alloy) (用 Si 把 Al 饱和掉这样不会渗入)
- 2.interdiffusion barrier metal: $TiW$ ,  $TiN$ (加一层金属防止渗入)
- 3.sintering in forming gas (把氧化层还原回去 Si)
- 4.reduce oxide by reacting with Ti

#### Interconnects

Features: 1.resistance as low as possible 2.reliability as high as possible (Cu better than Al)

## 3 Chapter 2 Hot processing and Ion implantation

### 3.1 Diffusion & Doping

#### 3.1.1 why diffusion

introduce impurities into silicon to control majority-carrier type and layer resistivity.

#### 3.1.2 Three diffusion mechanisms in solid

1. substitutional diffusion. (the impurity moves among vacancies in the lattice)
2. interstitial diffusion. (impurity atom replace a silicon atom, and silicon atom replace an interstitial site.)
3. interstitial diffusion. (impurity atom do not replace silicon atom in a crystal lattice)

#### 3.1.3 Fick's law and Calculation!

#### 3.1.4 Two-step diffusion, Control and Calculation!

##### Two-step diffusion

why: can not control dose and profile at the same time.

1. pre-deposition diffusion (dose control, 表面浓度  $C_s$  不变)
2. drive in diffusion (profile control, 总剂量  $Q$  不变)

##### Factors effect diffusion

temperature ( $D = D_0 e^{\frac{-E_a}{kT}}$ ), dopant concentration, charged impurities, oxidation

#### 3.1.5 Measure diffusion profile and Diffusion equipments

##### measure methods of doping profile

1. 4-point probe
2. Hall effect
3. SIMS
4. Spreading Resistance

##### Diffusion equipments

Diffusion Furnace (batch processing)

## 3.2 Thermal oxidation of silicon

跟 CVD 不一样, 这一步是消耗硅

#### 3.2.1 why $SiO_2$

1. Excellent Electrical Insulator
2. High breakdown Electric field.
3. stable and reproducible interface

- 4.conformal oxide growth on exposed *Si* surface
5. $SiO_2$  is a good diffusion mask for common dopants
- 6.good etching selectivity between *Si* and  $SiO_2$ .

### 3.2.2 structure and properties of $SiO_2$

- 1.Thermally oxidized: Amorphous
- 2.Quartz:Crystalline (热可以是无定型, 石英是晶体)

### 3.2.3 Applications of $SiO_2$

- 1.Gate Oxide
- 2.Diffusion Mask
- 3.Isolation
- 4.Passivation(表面钝化)

### 3.2.4 growth & deal-grove model & factors influencing thermal oxidation

#### growth

- 1.dry oxidation :  $Si + O_2 \rightarrow SiO_2$  (slow and density is high)
- 2.wet oxidation :  $Si + 2H_2O \rightarrow SiO_2 + 2H_2$  (fast and density is low)

#### deal-grove model(calculation!)

surface reaction-limited:  $t_{ox} = \frac{B}{A}(t + \tau)$  (in thin oxide, linear rate)

diffusion-limited:  $t_{ox}^2 = B(t + \tau)$  (in thick oxide,parabolic rate)

( $\tau$  是修正项,  $t_{ox}$  会给, 注意单位)

#### factors influencing thermal oxidation

- 1.Temperature
- 2.dry or wet oxidation and pressure
- 3.substrate orientation
- 4.doping concentration.

### 3.2.5 charge in oxide and equipment

#### charge

mobile, fixed, interface, oxide trapped charge.

#### equipment

horizontal/vertical diffusion furnace

### 3.3 rapid thermal processing

#### 3.3.1 why RTP?

$L_D = \sqrt{Dt}$ , 传统的  $t$  太大, 扩散太强, 但是又要做浅结

The shallow junction and thermal budget(浅结, 传统的热预算太高会扩散到深处)

#### 3.3.2 RTP tool

Lamp array

#### 3.3.3 RTA,RTO,RTN

##### RTA(rapid thermal annealing)

Purpose: 1.repair the damage 2.activation (dopant ions become part of the lattice) 3.suppress the diffusion

(退火修复晶格)

##### RTO(rapid thermal oxidation)

is well-suited to the growth of thin and high-quality layers

##### RTN(rapid thermal nitridation)

form  $SiON$ . high  $k$ , reduce leakage current, reduce breakdown

##### RTP road map

batch furnace  $\rightarrow$  RTA  $\rightarrow$  flash/laser annealing

### 3.4 Ion implantation

#### 3.4.1 Drawbacks of Doping by diffusion & Pros of ion implantation

##### drawback of doping by diffusion

- 1.Large thermal budget (横向扩散严重)
- 2.time consuming: two step diffusion
- 3.high temperature diffusion mask.
- 4.Toxic source gases.
- 5.Low dose and shallow junction difficult.

##### Pros of ion implantation

- 1.precise control of dose and depth profile.
- 2.Low temperature process
- 3.wide selection of mask materials(处理过程的温度低)
- 4.Less sensitive to surface cleaning procedures.
- 5.good lateral dose uniformity

### 3.4.2 Ion implanter: parts and functions (ion process)

- 1.ion source: supplies ions at fixed charge and energy.
- 2.mass spectrometer: species selection.
- 3.Accelerator: accelerate the ions
- 4.scanning system. (the beam is bent slightly to prevent neutral particles)
- 5.target chamber: wafer location.
- (6.post-anneal)

### 3.4.3 inside the materials

#### energy lost mechanisms

- 1.Nuclear stopping (result in crystalline Si substrate damaged by collision)(light ions 发生的多)
- 2.Electronic stopping (result in electronic excitation creates heat)(heavy ions more often)

### 3.4.4 Damage of ion implantation and damage anneal

#### Damage

- 1.crystal damage( $Si$  binding energy smaller than implant energy)
- 2.dopant distribution is not substitutional.(掺杂没有替位, 在空隙里)

#### Damage anneal

RTP(rapid thermal process) to anneal the damage.

### 3.4.5 composition profile and Non-Gaussian distribution

#### Ideal

Gaussian distribution

#### Non-ideal

- 1.Ion channeling. (result in long tail) (solve:  $7^\circ$  off)
- 2.Ion mass effects:  
light ions: such as  $B$  has backward scattering(图左边翘起来)  
heavy ions: such as  $As$  has forward scattering(图右边翘起来)  
(极值的位置都不变, 因为是能量决定)

### 3.4.6 masking and selective implant

#### mask

- 1.who can be: photoresist,  $SiO_2$ ,  $Si_3N_4$ , etc
- 2.lateral spread
- 3.implant mask need not to handle high temperature.

## Selective implant and application

1. shallow junction formation:

\*\*low energy implant (but result in beam divergence) (离子束发散, 太轻而且低能)

\*\*tilt implant (but result in shadowing)

\*\*Molecular Ion Implantation (use  $BF_2^+$ ) (重量够而且能量低, 能形成浅结, 后续再 RTA)

2. High energy implantation: high-dose: Silicon-on-insulator (SOI)

### Calculation!

(Gaussian Distribution, Dose, Peak Concentration, Junction Depth)

## 4 Chapter 5 Process Intergration

### 4.1 Device isolation

used to prevent separate transistors from interacting with each other through the substrate

#### 4.1.1 why device isolation

1. to prevent undesired conducting paths.

2. to avoid creation of inversion layers outside the channels (衬底表面的金属形成的寄生沟道)

3. to reduce the leakage currents.

#### 4.1.2 traditional device isolation

1. pn junction isolation (利用 pn 结反偏阻断)

2. oxide isolation (LOCOS and STI)

3. silicon-on-insulator isolation (SOI)

#### 4.1.3 LOCOS, STI, SOI

##### LOCOS (oxide isolation)

1. Process: CVD of  $SiO_2$ , CVD of  $Si_3N_4$ , etching of Nitride and oxide, growth of  $SiO_2$ , nitride layer removal.

(直接在 substrate 上面长) 2. Bird's beak: lateral diffusion through stress relief oxide. result in active region smaller.

##### STI (oxide isolation)

1. Process: Mask stack formation (pad oxide and Nitride) → STI etch → Liner oxidation → Gap fill with CVD oxide (oxide 长到 nitride 上面去) → CMP → Hard mask removal (remove Nitride)

(先挖一道沟, 然后长, 再抛光, 去掉 nitride)

2. Advantage compared with LOCOS:

\*\*No bird's beak

\*\*More scalable(可以应对更小的器件)

\*\*Better planarity

## SOI

1. Structure: Thin top silicon layer, Buried oxide, Thick bottom silicon.

2. Advantage compared with bulk silicon:

\*\*Lower parasitic capacitance.

\*\*Resistance to latch-up

\*\*Low leakage current(higher performance)

## 4.2 Interconnect

### 4.2.1 contact and interconnect

#### 4.2.2 First metal level: local interconnect

##### Process

1. (cobalt) silicide contact formation(reduce resistance)(只在 source, drain and gate 上, 金属硅化物降低与金属接触的电阻。)

2. Interlevel dielectrics(ILD)(formed by CVD then CMP)

3. Metal contact hole/via(通孔, use CVD tungsten, which filling ability is good)

#### 4.2.3 Three types of metal-silicon contact

##### schottky barrier, ohmic contact, tunneling contact

判断 (做题):

n-type semiconductor:  $\Phi_m - \Phi_n > 0$ , is schottky barrier, heavily doped becomes tunneling contact(有欧姆接触特点, 双向导通),  $< 0$  is ohmic contact.

p-type semiconductor:  $\Phi_p + E_g - \Phi_m > 0$ , is schottky barrier, heavily doped becomes tunneling contact,  $< 0$  is ohmic contact.

#### 4.2.4 Multilevel metallization: Al/Cu damascene and planarization

##### Copper compared with Al

1. Pros: Low resistivity, better electromigration and better adhesion.

2. Cons: Hard to be etched.

##### Damascene

1. why: RIE of Cu difficult due to low vapor pressure of by products.(铜难以被刻蚀) 2. conventional approach of metal etch for Al, damascene approach of metal etch for Cu.

## Pros of Planarization

CMP, SOG and reflow, Deposit and etch-back.

1. For photolithography: reduce DOF requirements, reduce reflection effect.
2. For etching: reduce over etching time
3. For deposition: improve step coverage and improve film uniformity.

### 4.2.5 interlayer dielectric (ILD)

1. Process: Deposition, use CVD to form a thick silicon oxide. CMP: dielectric film polishing.

2. Why not thermal oxidation:

\*\*thermal oxidation consumes silicon substrate.

\*\*growth rate is too slow to generate thick layers

\*\*thermal oxidation's temperature is too high. (CVD 生成的是 Low temperature oxide)

## 4.3 MOS technology

Process Module: 1. film formation and modification 2. photolithography 3. etching

### 4.3.1 NMOS

#### Process

1. active area definition (定义 active region, field implant 做 pn junction 隔离)
2. LOCOS device isolation (active region 两侧 bird's peek, 第二次隔离)
3. gate module (长一层 oxide, 和 gate)
4. contact and metallization (长一层 ICD 并且注入金属 interconnection)
5. final passivation (PECVD silicon nitride)(绝缘开窗)

#### Improve

1. Light doped drain (LDD): light dose implantation, spacer formation, high dose implantation. **Reduce hot carrier effect.** (gate 周围的浓度低, 减小最大场强)
2. self-aligned silicidation: spacer, silicide blanket deposition, anneal. **Reduces RC delay** (因为 silicide 减小了电阻, 纯硅的电阻很大)

### 4.3.2 PMOS (CMOS) process

contains NMOS and PMOS: gates and drains are connected each other.

substrate is P-type, so PMOS need n-well (衬底是 p 所以 PMOS 得加东西)

#### Process

1. Create N-wells (on p substrate)
2. Create Channel-stop implants (做三个高掺杂 p 区)

3. Grow field oxide (做 LOCOS, 就在高掺杂 p 区上做一个八边形)
4. gate grow oxide (先长一层 oxide, 然后长 gate)
5. S/D and body implantation
6. Contact formation

## **4.4 FinFET tech**

1. improved gate control
2. lower power consumption
3. but complex manufacturing process.

## **4.5 Bipolar tech**

### **4.5.1 bipolar process**

多了一个 buried 和 epitaxial layer, 另外 collector 在两侧。

1. buried layer formation
2. Epitaxial layer growth
3. isolation formation
4. base module (轻掺杂的 p 区, 重掺杂的左侧 n 区)
5. emitter and collector module
6. contact and metallization