MIPS improvement

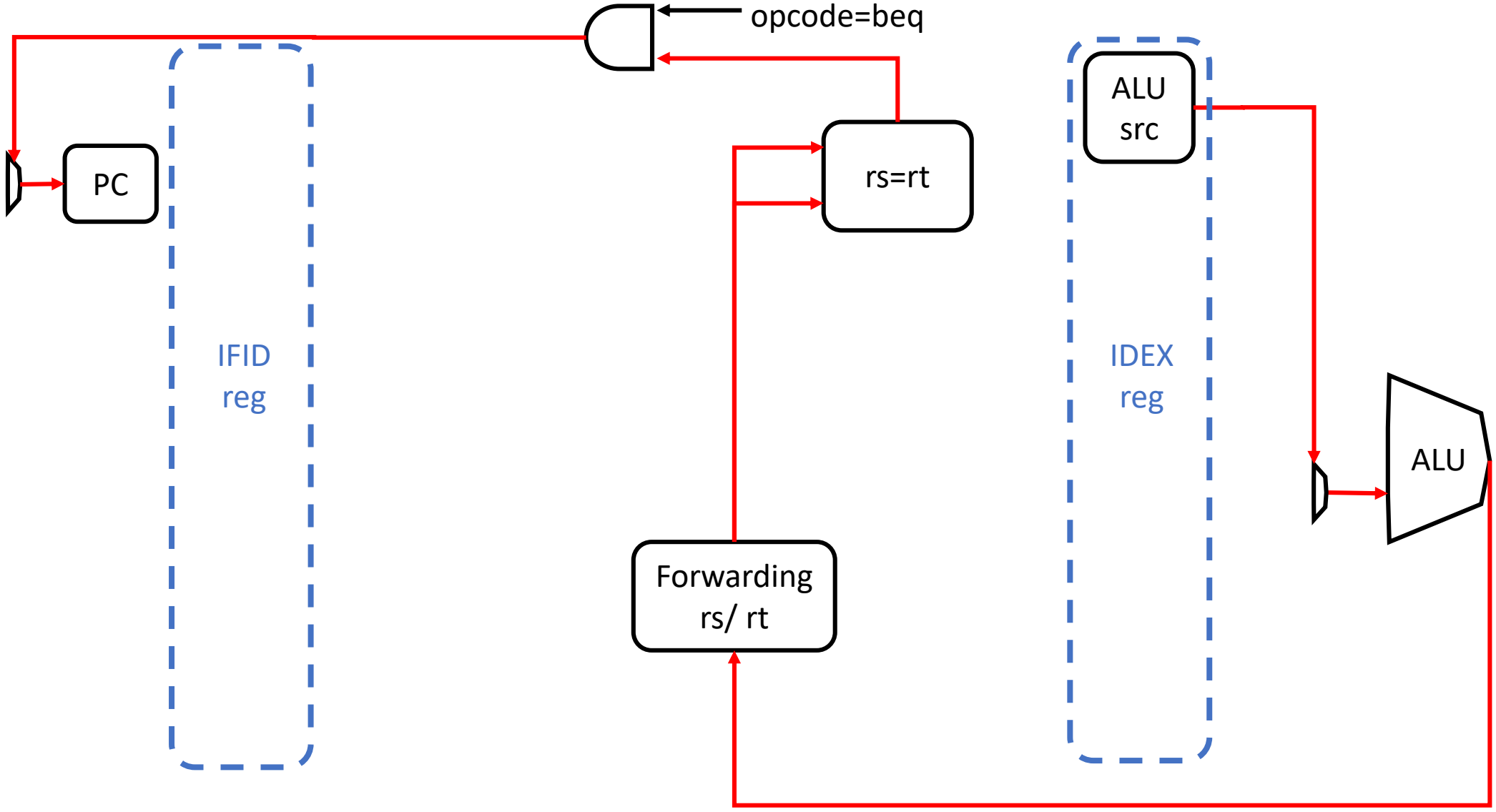
Outline

- Improvement
  - Fix potential cache bug
  - Pipeline
  - Verilog coding
- Results

Fix potential cache bug

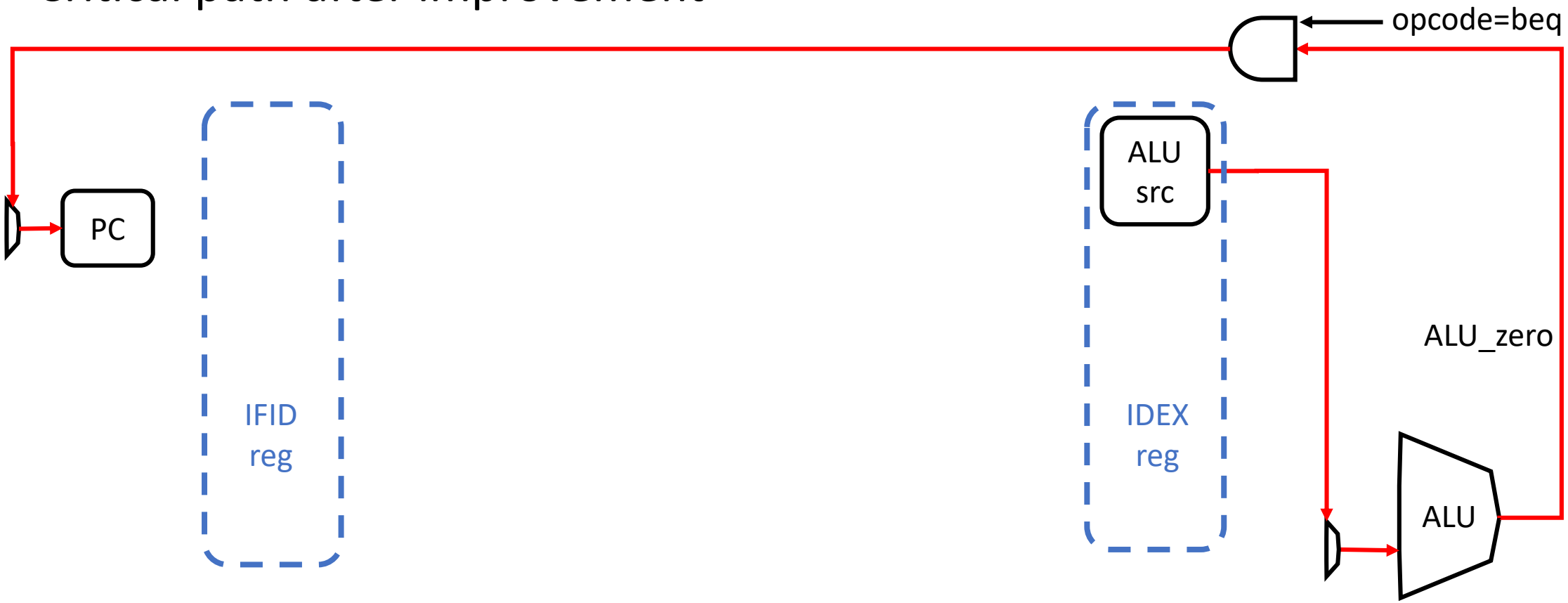
- The previous version use valid bit to indicate a dirty block
  - 1: clean/ 0: dirty
  - Set every bit in every cache block to 1 on cache reset
    - Potential error in LW/SW if the tag is 25’b1111111111…
      - This causes a valid hit, reading/ writing the wrong data.
      - Not presented in the testbench.
  - To fix this bug, add a dirty bit for each block.

Critical path of the previous version



Pipeline improvement

- Process beq in EX stage
- Critical path after improvement



Verilog coding improvement

- Remove redundant combinational circuit/ registers/ conditions….
- Improve readability
  - Separate control module from the MIPS dataflow module
  - Arrange combinational blocks according to different pipeline stages
  - Rewrite inline comments

Results

- Grading policy for this project:
  - Synthesis cell area * Post- synthesis simulation time
- Version 1
  - Area: 286618 um^2
  - Simulation time: 7145 ns
  - Area * Time: 2047878465 (um^2 *ns)
- Version 2 (after improvement)
  - Area: 264097 um^2
  - Simulation time: 5641 ns
  - Area * Time: 1489771177 (um^2 *ns)

Results of different synthesis constraint