Bo-Fan Chen

ASIC Engineer - Digital IC Design Profession
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Education

- **National Taiwan University** — Taipei, Taiwan
  Master of Electronics Engineering - Digital Integrated Circuit Design; GPA: 3.99/ 4.3 — *Sep. 2019 - Jul. 2022*
  Courses: *Computer-aided VLSI System Design, Computer Vision, Multimedia System-on-chip Design*
- **National Taiwan University** — Taipei, Taiwan
  Bachelor of Electrical Engineering, Minor in Economics; GPA: 3.67/ 4.3 — *Sep. 2015 - Jul. 2019*
  Courses: *Electronics, Digital System Design, Electrical Engineering Lab (Digital Circuit), Data Structure and Programming, Algorithms, Statistics and Econometrics*
- **Aarhus University** — Aarhus, Denmark
  Exchange Program in Software Engineering and Computer Science — *Sep. 2021 - Jul. 2022*
  Courses: *Mobile Application Development, Augmented Reality*

Research

- **CF-Net: Complementary Fusion Network for Rotation Invariant Point Cloud Completion, IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), 2022**: We proposed neural network architecture for rotation-invariant point cloud completion. The proposed architecture can process incomplete point clouds with arbitrary orientation, and the output point clouds are complete and uniformly oriented. CF-Net performs better in rotation-invariant point cloud completion compared to SOTA completion methods. (August '21)

Projects

- **MIPS**: The final project of Digital Circuit Design, a 5-stage pipeline MIPS implemented in Verilog. Re-implemented recently to improve code readability and performance. The final result, using TSMC .13um process library, runs at 2.6ns clock cycle in post-synthesis simulation. Tech: Verilog, ncVerilog, Design Vision (January '23)
- **Decision Tree Accelerator**: A Verilog implementation of a decision tree. This work uses Sci-Kit learn python package for decision tree training. The generated tree is further optimized for hardware design. The final result, using TSMC .13um process library, achieves 37 times acceleration compared to the Sci-Kit learn implementation. Tech: Python, NumPy, Sci-Kit learn, Verilog, ncVerilog, Design Vision, Innovus (February '22)
- **DCT**: The final project of Special Project. This work is a Verilog implementation of 2D 8*8 (Inverse) Discrete Cosine Transform. The final result, using TSMC .13um process library, runs at 5.4ns clock cycle in simulation. Tech: Verilog, ncVerilog, Design Vision, Innovus (July '18)

Honors and Awards

- Third place in Computer Vision final project competition - May, 2019
- Honorable Mention Award, Integrated Circuit Design Contest - May, 2020

Skills

- **Program Languages**: Verilog (Proficient), Python (Experienced), C++ (Basic)
- **Tools**: ncVerilog, nWave, Design Vision, Innovus, NumPy, Pytorch, Tensorflow, Docker, GIT

Languages

- **Mandarin**: Native Speaker
- **English**: TOEIC (900/ 990), TOEFL (103/ 120)
- **Čeština (Czech Language)**: Basic understanding, 2 years of Čeština courses at National Taiwan University

Volunteer Experience

- **Silver-Ranked Volunteer in Summer Universiade** — Linkou, Taiwan
  Assist the Universiade participants in the player village. — *Jul. 2017*