Brandon Taylor Brea

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EDUCATION

Wilkes University (ABET accredited) *Wilkes-Barre, PA*

- Bachelor of Science in Electrical Engineering **May 2020**
- Bachelor of Science in Physics
    - Minors in Mathematics ❖ Cum Laude (GPA: 3.5/4.0)

TECHNICAL SKILLS

- Programming languages and mathematical packages: C++, Java, Python, MATLAB, Mathematica, JMP.
- Computer aided design/engineering: Synopsys Tools (Avalon, SysNav), LTSpice, PSpice, SmarTest8, Agile.
- Other: die-level failure analysis, electrical fault isolation, electrical bench testing, DFT, MBIST, ATPG, Advantest 93k, device characterization, semiconductor device physics, semiconductor processing, semiconductor reliability, DVFS, physical failure analysis, IC packaging, cross-sectioning, microprobing, device decapsulation, circuit analysis, object-oriented programming (OOP), MS Visual Studio, statistical data analysis, soldering, Linux, Mac OS, Windows OS, MS Office, Agile, technical writing, laboratory research, strong interpersonal skills.

PROFESSIONAL WORK EXPERIENCE

Google, LLC *San Diego, CA*

Silicon Engineer **June 2022 – Present**

- Silicon Engineer working within the Product Development and Test Engineering team. Responsible for leading and driving the planning of design validation and PVT characterization on ATE, device qualification, wafer sort and final test solutions with design, verification, and Design for Test (DFT) teams. Contributes to the development of documentation, ATE hardware design, and final ATE test program generation while working to establish manufacturing requirements, focusing on yield improvement, and test cost reduction. Designs high-performance digital SoC test and characterization flows for PVT and participates in silicon debug, electrical fault isolation, and physical failure analysis initiatives to ensure product delivery with low DPPM and cost of test.
- Created multivariate linear regression model using python to devise new Dynamic Voltage Frequency Scaling (DVFS) methodology to predict and reduce minimum operating voltage for various IPs based on process variation of digital SoC products to improve power/performance KPIS

Qualcomm Technologies, Inc *San Diego, CA*

Failure Analysis Engineer **June 2020 – June 2022**

- Failure Analysis Engineer working within the Advanced Digital Fault Isolation team. Responsible for silicon debug, electrical fault isolation, and physical failure analysis to identify failure modes and corrective actions to help guide executive-level decisions for advanced microprocessor products.
- Worked as a Lead Electrical FA point of contact and drove over 100+ failure analysis requests to completion to support new product development, qualification/reliability stress test failures, yield learning initiatives, and RMA returns from high-profile consumer electronics customers.
- Reviewed ATE data, ATPG scan and BIST diagnostics, and historical production and quality data to devise optimal failure analysis approach in efforts to analyze reported failure down to an actionable root cause and drive product improvement. Required constant high-level communication and collaboration between multi-functional internal (PFA, TEM, Nanoprobe) and external (Design, RMA, Product, Test, Quality) engineering teams.

ON Semiconductor *Mountain Top, PA*

Process Engineering Intern – Diffusion/Cleans **May 2019 – June 2020**

- Process Engineering Intern working in diffusion and wafer clean semiconductor manufacturing areas. Responsible for integrating and qualifying new metrology equipment into the semiconductor fabrication process.
- Performed collection, correlation, interpretation, and presentation of semiconductor yield and parametric data to upper-level management and co-workers to guide decisions impacting manufacturing process flows.

PUBLICATIONS

Jake Bass, **Brandon Brea**, Huong Tran, Wei Du, Richard Soref, and Shui-Qing Yu "The effect of two-photon absorption on the dynamic range of integrated microwave photonics links", Proc. SPIE 11285, Silicon Photonics XV, 112851C (26 February 2020).