CALIFORNIA STATE UNIVERSITY
FULLERTON™

EGCP 441: Advanced Electronics for Computer

Spring 2019

Final Exam Review

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***Office Hour**: Monday and Wednesday 2:00 - 4:00 pm*
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Day and Time of Final Exam

- **Day- May 16, 2019**
- **Time – 9:30 am – 11:20 am**
- **Bring pen, pencil, calculator**
- **One page A4 cheatsheet (both sided)**
- **Note: Students are not allowed to use phone or computer during the exam.**

Question no 1

- **Some True and False**
  - **Example: The drain terminal of NMOS is at higher potential than source terminal (True/False)**
- **Fill in the blank**
  - **Example: The drain terminal of NMOS is _____ (higher/lower) potential than source terminal.**

Question no 2: Similar to Quiz no 1

Q1. An NMOS transistor is shown in Figure 1. (Use Vtn= 0.5V, Kn'=100 μA/V², W/L=2). Ignore the channel length modulation λ effect. Answer the following questions

a. Identify the node names such as drain, gate, source, and body/bulk, based on applied voltage.

b. Identify the type of material such as n-type and p-type in the figure below

c. If there is an inversion layer then it's consisted of electrons or holes?

d. Identify region of operation such as cut-off, linear or saturation? Explain?

e. Based on type of region from d) draw the inversion layer under the gate.

f. Calculate the current I_D and direction of it.

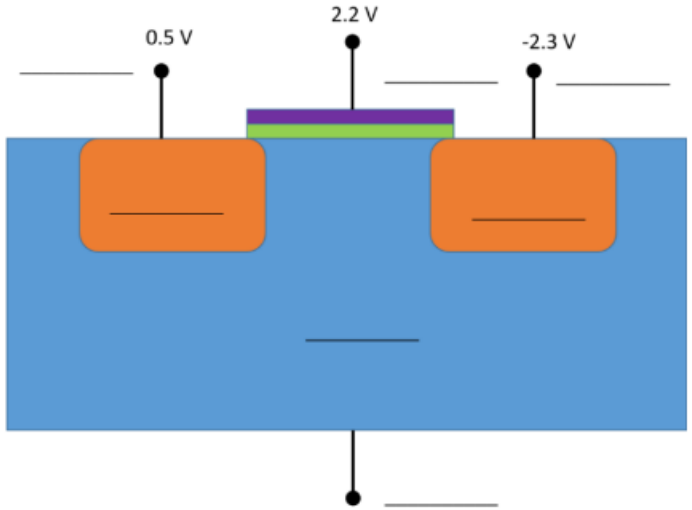
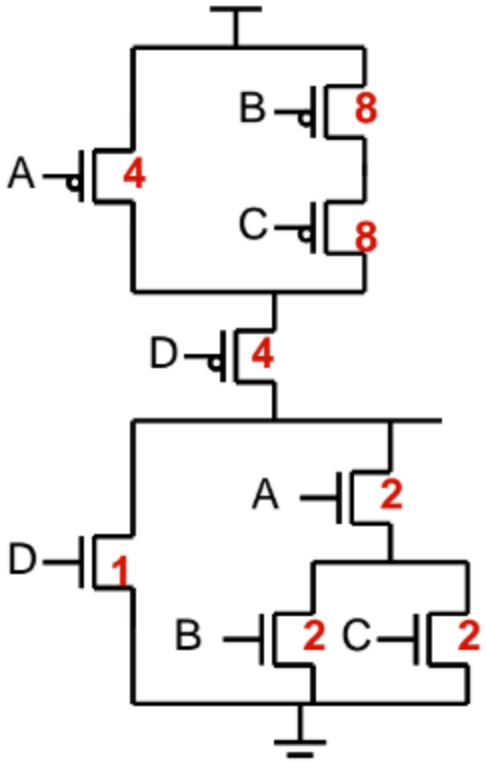


Figure 1 NMOS Transistor

Question no 3: Combination gate

- Example: A CMOS gate with V_{DD}=5V is designed such that the base (W/L)= 10. Assume that V_{Tn}=0.7, V_{Tp}=-0.6, K'_n=100 uA/V^2, K'_p=-60 uA/V^2, and the load capacitance is 100fF. Use the constant current source model to find the best case and the worst case t_{pHL} and t_{pLH}



$$OUT = \overline{D + A \cdot (B + C)}$$

Sample question: Voltage Transfer Combination Logic

(30 Points) CMOS Logic Analysis

A three-input CMOS NAND gate is designed as shown below. Assume that V_{DD}=1.2 V, K'n=90 uA/V^2, Vtn=0.4 V, K'p=50 uA/V^2, and Vtp= -0.5 V in the 100nm technology node.

(a) Determine the width of NMOS and PMOS transistors in this NAND gate, such that the worst case delay becomes equivalent to a referenced inverter with Wn=1um and Wp=2um.

(b) For the device sizes found in part (a), determine the switching threshold voltage, V_M when all inputs are tied together.

(c) Find the maximum I_{DD} current for this NAND gate.

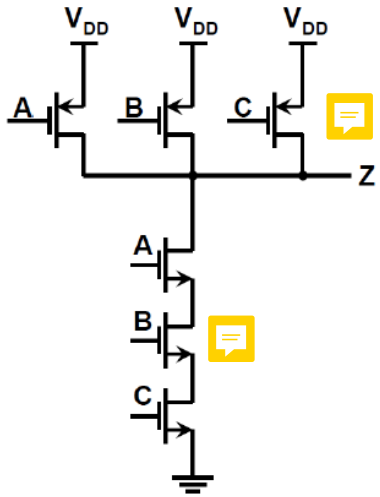


Figure 2 Three input NAND gate

Sample Question no 3: Combination gate

(20 points) Combinational Circuit and Delay Measurement

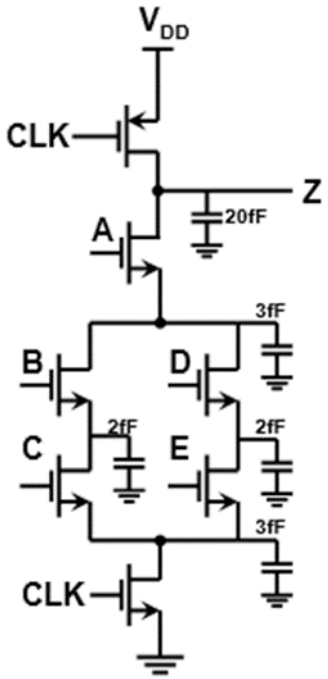
The following circuit is a dynamic logic.

(a) What logic function does this perform?

(b) What input vector imposes the worst case charge sharing during the evaluation time?

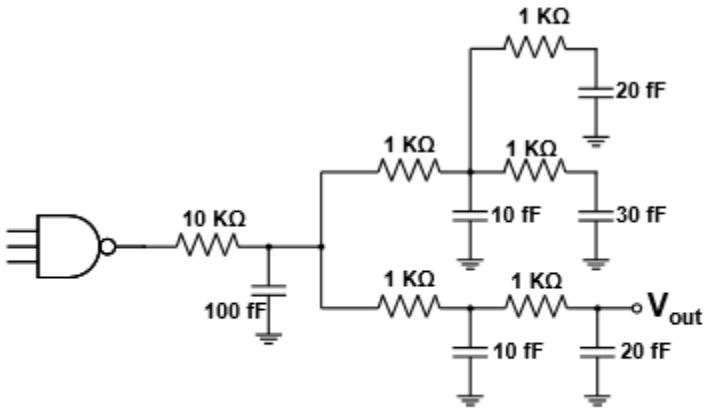
(c) Compute the final voltage at Z, if the input vector is ABCDE=11000 during evaluation after charge sharing. Assume that $V_{tn} = 0.4V$.

(d) Determine the width of the PMOS such that the maximum worst case precharge time delay (0 to 90%) is limited to 250ps. (The worst case is when all the inputs are at V_{DD} such that all the intermediate capacitors contribute to the delay). Assume that $V_{DD} = 1.2$ V, $K'_p = 50$ uA/V^2, and $V_{tp} = -0.5$ V in the 100nm technology node. For simplicity assume that the PMOS will stay in saturation during the transition.



Question no 4: Interconnection Modelling

(40 points) We would like to design the following circuit such that the worst case propagation delays (t_{pHL} and t_{pLH}) are limited to 2.14 ns. Use Elmore delay equation to determine the W/L for PMOS and NMOS used in the 3-input NAND gate. Assume that V_{DD}=1.2 V, K'_n=90 uA/V^2, V_{tn}=0.4 V, K'_p=50 uA/V^2, and V_{tp}=-0.5 V in the 100nm technology node. Also assume that the transistors stay in saturation region for the length of the transition.



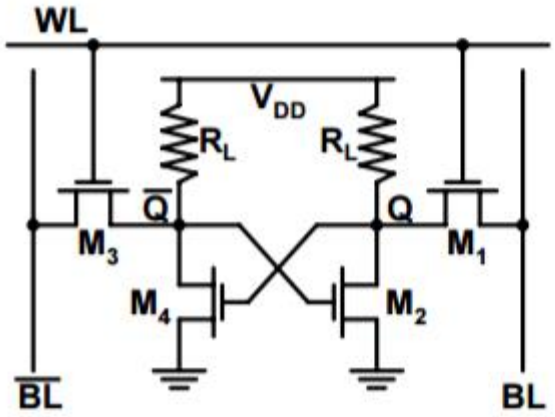
Sample question no 4: SRAM

EGCP 461 - 02 – Low Power IC Design
(Spring 2017)

(20 points) Consider a resistive load SRAM cell schematic shown below, also known as 4 transistor SRAM cell.

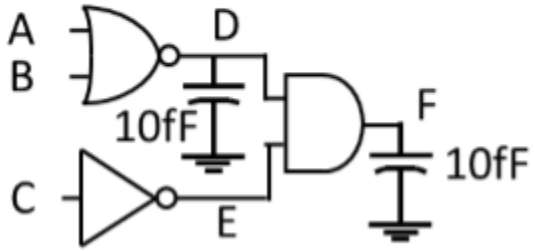
(a) Assume that node Q is in state 1. In order to write a 0 to node Q, bit line, BL, is lowered to 0 V. Determine the minimal size of transistor M_1 so that the cell just flips when this cell is selected. Assume that the switching threshold V_M of the resistive load inverter equals 0.6V. Also, assume that $V_{DD} = 2.5V$, $R_L = 100K\Omega$ $V_{Tn} = 0.4V$, and $K'_n = 100\mu A/V^2$. Ignore body effect.

(b) Now assume that node Q is in state 0. In order to read the cell, both bit lines, BL and $\overline{BL}$, are pre-charged to VDD. Determine the minimum size of transistor M_2 so that the cell does not flip during a read operation. Assume that $(W/L)_1 = 1.2$, which satisfies the constraint in part (a).



Sample question no 4: Power Calculation

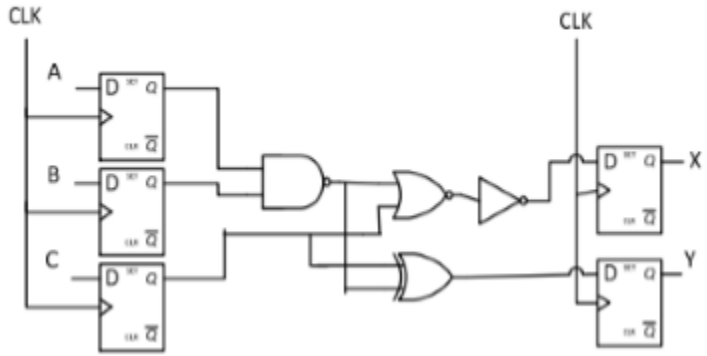
Q2. [Points 5] Given $V_{DD} = 1.2$ V and $f_{CLK} = 50$ MHz, calculate the activity coefficients and power dissipation at node-D and node-F.



Question no 5: Timing Analysis

a) Find contamination and critical delay.
b) Find the maximum clock frequency for reliable operation.
c) The amount of clock skew the circuit can tolerate if it needs to operate at 5 Ghz.

d) How much clock skew the circuit can tolerate before it experiences a hold time violation?



Gate	Tpd(ps)	Tcd(ps)
2-input NAND	20	15
2-input NOR	30	20
2-input XOR	60	40
NOT	15	10