CALIFORNIA STATE UNIVERSITY
FULLERTON

Final Project – Ping Pong Game

Lab Objectives

In this project, the students will be designing and implementing a Ping Pong game on Spartan 3 FPGA board. For designing the game, the students will be using the combinational and sequential digital logic concept and implement it using Verilog HDL. An additional sub-objective is to get more familiar with the Xilinx ISE environment.

Files

All the files (i.e., cover page, VHDL template files, reading material, etc.) are contained in a folder called "Project" which is available for download on TITANium. You must download these files prior to completing the following tasks.

Work Task

Project A – Creating symmetric Images

Before implementing the ping pong game on the FPGA board, it is crucial for the students to get familiarity with the operating of the VGA monitor. For this part of the project, the students are given Verilog files, pong_graph_st.v, vga_sync.v, pong_top_st.v and pong_top.ucf. The goal of this part is to train students in creating symmetric images on VGA screen using Verilog

These Verilog files are connected together as shown in Figure 1. In this task, the students are asked to modify the pong_graph_st.v to display a blue horizontal strip of width 40 pixels in the middle of the screen and a green vertical strip of width 40 pixels in the middle of the screen.

Red (R)	Green (G)	Blue (B)	Resulting Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

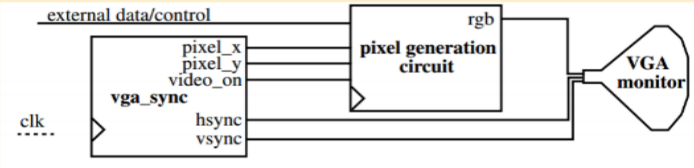

Figure 1: Symmetric Image Generation.

Project B – Creating Asymmetric Images

Implementing the asymmetric images requires ROM creation for each image. The students will be given Verilog files, pong_graph_anamate.v, pong_top_an.v, vga_sync.v, Zero.V, One.v, Two.v, and Three.v. The Verilog Zero.V, One.v, Two.v, and Three.v contain the ROM for creating integer digit zero, one, two, and three. The students are required to create ROM for creating digit four, five, six, seven, eight, and nine. Later they are required to modify the pong_graph_anamate.v such that based on the switching of 4-bit switches, the VGA screen should display one of the ten digits on the screen.

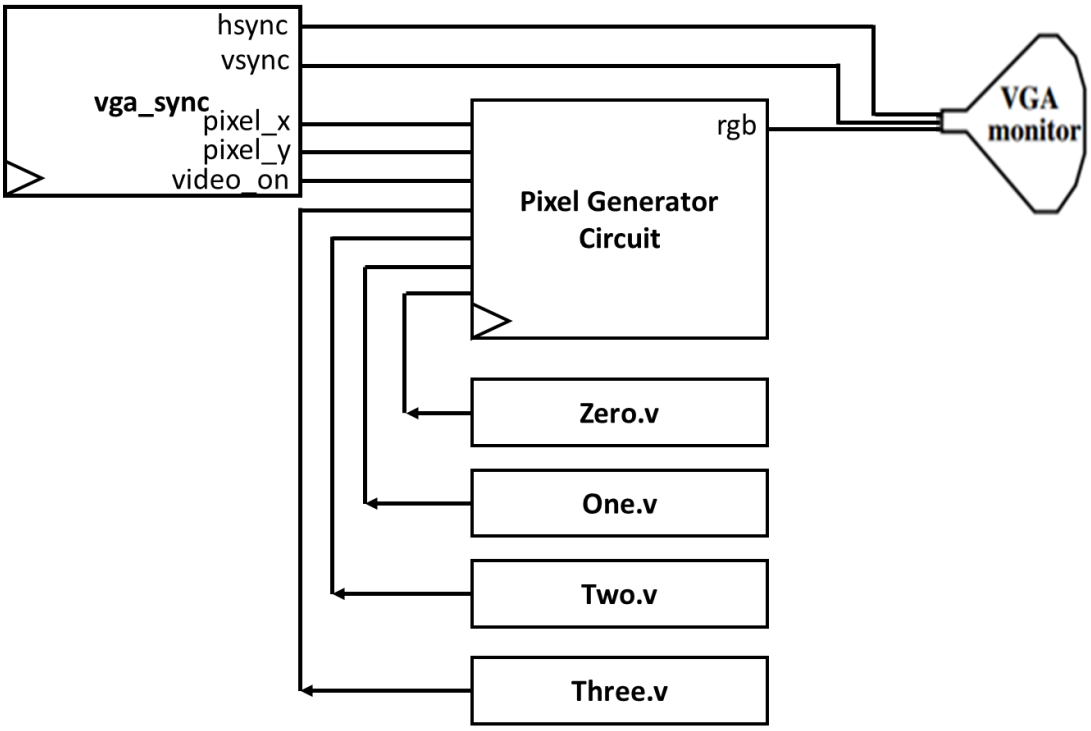

Figure 2 Block diagram of project part B

Project C – Creating State Machine for Score

One of the key components of logic system design is state machine. In part C, the students are asked to create a state machine such that every time the ball hits the paddle, the score on the screen increment by one. For sample, the students are given following Verilog files, pong_graph_anamate.v, pong_top_an.v, vga_sync.v, Zero.V, One.v, Two.v, and Three.v. The Verilog Zero.V, One.v, Two.v, Three.v, and Seven_Segment.v. This sample code displays numbers from "0" to "9" on 7-segment display. Every time the ball hit the paddle, the score on seven segment increments by one. The students are asked to use these files and modify the code and show the score on the VGA screen. The block diagram of the part C Verilog files given to the students is shown in Figure 3.

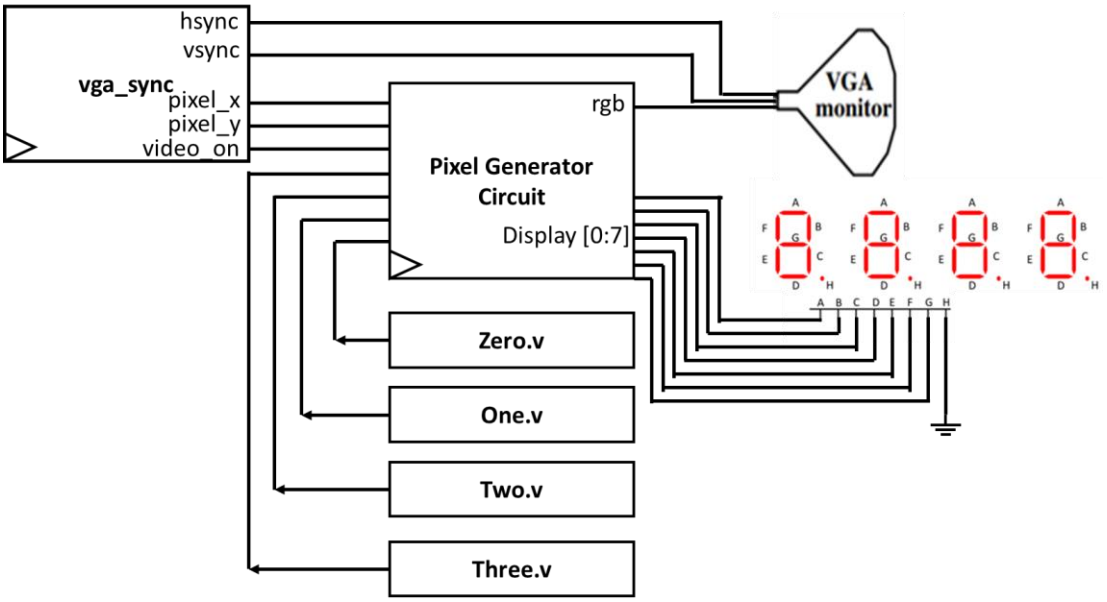

Figure 3 Block diagram of the files given in project part C

Project D – Apply Individual Creativity

In the project so far students followed all the instructions given to them by the instructor. In part D, the students are required to apply their creativity in the Ping Pong game. Students creativity and innovation can be following:

- Change the ball speed.
- Two players
- Adding I/O such as mouse and keyboard
- Scoring
- Adding a pause button
- Additional "End Game" screen
- Adding bouncing block

Presentation

The students in a group of four are required to do a presentation on the day selected by them. In the presentation, they need to present their outcome obtained in Part A, B, C, and D. Also, they are required to reveal the challenges they faced while doing the project and how they tackle them. In the end, they have to include in the slides the task divided among the group members.

What to Turn In (Please read this carefully)

For this project, you only need to provide the Verilog code for each part. You must put the complete Verilog code for part a, part b, part c and part d in a separate PDF file. You must label everything appropriately (i.e., label the code and work task sections). If I can't understand your answers or code, I will assume it is incorrect. Also, please include the cover page in your pdf document. The final group presentation slides. This project will be a digital submission and it will be submitted online using TITANium. No paper submissions will be accepted.